Output	Config 0
CLK0	25MHz LVCMOS1 2.5V
CLK1	90MHz LVCMOS2 3.3V
CLK2	50MHz LVCMOS2 3.3V
CLK3	100MHz HCSL 3.3V
CLK4	156.25MHz LVPECL 3.3V

IDD

Loads as specified in table headings below

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	2.5V Min	2.5V Typ	2.5V Max	3.3V Min	3.3V Typ	3.3V Max
IDD0	OUT0	25MHz LVCMOS1 2.5V		5		mA	-	2	-			
IDD1	OUT1	90MHz LVCMOS2 3.3V		25		mA				-	28	-
IDD2	OUT2	50MHz LVCMOS2 3.3V		16		mA				-	18	-
IDD3	OUT3	100MHz HCSL 3.3V		29		mA				-	28	-
IDD4	OUT4	156.25MHz LVPECL 3.3V		52		mA				-	43	-
IDD CORE	Core Supply Current			30		mA				-	31	-

DC CHAR LVCMOS

DC Electrical Characteristics for 3.3V LVCMOS (VDDO = 3.3V±5%, TA = -40°C to +85°C)

33 Ohm Series Resistor into 50 Ohm Transmission line with 5pF load capacitors to ground

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	2.5V Min	2.5V Typ	2.5V Max	3.3V Min	3.3V Typ	3.3V Max
VOH - not OUT0	Output HIGH Voltage	IOH = -15mA	2.4		VDDO	V				3.11	3.31	3.46
VOL - not OUT0	Output LOW Voltage	IOL = 15mA			0.4	V				-0.09	-0.06	-0.04
IOZDD - not OUT0	Output Leakage Current	Tri-state outputs, VDDO = 3.465V			5	µA				-0.2	0.0	0.1
VIH	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	0.7xVDDO		VDDD + 0.3	V				1.41	1.52	1.95
VIL	Input LOW Voltage	Single-ended inputs - CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	GND - 0.3		0.8	V				1.16	1.23	1.52
VIH	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	2		VDDO0 + 0.3	V				0.55	0.60	0.75
VIL	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V				0.35	0.55	0.55

DC Electrical Characteristics for 2.5V LVCMOS (VDDO = 2.5V±5%, TA = -40°C to +85°C)

33 Ohm Series Resistor into 50 Ohm Transmission line with 5pF load capacitors to ground

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	2.5V Min	2.5V Typ	2.5V Max	3.3V Min	3.3V Typ	3.3V Max
VOH - OUT0	Output HIGH Voltage	IOH = -12mA	0.7xVDDO		0	V	2.35	2.49	2.63			
VOL - OUT0	Output LOW Voltage	IOL = 12mA			0.4	V	-0.07	-0.05	-0.03			
IOZDD - OUT0	Output Leakage Current	Tri-state outputs, VDDO = 2.625V			30	µA	15.24	19.60	24.31			
VIH	Input HIGH Voltage	Single-ended inputs - CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	1.7		VDDD + 0.3	V	1.10	1.31	1.45			
VIL	Input LOW Voltage	Single-ended inputs - CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	GND - 0.3		0.8	V	0.80	0.89	1.00			
VIH	Input HIGH Voltage	Single-ended input OUT0_SEL_I2CB	1.7		VDDO0 + 0.3	V	0.55	0.60	0.70			
VIL	Input LOW Voltage	Single-ended input OUT0_SEL_I2CB	GND - 0.3		0.4	V	0.50	0.55	0.55			

DC CHAR HCSL

33 Ohm Series Resistor into 100 Ohm Differential Transmission lines with 50 Ohm, Termination resistors in parallel with 2 pF load capacitors to ground

Electrical Characteristics–DIF 0.7V Low Power HCSL Differential Outputs (VDDO = 3.3V±5%, 2.5V±5%, TA = -40°C to +85°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	2.5V Min	2.5V Typ	2.5V Max	3.3V Min	3.3V Typ	3.3V Max
dV/dt	Slew Rate	Scope averaging on	1		4	V/ns				1.86	2.14	2.54
VHIGH	Voltage High	Statistical measurement on single-ended signal using oscilloscope math function (Scope averaging ON)	660		850	mV				679	730	759
VLOW	Voltage Low		-150		150	mV				-20	28	82
VMAX	Maximum Voltage	Measurement on single-ended signal using absolute value (Scope averaging off)	0		1150	mV				702	745	798
VMIN	Minimum Voltage		-300			mV				-48	18	67
VSWING	Voltage Swing	Scope averaging off	300			mV				1514	1531	1550
VCROSS	Crossing Voltage Value	Scope averaging off	250		550	mV				329	368	391
ΔVCROSS	Crossing Voltage variation	Scope averaging off	0		140	mV				4	11	22

Note 1: Guaranteed by design and characterization. Not 100% tested in production

Note 2: Measured from differential waveform.

Note 3: Slew rate is measured through the VSWING voltage range centered around differential 0V. This results in a +/-150mV window around differntial 0V. rising and Clock# falling).

The intent is to limit VCROSS induced modulation by setting ΔVCROSS to be smaller than VCROSS absolute.

Note 6: Measured from single-ended waveform.

Note 7. Measured with scope averaging off, using statistics function. Variation is difference between min. and max

DC Char LVPECL

DC Electrical Characteristics for LVPECL (VDDO = 3.3V+5% or 2.5V+5%, TA = -40°C to +85°C)

Symbol	Parameter		Min	Typ	Max	Unit	2.5V Min	2.5V Typ	2.5V Max	3.3V Min	3.3V Typ	3.3V Max
VOH	Output Voltage HIGH, terminated through 50Ω tied to VDD-2 V		VDDO - 1.19	-	VDDO - 0.69	V				2.28	2.41	2.53
VOL	Output Voltage LOW, terminated through 50Ω tied to VDD-2 V		VDDO - 1.94	-	VDDO - 1.4	V				1.52	1.62	1.72
VSWING	Peak-to-Peak Output Voltage Swing		0.55		0.993	V				0.67	0.78	0.89

AC Char

AC Timing Electrical Characteristics

(VDDO = 3.3V+5% or 2.5V+5% or 1.8V ±5%, TA = -40°C to +85°C)

(Spread Spectrum Generation = OFF)

Symbol	Parameter		Min	Typ	Max	Unit	2.5V Min	2.5V Typ	2.5V Max	3.3V Min	3.3V Typ	3.3V Max
t3	Output Duty Cycle	All Outputs	45		55	%	48.69	49.43	49.87	49.11	50.00	50.54
	Slew Rate, SLEW[1:0] = 00			2.6		V/ns	1.6	2.2	3.0	1.8	3.4	4.5
t5	Rise Times	LVPECL, 20% to 80%		400		ps				283	337	399
	Fall Times	LVPECL, 80% to 20%		400						273	324	384
t6	Clock Jitter	Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, differential outputs (1.8V to 3.3V nominal output voltage)		46		ps					13	62
		Cycle-to-Cycle jitter (Peak-to-Peak), multiple output frequencies switching, LVCMOS outputs (1.8 to 3.3V nominal output voltage)		74		ps		23	97		22	100
		RMS Phase Jitter OUT1=90MHz LVCMOS 3.3V		0.75	1.5	ps					1.45	
		RMS Phase Jitter OUT1B=90MHz LVCMOS 3.3V									1.21	
		RMS Phase Jitter OUT2=50MHz LVCMOS 3.3V									0.59	
		RMS Phase Jitter OUT2B=50MHz LVCMOS 3.3V									0.60	
		RMS Phase Jitter OUT3=100MHz HCSL 3.3V									0.64	
		RMS Phase Jitter OUT4=156.25MHz LVPECL 3.3V									0.63	

1. Practical lower frequency is determined by loop filter settings.
2. A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.
3. Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.
4. Actual PLL lock time depends on the loop configuration.
5. Duty Cycle is only guaranteed at max slew rate settings.
6. LVCMOS programmed at 1.0x slew rate settings. RMS Phase Jitter integration range 12kHz to 20MHz