DESIGN TARGET DATASHEET

General Description

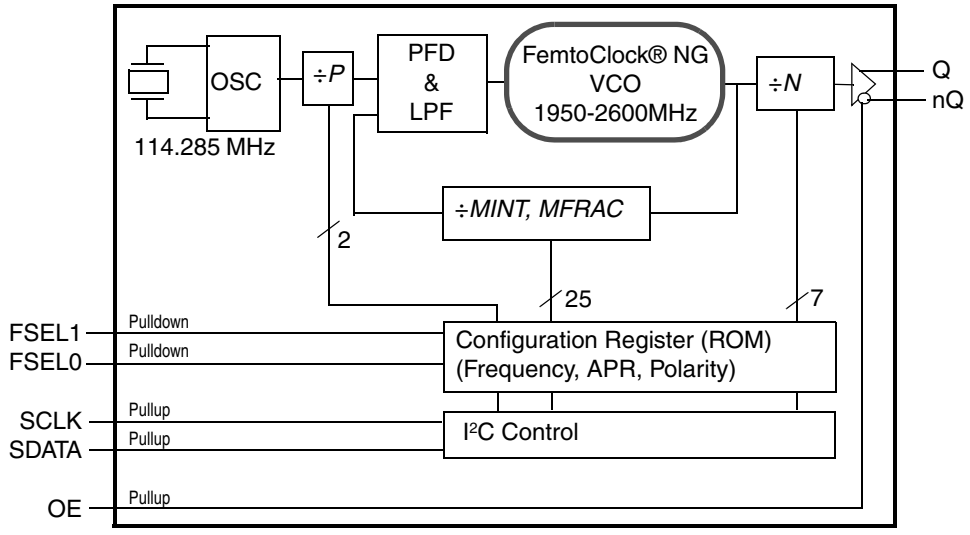
The ICS8N4Q001 is a Quad-Frequency Programmable Clock Oscillator with very flexible frequency programming and delivers excellent phase noise performance at <0.5 ps rms 1kHz - 20MHz. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance, combined with high power supply noise rejection. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 10-lead ceramic 5mm x 7mm x 1.55mm package.

Besides the 4 default power-up frequencies set by the FSEL0 and FSEL1 pins, the ICS8N4Q001 can be programmed via the I²C interface to output clock frequencies between 15.476 to 866.67MHz and from 975 to 1,300MHz to a very high degree of precision with a frequency step size of 435.9Hz ÷ *N* (*N*: PLL post divider). Since the FSEL0 and FSEL1 pins are mapped to 4 independent PLL M and N divider registers (P, MINT, MFRAC and N), reprogramming those registers to other frequencies under control of FSEL0 and FSEL1 is supported. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements. The device is a member of the high-performance clock family from IDT.

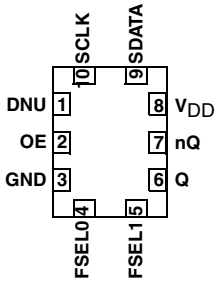
Features

- Fourth generation FemtoClock® Next Generation (NG) technology
- Programmable clock output frequency from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz
- Four power-up default frequencies (see part number order codes), re-programmable by I²C
- I²C programming interface for the output clock frequency and internal PLL control registers
- Frequency programming resolution is 435.9Hz ÷*N*
- One 2.5V/3.3V LVDS clock output
- Two control inputs for the power-up default frequency
- LVCMOS/LVTTL compatible control inputs
- RMS phase jitter @ 156.25MHz (12kHz - 20MHz): 0.5ps (typical), design target
- RMS phase jitter @ 156.25MHz (1kHz - 40MHz): TBD
- 2.5V or 3.3V supply
- -40°C to 85°C ambient operating temperature
- Available in Lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS8N4Q001
10-lead ceramic 5mm x 7mm x 1.55mm package body
J Package
Top View

The DESIGN TARGET DATASHEET presented herein represents a product that is developmental or prototype. The noted characteristics are design targets. Integrated Device Technologies, Inc. (IDT) reserves the right to change any circuitry or specifications without notice

Table 1. Pin Descriptions

Number	Name	Type		Description
1	DNU			Do not connect.
2	OE	Input	Pullup	Output enable pin. See Table 3B for function. LVCMOS/LVTTL interface levels.
3	GND	Power		Power supply ground.
5, 4	FSEL1, FSEL0	Input	Pulldown	Default frequency select pins. See Table 3A for function and Table 8 for the default frequency order codes. LVCMOS/LVTTL interface levels.
6, 7	Q, nQ	Output		Differential clock output. LVDS interface levels.
8	V_{DD}	Power		Power supply pin.
9	SDATA	Input	Pullup	I^2C Data Input. LVCMOS/LVTTL interface levels.
10	SCLK	Input	Pullup	I^2C Clock Input. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ

Function Tables

Table 3A. Default Frequency Selection

Input		Operation
FSEL1	FSEL0	
0 (default)	0 (default)	Default frequency 0
0	1	Default frequency 1
1	0	Default frequency 2
1	1	Default frequency 3

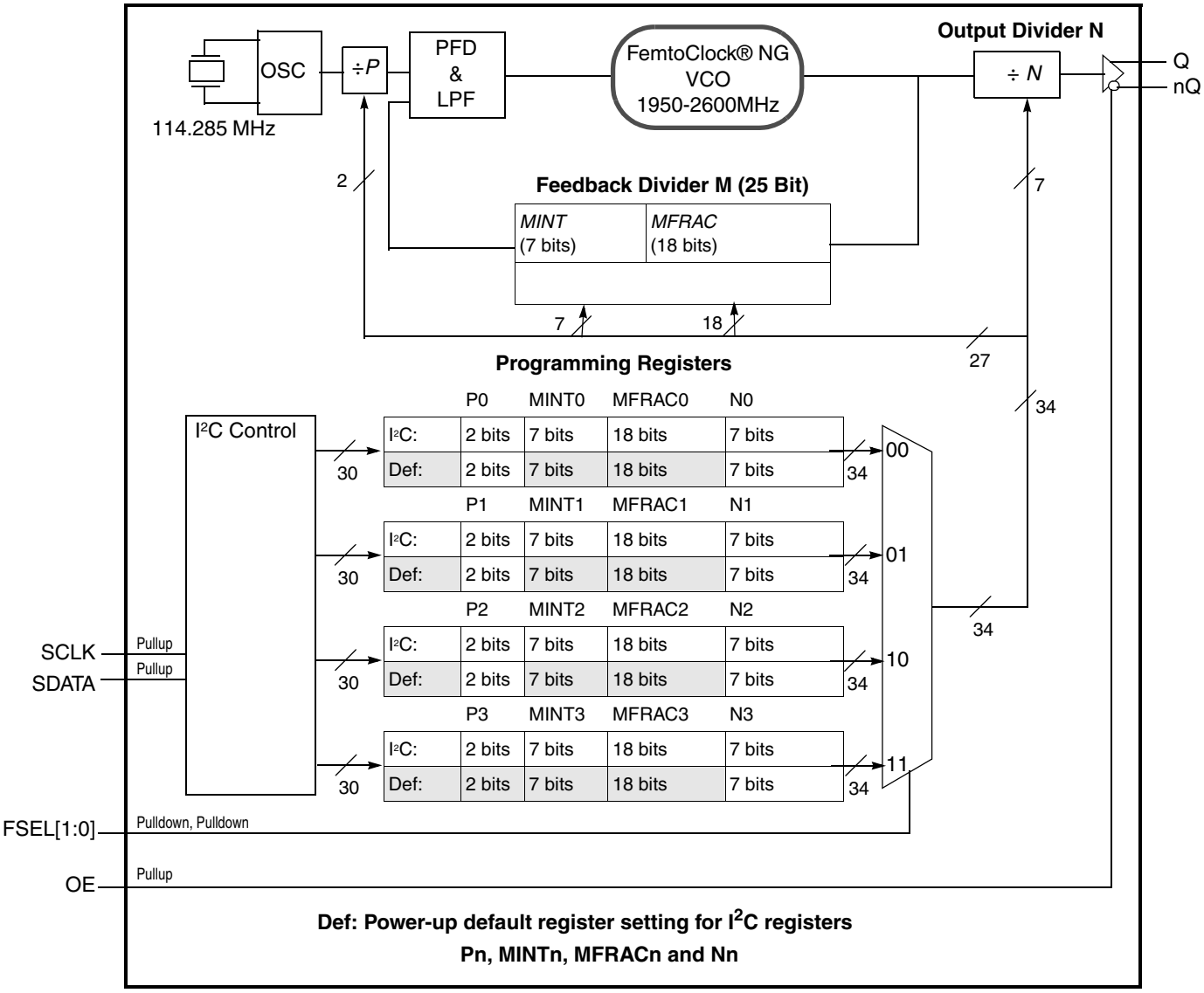
NOTE: The default frequency is the output frequency after power-up. One of four default frequencies is selected by FSEL[1:0]. See programming section for details.

Table 3B. OE Configuration

Input	Output Enable
OE	
0	Outputs Q/nQ are in high-impedance state.
1 (default)	Outputs are enabled.

NOTE: OE is an asynchronous control.

Block Diagram with Programming Registers



Principles of Operation

The ICS8N4Q001 uses a fractional feedback-divider synthesizer core with a Delta-Sigma modulator for noise shaping and is very robust in its frequency synthesis capability. Output frequencies are synthesized from an internal 114.285MHz third overtone crystal in order to minimize phase noise generation by frequency multiplication. The higher frequency reference crystal also allows more efficient “shaping” of noise by the Delta-Sigma modulator. The device contains a 25-bit PLL feedback divider with a 2-bit prescaler (P), a 7-bit integer portion (*MINT*), a 18-bit fractional portion (*MFRAC*) and a 7-bit output divider (*N*) for high-resolution frequency generation. The output frequency f_{OUT} is calculated by:

$$f_{OUT} = f_{REF} \cdot \frac{MINT + (MFRAC \div 2^{18})}{P \cdot N}$$

or

$$f_{OUT} = 114.285\ MHz \cdot \frac{MINT[4:0] + (MFRAC[17:0] \div 2^{18})}{P[1:0] \cdot N[6:0]}$$

The *P, MINT, MFRAC* and *N* PLL-dividers have four corresponding Pn, MINTn, MFRACn and Nn (n=0 to 3) registers. These four registers allow the device to store four independent frequency configurations. The configuration register selected by the FSEL[1:0] pins is loaded into the PLL-dividers (see table 3A).

Each of the four configuration registers is fully accessible by I²C to allow the re-configuration of the PLL and output frequency at any time after power-up. For frequency re-configuration, it is recommended to load the new frequency setting into a register that is not selected by FSEL[1:0] before the selection of this register. Changing the FSEL[1:0] pins results in re-loading PLL dividers from the selected register immediately.

Each of the four configuration registers has a default setting that is automatically loaded into the registers at power-up. The default settings are programmed by IDT and are read-only to the user (see order codes, Table 8).

Frequency Configuration: Calculation of *MINT, MFRAC* and *N*

1. Determine the VCO frequency and output divider *N*:
   Multiplying the desired output frequency f_{OUT} by some integer *N* (*N* is the output divider value and has the range of 2, 3, 4, 5, 6, 8, 10,...,126, see table 4D) that will place the VCO frequency within the PLL lock range (1950MHz to 2600MHz). For example, if an output frequency of 625MHz is desired, the output divider must be set to *N* = 4, which will result in a VCO frequency of 2500MHz. 2500MHz satisfies the PLL lock frequency range criteria. The setting for the N registers can be looked-up from table 4D: *N* = 4 corresponds to the register setting of 0x04.
2. Calculate the required multiplication value M:
   Divide the VCO frequency from step 1 by the PLL reference frequency f_{REF} and set P=1. The PLL reference frequency is the frequency of the internal crystal oscillator (114.285MHz):

   $M = f_{VCO} \div (f_{REF} \cdot P)$

   $M = 2500MHz \div 114.285MHz \cdot 1 = 21.8751$
3. Determine the integer part (*MINT*) and the fractional part (*MFRAC*) of M: The integer part of M equals 21 and will be the setting for the *MINT* register bits. *MINT* has the length of six bits. The fractional part of M equals 0.8751. The fractional PLL feedback divider is base 2 and has the length of 18 bits. Specify the value in the following form:

   $$\frac{MFRAC}{2^{18}} = 0.8751$$

   Resolving for *MFRAC*: $MFRAC = 2^{18} * 0.8751 = 229{,}402$. To second check the math, plug back in to the equation to ensure $229{,}402 \div 2^{18} = 0.8751$.
4. Program any of the four Pn, MINTn, MFRACn and Nn register sets (n = 0, 1, 2 or 3) with the calculated values: MINTn = 21 (0x15), MFRACn = 229,402 (0x3801A), N = 4 (0x04)). There are four MINTn, FRACn, Nn register sets and the FSEL[1:0] pins selects the register set that sets the output frequency.

   In cases where $MFRAC \div 2^{18}$ required decimal value does not yield a whole number, round to the nearest whole number and this will result in a small amount of frequency synthesis error. The following example illustrates this:

Desired Output Frequency: 600MHz

1. VCO frequency f_{VCO}:
   600MHz * N = 2400 MHz yields N = 4.
   f_{VCO} is within the PLL lock range: 1950MHz < 2400MHz < 2600MHz.
2. Multiplication factor M:
   2400MHz ÷ 114.285MHz = 21.000131251.
3. *MINT* and *MFRAC*:
   MINT = 21 and *MFRAC* = $0.000131251 * 2^{18} = 34.4066$.

   In this case, *MFRAC* must be round down to 34.
4. Loading *MINT, MFRAC* and *N* into the registers selected by FSEL[1:0] will result in an output frequency of:

   $f_{OUT} = f_{REF} * (MINT + (MFRAC \div 2^{18}))$

   $f_{OUT} = 114.285 * (21 + (34 \div 2^{18}))$

   $f_{OUT} = 599.99995568MHz$.

   The synthesis error in this case is:

   $err = 10^6 * (599.99995568 - 600) \div 600 = -0.0738621ppm$.

This example also hints at how to calculate the worst case ppm error for a given VCO frequency. The frequency resolution (frequency step size for P equals 1) is 114.285MHz ÷ (2^{18}· *N*) = 0.000435963MHz ÷ *N* = 435.963÷*N* Hz. The worst case error will occur when the desired VCO frequency is half-way between these 435.963Hz steps because that is when the maximum round-off error will occur. So dividing this number by 2 results in 217.981÷*N* Hz and this is the worst case frequency error. This is a fixed error and the relative (ppm) error will therefore be higher at lower VCO frequencies.

Default Frequencies and PLL settings

The default frequency is the output frequency after power-up. On power-up, four default frequency settings are loaded into the corresponding I²C registers. One of the four default frequencies is selected by FSEL[1:0] and sets the output frequency. All four default frequencies are programmed by IDT. An order code is assigned to each default frequency set (see Table 8 for order codes. More order codes are available on request). Each default frequency setting can use the entire output frequency range of 15.476MHz to 866.67MHz and 975MHz to 1,300MHz. The output frequency can be modified at any time after power-up by changing the I²C registers. On power-up, the device loads optimized PLL settings into the registers 16 to 18.

Register Settings

Table 4A. I²C Register Map

Register	Binary Register Address	Register Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
0	00000	CP0[1]	CP0[0]	MINT0[4]	MINT0[3]	MINT0[2]	MINT0[1]	MINT0[0]	MFRAC0[17]
1	00001	CP1[1]	CP1[0]	MINT1[4]	MINT1[3]	MINT1[2]	MINT1[1]	MINT1[0]	MFRAC1[17]
2	00010	CP2[1]	CP2[0]	MINT2[4]	MINT2[3]	MINT2[2]	MINT2[1]	MINT2[0]	MFRAC2[17]
3	00011	CP3[1]	CP3[0]	MINT3[4]	MINT3[3]	MINT3[2]	MINT3[1]	MINT3[0]	MFRAC3[17]
4	00100	MFRAC0[16]	MFRAC0[15]	MFRAC0[14]	MFRAC0[13]	MFRAC0[12]	MFRAC0[11]	MFRAC0[10]	MFRAC0[9]
5	00101	MFRAC1[16]	MFRAC1[15]	MFRAC1[14]	MFRAC1[13]	MFRAC1[12]	MFRAC1[11]	MFRAC1[10]	MFRAC1[9]
6	00110	MFRAC2[16]	MFRAC2[15]	MFRAC2[14]	MFRAC2[13]	MFRAC2[12]	MFRAC2[11]	MFRAC2[10]	MFRAC2[9]
7	00111	MFRAC3[16]	MFRAC3[15]	MFRAC3[14]	MFRAC3[13]	MFRAC3[12]	MFRAC3[11]	MFRAC3[10]	MFRAC3[9]
8	01000	MFRAC0[8]	MFRAC0[7]	MFRAC0[6]	MFRAC0[5]	MFRAC0[4]	MFRAC0[3]	MFRAC0[2]	MFRAC0[1]
9	01001	MFRAC1[8]	MFRAC1[7]	MFRAC1[6]	MFRAC1[5]	MFRAC1[4]	MFRAC1[3]	MFRAC1[2]	MFRAC1[1]
10	01010	MFRAC2[8]	MFRAC2[7]	MFRAC2[6]	MFRAC2[5]	MFRAC2[4]	MFRAC2[3]	MFRAC2[2]	MFRAC2[1]
11	01011	MFRAC3[8]	MFRAC3[7]	MFRAC3[6]	MFRAC3[5]	MFRAC3[4]	MFRAC3[3]	MFRAC3[2]	MFRAC3[1]
12	01100	MFRAC0[0]	N0[6]	N0[5]	N0[4]	N0[3]	N0[2]	N0[1]	N0[0]
13	01101	MFRAC1[0]	N1[6]	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
14	01110	MFRAC2[0]	N2[6]	N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]
15	01111	MFRAC3[0]	N3[6]	N3[5]	N3[4]	N3[3]	N3[2]	N3[1]	N3[0]
16	10000	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
17	10001	DBIT[0]	DBIT[1]	DBIT[2]	DBIT[3]	DBIT[4]	DBIT[5]	DBIT[6]	reserved
18	10010	reserved	reserved	nPLL_BYP	FSEL[1]	FSEL[0]	reserved	reserved	reserved
19	10011	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
20	10100	P0[1]	P0[0]	reserved	DSM0[1]	DSM0[0]	DG0	DSM_ENA0	LF0
21	10101	P1[1]	P1[0]	reserved	DSM1[1]	DSM1[0]	DG1	DSM_ENA1	LF1
22	10110	P2[1]	P2[0]	reserved	DSM2[1]	DSM2[0]	DG2	DSM_ENA2	LF2
23	10111	P3[1]	P3[0]	reserved	DSM3[1]	DSM3[0]	DG3	DSM_ENA3	LF3

Table 4B. I^2C Register Function Descriptions

Bits	Name	Function
MINTn[4:0]	Integer Feedback Divider Register n (n = 0...3)	Sets the integer portion of the feedback divider value. Can be set to a value of 4 to 127. For binary values < 4, the value is x+4. So programming 0000000 would yield a feedback divider of ÷4, 0000001 = ÷5, etc. It should also be noted that with a reference of 114.285MHz and P=1, the minimum value loaded into this register should be 17 to remain above the minimum VCO frequency of 1950MHz. The six bits MINTn[5:0] can be programmed independently on any register setting, while the MSB of MINTn (MINT[6]) is configured in conjunction with the Pn[1:0] divider. See also Table 4C.
MFRACn[17:0]	Fractional Feedback Divider Register n (n = 0...3)	Sets the fractional value of the feedback divider resulting in a fraction of MFRAC0[17:0]÷2^{18}. From a 114.285MHz reference, this means the frequency is incremented by about 436Hz÷*N* for each LSB increment.
Nn[6:0]	Output Divider Register n (n = 0...3)	Sets the output divider. The output divider value can range from 2, 3, 4, 5, 6 and 8, 10, 12 to 126 (step: 2). See Table 4D for the output divider coding.
Pn[1:0]	Pre-Scaler Register n (n = 0...3)	Sets the PLL pre-scaler. The pre-scaler divider value has the range of 1, 2, 4 and 5. See Table 4C for the prescaler coding. Note the Pn[1:0] registers also set the Mn[6] bit of MINT (MINTn[6]).
DG0	Dither Gain	Recommended setting = 1
DG1	Dither Gain	Recommended setting = 1
DG2	Dither Gain	Recommended setting = 1
DG3	Dither Gain	Recommended setting = 1
DSMn[1:0]	DSM Order (n = 0...3)	. Do not change the default value.
DBIT[6:0]	Test Bits	Default = 0000000. Do not change the default value
DSM_ENAn	DSM Enable (n = 0...3)	Delta Sigma Modulator Enable. 0 = DSM not enabled 1 = DSM Enabled (default)
LFn	Loop Filter Value (n = 0...3)	Together with CPn[1:0] sets the PLL loop parameters. A higher value results in lower bandwidth. Contact IDT for a recommendation for changing LFn.
CPn[1:0]	Charge Pump Current	Together with LFn sets the loop parameters. A higher value results in higher loop bandwidth (opposite of LFn). Contact IDT for a recommendation for changing LFn.
FSEL[1:0]	Frequency Select	Selects from 4 available power-up default M and N combinations to provide 4 available power-up default output frequencies. The value of these bits are OR'ed with the Frequency Select pin values.
nPLL_BYP	PLL Bypass	PLL Bypass. The output frequency = oscillator frequency (~114.285 MHz) divided by *N*. 0 = PLL Bypass 1 = PLL Enable (default)

Table 4C. PLL Pre-Scaler P and Feedback Divider M6 Coding

Register Bit		Pre-Scale *P*	Feedback-Divider Bit $M_N[6]$
P_N1	P_N0		
0	0	1	0
0	1	2	0
1	0	4	1
1	1	5	1

NOTE: The $P_N[1:0]$ bits control both the pre-scale P_N and the MSB of MINT ($MINT_N[6]$).

Table 4D. PLL Post Divider N Coding

Register Bit	Frequency Divider *N*	Output frequency range	
$N_N[6:0]$		$f_{OUT,MIN}$ (MHz)	$f_{OUT,MAX}$ (MHz)
000000X	2	975	1300
0000010	2	975	1300
0000011	3	650	866.66
0000100	4	487.5	650
0000101	5	390	520
000011X	6	325	433.33
000100X	8	243.75	325
000101X	10	195	260
000110X	12	162.5	216.66
000111X	14	139.29	185.71
001000X	16	121.87	162.5
...	N (even integer)	(1950 ÷ *N*)	(2600 ÷ *N*)
111101X	124	15.73	20.97
111111X	126	15.48	20.63

NOTE: “X” can be either 0 or 1 (don’t care).

Serial Interface Configuration Description

The ICS8N4Q001 has an I²C-compatible configuration interface to access any of the internal registers (Table 4A) for frequency and PLL parameter programming. The ICS8N4Q001 acts as a slave device on the I²C bus and has the address 0b1101110. The interface accepts byte-oriented block write and block read operations. An address byte (P) specifies the register address (Table 4A) as the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see Tables 4F, 4G). Read and write block transfers can be stopped after any complete byte transfer. It is recommended to terminate I²C the read or write transfer after accessing byte #23.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50kΩ typical.

Table 4E. I²C Device Slave Address

1	1	0	1	1	1	0	R/W

Table 4F. Block Write Operation

Bit	1	2:8	9	10	11:18	19	20:27	28	29-36	37	...	...	...
Description	START	Slave Address	W(0)	ACK	Address Byte P	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	8	1	1

Table 4G. Block Read Operation

Bit	1	2:8	9	10	11:18	19	20	21:27	28	29	30:37	38	39-46	47	...	...	...
Description	START	Slave Address	W (0)	ACK	Address Byte P	ACK	Repeated START	Slave Address	R (1)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte ...	ACK	STOP
Length (bits)	1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	TBD°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current					mA

Table 5B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current					mA

Table 5C. LVCMOS/LVTTL DC Characteristic, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE, SDATA, SCLK	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
		FSEL0, FSEL1	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	OE, SDATA, SCLK	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
		FSEL0, FSEL1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

Table 5D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage					mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage					V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 5E. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage					mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage					V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

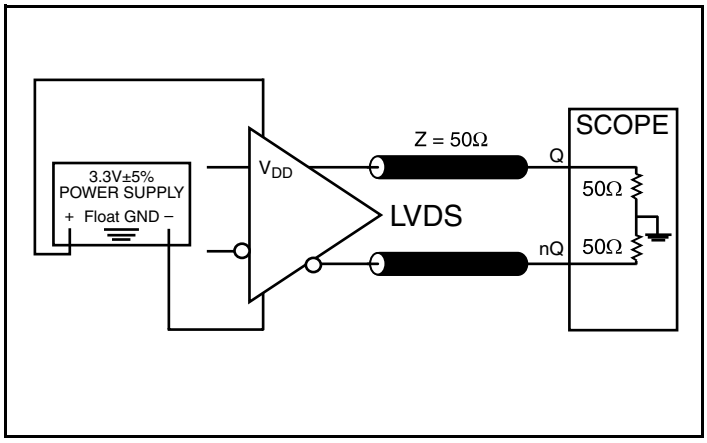
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C

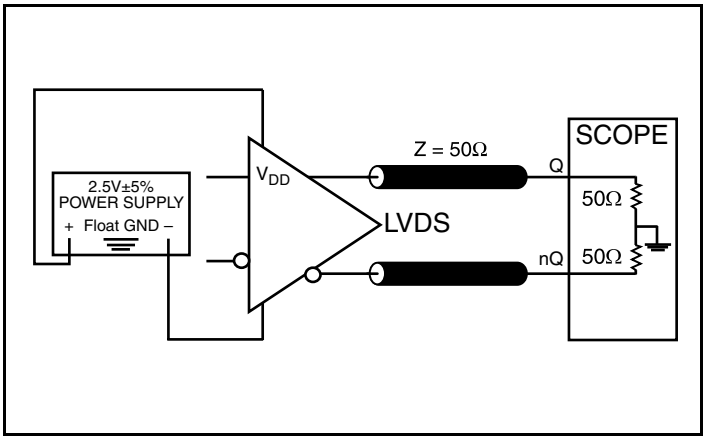
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Q, nQ	*P*=1, *N* = 3...126	15.476		866.67	MHz
		P=1, *N* = 2	975		1,300	MHz
f_I	Initial Accuracy	Measured at 25°C at final test		±1.5		ppm
	Temperature Stability	Option code = A or B			±100	ppm
		Option code = E or F			±50	ppm
		Option code = K or L			±20	ppm
f_A	Aging	Frequency drift over 1st year			±3	ppm
		Frequency drift over 15 year life			±10	ppm
	Total Stability	Option code A or B			±111.5	ppm
		Option code E or F			±61.5	ppm
		Option code K or L			±31.5	ppm
t_{jit}(cc)	Cycle-to-Cycle Jitter; NOTE 1			30		ps
t_{jit}(Ø)	RMS Phase Jitter (Random); NOTE 2	156.25MHz, Integration Range: 12kHz - 20MHz		0.5		ps
t_{jit}(Ø)	RMS Phase Jitter (Random); NOTE 2	156.25MHz, Integration Range: 50kHz - 80MHz				ps
Φ_N(100)	Single-side band phase noise, 100 Hz from Carrier	156.25MHz				dBc/Hz
Φ_N(1k)	Single-side band phase noise, 1kHz from Carrier	156.25MHz		-110		dBc/Hz
Φ_N(10k)	Single-side band phase noise, 10kHz from Carrier	156.25MHz		-125		dBc/Hz
Φ_N(100k)	Single-side band phase noise, 100kHz from Carrier	156.25MHz		-128		dBc/Hz
Φ_N(1M)	Single-side band phase noise, 1MHz from Carrier	156.25MHz		-137		dBc/Hz
Φ_N(10M)	Single-side band phase noise, 10MHz from Carrier	156.25MHz		-141		dBc/Hz
PSRR	Power Supply Rejection Ratio	50mV Sinusoidal Noise 1kHz - 50kHz				dB
t_R / t_F	Output Rise/Fall Time	20% to 80%				ps
odc	Output Duty Cycle		45		55	%
t_{OSC}	Oscillator Start-Up Time					ms
t_{SET}	Output frequency settling time after FSEL0 and FSEL1 values are changed					ms

NOTE: Design Target specs.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: This parameter is defined in accordance with JEDEC standard 65.
NOTE 2: Please refer to the phase noise plots.

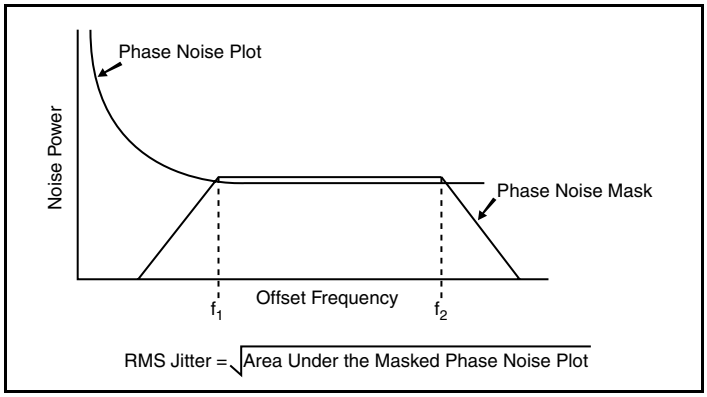
Parameter Measurement Information



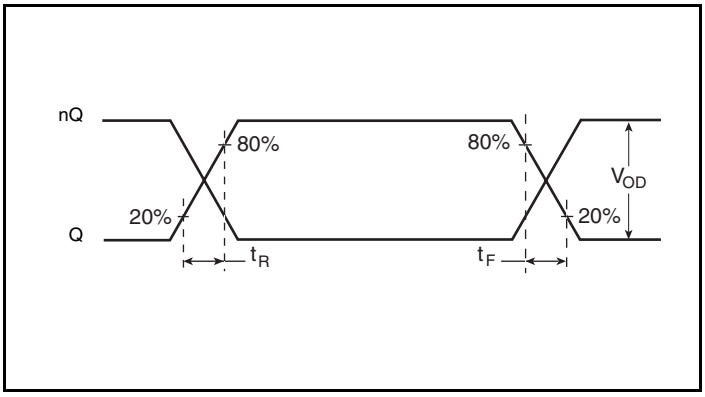
3.3V LVDS Output Load AC Test Circuit



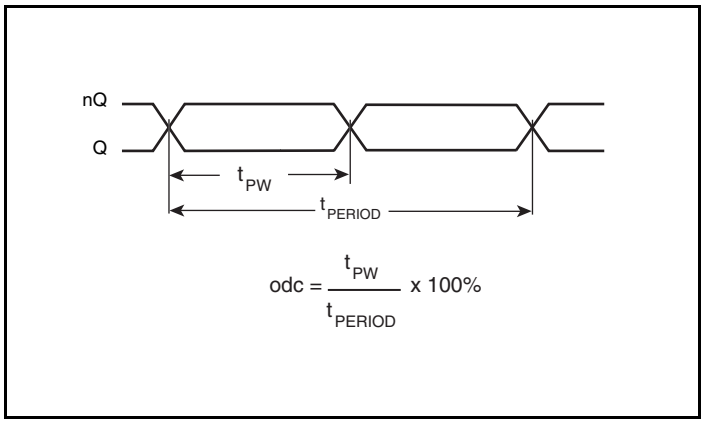
2.5V LVDS Output Load AC Test Circuit



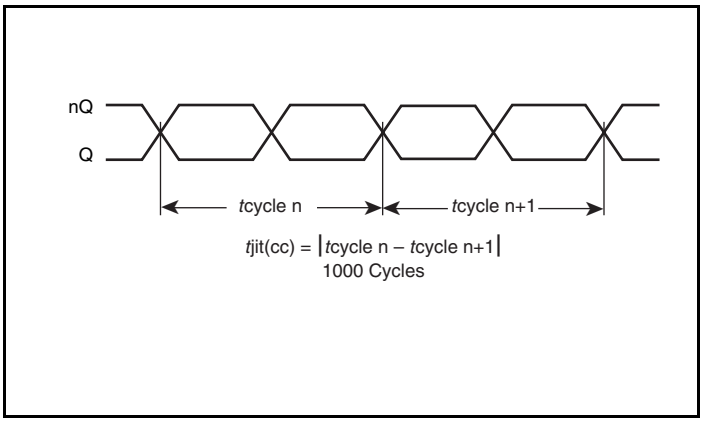
RMS Phase Jitter



Output Rise/Fall Time

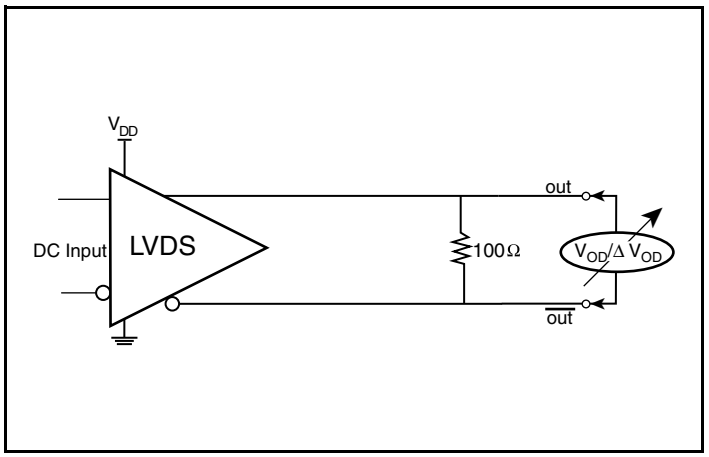


Output Duty Cycle/Pulse Width/Period

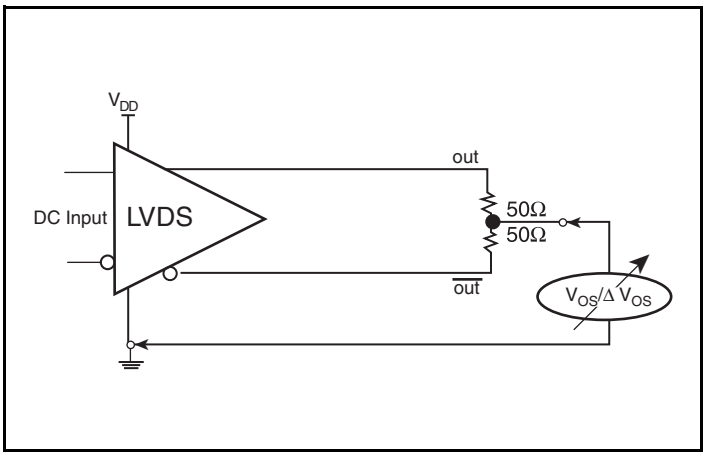


Cycle-to-Cycle Jitter

Parameter Measurement Information (continued)



Differential Output Voltage Setup



Offset Voltage Setup

Application Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Select Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

3.3V, 2.5V LVDS Driver Termination

A general LVDS interface is shown in *Figure 1.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

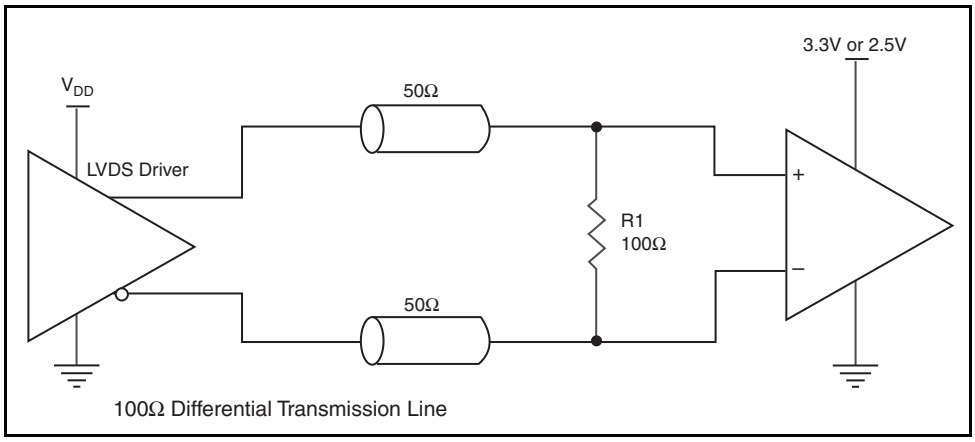


Figure 1. Typical LVDS Driver Termination

Reliability Information

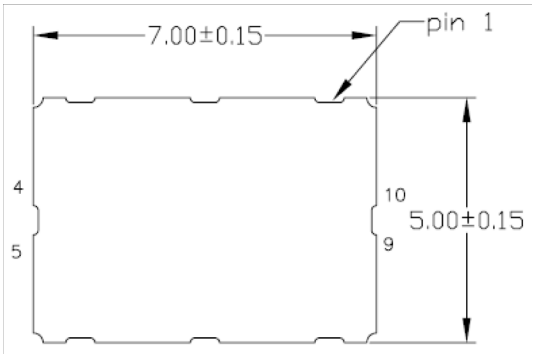
Table 7. θ_{JA} vs. Air Flow Table for a 10-lead Ceramic 5mm x 7mm Package

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	TBD°C/W	TBD°C/W	TBD°C/W

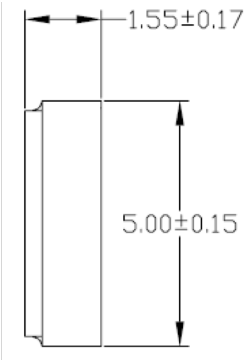
Transistor Count

The transistor count for ICS8N4Q001 is: TBD

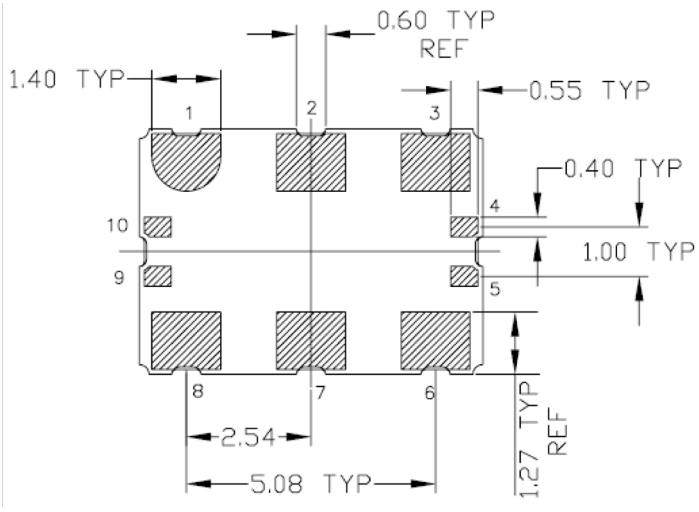
Package Outline and Package Dimensions



Top View



Side View



Bottom View

Ordering Information for FemtoClock NG Ceramic-Package XO and VCXO Products

The programmable VCXO and XO devices support a variety of devices options such as the output type, number of default frequencies, power supply voltage, ambient temperature range and the frequency accuracy. The device options, default frequencies and default VCXO pull range must be specified at the time of order and are programmed by IDT before the shipment. Table 8 specifies the available order codes, including the device options and default frequency configurations. Example part number: the order code 8N4QV01FAJI-001 specifies a programmable, quad default-frequency VCXO with a voltage supply of 2.5V, a ±50 ppm crystal frequency accuracy, industrial temperature range, a lead-free (6/6 RoHS) 10-lead ceramic 5mm x 7mm x 1.55mm package and is factory-programmed to the default frequencies of 100, 122.88, 125 and 156.25MHz and to the VCXO pull range of min. ±100 ppm.

Other default frequencies, VCXO pull ranges and order codes are available from IDT on request.

Table 8. Order Codes

Part/Order Number

8N X X XXX X X X X - ddd T

FemtoClock NG

Shipping Package
T = Tape & Reel
(no letter) = Tray

Default-Frequency and VCXO Pull Range
See Default Frequency & VCXO Pull-Range Ordering Information Table

I/O Identifier
0 = LVCMOS
3 = LVPECL
4 = LVDS

Ambient Temperature Range
"I" Industrial = (T_A = -40°C to 85°C)
(no letter) = (T_A = 0°C to 70°C)

Package Code
J = Lead-Free, 10-lead ceramic 5mm x 7mm x 1.55mm

Number of Default Frequencies
S = 1: Single
D = 2: Dual
Q = 4: Quad

Die Revision
A

Part Number
V01 = VCXO, (114.285MHz int. XTAL)
001 = XO, (114.285MHz int. XTAL)

Option Code (Supply Voltage and Frequency-Accuracy)
A = V_{DD} = 3.3V±5%,±100ppm
B = V_{DD} = 2.5V±5%,±100ppm
E = V_{DD} = 3.3V±5%, ±50ppm
F = V_{DD} = 2.5V±5%, ±50ppm
K = V_{DD} = 3.3V±5%, ±20ppm
L = V_{DD} = 2.5V±5%, ±20ppm

Marking	TBD

NOTE: For order information, see *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

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