Data Sheet

TI DN 2510443 Rev D

February 2012

DLP® Discovery™ 4100 Digital Controller (DDC4100)

This document describes the functionality of the Discovery™ 4100 Digital Controller (DDC4100). The DDC4100 provides the high-speed data and control interface for the 2XLVDS DMDs, and provides the DMD mirror reset and timing information to the DAD2000 DMD Power and Reset Driver.

Revisions		
Rev	Descriptions	Date
A	Initial release	August 2009
B	Added DCLKIN_* pin assignments to table 12	January 2010
C	Added note on initialization condition for RST2BLKZ, COMP_DATA, and NS_FLIP in sections 3.4 and 3.9	February 2011
D	Added 0.96 WUXGA Type A DMD	February 2012

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1 Overview

The Discovery™ Digital Controller 4100 (DDC4100) is the heart of the DLP® Discovery™ 4100 (D4100) Starter Kit. This document covers the functionality of the DDC4100. The DDC4100 provides the high-speed data and control interface for the TI 2XLVDS DMDs, and provides the DMD mirror reset and timing information to the TI DAD2000 DMD Power and Reset Drivers.

Below is a simplified system block diagram (Figure 1) showing the function of the D4100 with the following components:

- 2XLVDS DMD – Spatial Light Modulator
- DAD2000 – DMD reset drivers for DMD
- DDC4100 – Xilinx XC5VLX30 FPGA configured to provide high-speed DMD data and control, and DAD2000 timing and control

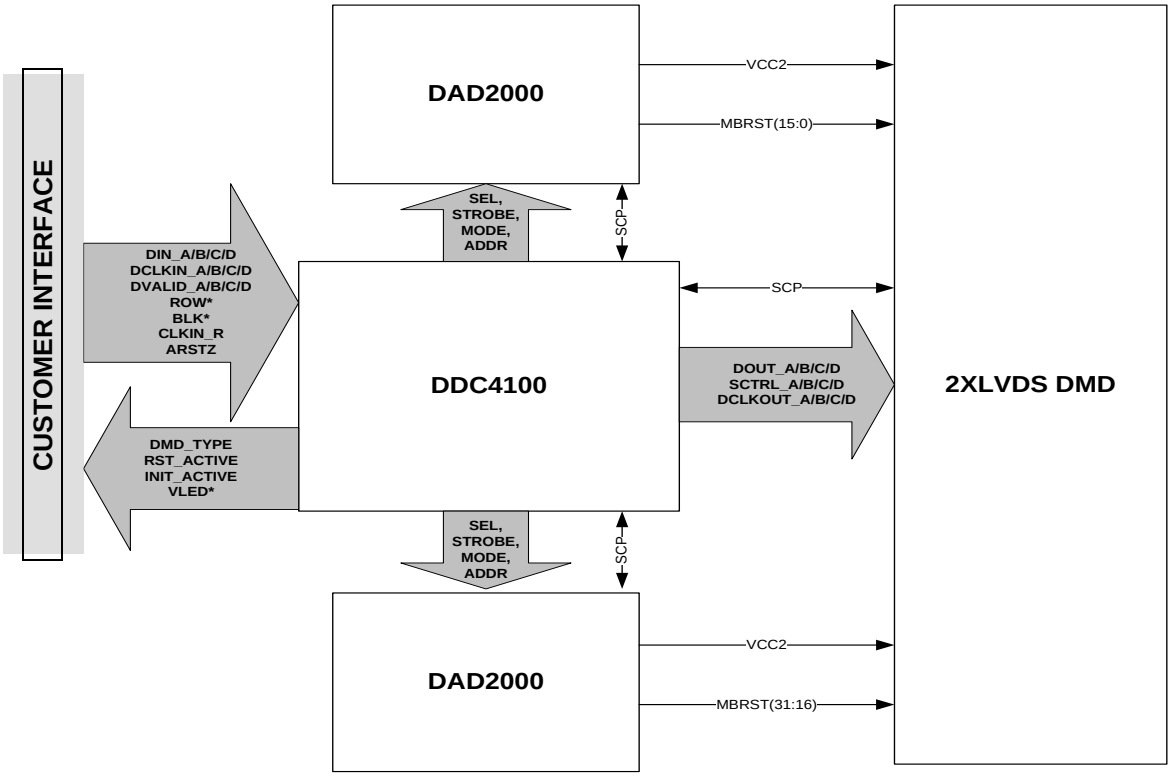

Figure 1. D4100 Functional Block Diagram

2 Electrical Interface

2.1 I/O

Table 1 lists the available controls and status pin names and their corresponding signal type, along with a brief functional description. A comprehensive description of pin functions is included in following sections.

Table 1. I/O Pin Descriptions

Pin Name	Description	I/O
ARSTZ	Asynchronous active low reset	I
CLKIN_R	Reference clock, 50 MHz	I
DDC_DIN_[A,B,C,D](15:0)	LVDS DDR input for Data Bus A,B,C,D (15:0)	I
DDC_DCLKIN_[A,B,C,D]	LVDS inputs for Data Clock (200 – 400MHz)	I
DVALID_[A,B,C,D]	LVDS inputs used to start write sequence for Data Busses	I
ROWMD(1:0)	DMD row address and row counter control	I
ROWAD(10:0)	DMD row address pointer	I
STEPVCC	Step DMD memory voltage to VCC2 to increase peak power threshold	I
COMP_DATA	Complement DMD input data	I
NS_FLIP	Reverse DMD row counter	I
BLK_AD(3:0)	DMD mirror block address pointer	I
BLK_MD(1:0)	DMD mirror block reset and clear command modes	I
WDT_ENBLZ	Enables watch-dog timer with auto DMD mirror reset	I
RST2BLKZ	Active low enable for dual block reset mode.	I
PWR_FLOAT	Used to float DMD mirrors before complete loss of power	I
DMD_TYPE(3:0)	DMD type in use	O
DDC_VERSION(2:0)	DDC4100 version number	O
RST_ACTIVE	Indicates DMD mirror reset in progress	O
INIT_ACTIVE	Initialization in progress.	O
VLED0	System “heartbeat” signal	O
VLED1	Denotes initialization complete	O

Pin Name	Description	I/O
DDCSPARE(1:0)	Extra signals reserved for future use	O
ECP2_FINISHED	Indicates DDC4100 configuration complete	O
SCPDI	Serial data bus input	I
SCPCLK	Serial data bus clock	O
SCPDO	Serial data bus output to DAD2000 and DMD	O
DAD_A_SCPENZ	Active low chip select for DAD2000 serial bus	O
DAD_A_STROBE	DAD2000 control signal strobe	O
DAD_A_MODE(1:0)	DAD2000 mode control	O
DAD_A_SEL(1:0)	DAD2000 select control	O
DAD_A_ADDR(3:0)	DAD2000 address control	O
DAD_B_SCPENZ	Active low chip select for DAD2000 serial bus	O
DAD_B_STROBE	DAD2000 control signal strobe	O
DAD_B_MODE(1:0)	DAD2000 mode control	O
DAD_B_SEL(1:0)	DAD2000 select control	O
DAD_B_ADDR(3:0)	DAD2000 address control	O
DAD_INIT	DAD2000 reset signal	O
DAD_OEZ	DAD2000 output enable	O
DMD_A_SCPENZ	Active low chip select for DMD serial bus	O
DMD_A_RESET	DMD active low reset	O
DDC_DOUT_[A,B,C,D](15:0)	LVDS DDR output to DMD Data Bus A,B,C,D (15:0)	O
DDC_DCLKOUT_[A,B,C,D]	LVDS output to DMD Data Clock A,B,C,D	O
DDC_SCTRL_[A,B,C,D]	LVDS DDR output to DMD Data Control A,B,C,D	O
ECP2M_TP(31:0)	Signals reserved for test access	O

3 DDC4100 Control Interface

3.1 Clocks and Reset Inputs

3.1.1 ARSTZ

ARSTZ is an active low, asynchronous reset. This reset can be sourced from a voltage supervisor or from the customer interface. Be aware that the chipset will not operate correctly if all DDC4100 power supplies are not in range at the time this reset is released.

3.1.2 CLKIN_R

The reference clock, CLKIN_R, supplied from an oscillator must be 50MHz. This is required for precise timing used to perform the DMD mirror reset. This clock should be valid prior to releasing ARSTZ.

3.1.3 DDC_DCLKIN_[A, B, C, D]

The data clock, DDC_DCLKIN, must operate continuously. All signals associated with the data clock should be synchronous to these signals. For example, DDC_DIN_* and DVALID should be synchronous to the rising edge of DDC_DCLKIN. This clock should be valid prior to releasing ARSTZ. DDC_DCLKIN is a DDR clock with data loaded on both rising and falling edges of DDC_DCLKIN. The jitter on this clock should be minimal.

3.2 Control Inputs

The DDC4100 supports four 2XLVDS DMD types as shown in Table 2:

Table 2. DMD Characteristics

TYPE	DMD_TYPE	#COLS	#ROWS	#BLKS	#ROWS /BLK	#CLKS/ ROW	#DIN
.96 WUXGA Type A	101	1920	1200	15	80	16	64
.95 1080p Type A	000	1920	1080	15	72	16	64
.7 XGA Type A	001	1024	768	16	48	16	32
.55 XGA Type X	011	1024	768	16	48	16	32

Note 1: The 1080p DMD is loaded as 15 blocks of 72 rows each. The WUXGA DMD is loaded as 15 blocks of 72 rows each. The first 64 bits of pixel data and last 64 bits of pixel data for all rows are not visible in both the DMDs.

3.2.1 DMD Operations

The DMD memory is loaded one row at a time by 2 or 4 semi-independent LVDS buses A,B or A,B,C,D. The 1080p and WUXGA DMDs require all 4 data buses A,B,C,D while the XGA DMDs require only 2 data buses A,B. Each DDC_DIN* bus is comprised of 16 differential pairs of LVDS signals that are input to the DDC4100 as listed in Table 1. Data and control are clocked into the DMD on both the rising and falling edges of the DDR data clocks DDC_DCLKOUT_[A, B, C, D].

For each row cycle, #CLKS/ROW clock cycles and 32 or 64 data lines load #COLS bits into the DMD (Table 2).

Data loading will not cause mirror movement until a reset operation is completed.

3.3 DDC4100 LVDS Input Data Bus Operations

Figure 2 shows an example of how the data should be formatted for 1080p and WUXGA DMDs which takes 16 clocks to load a row. The clock should be synchronous and edge aligned with all data and control signals. Depending on the design, skewing the clock to data relationship may cause a problem

No visible data is loaded for the first clock cycle for A and B data and for the last clock cycle for C and D data for each row load operation. This only applies to the 1080p and WUXGA DMDs.

Figure 3 shows an example of the data formatting for the XGA DMDs.

The DVALID signal should be asserted synchronous to the data it is meant to frame. DVALID can be asserted as:

- Framing individual row loads with breaks between rows
- Framing block loads
- Framing the entire DMD load

If the DVALID frames blocks or the whole DMD, assure that block and row controls are adjusted at the proper locations in the data stream. See section 3.4 for further information.

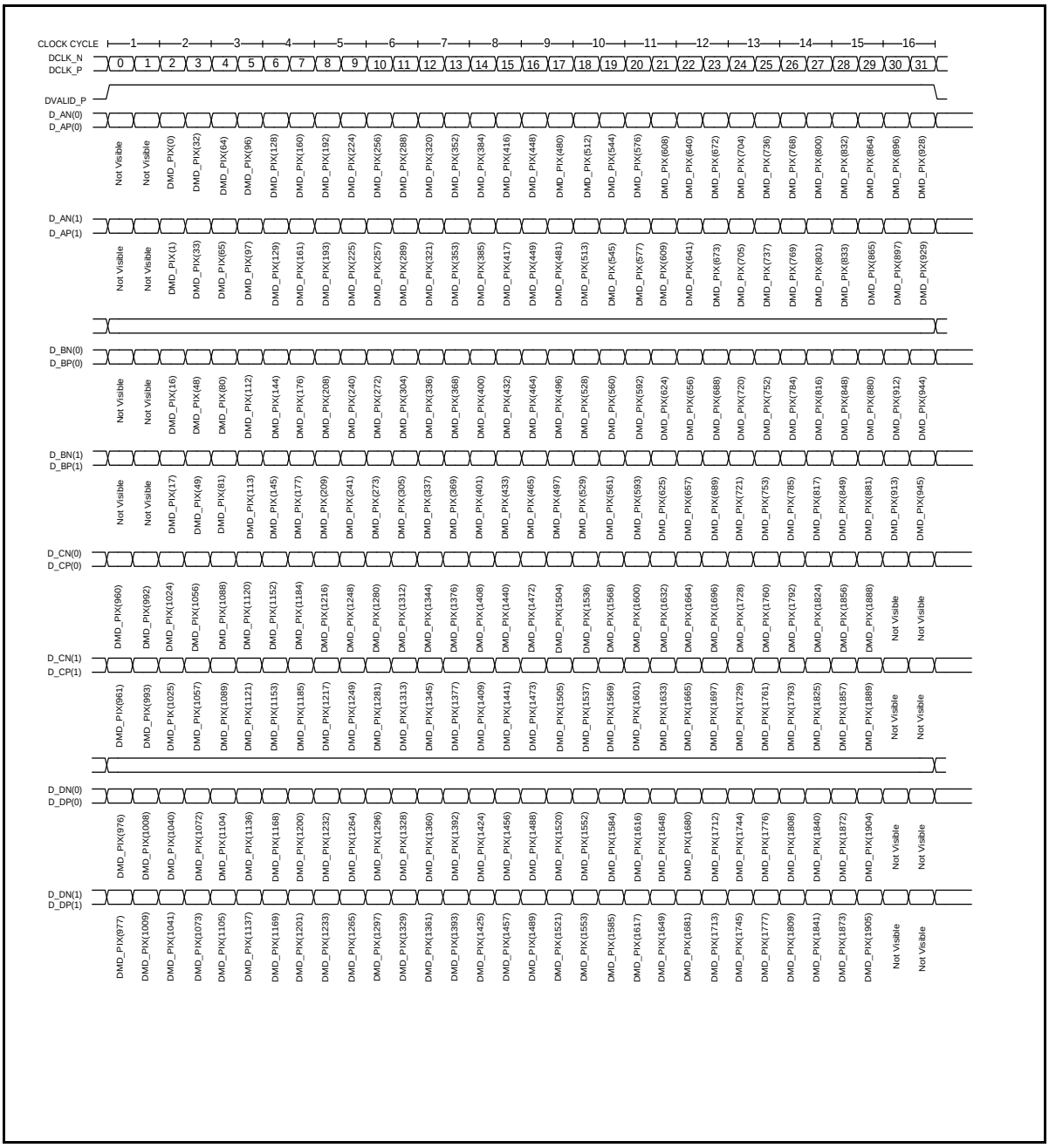

Figure 2. 1080p and WUXGA 2XLVDS DMD Input Data Bus

Table 3. 1080p and WUXGA 2XLVDS DMD Data Pixel Mapping

DCLK Edge	D_A(0)	D_A(1)	D_A(2)	D_A(3)	D_A(4)	D_A(5)	D_A(6)	D_A(7)	D_A(8)	D_A(9)	D_A(10)	D_A(11)	D_A(12)	D_A(13)	D_A(14)	D_A(15)
0	Not Visible															
1																
2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
3	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
5	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
6	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
7	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
8	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
9	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
10	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271
11	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
12	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335
13	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367
14	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399
15	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431
16	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463
17	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495
18	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527
19	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559
20	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591
21	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623
22	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655
23	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687

24	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719
25	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751
26	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783
27	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815
28	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847
29	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879
30	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911
31	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943

DCLK Edge	D_B(0)	D_B(1)	D_B(2)	D_B(3)	D_B(4)	D_B(5)	D_B(6)	D_B(7)	D_B(8)	D_B(9)	D_B(10)	D_B(11)	D_B(12)	D_B(13)	D_B(14)	D_B(15)
0	Not Visible															
1																
2	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
4	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
5	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
6	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
7	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
8	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
9	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
10	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
11	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
12	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
13	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
14	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
15	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447

16	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
17	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511
18	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
19	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
20	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
21	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
22	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
23	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
24	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
25	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
26	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
27	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
28	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
29	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
30	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
31	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959

DCLK Edge	D_C(0)	D_C(1)	D_C(2)	D_C(3)	D_C(4)	D_C(5)	D_C(6)	D_C(7)	D_C(8)	D_C(9)	D_C(10)	D_C(11)	D_C(12)	D_C(13)	D_C(14)	D_C(15)
0	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975
1	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007
2	1024	1025	1026	1027	1028	1029	1030	1031	1032	1033	1034	1035	1036	1037	1038	1039
3	1056	1057	1058	1059	1060	1061	1062	1063	1064	1065	1066	1067	1068	1069	1070	1071

4	1088	1089	1090	1091	1092	1093	1094	1095	1096	1097	1098	1099	1100	1101	1102	1103
5	1120	1121	1122	1123	1124	1125	1126	1127	1128	1129	1130	1131	1132	1133	1134	1135
6	1152	1153	1154	1155	1156	1157	1158	1159	1160	1161	1162	1163	1164	1165	1166	1167
7	1184	1185	1186	1187	1188	1189	1190	1191	1192	1193	1194	1195	1196	1197	1198	1199
8	1216	1217	1218	1219	1220	1221	1222	1223	1224	1225	1226	1227	1228	1229	1230	1231
9	1248	1249	1250	1251	1252	1253	1254	1255	1256	1257	1258	1259	1260	1261	1262	1263
10	1280	1281	1282	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293	1294	1295
11	1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324	1325	1326	1327
12	1344	1345	1346	1347	1348	1349	1350	1351	1352	1353	1354	1355	1356	1357	1358	1359
13	1376	1377	1378	1379	1380	1381	1382	1383	1384	1385	1386	1387	1388	1389	1390	1391
14	1408	1409	1410	1411	1412	1413	1414	1415	1416	1417	1418	1419	1420	1421	1422	1423
15	1440	1441	1442	1443	1444	1445	1446	1447	1448	1449	1450	1451	1452	1453	1454	1455
16	1472	1473	1474	1475	1476	1477	1478	1479	1480	1481	1482	1483	1484	1485	1486	1487
17	1504	1505	1506	1507	1508	1509	1510	1511	1512	1513	1514	1515	1516	1517	1518	1519
18	1536	1537	1538	1539	1540	1541	1542	1543	1544	1545	1546	1547	1548	1549	1550	1551
19	1568	1569	1570	1571	1572	1573	1574	1575	1576	1577	1578	1579	1580	1581	1582	1583
20	1600	1601	1602	1603	1604	1605	1606	1607	1608	1609	1610	1611	1612	1613	1614	1615
21	1632	1633	1634	1635	1636	1637	1638	1639	1640	1641	1642	1643	1644	1645	1646	1647
22	1664	1665	1666	1667	1668	1669	1670	1671	1672	1673	1674	1675	1676	1677	1678	1679
23	1696	1697	1698	1699	1700	1701	1702	1703	1704	1705	1706	1707	1708	1709	1710	1711
24	1728	1729	1730	1731	1732	1733	1734	1735	1736	1737	1738	1739	1740	1741	1742	1743
25	1760	1761	1762	1763	1764	1765	1766	1767	1768	1769	1770	1771	1772	1773	1774	1775
26	1792	1793	1794	1795	1796	1797	1798	1799	1800	1801	1802	1803	1804	1805	1806	1807
27	1824	1825	1826	1827	1828	1829	1830	1831	1832	1833	1834	1835	1836	1837	1838	1839
28	1856	1857	1858	1859	1860	1861	1862	1863	1864	1865	1866	1867	1868	1869	1870	1871
29	1888	1889	1890	1891	1892	1893	1894	1895	1896	1897	1898	1899	1900	1901	1902	1903
30																
31								Not	Visible							

DCLK Edge	D_D(0)	D_D(1)	D_D(2)	D_D(3)	D_D(4)	D_D(5)	D_D(6)	D_D(7)	D_D(8)	D_D(9)	D_D(10)	D_D(11)	D_D(12)	D_D(13)	D_D(14)	D_D(15)
0	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
1	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023
2	1040	1041	1042	1043	1044	1045	1046	1047	1048	1049	1050	1051	1052	1053	1054	1055
3	1072	1073	1074	1075	1076	1077	1078	1079	1080	1081	1082	1083	1084	1085	1086	1087
4	1104	1105	1106	1107	1108	1109	1110	1111	1112	1113	1114	1115	1116	1117	1118	1119
5	1136	1137	1138	1139	1140	1141	1142	1143	1144	1145	1146	1147	1148	1149	1150	1151
6	1168	1169	1170	1171	1172	1173	1174	1175	1176	1177	1178	1179	1180	1181	1182	1183
7	1200	1201	1202	1203	1204	1205	1206	1207	1208	1209	1210	1211	1212	1213	1214	1215
8	1232	1233	1234	1235	1236	1237	1238	1239	1240	1241	1242	1243	1244	1245	1246	1247
9	1264	1265	1266	1267	1268	1269	1270	1271	1272	1273	1274	1275	1276	1277	1278	1279
10	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
11	1328	1329	1330	1331	1332	1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343
12	1360	1361	1362	1363	1364	1365	1366	1367	1368	1369	1370	1371	1372	1373	1374	1375
13	1392	1393	1394	1395	1396	1397	1398	1399	1400	1401	1402	1403	1404	1405	1406	1407
14	1424	1425	1426	1427	1428	1429	1430	1431	1432	1433	1434	1435	1436	1437	1438	1439
15	1456	1457	1458	1459	1460	1461	1462	1463	1464	1465	1466	1467	1468	1469	1470	1471
16	1488	1489	1490	1491	1492	1493	1494	1495	1496	1497	1498	1499	1500	1501	1502	1503
17	1520	1521	1522	1523	1524	1525	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535
18	1552	1553	1554	1555	1556	1557	1558	1559	1560	1561	1562	1563	1564	1565	1566	1567
19	1584	1585	1586	1587	1588	1589	1590	1591	1592	1593	1594	1595	1596	1597	1598	1599
20	1616	1617	1618	1619	1620	1621	1622	1623	1624	1625	1626	1627	1628	1629	1630	1631
21	1648	1649	1650	1651	1652	1653	1654	1655	1656	1657	1658	1659	1660	1661	1662	1663
22	1680	1681	1682	1683	1684	1685	1686	1687	1688	1689	1690	1691	1692	1693	1694	1695
23	1712	1713	1714	1715	1716	1717	1718	1719	1720	1721	1722	1723	1724	1725	1726	1727

24	1744	1745	1746	1747	1748	1749	1750	1751	1752	1753	1754	1755	1756	1757	1758	1759
25	1776	1777	1778	1779	1780	1781	1782	1783	1784	1785	1786	1787	1788	1789	1790	1791
26	1808	1809	1810	1811	1812	1813	1814	1815	1816	1817	1818	1819	1820	1821	1822	1823
27	1840	1841	1842	1843	1844	1845	1846	1847	1848	1849	1850	1851	1852	1853	1854	1855
28	1872	1873	1874	1875	1876	1877	1878	1879	1880	1881	1882	1883	1884	1885	1886	1887
29	1904	1905	1906	1907	1908	1909	1910	1911	1912	1913	1914	1915	1916	1917	1918	1919
30	Not Visible															
31																

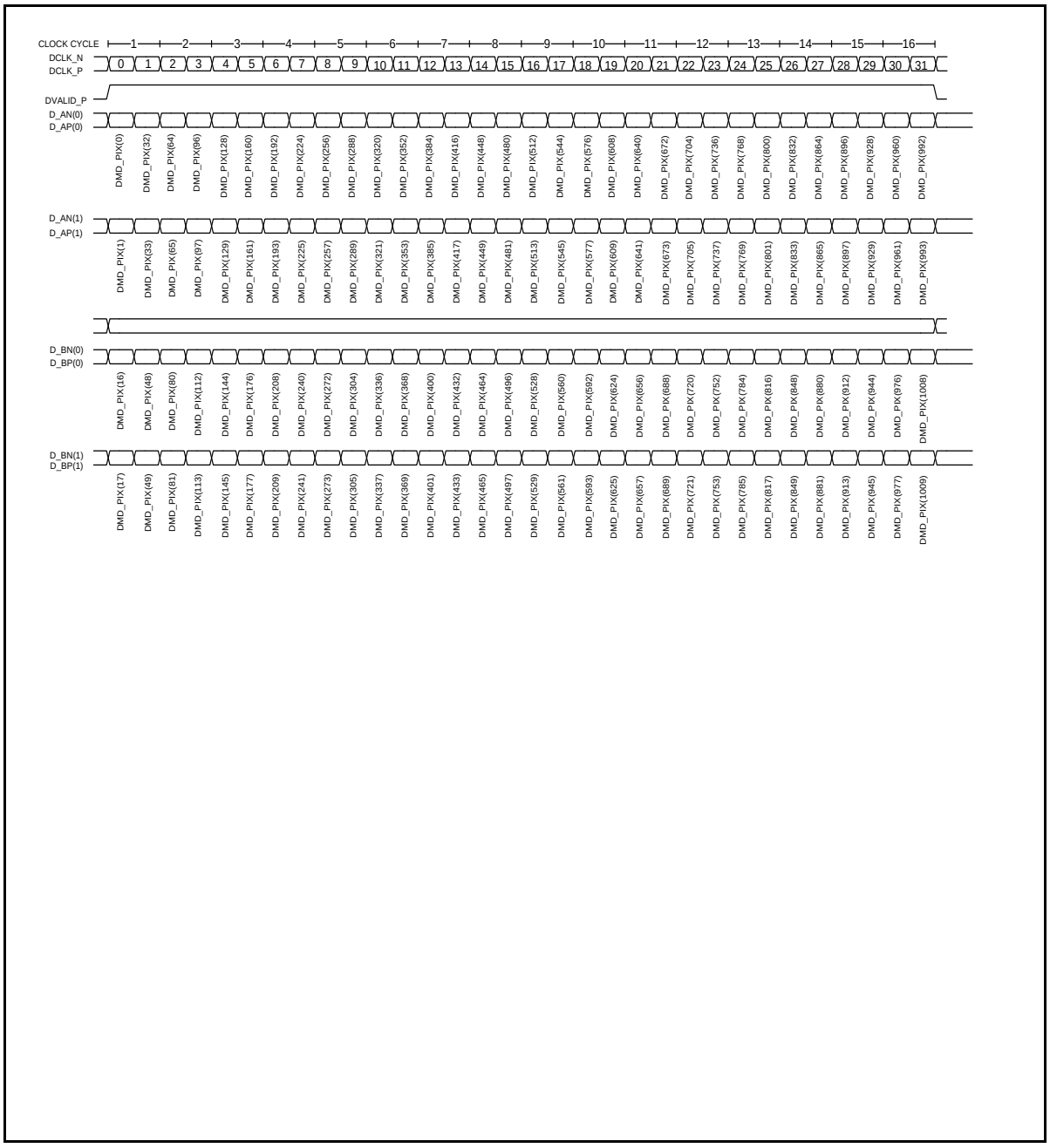

Figure 3. XGA 2XLVDS DMD Input Data Bus

Table 4. XGA 2XLVDS DMD Data Pixel Mapping

DCLK Edge	D_A(0)	D_A(1)	D_A(2)	D_A(3)	D_A(4)	D_A(5)	D_A(6)	D_A(7)	D_A(8)	D_A(9)	D_A(10)	D_A(11)	D_A(12)	D_A(13)	D_A(14)	D_A(15)
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
2	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
3	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
4	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
5	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
6	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
7	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
8	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271
9	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
10	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335
11	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367
12	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399
13	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431
14	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463
15	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495
16	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527
17	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559
18	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591
19	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623
20	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655
21	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687

22	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719
23	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751
24	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783
25	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815
26	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847
27	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879
28	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911
29	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943
30	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975
31	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007

DCLK Edge	D_B(0)	D_B(1)	D_B(2)	D_B(3)	D_B(4)	D_B(5)	D_B(6)	D_B(7)	D_B(8)	D_B(9)	D_B(10)	D_B(11)	D_B(12)	D_B(13)	D_B(14)	D_B(15)
0	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
1	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
2	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
3	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
4	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
5	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
6	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
7	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
8	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
9	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
10	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
11	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383

12	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
13	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
14	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
15	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511
16	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
17	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
18	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
19	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
20	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
21	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
22	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
23	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
24	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
25	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
26	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
27	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
28	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
29	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959
30	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
31	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

3.4 Block Operations

The DMD mirrors and corresponding SRAM pixels are organized into #BLKS and each block is broken into groups of #ROWS/BLK as described in Table 2. Mirror blocks are addressed for either the mirror reset or memory clear functions by asserting block control signals at the start of each row data load. RST2BLKZ, BLK_MD and BLK_AD are used as shown in Table 5 to designate which mirror block(s) is to be reset or cleared. Refer to the individual DMD data sheets for block location information.

- The clear operation sets all of the SRAM pixels in the designated block to logic zero during the current row cycle.
- It is possible to reset a block while loading a different block.
- It is not possible to clear a block while writing to a different block.
- It is not necessary to clear a block if it is going to be reloaded with new data (just like a normal memory cell).
- For the 1080p and WUXGA DMDs a block clear operation must be followed by two no-op row load cycles.
- Note that the 1080p and WUXGA DMD have 15 blocks (block 00 – block 14) so block operations on block 15 have no function for this DMD.
- It is recommended that RST2BLKZ be set to one value and not adjusted during normal system operation. A change in RST2BLKZ is not immediately effective and will require more than one row load cycle to complete.

WARNING: 1080p and WUXGA DMD only

To clear 1 Reset Group in the DMD Block, 1 Clear command followed by 2 consecutive No Operation commands are required. Therefore, 15 total Block Clear commands and 30 total No Operation commands are required to clear the entire DMD array.

Note: RST2BLKZ needs to be kept low during initialization for proper setup of the system. (NOT required in version 5 of the DDC4100)

Table 5. Block Operations

RST2BLKZ	BLK_MD 1	BLK_MD 0	BLK_AD 3	BLK_AD 2	BLK_AD 1	BLK_AD 0	Operation
X	0	0	X	X	X	X	None
X	0	1	0	0	0	0	Clear block 00
X	0	1	0	0	0	1	Clear block 01
X	0	1	0	0	1	0	Clear block 02
X	0	1	0	0	1	1	Clear block 03
X	0	1	0	1	0	0	Clear block 04
X	0	1	0	1	0	1	Clear block 05

RST2BLKZ	BLK_MD 1	BLK_MD 0	BLK_AD 3	BLK_AD 2	BLK_AD 1	BLK_AD 0	Operation
X	0	1	0	1	1	0	Clear block 06
X	0	1	0	1	1	1	Clear block 07
X	0	1	1	0	0	0	Clear block 08
X	0	1	1	0	0	1	Clear block 09
X	0	1	1	0	1	0	Clear block 10
X	0	1	1	0	1	1	Clear block 11
X	0	1	1	1	0	0	Clear block 12
X	0	1	1	1	0	1	Clear block 13
X	0	1	1	1	1	0	Clear block 14
X	0	1	1	1	1	1	Clear block 15
X	1	0	0	0	0	0	Reset block 00
X	1	0	0	0	0	1	Reset block 01
X	1	0	0	0	1	0	Reset block 02
X	1	0	0	0	1	1	Reset block 03
X	1	0	0	1	0	0	Reset block 04
X	1	0	0	1	0	1	Reset block 05
X	1	0	0	1	1	0	Reset block 06
X	1	0	0	1	1	1	Reset block 07
X	1	0	1	0	0	0	Reset block 08
X	1	0	1	0	0	1	Reset block 09
X	1	0	1	0	1	0	Reset block 10
X	1	0	1	0	1	1	Reset block 11
X	1	0	1	1	0	0	Reset block 12
X	1	0	1	1	0	1	Reset block 13
X	1	0	1	1	1	0	Reset block 14
X	1	0	1	1	1	1	Reset block 15
0	1	1	0	0	0	0	Reset blocks 00-01
0	1	1	0	0	0	1	Reset blocks 02-03

RST2BLKZ	BLK_MD 1	BLK_MD 0	BLK_AD 3	BLK_AD 2	BLK_AD 1	BLK_AD 0	Operation
0	1	1	0	0	1	0	Reset blocks 04-05
0	1	1	0	0	1	1	Reset blocks 06-07
0	1	1	0	1	0	0	Reset blocks 08-09
0	1	1	0	1	0	1	Reset blocks 10-11
0	1	1	0	1	1	0	Reset blocks 12-13
0	1	1	0	1	1	1	Reset blocks 14-15
1	1	1	0	0	0	X	Reset blocks 00-03
1	1	1	0	0	1	X	Reset blocks 04-07
1	1	1	0	1	0	X	Reset blocks 08-11
1	1	1	0	1	1	X	Reset blocks 12-15
X	1	1	1	0	X	X	Reset blocks 00-15
X	1	1	1	1	X	X	Float blocks 00-15

3.4.1 Mirror Reset and Float Operations

A mirror reset sequence begins by asserting BLK_MD and BLK_AD as described in Table 5. Shortly after, RST_ACTIVE will go high for approximately 4.5us, indicating a reset operation is in progress. During this time, no additional resets may be initiated until RST_ACTIVE returns low. RST_ACTIVE will not return to low unless continuous no-op or data loading row cycles are issued. Refer to Figure 4 and Figure 5 for typical reset sequences in which consecutive DMD blocks are loaded then reset. Reset time is identical for single, dual, quad or global reset operations.

Note that it may take longer to reset a block than it does to load, depending on the clock rate and the DMD type, so the scenario in Figure 4 does not show the situation when the reset time exceeds the block load time. The block load time may be calculated as:

Block Load Time = Clock Period * #CLKS/ROW * #ROWS/BLK

DMD	Minimum Block Load Time
XGA	1.92 usec
1080p	2.88 usec
WUXGA	3.2 usec

Table 6. DMD Block Load Time at 400MHz DMD Clock

For any case which involves resetting or clearing blocks without data loading, the customer interface must send no-op row cycles. This can be accomplished by asserting DVALID, while holding ROWMD at “00”

and BLKMD at “00” for #CLKS/ROW (Table 2) clock cycles, as in Figure 6. For example, the sequence shown in Figure 5 does not show the required no-op row during the Delay cycle where the reset of Block 0 occurs. At least one row cycle must be completed to initiate the reset. The same procedure applies to the global reset case as shown in Figure 7. Following the loading of all rows in the device, a no-op row cycle must be completed to initiate the reset. If the global reset is asserted prior to loading all rows of the device, rows which were not updated will show old data. Additional reset operations may not be initiated until RST_ACTIVE is low. Block clear operations for 1080p and WUXGA DMDs must be followed by two consecutive no-op row cycle commands.

To obtain full utilization of the 1080p and WUXGA DMD bandwidths (at 400MHz data rate), load and reset two blocks at a time by setting RST2BLKZ to “0” and BLK_MD to “11” and the appropriate address in BLK_AD. This method is indicated in Figure 8. To obtain full utilization of the XGA DMD bandwidth (at 400MHz data rate), load and reset four blocks at a time by setting RST2BLKZ to “1” and BLK_MD to “11” and the appropriate address in BLK_AD.

Important:

While RST_ACTIVE is high, and for 8us after, the data for the block(s) being reset should not be changed to allow for the settling required for the mirrors to become stable.

It is possible to load other blocks while the previously reset block is settling. Figure 9 shows a single block load, reset and reload sequence with the light gray areas indicating mirror settling time.

It is best to issue a float command to avoid leaving a static image on the DMD for extended periods of time. A mirror float sequence begins by asserting the proper BLK_MD and BLK_AD as described in Table 5. During the following row cycle, the DMD releases the tension under each mirror so that all mirrors are in a relatively flat position. The float operation takes approximately 3us to complete, during which time RST_ACTIVE is asserted.

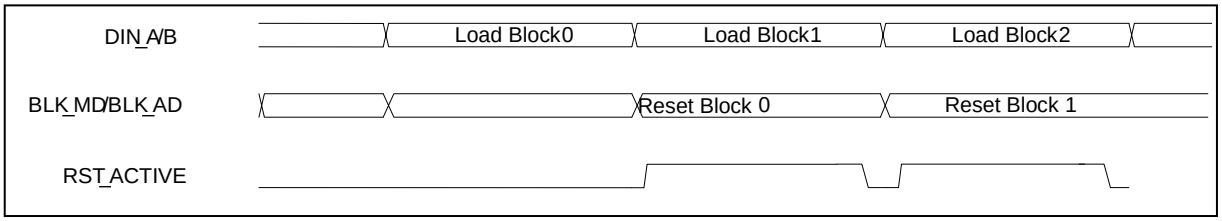

Figure 4. Typical Phased Reset Sequence

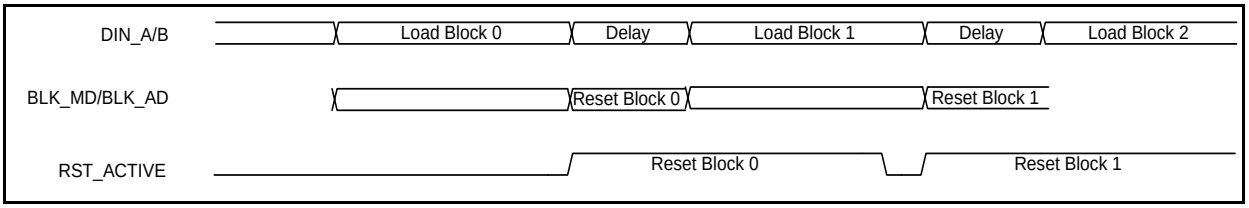

Figure 5. Alternate Phased Reset Sequence

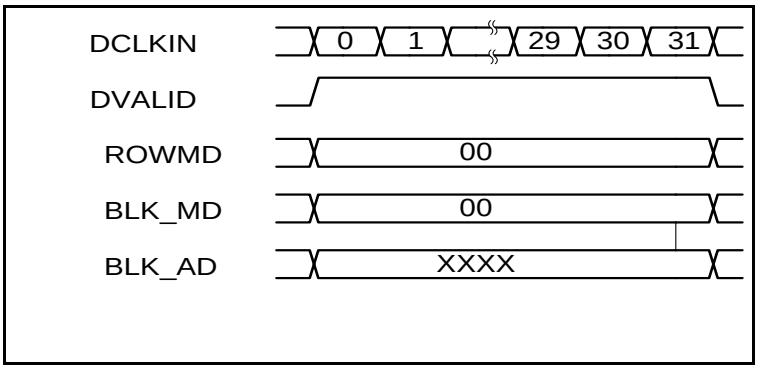

Figure 6. DMD No-op Row Cycle

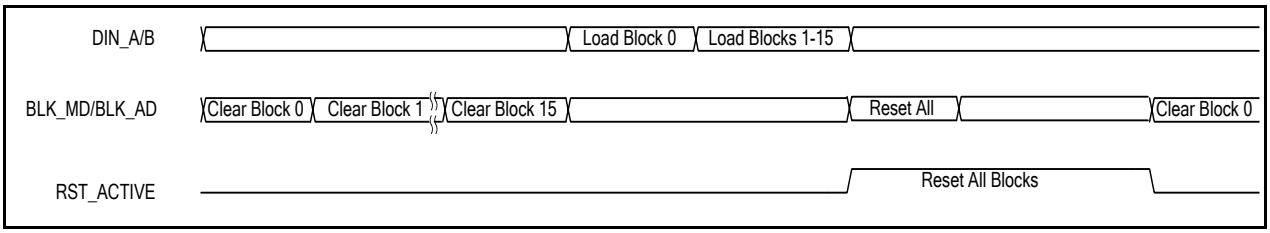

Figure 7. Full Device Load and Global Reset

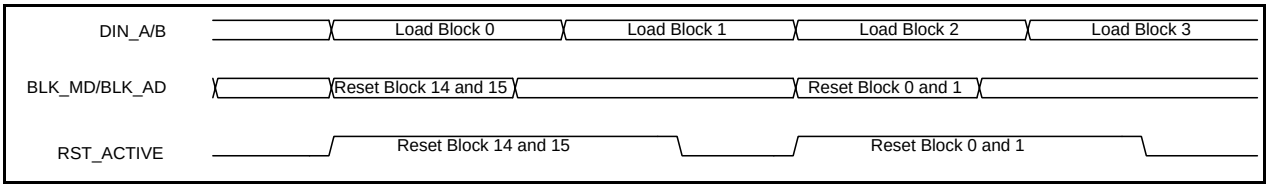

Figure 8. Phased Reset Sequence with Dual Block Resets without Memory Clear

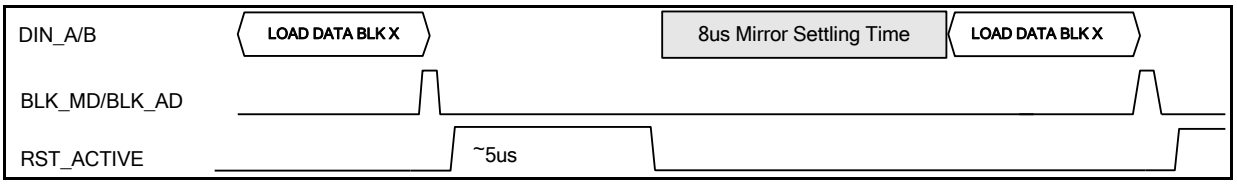

Figure 9. Block Load and Reload

Note:

After a reset or clear command is given, RST_ACTIVE may not be asserted until up to 60ns (depending on the clock frequency) after the command. During this time, no other command should be given.

3.4.2 Power Down Operation

For correct operation of DMD, the following power down procedure must be executed. Prior to power removal, assert PWR_FLOAT and allow approximately 300 µs for the procedure to complete. This procedure will assure the mirrors are in a flat state, similar to the float operation. On the evaluation platform, SW2 should be pressed momentarily to execute the shutdown procedure. Following this procedure, the power can be safely removed.

To restart after assertion of PWR_FLOAT the DDC4100 must be reset (ARSTZ low then high) or power must be cycled.

3.4.3 Global Reset Consideration

A global reset (BLK_MD = “11” and BLK_AD = “10XX”), takes the same amount of time as the single, dual, and quad block resets. In addition to requiring a no-op row cycle to initiate a global reset, a row cycle (either no-op or data loading) is also required to complete the operation. If the customer interface is monitoring RST_ACTIVE to determine when to send a subsequent row cycle, it will never see RST_ACTIVE transition low. One method of operation would be to continue sending no-op row cycles until RST_ACTIVE goes low then continue loading data with real row cycles. Another method of operation is to delay greater than 4.5us, then start loading new data to DMD.

3.4.4 RST_ACTIVE

After a mirror reset or float operation is requested, RST_ACTIVE will be asserted to indicate that the operation is in progress. Section 3.4.1 has more details about the use of this signal. RST_ACTIVE is synchronized to a version of DCLKIN. As such, circuits in the application FPGA should consider this signal asynchronous and use standard synchronization techniques to assure reliable registering of this signal.

3.4.5 Interface Training Pattern

The DDC4100 detects the phase differences between the ½ speed clock (used in the device driving the LVDS data) and the internally generated ½ speed data clocks and will automatically correct their alignment. This is done by supplying a simple repeating pattern on all of the data inputs while the "INIT_ACTIVE" output of the DDC4100 is high/active. The details of the training pattern are described below.

This is a simple block diagram of the training pattern insertion logic. TI will also provide example RTL code for the interface itself.

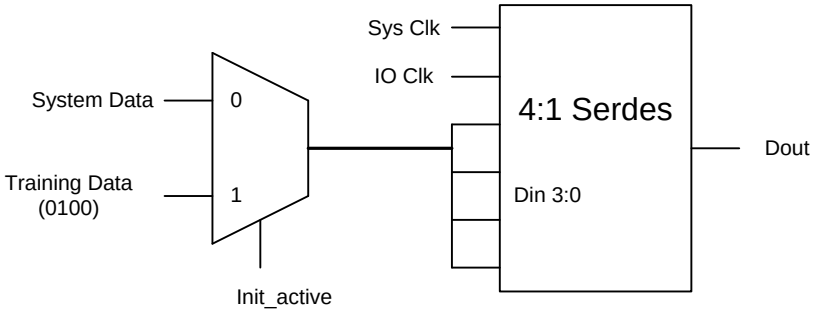

Figure 10. Block Diagram of Training Pattern Logic

The expected training pattern is "0100". In the diagram shown below, the data input to the 4:1 SERDES cells is captures on the rising edge of the ½ speed system clock. The output latency shown is based on the documentation for the Xilinx SERDES cells. Individual implementation may vary depending on the type of cells, technology, and design technique used.

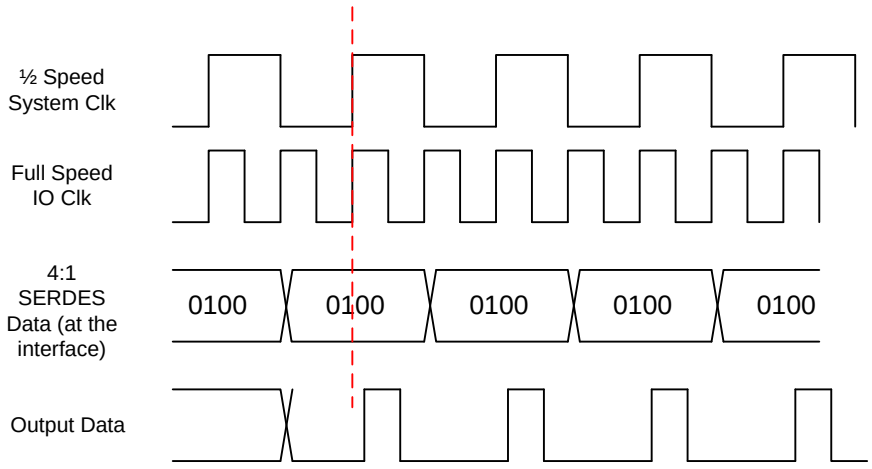

Figure 11. Training Pattern Alignment

Note: In Xilinx FPGA's (due to the construction of the ISERDES and OSERDES cells) a pattern of "0010" needs to be applied to the output/transmitting SERDES cells data pins (D1 = 0, D2 = 0, D3 = 1, D4 = 0) in order to receive a result of "0100" (Q1 = 0, Q2 = 1, Q3 = 0, Q4 = 0) at the input/receiving SERDES cell.

The patterns should be applied on all of the data and dvalid pins. In this respect, the interface is treated as a 17 bit interface with dvalid being the 17th data bit. The receiving logic in the DDC4100 will shift the data until the correct pattern is seen at the inputs. The SERDES cells align the incoming data with the ½ speed system clock (derived from the full speed data clock). This allows us to correctly align the dvalid signal and the incoming data and will contribute to a more robust interface. It is important that the training pattern is applied to the dvalid and data inputs of the DDC4100 before reset to the device is de-asserted, as training commences immediately on the de-assertion of reset. The INIT_ACTIVE signal is asserted while the device is held in reset in order to help facilitate this behavior.

3.4.6 System Initialization signals

The INIT_ACTIVE signal indicates that the DMD, DAD, and DDC are in an initialization state after power is applied. During this initialization period, the DDC is calibrating the data interface, and initializing the DMD and DAD2000 by setting all internal registers to their correct states. When this signal goes low, the system has completed initialization. System initialization takes approximately 220 ms to complete. Data and command write cycles must not be asserted during the initialization. This signal is driven by a CLK_R register and should be considered an asynchronous signal. Standard synchronization techniques should be applied if monitoring this signal with a synchronous circuit clocked by a clock other than CLK_R. After initialization is complete, a delay of at least 64 clocks should be observed before the first DVALID is asserted (to ensure a clean start up process).

Note: The NS_FLIP, COMP_DATA, and RST2BLKZ signals should be kept low during initialization to ensure proper setup of the system. (NOT required in version 5 of the DDC4100)

3.5 LED0

The LED0 signal is typically connected to an LED to show that the DDC4100 is operating normally. The signal is 1Hz with 50% duty cycle, otherwise known as the heartbeat.

3.6 LED1

The LED1 signal is typically connected to an LED indicator to show the status of system initialization and the status of the clock circuits. The LED1 signal is asserted only when system initialization is complete and clock circuits are initialized. Logically, these signals are ANDed together to show an indication of the health of the system. If the Phase Locked Loop (PLL) connected to the data clock and the DMD clock are functioning correctly after system initialization, the LED will be illuminated.

3.7 Data and Command Write Cycle

Once initialization is complete (INIT_ACTIVE = 0) the user is free to send data and control information to the DDC4100. When the user asserts the DVALID signal for the LVDS input buses, the DDC begins sampling the LVDS data inputs and synchronously sending this information to the DMD along with row address control information. The row cycle period is exactly #CLKS/ROW (Table 2) clocks long and begins with DVALID as shown in Figure 2. 1080p and WUXGA 2XLVDS DMD Input Data Bus. If DVALID is removed, the DDC will stop loading data and commands until DVALID goes active again.

Figure 12 shows an example of data written to the DDC4100 for a single row using the XGA DMD. Data is written to the DMD 32 bits (16 A bits + 16 B bits) on each clock edge. An entire line must be written for data to be latched into memory and it requires #CLKS/ROW (Table 2) DDR clock cycles to write a single

row of #COLS (Table 2) bits. For the 1080p and WUXGA DMDs, 64 data bits (16 A bits + 16 B bits + 16 C bits + 16 D bits) are written on each clock edge. C data and D data bits are not used for XGA DMDs.

The DMD incorporates single row write operations using a row address counter that is randomly addressable. As shown in

Table 7 and Table 8, ROWMD(1:0) determines the single row write count mode and ROWAD(10:0) determines the single row write address. ROWMD and ROWAD must be asserted and de-asserted synchronously with DVALID and must be valid synchronous to the beginning of the data as shown in Figure 12.

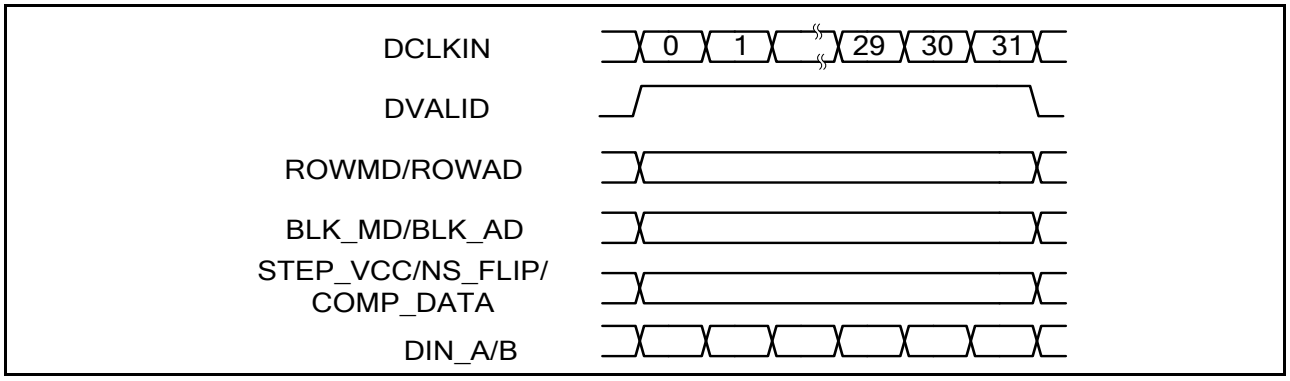

Figure 12. Single Row Write Operation

Row address orientation depends on the North / South Flip Flag (NS_FLIP) input to the DDC4100. Refer to the individual DMD data sheets for orientation of rows, columns, and reset blocks. The row address counter does not automatically wrap-around when using the increment row address pointer instruction. After the final row is addressed, the row address pointer must be cleared to 0.

Table 7. Row Write Modes - N/S Flip Flag = 0

ROWMD		ROWAD											Action
1	0	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	None
0	1	0	0	0	0	0	0	0	0	0	0	0	Increment row address pointer and write the concurrent data into that row
1	0	R	R	R	R	R	R	R	R	R	R	R	Set row address pointer to R and write the concurrent data into that row.
1	1	0	0	0	0	0	0	0	0	0	0	0	Clear row address pointer to 0 and write concurrent data into first row (e.g. row ‘0’)

Table 8. Row Write Modes - N/S Flip Flag = 1

ROWMD		ROWAD											Action
1	0	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	0	0	0	None
0	1	0	0	0	0	0	0	0	0	0	0	0	Decrement the row address pointer and write the concurrent data into that row
1	0	R	R	R	R	R	R	R	R	R	R	R	Set the row address pointer to R and write the concurrent data into that row.
1	1	0	0	0	0	0	0	0	0	0	0	0	PreSet row address pointer to row last row and write concurrent data into last row (e.g. row '767' for XGA)

3.8 Watchdog Timer

The DDC4100 contains a watchdog timer that initiates a global DMD mirror reset in the event that any DMD mirror reset block has not been reset by the user within 10 seconds. This auto-reset function can be disabled by taking WDT_ENABLEZ high.

3.9 Miscellaneous DMD Controls

It is recommended that the Complement and Flip flags be set to one value and not adjusted during normal system operation. These controls are asserted through a different mechanism than the data and row controls, hence their effect is asynchronous and cannot be expected to take effect immediately upon assertion.

3.9.1 Complement Data

By setting the COMP_DATA flag high, the user is able to command the DMD to internally complement its data inputs prior to loading the data into the mirror array. At least 0.6ms is needed for the signal to be loaded. This signal should not be used to invert data on a row basis. When used with the "Clear" command, the mirrors are still set to zero regardless of the COMP_DATA bit.

Note: The COMP_DATA signal should be kept low during initialization to ensure proper setup of the system. (NOT required in version 5 of the DDC4100)

3.9.2 North / South Flip

NS_FLIP allows the user to specify the loading direction of rows in the DMD when used with ROWMD = "01". This control will have no effect if ROWMD = "10".

Table 7 and Table 8 describe the effect of N/S flip. If NS_FLIP is set, this does not reverse the direction of reset groups. For example, the normal case is to reset blocks 0 – 15 in order. When NS_FLIP is set, the order of block resets must be reversed to 15 – 0.

Note: The NS_FLIP signal should be kept low during initialization to ensure proper setup of the system. (NOT required in version 5 of the DDC4100)

3.9.3 Step DMD SRAM Memory Voltage

When the STEP_VCC signal goes high, the DMD internal SRAM voltage is stepped from its normal VCC value (nominally 3.3V) to the higher VCC2 value (nominally 7.5V/8.5V). The SRAM voltage is stepped back down when this flag goes back low.

This input signal is provided for experimental use and should not be used for normal operation. Contact Texas Instruments for more information.

The step signal should only be asserted when data is not being loaded into the DMD. Therefore, it is necessary to assert a no-op row cycle when stepping up or stepping down the memory voltage.

The watchdog function may override the memory voltage setting if the watchdog times out. The watchdog will perform a global reset, which steps the memory voltage down at the end of the cycle. If this operation is undesirable, disable the watchdog before issuing the STEP_VCC signal.

3.9.4 DMD_A_RESET

DMD_A_RESET is an active low reset to the DMD. This signal is de-asserted as appropriate at the end of system initialization.

3.10 DAD2000 Control Signals

Coordinating the operation of the DAD2000 with the DMD is one of the primary functions of the DDC4100. During system initialization, the DDC4100 releases the reset pin (DAD_INIT) and communicates with the DAD2000 via a serial bus to configure the device. Once this is complete, the high voltage output pins are enabled to prepare for command execution. As the DDC4100 is commanded to load data and perform resets, the DAD_ADDR address, DAD_MODE mode, DAD_SEL select and DAD_STROBE strobe signals are asserted as appropriate to cause the mirror reset.

3.11 DDC_VERSION(3:0)

These four pins will identify the version of the DDC4100. If a problem is encountered, provide the version number with detailed information of the problem.

3.12 DMD_TYPE(3:0)

Four Output pins from the DDC4100 identify the DMD type detected by the DDC4100 (shown in Table 2). DMD_TYPE will return “1111” if the DMD is not attached or not recognized.

3.13 ecm2m_tp_ (31:0)

Reserved signals for test signal output. Do not drive these signals.

4 Electrical Characteristics

The information contained in the following sections has been adapted from the Xilinx Virtex5 Datasheet. For any information beyond what is listed here, consult the Xilinx Virtex5 Datasheet. Where appropriate, DDC4100 specific values have been substituted in place of generic parameters.

4.1 Absolute Maximum Ratings Over Recommended Operating Free-air Temperature Range (unless otherwise noted)†

Supply voltage range (see Note 1):	V_{CCINT}	-0.5 V to 1.11 V
	V_{CCO}	-0.5 V to 3.75 V
	V_{CCAUX}	-0.5 V to 3.00 V
Input voltage range, V_I (see Note 2):	2.5 V	–0.75 V to V_{CCO} + 0.5 V
Output voltage range, V_O (see Note 3):	2.5 V	–0.3 V to V_{CCO} + 0.3 V

Continuous total power dissipation:	Typical	2.7W
	Maximum	2.8 W
Operating free-air temperature range, T_A (see Note 4)		0°C to 85°C
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values are with respect to GND.
2. Applies to external input and bidirectional buffers.
3. Applies to external output and bidirectional buffers.
4. Maximum Ambient Temperature may be further limited by the device’s power dissipation (which is data and configuration dependent), air flow and resultant junction temperature.

4.2 Recommended Operating Conditions

Table 9. Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CCINT}	1.0V Supply voltage, core logic		0.95	1.0	1.05	V
V_{CCO}	2.5 V Supply voltage, I/O		1.14	2.5	3.45	V
V_{CCAUX}	2.5V Supply voltage, I/O		2.375	2.5	2.625	V
V_{IH}	High-level Input voltage	2.5V CMOS	1.7			V
V_{IL}	Low-level Input voltage	2.5V CMOS			0.7	V
V_I	Input voltage	2.5V CMOS	0		V_{CCO}	V
		2.5V LVDS	0.3		2.2	V
V_O	Output voltage	2.5V CMOS	0		V_{CCO}	V
		2.5V LVDS	0.825		1.675	
T_A	Operating ambient temperature range	Note 1	0		70	°C
T_J	Operating virtual-junction temperature	Note 1	0		125	°C

Note : Thermal analysis and design should be carefully considered to ensure that the junction temperature is maintained within the above specifications.

4.3 Electrical Characteristics over Recommended Operating Conditions

Table 10. Electrical Characteristics Over Recommended Operating Conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	2.5V Interface		V_{CCO}-.4			V
		2.5V LVDS			1.38		
V_{OL}	Low-level output voltage	2.5V Interface				0.4	V
		2.5V LVDS			1.03		
C_I	Input capacitance	2.5V Interface			8		pF
		2.5V LVDS			8		
I_{CCINT}	Supply voltage range, Core Supply				300		mA
I_{CCO}	Supply voltage range, I/O Supply				850		mA

4.4 Timing Requirements

Table 11. Timing Requirements

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f_{cd}	Clock frequency, DCLKIN_n (Note 1)		200	400	MHz
f_{cr}	Clock frequency, CLK_R		50	50	MHz
t_C	Cycle time, DCLKIN_n		2.5	5	ns
$t_{W(H)}$	Pulse duration, high	50% to 50% reference points (signal)	1.25	2.5	ns
$t_{W(L)}$	Pulse duration, low	50% to 50% reference points (signal)	1.25	2.5	ns
t_t	Transition time, $t_t = t_f / t_r$	20% to 80% reference points (signal)		.6	ns
tjp	Period Jitter DCLKIN_n (Note 2)		150	150	ps
t_{SK}	Skew, DIN_A(15-0) to DCLKIN_A (Note 2)		-150	150	ps
t_{SK}	Skew, DIN_B(15-0) to DCLKIN_B		-150	150	ps
t_{SK}	Skew, DIN_C(15-0) to DCLKIN_C		-150	150	ps
t_{SK}	Skew, DIN_D(15-0) to DCLKIN_D		-150	150	ps
t_{SK}	Skew, DVALID_n to DCLKIN_n↑		-150	150	ps
t_{SK}	Skew, BLK_MD / BLK_AD to DCLKIN_n↑ (See note 3)		-150	150	ps
t_{SK}	Skew, ROWMD / ROWAD to DCLKIN_n↑ (See note 3)		-150	150	ps
t_{SK}	Skew, STEPVCC to DCLKIN↑ (See note 3)		-150	150	ps

Notes:

1. Preferred DCLKIN_n duty cycle = 50%
2. This is the deviation in period from ideal period due solely to high frequency jitter.
3. First edge of DIN*, ROW*, BLK* and STEPVCC should be synchronous to DVALID rising edge
4. It is recommended that the COMP_DATA, NS_FLIP and RST2BLKZ flags be set to one value and not adjusted during normal system operation.

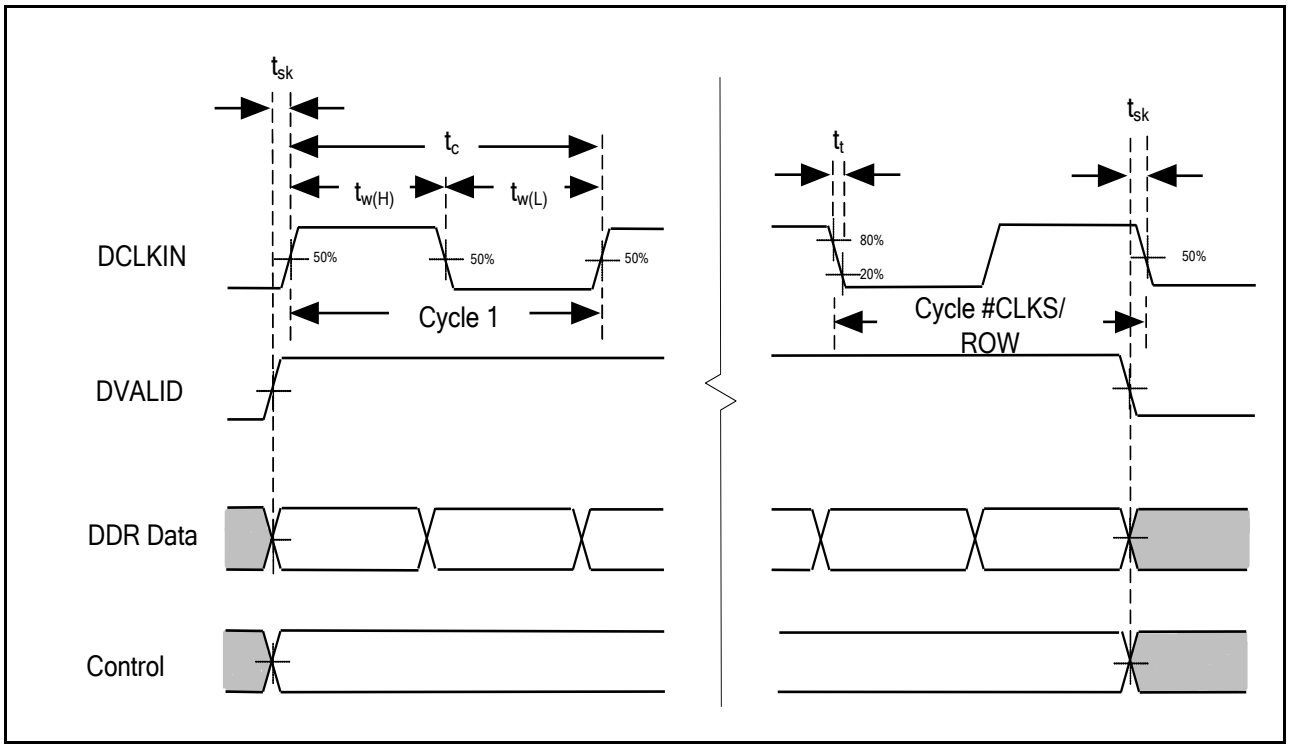

Figure 13. Input Interface Timing

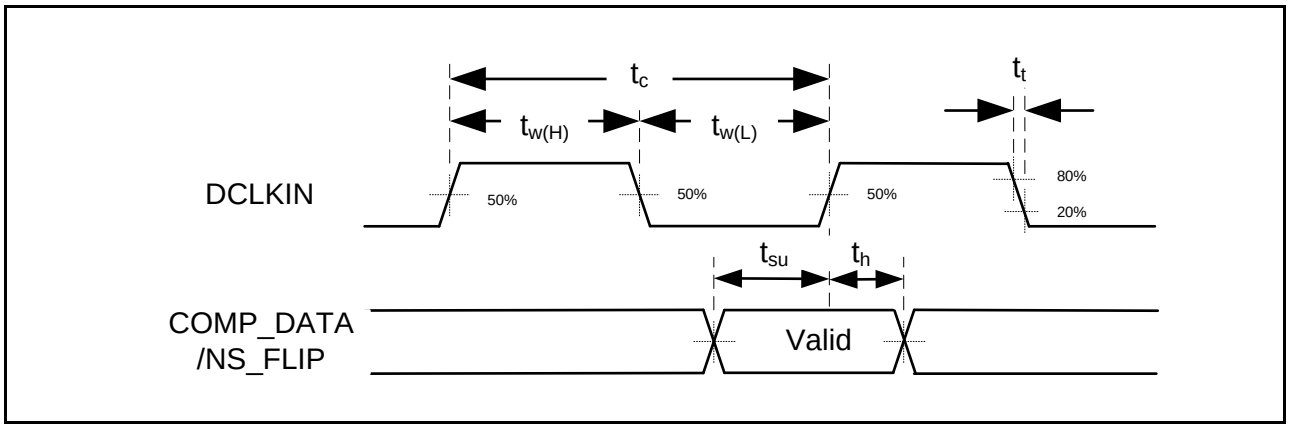

Figure 14. Control Timing

Note: Dynamic changes to NS_FLIP and COMP_DATA during nomal operation is not recommended.

5 Package Pinout

5.1 Customer Interface Signals

Table 12. Customer Interface Signal Pins

Pin	Name	I/O	Signal Type	Data Rate	Pin	Name	I/O	Signal Type	Data Rate
F7	APPS_CNTL_AN	O	LVDS	TBD	H2	DDC_DOUT_A13_DPN	O	LVDS	Double
E7	APPS_CNTL_AP	O	LVDS	TBD	J1	DDC_DOUT_A13_DPP	O	LVDS	Double
AC13	ARSTZ	I	LVCMOS	Single	H1	DDC_DOUT_A14_DPN	O	LVDS	Double
E12	BLKAD_0	I	LVCMOS	Single	G1	DDC_DOUT_A14_DPP	O	LVDS	Double
D13	BLKAD_1	I	LVCMOS	Single	G2	DDC_DOUT_A15_DPN	O	LVDS	Double
E13	BLKAD_2	I	LVCMOS	Single	F2	DDC_DOUT_A15_DPP	O	LVDS	Double
F13	BLKAD_3	I	LVCMOS	Single	AC1	DDC_DOUT_A2_DPN	O	LVDS	Double
H13	BLKMD_0	I	LVCMOS	Single	AC2	DDC_DOUT_A2_DPP	O	LVDS	Double
H14	BLKMD_1	I	LVCMOS	Single	AB1	DDC_DOUT_A3_DPN	O	LVDS	Double
AD13	CLK_R	I	LVCMOS	Single	AB2	DDC_DOUT_A3_DPP	O	LVDS	Double
G19	COMP_DATA	I	LVCMOS	Single	Y2	DDC_DOUT_A4_DPN	O	LVDS	Double
E1	DAD_A_ADDR0	O	LVCMOS	Single	AA2	DDC_DOUT_A4_DPP	O	LVDS	Double
E2	DAD_A_ADDR1	O	LVCMOS	Single	W1	DDC_DOUT_A5_DPN	O	LVDS	Double
E3	DAD_A_ADDR2	O	LVCMOS	Single	Y1	DDC_DOUT_A5_DPP	O	LVDS	Double
F3	DAD_A_ADDR3	O	LVCMOS	Single	V1	DDC_DOUT_A6_DPN	O	LVDS	Double
C1	DAD_A_MODE0	O	LVCMOS	Single	V2	DDC_DOUT_A6_DPP	O	LVDS	Double
D1	DAD_A_MODE1	O	LVCMOS	Single	U1	DDC_DOUT_A7_DPN	O	LVDS	Double
AE3	DAD_A_SCPENZ	O	LVCMOS	Single	U2	DDC_DOUT_A7_DPP	O	LVDS	Double
AB12	DAD_A_SEL0	O	LVCMOS	Single	R2	DDC_DOUT_A8_DPN	O	LVDS	Double
AC12	DAD_A_SEL1	O	LVCMOS	Single	T2	DDC_DOUT_A8_DPP	O	LVDS	Double
AF3	DAD_A_STROBE	O	LVCMOS	Single	N2	DDC_DOUT_A9_DPN	O	LVDS	Double
E26	DAD_B_ADDR0	O	LVCMOS	Single	M2	DDC_DOUT_A9_DPP	O	LVDS	Double
E25	DAD_B_ADDR1	O	LVCMOS	Single	AE5	DDC_DOUT_B0_DPN	O	LVDS	Double
F25	DAD_B_ADDR2	O	LVCMOS	Single	AE6	DDC_DOUT_B0_DPP	O	LVDS	Double
F24	DAD_B_ADDR3	O	LVCMOS	Single	AD3	DDC_DOUT_B1_DPN	O	LVDS	Double
D26	DAD_B_MODE0	O	LVCMOS	Single	AD4	DDC_DOUT_B1_DPP	O	LVDS	Double

Pin	Name	I/O	Signal Type	Data Rate	Pin	Name	I/O	Signal Type	Data Rate
D25	DAD_B_MODE1	O	LVCMOS	Single	W6	DDC_DOUT_B10_DPN	O	LVDS	Double
AB19	DAD_B_SCPENZ	O	LVCMOS	Single	W5	DDC_DOUT_B10_DPP	O	LVDS	Double
R22	DAD_B_SEL0	O	LVCMOS	Single	V7	DDC_DOUT_B11_DPN	O	LVDS	Double
R23	DAD_A_SEL1	O	LVCMOS	Single	V6	DDC_DOUT_B11_DPP	O	LVDS	Double
AB20	DAD_B_STROBE	O	LVCMOS	Single	U4	DDC_DOUT_B12_DPN	O	LVDS	Double
AF4	DAD_INIT	O	LVCMOS	Single	V3	DDC_DOUT_B12_DPP	O	LVDS	Double
AF5	DAD_OEZ	O	LVCMOS	Single	T4	DDC_DOUT_B13_DPN	O	LVDS	Double
N1	DCLK_A_DPN	O	LVDS	Double	T5	DDC_DOUT_B13_DPP	O	LVDS	Double
M1	DCLK_A_DPP	O	LVDS	Double	U6	DDC_DOUT_B14_DPN	O	LVDS	Double
Y5	DCLK_B_DPN	O	LVDS	Double	U5	DDC_DOUT_B14_DPP	O	LVDS	Double
Y6	DCLK_B_DPP	O	LVDS	Double	U7	DDC_DOUT_B15_DPN	O	LVDS	Double
AA22	DCLK_C_DPN	O	LVDS	Double	T7	DDC_DOUT_B15_DPP	O	LVDS	Double
AB22	DCLK_C_DPP	O	LVDS	Double	AD5	DDC_DOUT_B2_DPN	O	LVDS	Double
M26	DCLK_D_DPN	O	LVDS	Double	AD6	DDC_DOUT_B2_DPP	O	LVDS	Double
M25	DCLK_D_DPP	O	LVDS	Double	AC3	DDC_DOUT_B3_DPN	O	LVDS	Double
F18	DDC_VERSION0	O	LVCMOS	Single	AC4	DDC_DOUT_B3_DPP	O	LVDS	Double
G17	DDC_VERSION1	O	LVCMOS	Single	AB5	DDC_DOUT_B4_DPN	O	LVDS	Double
H18	DDC_VERSION2	O	LVCMOS	Single	AB6	DDC_DOUT_B4_DPP	O	LVDS	Double
A15	DDC_DIN_A0_DPN	I	LVDS	Double	AB7	DDC_DOUT_B5_DPN	O	LVDS	Double
A14	DDC_DIN_A0_DPP	I	LVDS	Double	AC6	DDC_DOUT_B5_DPP	O	LVDS	Double
B14	DDC_DIN_A1_DPN	I	LVDS	Double	AA5	DDC_DOUT_B6_DPN	O	LVDS	Double
C14	DDC_DIN_A1_DPP	I	LVDS	Double	AA4	DDC_DOUT_B6_DPP	O	LVDS	Double
A22	DDC_DIN_A10_DPN	I	LVDS	Double	AA7	DDC_DOUT_B7_DPN	O	LVDS	Double
B22	DDC_DIN_A10_DPP	I	LVDS	Double	Y7	DDC_DOUT_B7_DPP	O	LVDS	Double
A24	DDC_DIN_A11_DPN	I	LVDS	Double	Y3	DDC_DOUT_B8_DPN	O	LVDS	Double
A23	DDC_DIN_A11_DPP	I	LVDS	Double	W3	DDC_DOUT_B8_DPP	O	LVDS	Double
C23	DDC_DIN_A12_DPN	I	LVDS	Double	W4	DDC_DOUT_B9_DPN	O	LVDS	Double
B24	DDC_DIN_A12_DPP	I	LVDS	Double	V4	DDC_DOUT_B9_DPP	O	LVDS	Double
C24	DDC_DIN_A13_DPN	I	LVDS	Double	T22	DDC_DOUT_C0_DPN	O	LVDS	Double
D24	DDC_DIN_A13_DPP	I	LVDS	Double	T23	DDC_DOUT_C0_DPP	O	LVDS	Double

Pin	Name	I/O	Signal Type	Data Rate	Pin	Name	I/O	Signal Type	Data Rate
A25	DDC_DIN_A14_DPN	I	LVDS	Double	R20	DDC_DOUT_C1_DPN	O	LVDS	Double
B25	DDC_DIN_A14_DPP	I	LVDS	Double	R21	DDC_DOUT_C1_DPP	O	LVDS	Double
C26	DDC_DIN_A15_DPN	I	LVDS	Double	Y20	DDC_DOUT_C10_DPN	O	LVDS	Double
B26	DDC_DIN_A15_DPP	I	LVDS	Double	Y21	DDC_DOUT_C10_DPP	O	LVDS	Double
B16	DDC_DIN_A2_DPN	I	LVDS	Double	AA24	DDC_DOUT_C11_DPN	O	LVDS	Double
B15	DDC_DIN_A2_DPP	I	LVDS	Double	AA23	DDC_DOUT_C11_DPP	O	LVDS	Double
C16	DDC_DIN_A3_DPN	I	LVDS	Double	AA19	DDC_DOUT_C12_DPN	O	LVDS	Double
D16	DDC_DIN_A3_DPP	I	LVDS	Double	AA20	DDC_DOUT_C12_DPP	O	LVDS	Double
A17	DDC_DIN_A4_DPN	I	LVDS	Double	AC24	DDC_DOUT_C13_DPN	O	LVDS	Double
B17	DDC_DIN_A4_DPP	I	LVDS	Double	AB24	DDC_DOUT_C13_DPP	O	LVDS	Double
C17	DDC_DIN_A5_DPN	I	LVDS	Double	AC19	DDC_DOUT_C14_DPN	O	LVDS	Double
D18	DDC_DIN_A5_DPP	I	LVDS	Double	AD19	DDC_DOUT_C14_DPP	O	LVDS	Double
A19	DDC_DIN_A6_DPN	I	LVDS	Double	AC22	DDC_DOUT_C15_DPN	O	LVDS	Double
A18	DDC_DIN_A6_DPP	I	LVDS	Double	AC23	DDC_DOUT_C15_DPP	O	LVDS	Double
C18	DDC_DIN_A7_DPN	I	LVDS	Double	T19	DDC_DOUT_C2_DPN	O	LVDS	Double
B19	DDC_DIN_A7_DPP	I	LVDS	Double	T20	DDC_DOUT_C2_DPP	O	LVDS	Double
D19	DDC_DIN_A8_DPN	I	LVDS	Double	U21	DDC_DOUT_C3_DPN	O	LVDS	Double
C19	DDC_DIN_A8_DPP	I	LVDS	Double	U22	DDC_DOUT_C3_DPP	O	LVDS	Double
B20	DDC_DIN_A9_DPN	I	LVDS	Double	U20	DDC_DOUT_C4_DPN	O	LVDS	Double
A20	DDC_DIN_A9_DPP	I	LVDS	Double	U19	DDC_DOUT_C4_DPP	O	LVDS	Double
A12	DDC_DIN_B0_DPN	I	LVDS	Double	V23	DDC_DOUT_C5_DPN	O	LVDS	Double
A13	DDC_DIN_B0_DPP	I	LVDS	Double	V24	DDC_DOUT_C5_DPP	O	LVDS	Double
B12	DDC_DIN_B1_DPN	I	LVDS	Double	V22	DDC_DOUT_C6_DPN	O	LVDS	Double
C13	DDC_DIN_B1_DPP	I	LVDS	Double	V21	DDC_DOUT_C6_DPP	O	LVDS	Double
B6	DDC_DIN_B10_DPN	I	LVDS	Double	W19	DDC_DOUT_C7_DPN	O	LVDS	Double
B5	DDC_DIN_B10_DPP	I	LVDS	Double	V19	DDC_DOUT_C7_DPP	O	LVDS	Double
D4	DDC_DIN_B11_DPN	I	LVDS	Double	W23	DDC_DOUT_C8_DPN	O	LVDS	Double
D3	DDC_DIN_B11_DPP	I	LVDS	Double	W24	DDC_DOUT_C8_DPP	O	LVDS	Double
B4	DDC_DIN_B12_DPN	I	LVDS	Double	Y22	DDC_DOUT_C9_DPN	O	LVDS	Double
C4	DDC_DIN_B12_DPP	I	LVDS	Double	Y23	DDC_DOUT_C9_DPP	O	LVDS	Double

Pin	Name	I/O	Signal Type	Data Rate	Pin	Name	I/O	Signal Type	Data Rate
C3	DDC_DIN_B13_DPN	I	LVDS	Double	AB26	DDC_DOUT_D0_DPN	O	LVDS	Double
C2	DDC_DIN_B13_DPP	I	LVDS	Double	AC26	DDC_DOUT_D0_DPP	O	LVDS	Double
A3	DDC_DIN_B14_DPN	I	LVDS	Double	AA25	DDC_DOUT_D1_DPN	O	LVDS	Double
A2	DDC_DIN_B14_DPP	I	LVDS	Double	AB25	DDC_DOUT_D1_DPP	O	LVDS	Double
B2	DDC_DIN_B15_DPN	I	LVDS	Double	L25	DDC_DOUT_D10_DPN	O	LVDS	Double
B1	DDC_DIN_B15_DPP	I	LVDS	Double	L24	DDC_DOUT_D10_DPP	O	LVDS	Double
D10	DDC_DIN_B2_DPN	I	LVDS	Double	K26	DDC_DOUT_D11_DPN	O	LVDS	Double
D11	DDC_DIN_B2_DPP	I	LVDS	Double	K25	DDC_DOUT_D11_DPP	O	LVDS	Double
C12	DDC_DIN_B3_DPN	I	LVDS	Double	J26	DDC_DOUT_D12_DPN	O	LVDS	Double
C11	DDC_DIN_B3_DPP	I	LVDS	Double	J25	DDC_DOUT_D12_DPP	O	LVDS	Double
A10	DDC_DIN_B4_DPN	I	LVDS	Double	J24	DDC_DOUT_D13_DPN	O	LVDS	Double
B11	DDC_DIN_B4_DPP	I	LVDS	Double	H24	DDC_DOUT_D13_DPP	O	LVDS	Double
D9	DDC_DIN_B5_DPN	I	LVDS	Double	H26	DDC_DOUT_D14_DPN	O	LVDS	Double
C9	DDC_DIN_B5_DPP	I	LVDS	Double	G26	DDC_DOUT_D14_DPP	O	LVDS	Double
B10	DDC_DIN_B6_DPN	I	LVDS	Double	G25	DDC_DOUT_D15_DPN	O	LVDS	Double
B9	DDC_DIN_B6_DPP	I	LVDS	Double	G24	DDC_DOUT_D15_DPP	O	LVDS	Double
A8	DDC_DIN_B7_DPN	I	LVDS	Double	Y26	DDC_DOUT_D2_DPN	O	LVDS	Double
A9	DDC_DIN_B7_DPP	I	LVDS	Double	Y25	DDC_DOUT_D2_DPP	O	LVDS	Double
D6	DDC_DIN_B8_DPN	I	LVDS	Double	W26	DDC_DOUT_D3_DPN	O	LVDS	Double
D5	DDC_DIN_B8_DPP	I	LVDS	Double	W25	DDC_DOUT_D3_DPP	O	LVDS	Double
C7	DDC_DIN_B9_DPN	I	LVDS	Double	U26	DDC_DOUT_D4_DPN	O	LVDS	Double
C6	DDC_DIN_B9_DPP	I	LVDS	Double	V26	DDC_DOUT_D4_DPP	O	LVDS	Double
E20	DDC_DIN_C0_DPN	I	LVDS	Double	U25	DDC_DOUT_D5_DPN	O	LVDS	Double
E21	DDC_DIN_C0_DPP	I	LVDS	Double	U24	DDC_DOUT_D5_DPP	O	LVDS	Double
F20	DDC_DIN_C1_DPN	I	LVDS	Double	T25	DDC_DOUT_D6_DPN	O	LVDS	Double
G20	DDC_DIN_C1_DPP	I	LVDS	Double	T24	DDC_DOUT_D6_DPP	O	LVDS	Double
M19	DDC_DIN_C10_DPN	I	LVDS	Double	R26	DDC_DOUT_D7_DPN	O	LVDS	Double
M20	DDC_DIN_C10_DPP	I	LVDS	Double	R25	DDC_DOUT_D7_DPP	O	LVDS	Double
M21	DDC_DIN_C11_DPN	I	LVDS	Double	P24	DDC_DOUT_D8_DPN	O	LVDS	Double
M22	DDC_DIN_C11_DPP	I	LVDS	Double	P25	DDC_DOUT_D8_DPP	O	LVDS	Double

Pin	Name	I/O	Signal Type	Data Rate	Pin	Name	I/O	Signal Type	Data Rate
N19	DDC_DIN_C12_DPN	I	LVDS	Double	N24	DDC_DOUT_D9_DPN	O	LVDS	Double
P19	DDC_DIN_C12_DPP	I	LVDS	Double	M24	DDC_DOUT_D9_DPP	O	LVDS	Double
N21	DDC_DIN_C13_DPN	I	LVDS	Double	D20	DVALID_A_DPN	I	LVDS	Double
N22	DDC_DIN_C13_DPP	I	LVDS	Double	D21	DVALID_A_DPP	I	LVDS	Double
P20	DDC_DIN_C14_DPN	I	LVDS	Double	C8	DVALID_B_DPN	I	LVDS	Double
P21	DDC_DIN_C14_DPP	I	LVDS	Double	D8	DVALID_B_DPP	I	LVDS	Double
N23	DDC_DIN_C15_DPN	I	LVDS	Double	L19	DVALID_C_DPN	I	LVDS	Double
P23	DDC_DIN_C15_DPP	I	LVDS	Double	L20	DVALID_C_DPP	I	LVDS	Double
H19	DDC_DIN_C2_DPN	I	LVDS	Double	L3	DVALID_D_DPN	I	LVDS	Double
J19	DDC_DIN_C2_DPP	I	LVDS	Double	L4	DVALID_D_DPP	I	LVDS	Double
E23	DDC_DIN_C3_DPN	I	LVDS	Double	AB10	ECP2M_TP10	O	LVCMOS	Single
E22	DDC_DIN_C3_DPP	I	LVDS	Double	AA10	ECP2M_TP11	O	LVCMOS	Single
F23	DDC_DIN_C4_DPN	I	LVDS	Double	Y10	ECP2M_TP12	O	LVCMOS	Single
F22	DDC_DIN_C4_DPP	I	LVDS	Double	AC11	ECP2M_TP13	O	LVCMOS	Single
G22	DDC_DIN_C5_DPN	I	LVDS	Double	Y12	ECP2M_TP14	O	LVCMOS	Single
G21	DDC_DIN_C5_DPP	I	LVDS	Double	Y11	ECP2M_TP15	O	LVCMOS	Single
J20	DDC_DIN_C6_DPN	I	LVDS	Double	AB11	ECP2M_TP16	O	LVCMOS	Single
J21	DDC_DIN_C6_DPP	I	LVDS	Double	H8	ECP2M_TP17	O	LVCMOS	Single
H22	DDC_DIN_C7_DPN	I	LVDS	Double	H9	ECP2M_TP18	O	LVCMOS	Single
H21	DDC_DIN_C7_DPP	I	LVDS	Double	F12	ECP2M_TP19	O	LVCMOS	Single
J23	DDC_DIN_C8_DPN	I	LVDS	Double	G11	ECP2M_TP20	O	LVCMOS	Single
H23	DDC_DIN_C8_DPP	I	LVDS	Double	G12	ECP2M_TP21	O	LVCMOS	Single
K22	DDC_DIN_C9_DPN	I	LVDS	Double	E11	ECP2M_TP22	O	LVCMOS	Single
K23	DDC_DIN_C9_DPP	I	LVDS	Double	E10	ECP2M_TP23	O	LVCMOS	Single
T3	DDC_DIN_D0_DPN	I	LVDS	Double	E8	ECP2M_TP24	O	LVCMOS	Single
R3	DDC_DIN_D0_DPP	I	LVDS	Double	F10	ECP2M_TP25	O	LVCMOS	Single
R5	DDC_DIN_D1_DPN	I	LVDS	Double	F9	ECP2M_TP26	O	LVCMOS	Single
R6	DDC_DIN_D1_DPP	I	LVDS	Double	F8	ECP2M_TP27	O	LVCMOS	Single
H7	DDC_DIN_D10_DPN	I	LVDS	Double	G10	ECP2M_TP28	O	LVCMOS	Single
J6	DDC_DIN_D10_DPP	I	LVDS	Double	G9	ECP2M_TP29	O	LVCMOS	Single

Pin	Name	I/O	Signal Type	Data Rate	Pin	Name	I/O	Signal Type	Data Rate
G4	DDC_DIN_D11_DPN	I	LVDS	Double	AC8	ECP2M_TP3	O	LVCMOS	Single
H4	DDC_DIN_D11_DPP	I	LVDS	Double	H11	ECP2M_TP30	O	LVCMOS	Single
G5	DDC_DIN_D12_DPN	I	LVDS	Double	H12	ECP2M_TP31	O	LVCMOS	Single
H6	DDC_DIN_D12_DPP	I	LVDS	Double	AC7	ECP2M_TP4	O	LVCMOS	Single
G7	DDC_DIN_D13_DPN	I	LVDS	Double	AC9	ECP2M_TP5	O	LVCMOS	Single
G6	DDC_DIN_D13_DPP	I	LVDS	Double	AB9	ECP2M_TP6	O	LVCMOS	Single
F4	DDC_DIN_D14_DPN	I	LVDS	Double	AA8	ECP2M_TP7	O	LVCMOS	Single
F5	DDC_DIN_D14_DPP	I	LVDS	Double	AA9	ECP2M_TP8	O	LVCMOS	Single
E5	DDC_DIN_D15_DPN	I	LVDS	Double	Y8	ECP2M_TP9	O	LVCMOS	Single
E6	DDC_DIN_D15_DPP	I	LVDS	Double	AA18	INIT_ACTIVE	O	LVCMOS	Single
R7	DDC_DIN_D2_DPN	I	LVDS	Double	AC18	VLED0	O	LVCMOS	Single
P6	DDC_DIN_D2_DPP	I	LVDS	Double	AD18	VLED1	O	LVCMOS	Single
N3	DDC_DIN_D3_DPN	I	LVDS	Double	F19	NS_FLIP	I	LVCMOS	Single
P3	DDC_DIN_D3_DPP	I	LVDS	Double	AC17	PWR_FLOAT	I	LVCMOS	Single
P4	DDC_DIN_D4_DPN	I	LVDS	Double	D14	ROWAD_0	I	LVCMOS	Single
P5	DDC_DIN_D4_DPP	I	LVDS	Double	D15	ROWAD_1	I	LVCMOS	Single
N6	DDC_DIN_D5_DPN	I	LVDS	Double	G16	ROWAD_10	I	LVCMOS	Single
N7	DDC_DIN_D5_DPP	I	LVDS	Double	E15	ROWAD_2	I	LVCMOS	Single
N4	DDC_DIN_D6_DPN	I	LVDS	Double	F14	ROWAD_3	I	LVCMOS	Single
M4	DDC_DIN_D6_DPP	I	LVDS	Double	G14	ROWAD_4	I	LVCMOS	Single
M7	DDC_DIN_D7_DPN	I	LVDS	Double	E16	ROWAD_5	I	LVCMOS	Single
L7	DDC_DIN_D7_DPP	I	LVDS	Double	F15	ROWAD_6	I	LVCMOS	Single
K7	DDC_DIN_D8_DPN	I	LVDS	Double	G15	ROWAD_7	I	LVCMOS	Single
K6	DDC_DIN_D8_DPP	I	LVDS	Double	E17	ROWAD_8	I	LVCMOS	Single
J4	DDC_DIN_D9_DPN	I	LVDS	Double	F17	ROWAD_9	I	LVCMOS	Single
J5	DDC_DIN_D9_DPP	I	LVDS	Double	H17	ROWMD_0	I	LVCMOS	Single
AD14	DMD_A_RESET	O	LVCMOS	Single	H16	ROWMD_1	I	LVCMOS	Single
AA17	DMD_TYPE_0	O	LVCMOS	Single	AB16	RST_ACTIVE	O	LVCMOS	Single
AC16	DMD_TYPE_1	O	LVCMOS	Single	E18	RST2BLKZ	I	LVCMOS	Single
AB17	DMD_TYPE_2	O	LVCMOS	Single	AB15	SCPCLK	O	LVCMOS	Single

Pin	Name	I/O	Signal Type	Data Rate	Pin	Name	I/O	Signal Type	Data Rate
AD15	DMD_TYPE_3	O	LVCMOS	Single	AA15	SCPDI	I	LVCMOS	Single
AB14	DMD_SCPENZ	O	LVCMOS	Single	AA14	SCPDO	O	LVCMOS	Single
AE2	DDC_DOUT_A0_DPN	O	LVDS	Double	R1	SCTRL_A_DPN	O	LVDS	Double
AF2	DDC_DOUT_A0_DPP	O	LVDS	Double	P1	SCTRL_A_DPP	O	LVDS	Double
AD1	DDC_DOUT_A1_DPN	O	LVDS	Double	AA3	SCTRL_B_DPN	O	LVDS	Double
AE1	DDC_DOUT_A1_DPP	O	LVDS	Double	AB4	SCTRL_B_DPP	O	LVDS	Double
K1	DDC_DOUT_A10_DPN	O	LVDS	Double	W20	SCTRL_C_DPN	O	LVDS	Double
K2	DDC_DOUT_A10_DPP	O	LVDS	Double	W21	SCTRL_C_DPP	O	LVDS	Double
K2	DDC_DOUT_A11_DPN	O	LVDS	Double	N26	SCTRL_D_DPN	O	LVDS	Double
K3	DDC_DOUT_A11_DPP	O	LVDS	Double	P26	SCTRL_D_DPP	O	LVDS	Double
J3	DDC_DOUT_A12_DPN	O	LVDS	Double	Y13	STEPVCC	I	LVCMOS	Single
H3	DDC_DOUT_A12_DPP	O	LVDS	Double	AA13	WDT_ENBLZ	I	LVCMOS	Single
B21	DDC_DCLKIN_AN	I	LVDS	Double	A7	DDC_DCLKIN_BN	I	LVDS	Double
C21	DDC_DCLKIN_AP	I	LVDS	Double	B7	DDC_DCLKIN_BP	I	LVDS	Double
K20	DDC_DCLKIN_CN	I	LVDS	Double	L5	DDC_DCLKIN_DN	I	LVDS	Double
K21	DDC_DCLKIN_CP	I	LVDS	Double	K5	DDC_DCLKIN_DP	I	LVDS	Double
Y18	ECP2_FINISHED	O	LVCMOS	Single					

5.2 JTAG and Configuration

Table 13. JTAG and Configuration Signal Pins

Signal	Name	I/O	Description
J18	PROGRAM_B	I	Active low signal to start configuration process
N18	CS_B	O	Active low configuration flash select
J10	CCLK	O	SPI clock to configuration flash
K10	DONE	IO	JTAG open drain pin, low during configuration
U11	TCK	I	JTAG clock
V11	TDI	I	JTAG data in
W10	TDO	O	JTAG data out
V12	TMS	I	JTAG mode select
W18	M0_0	I	Configuration Mode Select
Y17	M1_0	I	Configuration Mode Select
V18	M2_0	I	Configuration Mode Select
L18	HSWAPEN	I	Enable IO Pullups during Config.
K11	D_IN	I	Data Input
J11	INIT_B	IO	Config Control/Status signal

5.3 Power, Ground and No connect

Table 14. Power, Ground and No Connect Pins

Signal	Pin Number	I/O
VCC_1P0V	H15, J12, J14, J16, K9, K13, K15, L10, L12, L14, L16, M9, M11, M15, N10, N12, N16, P9, P11, P15, R10, R12, R16, T9, T11, T13, T15, U10, U12, U14, U16, V9, V13, V15, W14, Y15	PWR
VCC_2P5V (VCCAUX)	J8, K17, L8, M17, N8, P17, R8, T17, U8, V17, W8, W16	PWR
VCC_2P5V (VCCO)	AA6, AA16, AB3, AB13, AC10, AD7, AD17, B23, C10, C20, D7, D17, E4, E14, E24, F11, F21, G8, H5, H25, J2, J22, L6, M23, N20, R4, R24, T21, V5, V25, W2, W12, W22, Y9,	PWR
GND	A1, A6, A11, A16, A21, A26, AA1, AA11, AA21, AA26, AB8, AB18, AC5, AC15, AC25, AD2, AD12, AD22, AE4, AE9, AE14, AE19, AF1, AF6, AF11, AF16, AF21, AF26, B3, B8, B13, B18, C5, C15, C25, D2, D12, D22, E9, E19, F1, F6, F16, F26, G3, G13, G18, G23, H10, H20, J7, J9, J13, J15, J17, K4, K8, K12, K14, K16, K19, K24, L1, L9, L11, L13, L15, L17, L21, L26, M3, M8, M10, M12, M16, M18, N5, N9, N11, N15, N17, N25, P2, P7, P8, P10, P12, P16, P22, R9, R11, R15, R17, R19, T1, T6, T8, T10, T12, T14, T16, T26, U3, U9, U13, U15, U17, U18, U23, V8, V10, V14, V16, V20, W7, W9, W13, W15, W17, Y4, Y14, Y16, Y19, Y24, M13, M14	PWR
NC	AD9, AD16, AD20, AD21, AD23, AD24, AD25, AD26, AE7, AE8, AE10, AE11, AE12, AE13, AE15, AE16, AE17, AE18, AE20, AE21, AE22, AE23, AE25, AE26, AF7, AF8, AF9, AF10, AF12, AF13, AF14, AF15, AF17, AF18, AF19, AF20, AF22, AF23, AF24, AF25, AB23, AC20, AE24	No connect

6 Related Documentation

This section lists related documents associated with the use of the DDC4100 Controller Board.

2510299 - DLP® Discovery™ 4100 ESD

2510300 - DLP® Discovery™ 4100 Printed Circuit Board

2510301 - DLP® Discovery™ 4100 Circuit Card Assembly

2510617 - DLP® Discovery™ 4100 PCB Mechanical Outline Drawing

2509506 - DLP® Discovery™ .95” 1080p interface board ESD

2509507 - DLP® Discovery™ .95” 1080p interface Printed Circuit Board

2509508 - DLP® Discovery™ .95” 1080p interface board Circuit Card Assembly

2509509 - DLP® Discovery™ .95” 1080p interface board Mechanical Outline Drawing

2508692 - DLP® Discovery™ .96” WUXGA Type A DMD data sheet

2510455 - DLP® Discovery™ 4100 Technical Reference Manual

2510443 - DDC4100 Datasheet

www.xilinx.com APPSFPGA development tools and information

www.em.avnet.com/exp EXP specification and products

7 Labeling and Configuration

The DDC4100 is labeled with the corresponding part number and description for the specified dash number as indicated below. See the table below for the label information. All markings should be uniform in clarity. The label should not cover the pin 1 marking on the FPGA.

Table 15. DDC4100 Label

Revision Label	Description	Information
2510440-0001	DDC4100 Xilinx Part number: XC5VLX30-1FFG676C	Initial Release