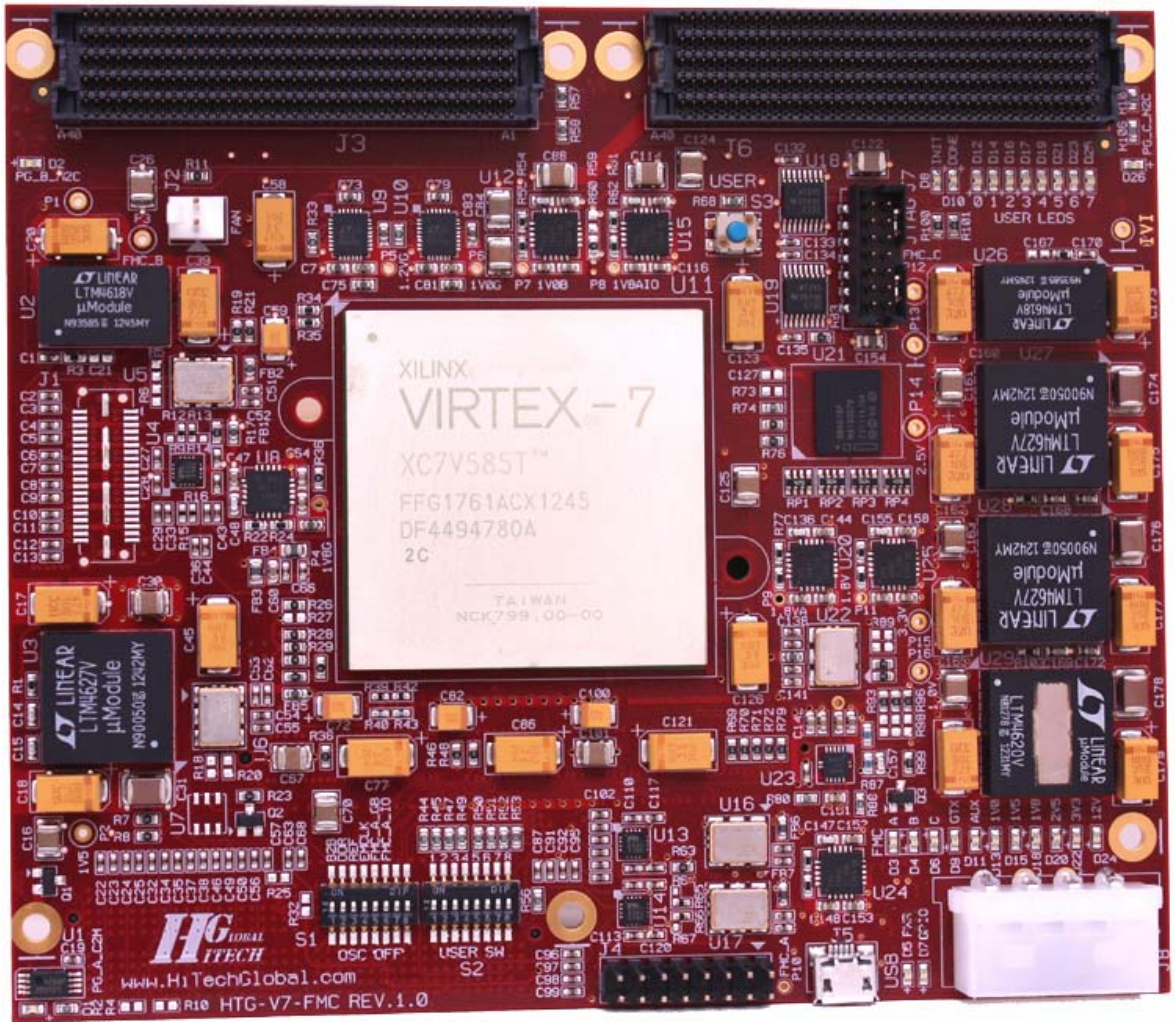
HTG-777 User Manual

Version 1.0 September 2013



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Revision History

Date	Version	Notes
9/30/2013	1.0	

Table Of Contents

Figure (9): I2C Bus Switch

Image (1): Stackable Option
Image (2): Host Option
Image (3): Daughter Card Option
Image (4): FMC To FMC Cable
Image (5): Dual SFP+ FMC Module
Image (6): Dual CX4 FMC Module
Image (7): Serial Connectivity FMC Module
Image (8): PCI Express FMC Module
Image (9): 8-Port FMC Module
Image (10): Quade SFP/SATA FMC Module
Image (11): 8-Port SMA/LVDS FMC Module
Image (12): Quade SFP/SFP+ FMC Module
Image (13): QSFP/QSFP+/SFP/SFP+ FMC Module
Image (14): Dual QSFP/QSFP+ FMC Module

Chapter 1: Introduction to Xilinx Virtex-7

1.1) Overview

The Virtex®-7 FPGAs are the programmable silicon foundation for Targeted Design Platform that deliver integrated software and hardware components to enable designers to focus on innovation as soon as their development cycle begins.

Optimized for applications that require ultra high-speed serial connectivity, Virtex®-7 FPGAs offer the industry's highest serial bandwidth through a combination of GTX and GTH transceivers to enable next-generation packet and transport, switch fabric, video switching, and imaging equipment.

Xilinx's Virtex-7 2000T FPGA enabled by Stacked Silicon Interconnect (SSI) technology delivers 2 million logic cells, 6.8 billion transistors and 12.5Gb/s serial transceivers, making it ideally suited for the ASIC prototyping and emulation applications.

The Virtex-7 2000T device:

- Eliminates the need for multi-chip partitioning
- Provides equivalent capacity and performance to high density ASIC and ASSPs
- Mitigates development risks for large ASIC and ASSP designs
- Reduces board space requirements and complexity
- Delivers flexible IO to create a contiguous device to match very large ASICs
- Reduces system level power consumption

Table (1) illustrates key features of the Virtex-7 devices (V585T, V2000T, and X690T) supported by the HTG-777 platforms.

	Part Number	XC7V585T	XC7V2000T	XC7VX690T
	EasyPath™ Cost Reduction Solutions[1]	XCE7V585T	XCE7V2000T	XCE7VX690T
Logic Resources	Slices	91,050	305,400	108,300
	Logic Cells	582,720	1,954,560	693,120
	CLB Flip-Flops	728,400	2,443,200	866,400
Memory Resources	Maximum Distributed RAM (Kb)	6,938	21,550	10,888
	Block RAM/FIFO w/ ECC (36 Kb each)	795	1,292	1,470
	Total Block RAM (Kb)	28,620	46,512	52,920
Clocking	CMTs (1 MMCM + 1 PLL)	18	24	20
I/O Resources	Maximum Single-Ended I/O	850	1,200	1,000
	Maximum Differential I/O Pairs	408	576	480
Embedded IP Resources	DSP48E1 Slices	1,260	2,160	3,600
	PCI Express Gen2	3	4	—
	PCI Express Gen3	—	—	3
	Agile Mixed Signal (AMS) / XADC	1	1	1
	Configuration AES / HMAC Blocks	1	1	1
	GTX 12.5 Gb/s Transceivers[2]	36	36	—
	GTH 13.1 Gb/s Transceivers[3]	—	—	80
	GTZ 28.05 Gb/s Transceivers	—	—	—
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2
	Extended[4]	-2L, -3	-2L, -2G	-2L, -3
	Industrial	-1, -2	-1	-1, -2

Table (1) Summary of Virtex-7 FPGA Features

1.2) Virtex-7 Family Serial I/O Protocol Support

GTX and GTH serial transceivers of the Virtex-7 devices support different ranges of serial protocol standards. Table (2) illustrates the supported standards and protocols.

Protocol	Virtex-7 GTX	Virtex-7 GTH
PCI Express®	Gen 1,2,3	Gen 1,2,3
QPI	✓	✓
Fibre Channel	✓	✓
SATA/SAS	✓	✓
Aurora	✓	✓
Ethernet	1000BASE-X/SGMII, QSGMII, XAUI, RXAUI	1000BASE-X/SGMII, QSGMII, XAUI, RXAUI
	10GBase-R, 10GBASE-KR, 40GBASE-R,	10GBase-R, 10GBASE-KR, 40GBASE-R,

	(XLAUI), 40GBASE-KR4, 100GBASE-R (CAUI), 100GBASE-CR10	(XLAUI), 40GBASE-KR4, 100GBASE-R (CAUI), 100GBASE-CR10
OTU	✓	✓
SONET	✓	✓
Interlaken	✓	✓
SFI-S	✓	✓
CEI Back Plane	✓	✓
BPON GPON GEPON GEPON 10GGPON (up to 2.5G BCDR)	BPON, GPON, GEPON, 10GEPON	BPON, GPON, GEPON
	10GGPON (up to 2.5G BCDR)	10GEPON, 10GGPON
OBSAI	✓	✓
CPRI	✓	✓
Serial Rapid IO	✓	✓
JESD204	✓	✓
SDI	✓	✓
V By One	✓	✓

Table (2) Supported Serial Protocols

Chapter 2:Development Platform Introduction

2.1) Introduction

Powered by four Xilinx Virtex-7 **V2000T, V585T, or X690** FPGAs, the HTG-777 is ideal for ASIC/SOC prototyping , emulation, and high-performance computing requiring large FPGA gate counts.

Available resources such as three high pin count (HPC) FPGA Mezzanine Connectors (FMC) , one DDR3 memory, and flexible high performance clocking scheme enable the HTG-777platofm for using in different applications requiring high speed interfaces.

Special form factor of the HTG-777 platform allows Stackable, Host, and Daughter Card use options.

Image (1): **Stackable Option:** connecting multiple boards to each other through FMC connectors expanding logic density

Image (2): **Host Option:** hosting multiple FMC daughter cards expanding functionality

Image (3): **Daughter Card Option:** mating with another FPGA carrier board expanding logic density

2.2) HTG-777 Platform's Features

► x1 Virtex-7 V2000T, X690T, or V585T FPGA in FHG1761 package
►x3 High Pin Count (HPC) FMC
- FMC #B & C: Each providing 160 Single-end (80 LVDS) + 8 GTX/GTH Serial Transceivers - used for hosting FMC daughter cards or another HTG-777 card expanding the total density of the design
- FMC #A: 160 Single-end (80 LVDS) + 8 GTX/GTH Serial Transceivers - used for mating with FPGA carrier cards
► x2 Samtec QSE and QTE connectors each with 6 GXT/GTX Serial Transceivers - used for I/O expansion or stack up of multiple V7-FMC module
► x1 DDR3 SODIMM socket supporting up to 8GB of memory (shipped with 1GB module)
► Flash for configuration
► x1 USB/UART port
► I2C Bus Control Switch
► Size: 5 1/2" x 4 1/2"

2.3) Platform Block Diagram

Figure (1) illustrates high-level block diagram and component placement of the HTG-777 platform

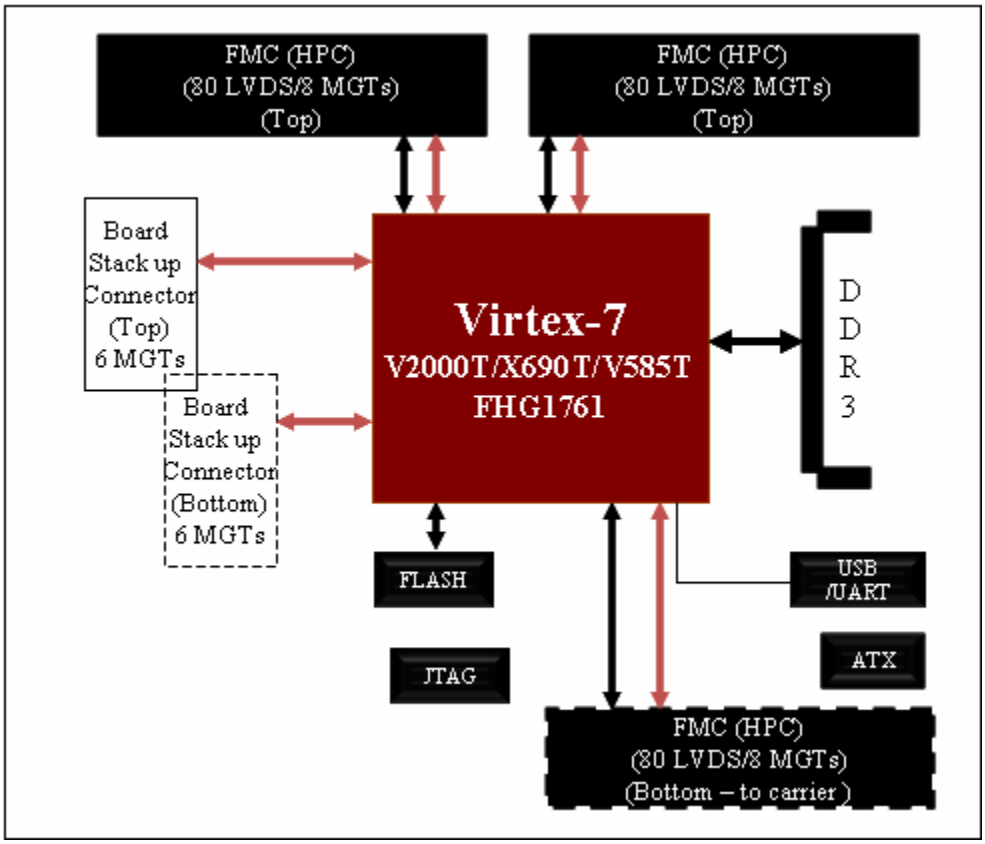

Figure (1): Block Diagram & Placement

2.4) FPGA Bank Assignment

Figure (2) illustrates utilization of the I/O banks for the Virtex-7 FPGAs.

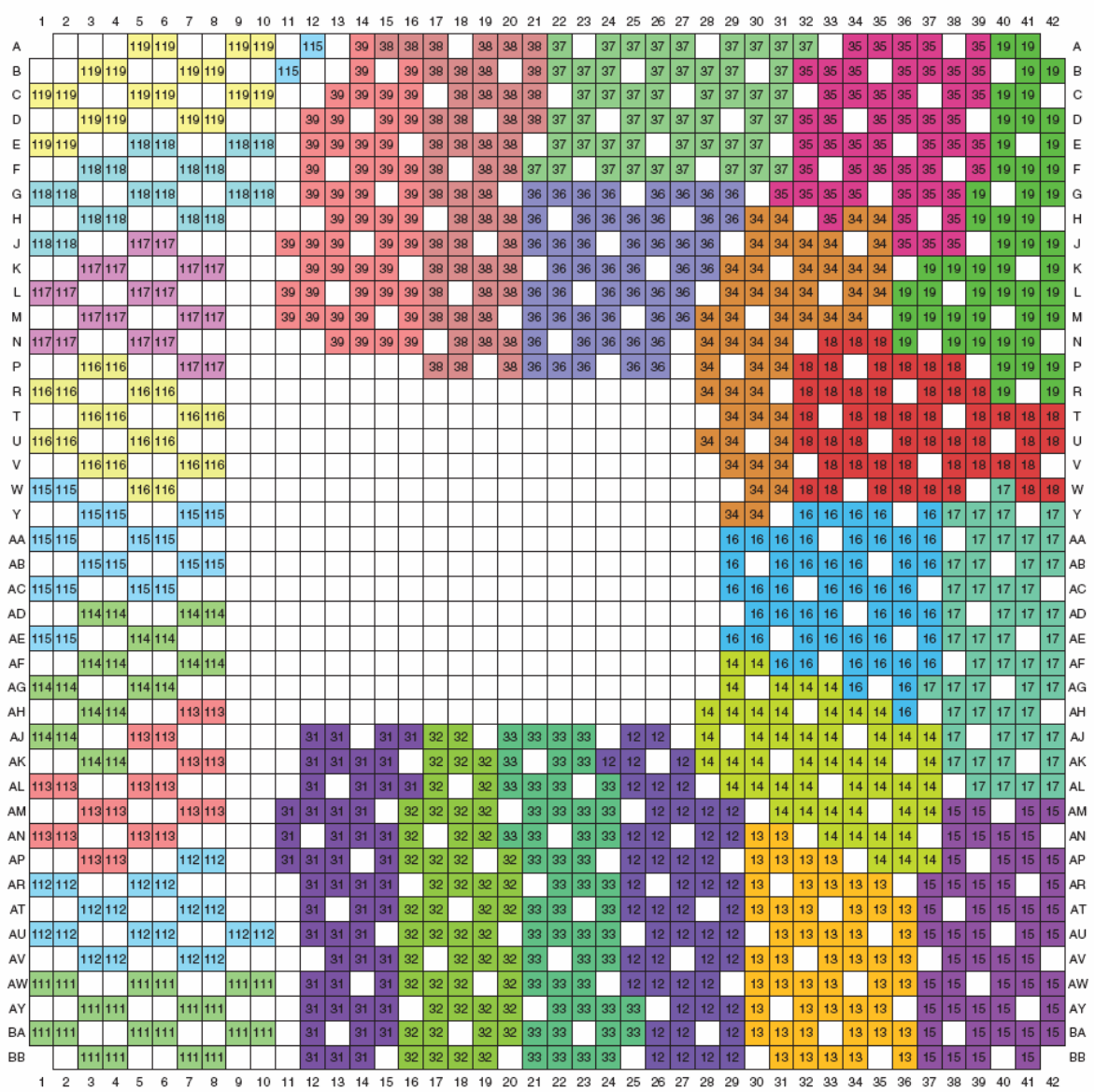

Figure (2) FFG1761 Package – I/O Banks

Bank 19 FMC 'C'		Bank 39 FMC 'A'		GTX 119 FMC 'B'
Bank 18 FMC 'C'		Bank 38 FMC 'A'		GTX 118 FMC 'B'
Bank 17 FMC 'C'		Bank 37 FMC 'A'		GTX 117 FMC 'C'
Bank 16 FMC 'B'		Bank 36 FMC 'B'		GTX 116 FMC 'C'
Bank 15 FLASH		Bank 35 FMC 'B'		GTX 115 B2B
Bank 14 FLASH		Bank 34 FMC 'B'		GTX 114 B2B
Bank 13 FMC 'C'		Bank 33 DDR3		GTX 113 B2B
Bank 12 FMC 'A'		Bank 32 DDR3		GTX 112 FMC 'A'
		Bank 31 DDR3		GTX 111 FMC 'A'

Figure (3): FPGA Bank Assignment

2.5) Clock Distribution

For providing high performance of different onboard resources, the HTG-777 platform is supported by different low-jitter crystal oscillators and synthesizers manufactured by IDT and Silicon Labs. These clock resources have default factory start up frequencies but are programmable to wide range of different values through I2C bus. Figure (5) illustrates the entire platform's clock diagram.

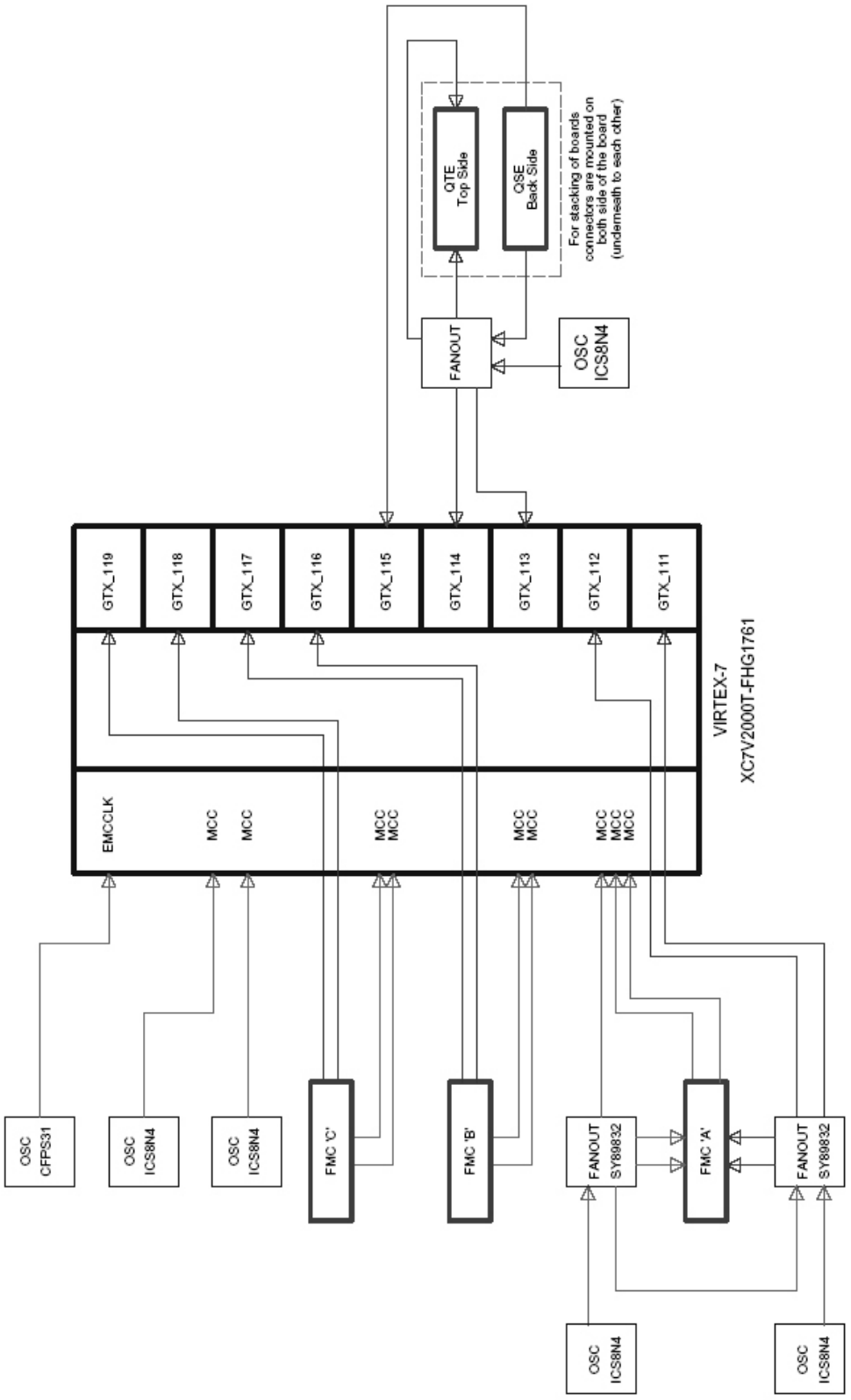

Figure (4): Clock Diagram

Table (3) illustrates summary of all clock components on the HTG-777 platform:

Ref. Designator	Part Number	Description
U5	8N4Q001LG-0055CDI	I2C Programmable XO, LVDS, 2.5V, 20ppm with start up frequency of 156.25MHz . Provides reference clocks to MGT 113 and 114 for QTE/QSE board to board connectors (vertical stack up). It also provides clock to the J1 (QTE) and J11 (QSE) connectors
U17	8N4Q001LG-0055CDI	I2C Programmable XO, LVDS, 2.5V, 20ppm with start up frequency of 156.25MHz . Provides reference clocks to MGT 111, and 112 for FMC ”A”,
U16	8N4Q001LG-0102CDI	I2C Programmable XO, LVDS, 2.5V, 20ppm with start up frequency of 25MHz . Provides reference clocks for FMC “A”
U22	8N4Q001LG-0102CDI	I2C Programmable XO, LVDS, 2.5V, 20ppm with start up frequency of 25MHz . Provides reference clocks for DDR3 memory
U6	8N4Q001LG-0139CDI	2C Programmable XO, LVDS, 2.5V, 20ppm with start up frequency of 200MHz. Provides clocks for DDR3 interface
U4	SY89832U	1:4 LVDS Fanout Buffer (used with U5 to provide clock for QSE and QTE board to board connectors)
U14	SY89832U	1:4 LVDS Fanout Buffer (used with U17 to provide clock for FMC “A”
U13	SY89832U	1:4 LVDS Fanout Buffer (used with U17 to provide clock for FMC “A”
U32	XG-1000CA 100.0000M-EBL3	EMCC clock for faster configuration

U5, U17 (8N4Q001LG-0055CDI)	**FSEL1 (R182)**	**FSEL0 (R184)**	**Selects**
	0 (default)	**0 (default)**	**Frequency 0 (156.25MHz)**
	0	1	Frequency 1 (125.00MHz)
	1	0	Frequency 2 (100.00MHz)
	1	1	Frequency 3 (25.175MHz)
U16,U22 (8N4Q001LG-0102CDI)	**FSEL1 (R143)**	**FSEL0 (R142)**	**Selects**
	0 (default)	**0 (default)**	**Frequency 0 (25.00MHz)**
	0	1	Frequency 1 (50.00MHz)
	1	0	Frequency 2 (100.00MHz)
	1	1	Frequency 3 (125.00MHz)
U6 (8N4Q001LG-0139CDI)	**FSEL1 (R140)**	**FSEL0 (R141)**	**Selects**
	0	0	Frequency 0 (170.00MHz)
	0 (default)	**1 (default)**	**Frequency 1 (200.00MHz)**
	1	0	Frequency 2 (220.00MHz)
	1	1	Frequency 3 (250.00MHz)

Table (3): Clock Summary

2.6) DDR-III Interfaces

The HTG-777 platform is populated with one 204-pin DDR3 SODIMM socket supporting up to 8 GB of memory density.

Table (4) illustrates FPGA pin assignment for the DDR3 interfaces.

DDR3 Signal Name	Virtex 7 FPGA Pin Number
DDR3_A[0]	AN18
DDR3_A[1]	BB16
DDR3_A[10]	AN19
DDR3_A[11]	AU18
DDR3_A[12]	AR17
DDR3_A[13]	AW20
DDR3_A[14]	AW17
DDR3_A[15]	AV18
DDR3_A[2]	AT20
DDR3_A[3]	AR18
DDR3_A[4]	AV20
DDR3_A[5]	AR19
DDR3_A[6]	AU19
DDR3_A[7]	AV19
DDR3_A[8]	AU16
DDR3_A[9]	AT16
DDR3_BA[0]	AY19
DDR3_BA[1]	BA16
DDR3_BA[2]	AP17
DDR3_CAS_N	AY20
DDR3_CK0_N	AM17
DDR3_CK0_P	AM18
DDR3_CK1_N	AM19
DDR3_CK1_P	AL19
DDR3_CKE0	AW18
DDR3_CKE1	AV16
DDR3_CS0_N	AY18
DDR3_CS1_N	AT19
DDR3_DM[0]	BB13
DDR3_DM[1]	AV13
DDR3_DM[2]	AM11
DDR3_DM[3]	AK14
DDR3_DM[4]	AK23
DDR3_DM[5]	AN24
DDR3_DM[6]	AW22
DDR3_DM[7]	AY24
DDR3_DQ[0]	AY12
DDR3_DQ[1]	AW12
DDR3_DQ[10]	AV15
DDR3_DQ[11]	AR15

DDR3_DQ[12]	AT12
DDR3_DQ[13]	AU12
DDR3_DQ[14]	AU14
DDR3_DQ[15]	AT15
DDR3_DQ[16]	AN13
DDR3_DQ[17]	AR14
DDR3_DQ[18]	AM12
DDR3_DQ[19]	AM13
DDR3_DQ[2]	AY13
DDR3_DQ[20]	AP11
DDR3_DQ[21]	AN11
DDR3_DQ[22]	AP13
DDR3_DQ[23]	AT14
DDR3_DQ[24]	AJ12
DDR3_DQ[25]	AK13
DDR3_DQ[26]	AL15
DDR3_DQ[27]	AL16
DDR3_DQ[28]	AK12
DDR3_DQ[29]	AJ13
DDR3_DQ[3]	BB14
DDR3_DQ[30]	AJ15
DDR3_DQ[31]	AJ16
DDR3_DQ[32]	AL21
DDR3_DQ[33]	AK20
DDR3_DQ[34]	AJ21
DDR3_DQ[35]	AJ20
DDR3_DQ[36]	AL20
DDR3_DQ[37]	AM21
DDR3_DQ[38]	AL22
DDR3_DQ[39]	AJ23
DDR3_DQ[4]	BA12
DDR3_DQ[40]	AN21
DDR3_DQ[41]	AN23
DDR3_DQ[42]	AM23
DDR3_DQ[43]	AM24
DDR3_DQ[44]	AP21
DDR3_DQ[45]	AT22
DDR3_DQ[46]	AR23
DDR3_DQ[47]	AR22
DDR3_DQ[48]	AU23
DDR3_DQ[49]	AW23
DDR3_DQ[5]	BB12
DDR3_DQ[50]	AV23
DDR3_DQ[51]	AR24
DDR3_DQ[52]	AW21
DDR3_DQ[53]	AV21
DDR3_DQ[54]	AT24
DDR3_DQ[55]	AU24

DDR3_DQ[56]	BA21
DDR3_DQ[57]	AY25
DDR3_DQ[58]	BB23
DDR3_DQ[59]	BA24
DDR3_DQ[6]	AY14
DDR3_DQ[60]	BB21
DDR3_DQ[61]	AY23
DDR3_DQ[62]	BB24
DDR3_DQ[63]	BA25
DDR3_DQ[7]	AW15
DDR3_DQ[8]	AU13
DDR3_DQ[9]	AW13
DDR3_DQS_N[0]	BA14
DDR3_DQS_N[1]	AR12
DDR3_DQS_N[2]	AN14
DDR3_DQS_N[3]	AL14
DDR3_DQS_N[4]	AK22
DDR3_DQS_N[5]	AP22
DDR3_DQS_N[6]	AU21
DDR3_DQS_N[7]	BB22
DDR3_DQS_P[0]	BA15
DDR3_DQS_P[1]	AP12
DDR3_DQS_P[2]	AN15
DDR3_DQS_P[3]	AK15
DDR3_DQS_P[4]	AJ22
DDR3_DQS_P[5]	AP23
DDR3_DQS_P[6]	AT21
DDR3_DQS_P[7]	BA22
DDR3_EVENT_N	AP20
DDR3_ODT0	BA19
DDR3_ODT1	BA20
DDR3_RAS_N	AY17
DDR3_RST_N	AW16
DDR3_WE_N	BB19
SYS_CLK_DDR3_N	AU17
SYS_CLK_DDR3_P	AT17

Table (4): DDR3 SODIMM FPGA Pin Assignment

2.6.1) DDR3 Clock

As illustrated by figure (5), the DDR3 clock for the SODIMM is generated by high-performance low-jitter IDT 8N4Q001LG-0102CDI programmable Oscillator. Each oscillator can hold up to 4 factory pre-programmed frequencies. As shown by table (3), pre-programmed values of the U6 are 170, 200, 220 and 250MHz (selectable by R18 and R20). The default setting is for output frequency of 200MHz. Although the default frequencies are set, this oscillator can be controlled by FPGA through I2C interface for different clock values.

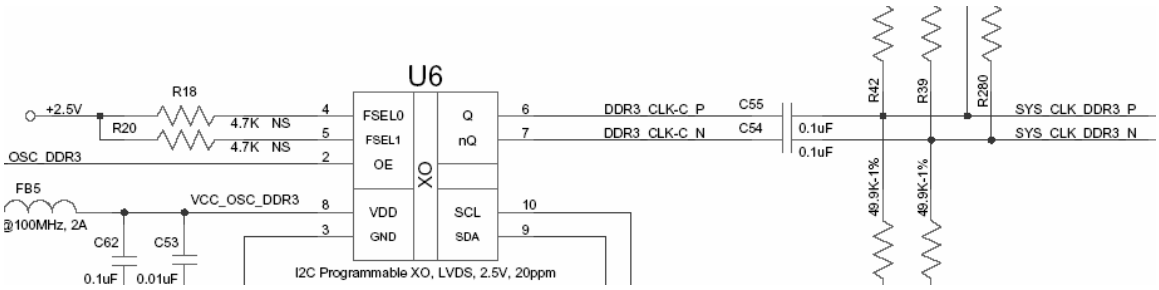

Figure (5): DDR3 Clock Circuit

The ICS8N4Q001 is a Quad-Frequency Programmable Clock Oscillator with very flexible frequency programming and delivers excellent phase noise performance at <0.5 ps rms 1kHz - 20MHz. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance, combined with high power supply noise rejection. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 10-lead ceramic 5mm x 7mm x 1.55mm package. Besides the 4 default power-up frequencies set by the FSEL0 and FSEL1 pins, the ICS8N4Q001 can be programmed via the I2C interface to output clock frequencies between 15.476 to 866.67MHz and from 975 to 1,300MHz to a very high degree of precision with a frequency step size of 435.9Hz ÷ N (N: PLL post divider). Since the FSEL0 and FSEL1 pins are mapped to 4 independent PLL M and N divider registers (P, MINT, MFRAC and N), reprogramming those registers to other frequencies under control of FSEL0 and FSEL1 is supported.

2.7) FPGA Mezzanine Card FMC) Interfaces

The HTG-777 development platform is populated with **three** 400-pin Samtec connector for High Pin Count (HPC) implementation of Vita 57 FPGA Mezzanine Card (FMC) interface. The Vita57 calls for fixed location of IOs, Power, Clocks, and Jtag signals so any compliant module can easily be pluggable into any compliant carrier card.

Each FMC connector provides access to **160** single-ended I/Os and **8** Serial Transceivers. The HTG-777 provides access to total of 480 single-ended and 24 Serial I/Os through three FMC connectors.

Figure (6) illustrates carrier card connector (Samtec Part # **ASP-134486-01)** grid labeling (used for hosting FMC daughter cards – FMC "A")

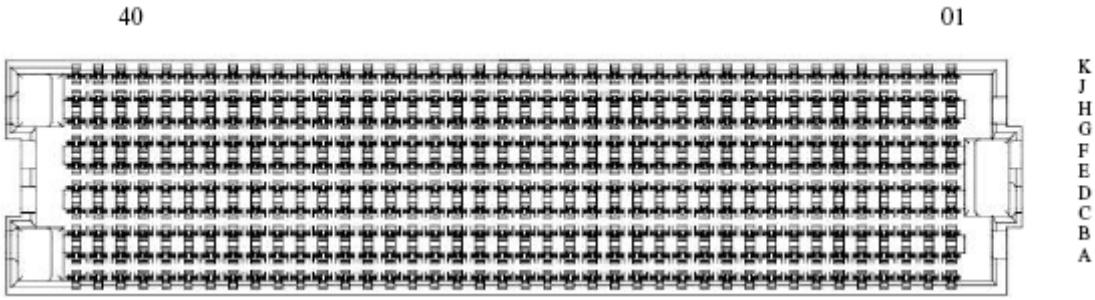

Figure (6): Carrier Card Connector Grid Labeling

Figure (7) illustrates FMC Module connector (Samtec Part # **ASP-134488-01**) grid labeling (used for connecting the HTG-777 as daughter card to carrier cards – FMC "B" and "C")

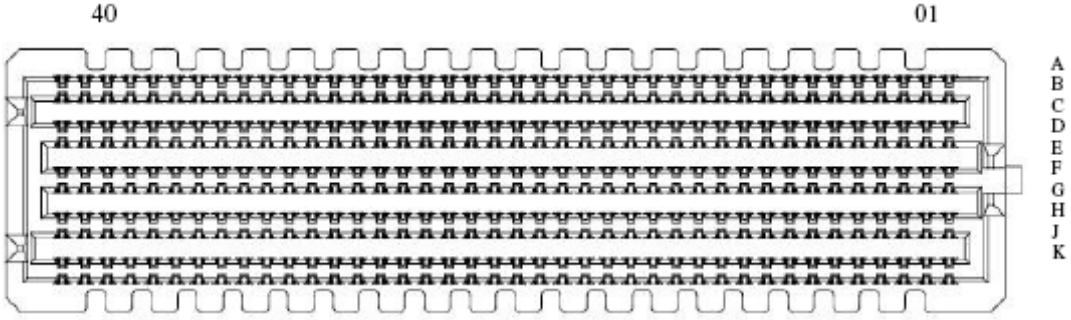

Figure (7): FMC Module Connector Grid Labeling

To increase FPGA gate count of the HTG-777 platform, the FMC connectors can be used in conjunction with additional HTG-777 modules.

FMC to FMC cables are also available for connecting the HTG-777 platforms to each other or similar Vita57 compliant carrier boards or modules. Additional information is available at http://hitechglobal.com/FMCModules/FMC_Cable.htm

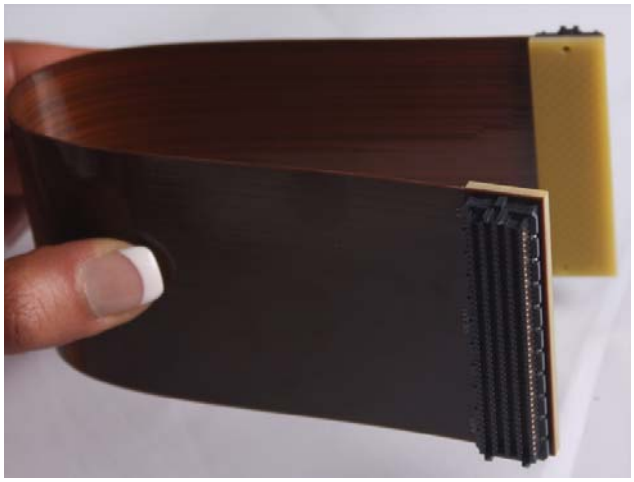

Image (4): FMC To FMC Cable

Table (5) illustrates the exact location of the fixed functional pins on a High Pin Count (HPC) FMC connector.

K	J	H	G	F	E	D	C	B	A
VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
		LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table (5): Vita57 FMC Pin Assignment

Table (6a, b, and c) illustrate FPGA pin assignments for the FMC Connectors J3, J6, and J10

FMC "A" Signal Name (J10)	Virtex-7 FPGA Pin Number
FMC_A_CLK[2]_BI_N	H14
FMC_A_CLK[2]_BI_P	H15
FMC_A_CLK[3]_BI_N	G18
FMC_A_CLK[3]_BI_P	H19
FMC_A_DP[0]_C2M_N	BA5
FMC_A_DP[0]_C2M_P	BA6
FMC_A_DP[0]_M2C_N	BA1
FMC_A_DP[0]_M2C_P	BA2
FMC_A_DP[1]_C2M_N	BB7
FMC_A_DP[1]_C2M_P	BB8

FMC_A_DP[1]_M2C_N	BB3
FMC_A_DP[1]_M2C_P	BB4
FMC_A_DP[2]_C2M_N	AY7
FMC_A_DP[2]_C2M_P	AY8
FMC_A_DP[2]_M2C_N	AY3
FMC_A_DP[2]_M2C_P	AY4
FMC_A_DP[3]_C2M_N	AW5
FMC_A_DP[3]_C2M_P	AW6
FMC_A_DP[3]_M2C_N	AW1
FMC_A_DP[3]_M2C_P	AW2
FMC_A_DP[4]_C2M_N	AU5
FMC_A_DP[4]_C2M_P	AU6
FMC_A_DP[4]_M2C_N	AU1
FMC_A_DP[4]_M2C_P	AU2
FMC_A_DP[5]_C2M_N	AP7
FMC_A_DP[5]_C2M_P	AP8
FMC_A_DP[5]_M2C_N	AR1
FMC_A_DP[5]_M2C_P	AR2
FMC_A_DP[6]_C2M_N	AR5
FMC_A_DP[6]_C2M_P	AR6
FMC_A_DP[6]_M2C_N	AT3
FMC_A_DP[6]_M2C_P	AT4
FMC_A_DP[7]_C2M_N	AV7
FMC_A_DP[7]_C2M_P	AV8
FMC_A_DP[7]_M2C_N	AV3
FMC_A_DP[7]_M2C_P	AV4
FMC_A_HA[0]_CC_N	F27
FMC_A_HA[0]_CC_P	F26
FMC_A_HA[1]_CC_N	F31
FMC_A_HA[1]_CC_P	F30
FMC_A_HA[10]_N	C26
FMC_A_HA[10]_P	C25
FMC_A_HA[11]_N	D26
FMC_A_HA[11]_P	D25
FMC_A_HA[12]_N	A25
FMC_A_HA[12]_P	A24
FMC_A_HA[13]_N	C29
FMC_A_HA[13]_P	C28
FMC_A_HA[14]_N	B27
FMC_A_HA[14]_P	B26
FMC_A_HA[15]_N	D28
FMC_A_HA[15]_P	D27
FMC_A_HA[16]_N	A32
FMC_A_HA[16]_P	A31
FMC_A_HA[17]_CC_N	A27
FMC_A_HA[17]_CC_P	A26
FMC_A_HA[18]_CC_N	B29
FMC_A_HA[18]_CC_P	B28

FMC_A_HA[19]_N	B31
FMC_A_HA[19]_P	C31
FMC_A_HA[2]_N	E22
FMC_A_HA[2]_P	F22
FMC_A_HA[20]_N	C30
FMC_A_HA[20]_P	D30
FMC_A_HA[21]_N	A30
FMC_A_HA[21]_P	A29
FMC_A_HA[22]_N	B24
FMC_A_HA[22]_P	C24
FMC_A_HA[23]_N	D31
FMC_A_HA[23]_P	E30
FMC_A_HA[3]_N	E25
FMC_A_HA[3]_P	F25
FMC_A_HA[4]_N	E28
FMC_A_HA[4]_P	E27
FMC_A_HA[5]_N	E29
FMC_A_HA[5]_P	F29
FMC_A_HA[6]_N	B23
FMC_A_HA[6]_P	C23
FMC_A_HA[7]_N	D23
FMC_A_HA[7]_P	D22
FMC_A_HA[8]_N	E24
FMC_A_HA[8]_P	E23
FMC_A_HA[9]_N	A22
FMC_A_HA[9]_P	B22
FMC_A_HB[0]_CC_N	BA27
FMC_A_HB[0]_CC_P	BA26
FMC_A_HB[1]_N	BB29
FMC_A_HB[1]_P	BB28
FMC_A_HB[10]_N	AV28
FMC_A_HB[10]_P	AU28
FMC_A_HB[11]_N	AT26
FMC_A_HB[11]_P	AT25
FMC_A_HB[12]_N	AP28
FMC_A_HB[12]_P	AN28
FMC_A_HB[13]_N	AM27
FMC_A_HB[13]_P	AM26
FMC_A_HB[14]_N	AN26
FMC_A_HB[14]_P	AN25
FMC_A_HB[15]_N	AT27
FMC_A_HB[15]_P	AR27
FMC_A_HB[16]_N	AU27
FMC_A_HB[16]_P	AU26
FMC_A_HB[17]_CC_N	AJ26
FMC_A_HB[17]_CC_P	AJ25
FMC_A_HB[18]_N	AK25
FMC_A_HB[18]_P	AK24

FMC_A_HB[19]_N	AL27
FMC_A_HB[19]_P	AK27
FMC_A_HB[2]_N	AW28
FMC_A_HB[2]_P	AW27
FMC_A_HB[20]_N	AL26
FMC_A_HB[20]_P	AL25
FMC_A_HB[21]_N	AR25
FMC_A_HB[21]_P	AP25
FMC_A_HB[3]_N	AT29
FMC_A_HB[3]_P	AR29
FMC_A_HB[4]_N	AY28
FMC_A_HB[4]_P	AY27
FMC_A_HB[5]_N	AV29
FMC_A_HB[5]_P	AU29
FMC_A_HB[6]_CC_N	AW26
FMC_A_HB[6]_CC_P	AW25
FMC_A_HB[7]_N	AV26
FMC_A_HB[7]_P	AV25
FMC_A_HB[8]_N	BB27
FMC_A_HB[8]_P	BB26
FMC_A_HB[9]_N	AR28
FMC_A_HB[9]_P	AP27
FMC_A_LA[0]_CC_N	N20
FMC_A_LA[0]_CC_P	P20
FMC_A_LA[1]_CC_N	H20
FMC_A_LA[1]_CC_P	J20
FMC_A_LA[10]_N	C20
FMC_A_LA[10]_P	D20
FMC_A_LA[11]_N	D17
FMC_A_LA[11]_P	D18
FMC_A_LA[12]_N	E17
FMC_A_LA[12]_P	F17
FMC_A_LA[13]_N	A17
FMC_A_LA[13]_P	B17
FMC_A_LA[14]_N	A19
FMC_A_LA[14]_P	A20
FMC_A_LA[15]_N	A15
FMC_A_LA[15]_P	A16
FMC_A_LA[16]_N	B19
FMC_A_LA[16]_P	C19
FMC_A_LA[17]_CC_N	J15
FMC_A_LA[17]_CC_P	K15
FMC_A_LA[18]_CC_N	L15
FMC_A_LA[18]_CC_P	L16
FMC_A_LA[19]_N	N14
FMC_A_LA[19]_P	N15
FMC_A_LA[2]_N	N18
FMC_A_LA[2]_P	N19

FMC_A_LA[20]_N	M16
FMC_A_LA[20]_P	N16
FMC_A_LA[21]_N	M11
FMC_A_LA[21]_P	M12
FMC_A_LA[22]_N	M13
FMC_A_LA[22]_P	N13
FMC_A_LA[23]_N	L14
FMC_A_LA[23]_P	M14
FMC_A_LA[24]_N	H13
FMC_A_LA[24]_P	J13
FMC_A_LA[25]_N	J12
FMC_A_LA[25]_P	K12
FMC_A_LA[26]_N	K13
FMC_A_LA[26]_P	K14
FMC_A_LA[27]_N	G13
FMC_A_LA[27]_P	G14
FMC_A_LA[28]_N	E13
FMC_A_LA[28]_P	E14
FMC_A_LA[29]_N	F12
FMC_A_LA[29]_P	G12
FMC_A_LA[3]_N	L17
FMC_A_LA[3]_P	M17
FMC_A_LA[30]_N	C13
FMC_A_LA[30]_P	D13
FMC_A_LA[31]_N	D15
FMC_A_LA[31]_P	D16
FMC_A_LA[32]_N	A14
FMC_A_LA[32]_P	B14
FMC_A_LA[33]_N	C14
FMC_A_LA[33]_P	C15
FMC_A_LA[4]_N	L19
FMC_A_LA[4]_P	L20
FMC_A_LA[5]_N	J17
FMC_A_LA[5]_P	K17
FMC_A_LA[6]_N	M18
FMC_A_LA[6]_P	M19
FMC_A_LA[7]_N	G17
FMC_A_LA[7]_P	H18
FMC_A_LA[8]_N	J18
FMC_A_LA[8]_P	K19
FMC_A_LA[9]_N	F19
FMC_A_LA[9]_P	G19
FMC_A_PG_C2M_F	L37
FMC_A_PG_M2C_F	M37
CLK_MRCC_FMC_A_N	AW40
CLK_MRCC_FMC_A_P	AV40
CLK0_MGT_FMC_A_N	AT7
CLK0_MGT_FMC_A_P	AT8

CLK1_MGT_FMC_A_N	AW9
CLK1_MGT_FMC_A_P	AW10
CLK_MRCC_FMC_A_N	AW40

Table (6.a): FPGA Mezzanine Connectors pin assignment (FMC "A")

FMC "B" Signal Name (J3)	Virtex-7 FPGA Pin Number
FMC_B_CLK[0]_M2C_N	L24
FMC_B_CLK[0]_M2C_P	M24
FMC_B_CLK[1]_M2C_N	E35
FMC_B_CLK[1]_M2C_P	E34
FMC_B_DP[0]_C2M_N	K3
FMC_B_DP[0]_C2M_P	K4
FMC_B_DP[0]_M2C_N	J5
FMC_B_DP[0]_M2C_P	J6
FMC_B_DP[1]_C2M_N	L1
FMC_B_DP[1]_C2M_P	L2
FMC_B_DP[1]_M2C_N	L5
FMC_B_DP[1]_M2C_P	L6
FMC_B_DP[2]_C2M_N	M3
FMC_B_DP[2]_C2M_P	M4
FMC_B_DP[2]_M2C_N	N5
FMC_B_DP[2]_M2C_P	N6
FMC_B_DP[3]_C2M_N	N1
FMC_B_DP[3]_C2M_P	N2
FMC_B_DP[3]_M2C_N	P7
FMC_B_DP[3]_M2C_P	P8
FMC_B_DP[4]_C2M_N	R1
FMC_B_DP[4]_C2M_P	R2
FMC_B_DP[4]_M2C_N	U5
FMC_B_DP[4]_M2C_P	U6
FMC_B_DP[5]_C2M_N	U1
FMC_B_DP[5]_C2M_P	U2
FMC_B_DP[5]_M2C_N	W5
FMC_B_DP[5]_M2C_P	W6
FMC_B_DP[6]_C2M_N	T3
FMC_B_DP[6]_C2M_P	T4
FMC_B_DP[6]_M2C_N	V3
FMC_B_DP[6]_M2C_P	V4
FMC_B_DP[7]_C2M_N	P3
FMC_B_DP[7]_C2M_P	P4
FMC_B_DP[7]_M2C_N	R5
FMC_B_DP[7]_M2C_P	R6
FMC_B_GBTCLK[0]_M2	K7
FMC_B_GBTCLK[0]_M2	K8
FMC_B_GBTCLK[1]_M2	T7
FMC_B_GBTCLK[1]_M2	T8
FMC_B_HA[0]_CC_N	M31

FMC_B_HA[0]_CC_P	N30
FMC_B_HA[1]_CC_N	N31
FMC_B_HA[1]_CC_P	P30
FMC_B_HA[10]_N	W31
FMC_B_HA[10]_P	W30
FMC_B_HA[11]_N	L35
FMC_B_HA[11]_P	L34
FMC_B_HA[12]_N	M29
FMC_B_HA[12]_P	M28
FMC_B_HA[13]_N	L30
FMC_B_HA[13]_P	L29
FMC_B_HA[14]_N	K30
FMC_B_HA[14]_P	K29
FMC_B_HA[15]_N	P28
FMC_B_HA[15]_P	R28
FMC_B_HA[16]_N	N29
FMC_B_HA[16]_P	N28
FMC_B_HA[17]_CC_N	K32
FMC_B_HA[17]_CC_P	L31
FMC_B_HA[18]_CC_N	L32
FMC_B_HA[18]_CC_P	M32
FMC_B_HA[19]_N	U29
FMC_B_HA[19]_P	V29
FMC_B_HA[2]_N	P31
FMC_B_HA[2]_P	R30
FMC_B_HA[20]_N	T30
FMC_B_HA[20]_P	T29
FMC_B_HA[21]_N	Y30
FMC_B_HA[21]_P	Y29
FMC_B_HA[22]_N	T31
FMC_B_HA[22]_P	U31
FMC_B_HA[23]_N	H35
FMC_B_HA[23]_P	H34
FMC_B_HA[3]_N	M34
FMC_B_HA[3]_P	M33
FMC_B_HA[4]_N	J33
FMC_B_HA[4]_P	J32
FMC_B_HA[5]_N	K34
FMC_B_HA[5]_P	K33
FMC_B_HA[6]_N	V31
FMC_B_HA[6]_P	V30
FMC_B_HA[7]_N	J35
FMC_B_HA[7]_P	K35
FMC_B_HA[8]_N	H30
FMC_B_HA[8]_P	J30
FMC_B_HA[9]_N	H31
FMC_B_HA[9]_P	J31
FMC_B_HB[0]_CC_N	AD33

FMC_B_HB[0]_CC_P	AD32
FMC_B_HB[1]_N	AE30
FMC_B_HB[1]_P	AE29
FMC_B_HB[10]_N	AF36
FMC_B_HB[10]_P	AF35
FMC_B_HB[11]_N	AE35
FMC_B_HB[11]_P	AE34
FMC_B_HB[12]_N	AA37
FMC_B_HB[12]_P	Y37
FMC_B_HB[13]_N	AA36
FMC_B_HB[13]_P	Y35
FMC_B_HB[14]_N	AC29
FMC_B_HB[14]_P	AB29
FMC_B_HB[15]_N	AA35
FMC_B_HB[15]_P	AA34
FMC_B_HB[16]_N	AB32
FMC_B_HB[16]_P	AB31
FMC_B_HB[17]_CC_N	AC33
FMC_B_HB[17]_CC_P	AB33
FMC_B_HB[18]_N	AD30
FMC_B_HB[18]_P	AC30
FMC_B_HB[19]_N	AA32
FMC_B_HB[19]_P	AA31
FMC_B_HB[2]_N	AE33
FMC_B_HB[2]_P	AE32
FMC_B_HB[20]_N	AD31
FMC_B_HB[20]_P	AC31
FMC_B_HB[21]_N	AA30
FMC_B_HB[21]_P	AA29
FMC_B_HB[3]_N	AG34
FMC_B_HB[3]_P	AF34
FMC_B_HB[4]_N	AD37
FMC_B_HB[4]_P	AD36
FMC_B_HB[5]_N	AF37
FMC_B_HB[5]_P	AE37
FMC_B_HB[6]_CC_N	AD35
FMC_B_HB[6]_CC_P	AC34
FMC_B_HB[7]_N	AF32
FMC_B_HB[7]_P	AF31
FMC_B_HB[8]_N	AB37
FMC_B_HB[8]_P	AB36
FMC_B_HB[9]_N	AC36
FMC_B_HB[9]_P	AC35
FMC_B_LA[0]_CC_N	C36
FMC_B_LA[0]_CC_P	C35
FMC_B_LA[1]_CC_N	D36
FMC_B_LA[1]_CC_P	D35
FMC_B_LA[10]_N	G33

FMC_B_LA[10]_P	H33
FMC_B_LA[11]_N	F35
FMC_B_LA[11]_P	F34
FMC_B_LA[12]_N	C34
FMC_B_LA[12]_P	C33
FMC_B_LA[13]_N	F37
FMC_B_LA[13]_P	F36
FMC_B_LA[14]_N	G37
FMC_B_LA[14]_P	G36
FMC_B_LA[15]_N	G38
FMC_B_LA[15]_P	H38
FMC_B_LA[16]_N	H36
FMC_B_LA[16]_P	J36
FMC_B_LA[17]_CC_N	J26
FMC_B_LA[17]_CC_P	J25
FMC_B_LA[18]_CC_N	K25
FMC_B_LA[18]_CC_P	K24
FMC_B_LA[19]_N	J28
FMC_B_LA[19]_P	K28
FMC_B_LA[2]_N	C39
FMC_B_LA[2]_P	C38
FMC_B_LA[20]_N	L26
FMC_B_LA[20]_P	L25
FMC_B_LA[21]_N	H26
FMC_B_LA[21]_P	H25
FMC_B_LA[22]_N	G27
FMC_B_LA[22]_P	G26
FMC_B_LA[23]_N	H29
FMC_B_LA[23]_P	H28
FMC_B_LA[24]_N	G24
FMC_B_LA[24]_P	H24
FMC_B_LA[25]_N	J23
FMC_B_LA[25]_P	K23
FMC_B_LA[26]_N	G29
FMC_B_LA[26]_P	G28
FMC_B_LA[27]_N	J27
FMC_B_LA[27]_P	K27
FMC_B_LA[28]_N	G22
FMC_B_LA[28]_P	G21
FMC_B_LA[29]_N	J22
FMC_B_LA[29]_P	K22
FMC_B_LA[3]_N	A36
FMC_B_LA[3]_P	A35
FMC_B_LA[30]_N	L22
FMC_B_LA[30]_P	M22
FMC_B_LA[31]_N	H21
FMC_B_LA[31]_P	J21
FMC_B_LA[32]_N	P23

FMC_B_LA[32]_P	P22
FMC_B_LA[33]_N	L21
FMC_B_LA[33]_P	M21
FMC_B_LA[4]_N	A39
FMC_B_LA[4]_P	B39
FMC_B_LA[5]_N	D33
FMC_B_LA[5]_P	E33
FMC_B_LA[6]_N	D32
FMC_B_LA[6]_P	E32
FMC_B_LA[7]_N	B33
FMC_B_LA[7]_P	B32
FMC_B_LA[8]_N	A34
FMC_B_LA[8]_P	B34
FMC_B_LA[9]_N	F32
FMC_B_LA[9]_P	G32
FMC_B_PG_C2M_F	K38
FMC_B_PG_M2C_F	M36
FMC_B_PRSNT_M2C_L_	K37

Table (6.b): FPGA Mezzanine Connectors pin assignment (FMC "B")

FMC "C" Signal Name (J6)	Virtex-7 FPGA Pin Number
FMC_C_CLK[0]_M2C_N	L40
FMC_C_CLK[0]_M2C_P	L39
FMC_C_CLK[1]_M2C_N	T37
FMC_C_CLK[1]_M2C_P	U36
FMC_C_DP[0]_C2M_N	B3
FMC_C_DP[0]_C2M_P	B4
FMC_C_DP[0]_M2C_N	A5
FMC_C_DP[0]_M2C_P	A6
FMC_C_DP[1]_C2M_N	C1
FMC_C_DP[1]_C2M_P	C2
FMC_C_DP[1]_M2C_N	B7
FMC_C_DP[1]_M2C_P	B8
FMC_C_DP[2]_C2M_N	D3
FMC_C_DP[2]_C2M_P	D4
FMC_C_DP[2]_M2C_N	C5
FMC_C_DP[2]_M2C_P	C6
FMC_C_DP[3]_C2M_N	E1
FMC_C_DP[3]_C2M_P	E2
FMC_C_DP[3]_M2C_N	D7
FMC_C_DP[3]_M2C_P	D8
FMC_C_DP[4]_C2M_N	G1
FMC_C_DP[4]_C2M_P	G2
FMC_C_DP[4]_M2C_N	F7
FMC_C_DP[4]_M2C_P	F8
FMC_C_DP[5]_C2M_N	J1
FMC_C_DP[5]_C2M_P	J2

FMC_C_DP[5]_M2C_N	H7
FMC_C_DP[5]_M2C_P	H8
FMC_C_DP[6]_C2M_N	H3
FMC_C_DP[6]_C2M_P	H4
FMC_C_DP[6]_M2C_N	G5
FMC_C_DP[6]_M2C_P	G6
FMC_C_DP[7]_C2M_N	F3
FMC_C_DP[7]_C2M_P	F4
FMC_C_DP[7]_M2C_N	E5
FMC_C_DP[7]_M2C_P	E6
FMC_C_GBTCLK[0]_M2	A9
FMC_C_GBTCLK[0]_M2	A10
FMC_C_GBTCLK[1]_M2	E9
FMC_C_GBTCLK[1]_M2	E10
FMC_C_HA[0]_CC_N	AF40
FMC_C_HA[0]_CC_P	AF39
FMC_C_HA[1]_CC_N	AG41
FMC_C_HA[1]_CC_P	AF41
FMC_C_HA[10]_N	AH39
FMC_C_HA[10]_P	AG39
FMC_C_HA[11]_N	AE42
FMC_C_HA[11]_P	AD42
FMC_C_HA[12]_N	AA39
FMC_C_HA[12]_P	Y39
FMC_C_HA[13]_N	AC41
FMC_C_HA[13]_P	AC40
FMC_C_HA[14]_N	AB42
FMC_C_HA[14]_P	AB41
FMC_C_HA[15]_N	AA42
FMC_C_HA[15]_P	Y42
FMC_C_HA[16]_N	AB39
FMC_C_HA[16]_P	AB38
FMC_C_HA[17]_CC_N	AD41
FMC_C_HA[17]_CC_P	AD40
FMC_C_HA[18]_CC_N	AE40
FMC_C_HA[18]_CC_P	AE39
FMC_C_HA[19]_N	AC39
FMC_C_HA[19]_P	AC38
FMC_C_HA[2]_N	AH38
FMC_C_HA[2]_P	AG38
FMC_C_HA[20]_N	Y40
FMC_C_HA[20]_P	W40
FMC_C_HA[21]_N	AE38
FMC_C_HA[21]_P	AD38
FMC_C_HA[22]_N	AA41
FMC_C_HA[22]_P	AA40
FMC_C_HA[23]_N	AL40
FMC_C_HA[23]_P	AK40

FMC_C_HA[3]_N	AK38
FMC_C_HA[3]_P	AJ38
FMC_C_HA[4]_N	AJ41
FMC_C_HA[4]_P	AJ40
FMC_C_HA[5]_N	AK42
FMC_C_HA[5]_P	AJ42
FMC_C_HA[6]_N	AL39
FMC_C_HA[6]_P	AK39
FMC_C_HA[7]_N	AL42
FMC_C_HA[7]_P	AL41
FMC_C_HA[8]_N	AG42
FMC_C_HA[8]_P	AF42
FMC_C_HA[9]_N	AH41
FMC_C_HA[9]_P	AH40
FMC_C_HB[0]_CC_N	AW33
FMC_C_HB[0]_CC_P	AW32
FMC_C_HB[1]_N	AW31
FMC_C_HB[1]_P	AV30
FMC_C_HB[10]_N	AV33
FMC_C_HB[10]_P	AU32
FMC_C_HB[11]_N	BB34
FMC_C_HB[11]_P	BA34
FMC_C_HB[12]_N	AU36
FMC_C_HB[12]_P	AT36
FMC_C_HB[13]_N	AW36
FMC_C_HB[13]_P	AV36
FMC_C_HB[14]_N	AP30
FMC_C_HB[14]_P	AN30
FMC_C_HB[15]_N	AU34
FMC_C_HB[15]_P	AT34
FMC_C_HB[16]_N	AR33
FMC_C_HB[16]_P	AP33
FMC_C_HB[17]_CC_N	AV35
FMC_C_HB[17]_CC_P	AV34
FMC_C_HB[18]_N	AP31
FMC_C_HB[18]_P	AN31
FMC_C_HB[19]_N	AT35
FMC_C_HB[19]_P	AR34
FMC_C_HB[2]_N	AY30
FMC_C_HB[2]_P	AW30
FMC_C_HB[20]_N	AR32
FMC_C_HB[20]_P	AP32
FMC_C_HB[21]_N	AU33
FMC_C_HB[21]_P	AT32
FMC_C_HB[3]_N	BB31
FMC_C_HB[3]_P	BA30
FMC_C_HB[4]_N	BB33
FMC_C_HB[4]_P	BB32

FMC_C_HB[5]_N	BA32
FMC_C_HB[5]_P	BA31
FMC_C_HB[6]_CC_N	AY33
FMC_C_HB[6]_CC_P	AY32
FMC_C_HB[7]_N	AV31
FMC_C_HB[7]_P	AU31
FMC_C_HB[8]_N	BB36
FMC_C_HB[8]_P	BA36
FMC_C_HB[9]_N	BA35
FMC_C_HB[9]_P	AY34
FMC_C_LA[0]_CC_N	T39
FMC_C_LA[0]_CC_P	U39
FMC_C_LA[1]_CC_N	V36
FMC_C_LA[1]_CC_P	V35
FMC_C_LA[10]_N	T42
FMC_C_LA[10]_P	U41
FMC_C_LA[11]_N	R35
FMC_C_LA[11]_P	T34
FMC_C_LA[12]_N	R37
FMC_C_LA[12]_P	T36
FMC_C_LA[13]_N	R39
FMC_C_LA[13]_P	R38
FMC_C_LA[14]_N	P38
FMC_C_LA[14]_P	P37
FMC_C_LA[15]_N	N34
FMC_C_LA[15]_P	N33
FMC_C_LA[16]_N	P36
FMC_C_LA[16]_P	P35
FMC_C_LA[17]_CC_N	K40
FMC_C_LA[17]_CC_P	K39
FMC_C_LA[18]_CC_N	L41
FMC_C_LA[18]_CC_P	M41
FMC_C_LA[19]_N	P40
FMC_C_LA[19]_P	R40
FMC_C_LA[2]_N	W33
FMC_C_LA[2]_P	W32
FMC_C_LA[20]_N	P42
FMC_C_LA[20]_P	R42
FMC_C_LA[21]_N	J42
FMC_C_LA[21]_P	K42
FMC_C_LA[22]_N	M39
FMC_C_LA[22]_P	N38
FMC_C_LA[23]_N	L42
FMC_C_LA[23]_P	M42
FMC_C_LA[24]_N	E42
FMC_C_LA[24]_P	F42
FMC_C_LA[25]_N	G42
FMC_C_LA[25]_P	G41

FMC_C_LA[26]_N	H41
FMC_C_LA[26]_P	H40
FMC_C_LA[27]_N	J41
FMC_C_LA[27]_P	J40
FMC_C_LA[28]_N	D42
FMC_C_LA[28]_P	D41
FMC_C_LA[29]_N	G39
FMC_C_LA[29]_P	H39
FMC_C_LA[3]_N	V34
FMC_C_LA[3]_P	V33
FMC_C_LA[30]_N	B42
FMC_C_LA[30]_P	B41
FMC_C_LA[31]_N	F41
FMC_C_LA[31]_P	F40
FMC_C_LA[32]_N	D40
FMC_C_LA[32]_P	E40
FMC_C_LA[33]_N	A41
FMC_C_LA[33]_P	A40
FMC_C_LA[4]_N	W37
FMC_C_LA[4]_P	W36
FMC_C_LA[5]_N	V38
FMC_C_LA[5]_P	W38
FMC_C_LA[6]_N	U38
FMC_C_LA[6]_P	U37
FMC_C_LA[7]_N	U42
FMC_C_LA[7]_P	V41
FMC_C_LA[8]_N	W42
FMC_C_LA[8]_P	W41
FMC_C_LA[9]_N	T41
FMC_C_LA[9]_P	T40
FMC_C_PG_C2M_F	C40
FMC_C_PG_M2C_F	M38
FMC_C_PRSNT_M2C_L_	N39

Table (6.c): FPGA Mezzanine Connectors pin assignment (FMC "C")

FMC Vadjust

V_Adjust for FMC "B" and "C" (hosting FMC modules) can be set to different values below 1.8V (supported by Virtex-7 FPGAs) by using the changing value of RFB as shown by the following formula:

$$V_{OUT} = 0.8V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

Figure (8) illustrates RFB resistor setting for FMC "B" and "C"

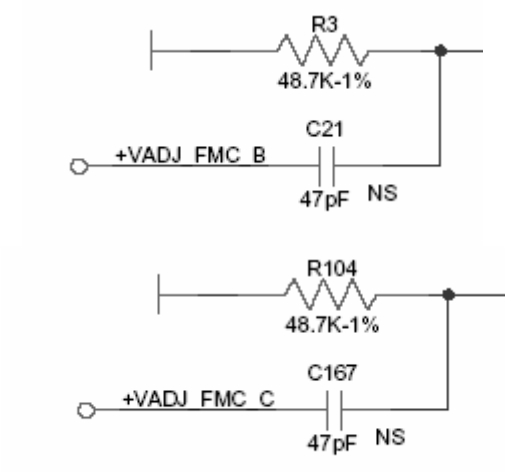

Figure (8): V_Adjust Setting For FMC "B" & "C"

2.8) Additional Board To Board Connectors

In addition to stacking option through the FMC connectors, two or more HTG-777 boards can be connected through twelve serial I/Os available on J1 (QTE) and J11 (QSE) connectors. These connectors can also be used for additional daughter card or cable interface.

Table (7) illustrates pin assignment for the J1 and J11 connectors.

Signal Name	Virtex-7 FPGA Pin Number
B2B_Gb_MGT1_CLK_N	AH7
B2B_Gb_MGT1_CLK_P	AH8
B2B_Gb_MGT2_CLK_N	Y7
B2B_Gb_MGT2_CLK_P	Y8
B2B_Gb_MGT3_CLK_N	AD7
B2B_Gb_MGT3_CLK_P	AD8
B2B_Gb_QSE_RX0_N	AN5
B2B_Gb_QSE_RX0_P	AN6
B2B_Gb_QSE_RX1_N	AM7
B2B_Gb_QSE_RX1_P	AM8
B2B_Gb_QSE_RX2_N	AL5
B2B_Gb_QSE_RX2_P	AL6
B2B_Gb_QSE_RX3_N	AJ5
B2B_Gb_QSE_RX3_P	AJ6
B2B_Gb_QSE_RX4_N	AG5
B2B_Gb_QSE_RX4_P	AG6
B2B_Gb_QSE_RX5_N	AF3
B2B_Gb_QSE_RX5_P	AF4
B2B_GB_QSE_TX0_N	AP3
B2B_Gb_QSE_TX0_P	AP4
B2B_Gb_QSE_TX1_N	AN1
B2B_GB_QSE_TX1_P	AN2

B2B_Gb_QSE_TX2_N	AM3
B2B_Gb_QSE_TX2_P	AM4
B2B_Gb_QSE_TX3_N	AL1
B2B_Gb_QSE_TX3_P	AL2
B2B_Gb_QSE_TX4_N	AK3
B2B_Gb_QSE_TX4_P	AK4
B2B_Gb_QSE_TX5_N	AJ1
B2B_Gb_QSE_TX5_P	AJ2
B2B_Gb_QTE_RX0_N	AC5
B2B_Gb_QTE_RX0_P	AC6
B2B_Gb_QTE_RX1_N	AB3
B2B_Gb_QTE_RX1_P	AB4
B2B_Gb_QTE_RX2_N	AA5
B2B_Gb_QTE_RX2_P	AA6
B2B_Gb_QTE_RX3_N	Y3
B2B_Gb_QTE_RX3_P	Y4
B2B_Gb_QTE_RX4_N	AE5
B2B_Gb_QTE_RX4_P	AE6
B2B_Gb_QTE_RX5_N	AD3
B2B_Gb_QTE_RX5_P	AD4
B2B_Gb_QTE_TX0_N	AE1
B2B_Gb_QTE_TX0_P	AE2
B2B_Gb_QTE_TX1_N	AC1
B2B_Gb_QTE_TX1_P	AC2
B2B_Gb_QTE_TX2_N	AA1
B2B_Gb_QTE_TX2_P	AA2
B2B_Gb_QTE_TX3_N	W1
B2B_Gb_QTE_TX3_P	W2
B2B_Gb_QTE_TX4_N	AH3
B2B_Gb_QTE_TX4_P	AH4
B2B_Gb_QTE_TX5_N	AG1
B2B_Gb_QTE_TX5_P	AG2

Table (7): Additional Board To Board Connection FPGA Pin Assignment

2.9) User Interfaces

The HTG-777 provides series of user LEDs, user I/Os and Push Buttons. Table (8) illustrates FPGA pin assignments and reference designators for each interface.

Signal Name	Virtex-7 FPGA Pin Number	Reference Designator
FPGA_USER_IO0_F	AY40	J4 - Pin # 1
FPGA_USER_IO1_F	AY39	J4 - Pin # 3
FPGA_USER_IO2_F	AT37	J4 - Pin # 5
FPGA_USER_IO3_F	BA37	J4 - Pin # 7
FPGA_USER_IO4_F	BB37	J4 - Pin # 9
FPGA_USER_IO5_F	AR37	J4 - Pin # 11
FPGA_USER_IO6_F	AY42	J4 - Pin # 13

FPGA_USER_IO7_F	AP38	J4 - Pin # 15
FPGA_USER_LED0	AU38	D12
FPGA_USER_LED1	AM34	D14
FPGA_USER_LED2	AV38	D16
FPGA_USER_LED3	AK32	D17
FPGA_USER_LED4	AN34	D19
FPGA_USER_LED5	AW38	D21
FPGA_USER_LED6	AL32	D23
FPGA_USER_LED7	AW37	D25
FPGA_USER_PB	AP18	S3
FPGA_USER_SW1	AJ18	S2: Pin # 16
FPGA_USER_SW2	AN16	S2: Pin # 15
FPGA_USER_SW3	BB17	S2: Pin # 14
FPGA_USER_SW4	AM16	S2: Pin # 13
FPGA_USER_SW5	AL17	S2: Pin # 12
FPGA_USER_SW6	AK18	S2: Pin # 11
FPGA_USER_SW7	AK19	S2: Pin # 10
FPGA_USER_SW8	AK17	S2: Pin # 9

Table (8): User Interface FPGA Pin Assignment

2.10) IP Protection

The HTG-777 provides a special 1-wire circuit (connected to the FPGA pin # AL31) for protection of intellectual properties loaded to the FPGAs by using one Maxim DS2432 chips

The DS2432 combines 1024 bits of EEPROM, a 64-bit secret, an 8-byte register/control page with up to five user read/write bytes, a 512-bit SHA-1 engine, and a fully-featured 1-Wire interface in a single chip. Each DS2432 has its own 64-bit ROM registration number that is factory lasered into the chip to provide a guaranteed unique identity for absolute traceability. Data is transferred serially via the 1-Wire protocol, which requires only a single data lead and a ground return. The DS2432 has an additional memory area called the scratchpad that acts as a buffer when writing to the main memory, the register page or when installing a new secret. Data is first written to the scratchpad from where it can be read back. After the data has been verified, a copy scratchpad command will transfer the data to its final memory location, provided that the DS2432 receives a matching 160-Bit MAC. The computation of the MAC involves the secret and additional data stored in the DS2432 including the device's registration number. Only a new secret can be loaded without providing a MAC. The SHA-1 engine can also be activated to compute 160-bit message authentication codes (MAC) when reading a memory page or to compute a new secret, instead of loading it. Applications of the DS2432 include intellectual property security, after-market management of consumables, and tamper-proof data carriers.

Additional information is available at
http://datasheets.maximintegrated.com/en/ds/DS2432.pdf

2.11) USB To UART Port

The HTG-777 board provides one UART port through a peripheral USB connector. The port is supported by the Silicon labs CP2103 USB to UART controller chip.

The CP2103 is a highly-integrated USB-to-UART Bridge Controller providing a simple solution for updating RS-232/RS-485 designs to USB using a minimum of components and PCB space. The CP2103 includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and asynchronous serial data bus (UART) with full modem control signals in a compact 5x5 mm QFN-28 package (sometimes called "MLF" or "MLP"). No other external USB components are required.
The on-chip EEPROM may be used to customize the USB Vendor ID, Product ID, Product Description String, Power Descriptor, Device Release Number, and Device Serial Number as desired for OEM applications. The EEPROM is programmed on-board via the USB, allowing the programming step to be easily integrated into the product manufacturing and testing process.
Royalty-free Virtual COM Port (VCP) device drivers provided by Silicon Laboratories allow a CP2103-based product to appear as a COM port to PC applications. The CP2103 UART interface implements all RS-232/RS-485 signals, including control and handshaking signals; so, existing system firmware does not need to be modified. The device also features up to four GPIO signals that can be user-defined for status and control information. Support for I/O interface voltages down to 1.8 V is provided via a VIO pin. In many existing RS-232 designs, all that is required to update the design from RS-232 to USB is to replace the RS-232 level-translator with the CP2103.

Direct access driver support is available through the Silicon Laboratories USBXpress driver set. Go to www.silabs.com for the latest application notes and product support information for CP2103.

Table (9) illustrates FPGA pin assignment for the USB-TO-UART interface:

UART/USB Signal Name	Virtex-7 FPGA Pin Number
UART_CTS	AR42
UART_DCD	AV39
UART_DSR	AU39
UART_DTR	AN39
UART_GPIO0	AP40
UART_GPIO1	AP41
UART_GPIO2	AP42
UART_GPIO3	AN40
UART_RI	AN38
UART_RST_N	AT40
UART_RTS	AR40
UART_RXD	AR39
UART_SUSPEND_N	AT39
UART_TXD	AT42
USB_PERI_PWR	AR38

Table (9): USB/UART Interface FPGA Pin Assignment

2.12) Configuration

Xilinx FPGAs are CMOS configurable latch (CCL) based and must be configured at power-up from a non-volatile source. FPGA configuration is traditionally accomplished with a JTAG interface, a microprocessor, or the Xilinx PROMs (Platform Flash PROMs).

The onboard FPGA can be programmed either through JTAG connector (J7) or 1Gb (PC28F00AG18FE) Micron Flash device. Upon successful configuration of the onboard FPGA, the D10 LED illuminates.

The Flash device can also be used for storage.

Table (10) illustrates FPGA pin assignment for the Flash interface.

Flash Signal Name	Virtex-7 FPGA Pin Number
FPGA_A[0]	AJ28
FPGA_A[1]	AH28
FPGA_A[10]	AH29
FPGA_A[11]	AL30
FPGA_A[12]	AL29
FPGA_A[13]	AN33
FPGA_A[14]	AM33
FPGA_A[15]	AM32
FPGA_A[16]	AV41
FPGA_A[17]	AU41
FPGA_A[18]	BA42
FPGA_A[19]	AU42
FPGA_A[2]	AG31
FPGA_A[20]	AT41
FPGA_A[21]	BA40
FPGA_A[22]	BA39
FPGA_A[23]	BB39
FPGA_A[3]	AF30
FPGA_A[4]	AK29
FPGA_A[5]	AK28
FPGA_A[6]	AG29
FPGA_A[7]	AK30
FPGA_A[8]	AJ30
FPGA_A[9]	AH30
FPGA_ADV_N	AY37
FPGA_DONE	AL11
FPGA_DQ[0]	AM36
FPGA_DQ[1]	AN36
FPGA_DQ[10]	AH33
FPGA_DQ[11]	AK35
FPGA_DQ[12]	AL35
FPGA_DQ[13]	AJ31
FPGA_DQ[14]	AH34
FPGA_DQ[15]	AJ35
FPGA_DQ[2]	AJ36
FPGA_DQ[3]	AJ37
FPGA_DQ[4]	AK37
FPGA_DQ[5]	AL37
FPGA_DQ[6]	AN35
FPGA_DQ[7]	AP35
FPGA_DQ[8]	AM37
FPGA_DQ[9]	AG33
FPGA_FCS_N	AL36
FPGA_FOE_N	BA41

FPGA_FWE_N	BB41
FPGA_INIT	AG11
FPGA_RS0	AW42
FPGA_RS1	AW41

Table (10): Flash Interface FPGA Pin Assignment

2.13) I2C Bus Switch

The HTG-777 platform is supported by one I2C bus switch for controlling different onboard I2C Device. The PCA9548A is an octal bidirectional translating switch controlled via the I²C-bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register.

Figure (9) and table (11) illustrate the I2C system diagram and FPGA pin assignment for the I2C control signals

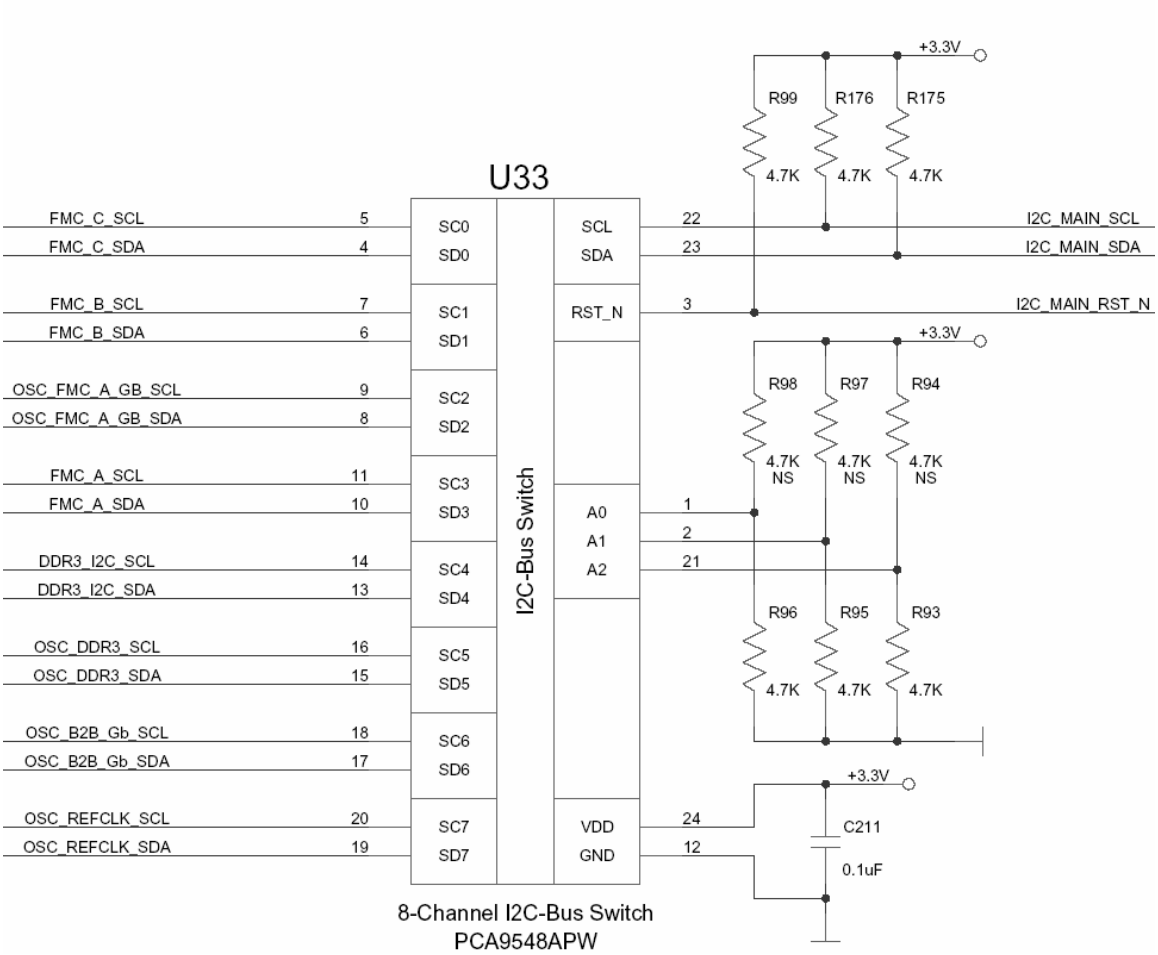

Figure (9): I2C Bus Switch

Signal Name	Virtex-7 FPGA Pin Number
I2C_MAIN_RST_F	AM42
I2C_MAIN_SCL_F	AM41
I2C_MAIN_SDA_F	AN41

Table (11): I2C Bus FPGA Pin Assignment

Chapter 3:Mezannine Cards

Vita 57 provides a mechanical standard for I/O mezzanine modules. This standard introduces a methodology that shall allow the front panel IO of IEEE 1101 form factor cards to be configured via mezzanine boards. Vita 57 modules have fixed locations for serial/parallel IOs, clocks, Jtag signals, VCC, and GND. HiTech Global's Vita 57 modules work with any Vita 57 compliant carrier boards.

The FMC standard specifies Samtec's SEARAY™ connector set. The VITA 57 SEAM/SEAF Series system provides 400 I/Os in a 40 x 10 configuration or 160 I/Os in a selectively loaded 40 x 10 configuration, in 8.5mm and 10mm stack heights.

HiTech Global offers a wide range of FMC daughter cards which can be used for expanding functionality of the main board. All of these FMC Modules should be used in conjunction with the HTG-AIRMAX-FMC conversion module when used with the HTG-777 platform.

3.1) Dual SFP+ (with external PHY)

The Dual SFP+ FMC daughter card provides access to two SFP+ ports (10Gbps each) interfacing to total of 8 serial transceivers (XUAI).

The onboard 10Gig PHY device is a physical layer transceiver with an integrated Electronic Dispersion Compensation (EDC) engine - compliant with IEEE802.3aq specifications. The device integrates industry-leading SerDes/PHY technology with low-power EDC engine with up to 5db of margin over the symmetric stress test pulse sensitivity specifications defined in the 10GASE-LRM standard.

Each PHY device provides full PCS, PMA, and XGXS sub-layer functionality through the consolidation of the receiver and transmitter PHY functions on a single chip along with the integration of encode/decode/alignment logic, FIFOs, on-chip clock drivers, multiple loop-back features and PRBS & Ethernet frame generation & verification for both the line side and the system side.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_SFP+.htm

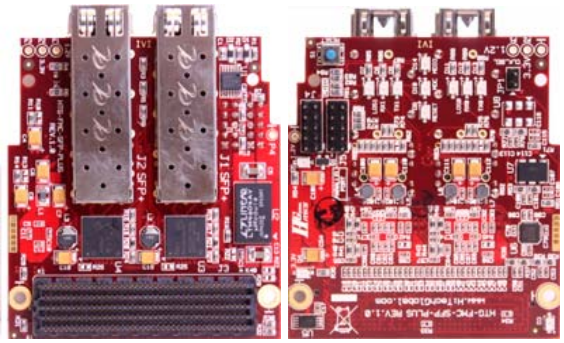

Image (5): Dual SFP+ FMC Module

3.2) Dual CX4

The dual CX4 FMC daughter card provides access to two CX4 ports (10Gbps) interfacing to total of 8 serial transceivers (XUAI).

More information is available at http://www.hitechglobal.com/FMCModules/FMC_Dual_CX4.htm

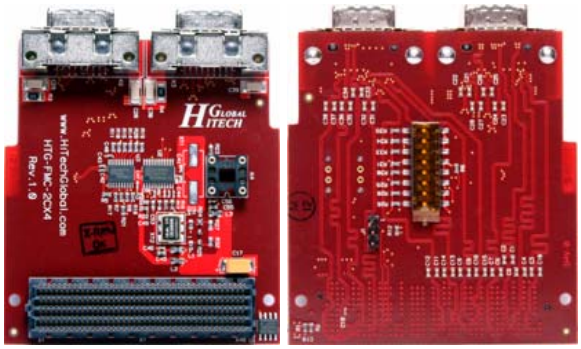

Image (6): Dual CX4 FMC Module

3.3) CX4/SATA/SMA Serial Connectivity

The Serial Connectivity FMC daughter card provides access to one CX4, two SATA, and two SMA ports (interfacing to total of 8 serial transceivers). Each port has its own on-board dedicated clock for maximum flexibility and ease of use.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_CX4-SMA-SATA.htm

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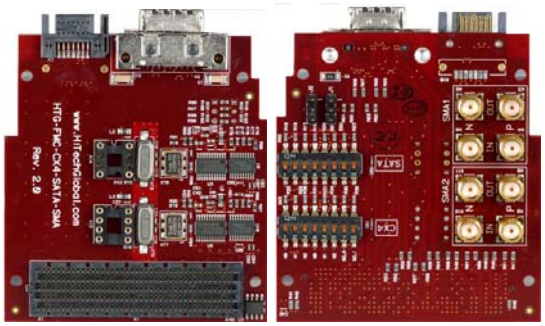

Image (7): Serial Connectivity FMC Module

3.4) PCI Express Root Complex

The PCI Express Root FMC daughter card provides access to 8 lanes of PCI Express Gen 1 and port. The module is supported by 100MHz and 250MHz low-jitter clocks.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_PCIExpress.htm

Image (8): PCI Express FMC Module

3.5) 8-Port SMA

The 8-Port SMA FMC daughter card provides access to 32 SMA connecters providing access to 8 Serial Transceivers. The module is supported by on-board and external clocks.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_SMA.htm

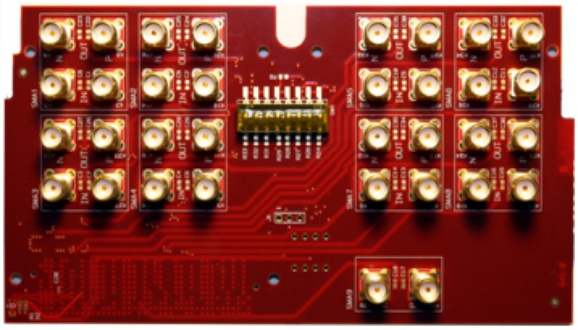

Image (9): 8-Port FMC Module

3.6) Quad SFP/SATA

The Quad SFP/SATA FMC daughter card provides access to four SFP and four SATA connectors. Each interface is supported by its own independent clock.

More information is available at http://www.hitechglobal.com/FMCModules/FMC_x4SFP_x4SATA.htm

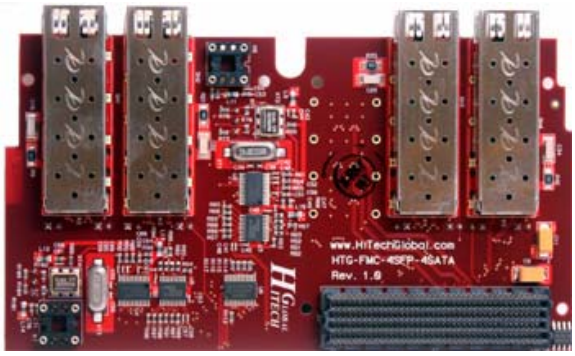

Image (10): Quad SFP/SATA FMC Module

3.7) 8-port SMA/LVDS

The FMC SMA/LVDSt (HTG-FMC-SMA-LVDS) is a single-size FPGA Mezzanine Connector (FMC) daughter card with support for 8 SMA ports through 32 SMA connectors and 33 pairs of LVDS signals through standard pin headers.

More information is available at http://hitechglobal.com/FMCModules/FMC_SMA_LVDS.htm

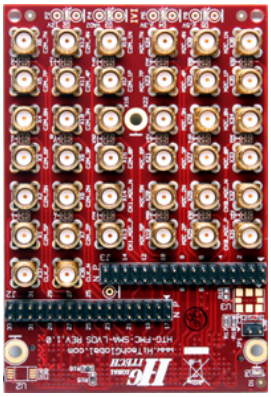

Image (11): 8-Port SMA/LVDS FMC Module

3.8) Quad SFP/SFP+

The Quad SFP/SFP+ FMC module is supported by four SFP/SFP+ ports and high-performance low-jitter Silicon Labs programmable clock (default = 156.25Mhz). The I2C interface between the oscillator and FPGA allows direct control of the SFP/SFP+ ports for wide range of different frequencies. The SFP/SFP+ ports are directly connected to four multi-gigabit serial transceivers of the FPGA carrier board.

More information is available at http://hitechglobal.com/FMCModules/FMC_4SFP+_Module.htm

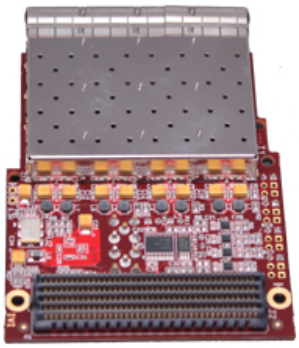

Image (12): Quad SFP/SFP+ FMC Module

3.9) QSFP/QSFP+/SFP/SFP+

The CPRI/OBSAI FMC module is supported by one QSFP+ and two SFP+ connectors. The required 122.88MHz and 153.60MHz crystal oscillators for CPRI/OBSAI standards are available on the module. Different gigabit standards can also be supported by changing crystal value (i.e. 10G and 40G Ethernet)

More information is available at http://hitechglobal.com/FMCModules/FMC_QSFP+.htm

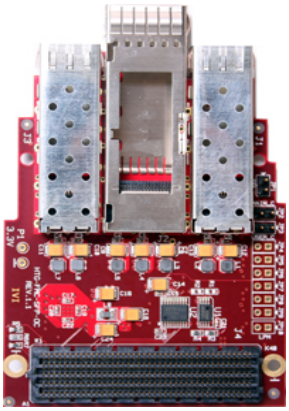

Image (13): QSFP/QSFP+/SFP/SFP+ FMC Module

3.10) Dual QSFP/QSFP+

The Dual QSFP/QSFP+ FMC module is supported by two QSFP/QSFP+ ports and high-performance low-jitter Silicon Labs programmable clock (default = 156.25Mhz). The I2C interface between the oscillator and FPGA allows direct control of the SFP/SFP+ ports for wide range of different frequencies. The QSFP/QSFP+ ports are directly connected to eight multi-gigabit serial transceivers of the FPGA carrier board.

Image (14): Dual QSFP/QSFP+ FMC Module

Technical Support:
Technical support can be provided by contacting support@HiTechGlobal.com Support requests are responded in less than 24 hours.

Sales Support:
Sales support can be provided by contacting info@HiTechGlobal.com or +1 408 781-7778 (8:00 AM – 6:00 PM Pacific Standard Time)