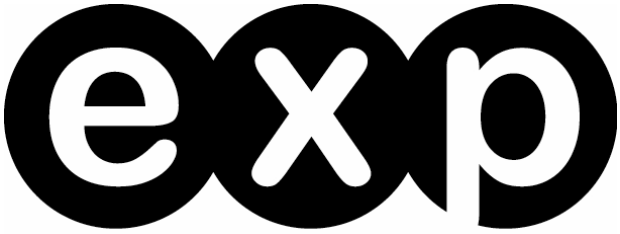

EXP Expansion Connector Specification

Revision 1.4
26 September 2007

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1 REVISION HISTORY

Revision	Date	Comment & Major Changes/Updates
0.1	7 November, 2005	Initial release of draft spec.
0.2	14 January, 2006	Removed 5V, minor signal naming changes
0.3	11 June, 2006	Major reformat of spec
1.0	15 June, 2006	Minor edits
1.1	17 July, 2006	Added MGT support to Differential pairs #20 and #21
1.2	1 November, 2006	Add length-matching requirements; Add clock capability to Diff pair #10; Modify Diff Clock inputs to be GCLK on FPGAs that don't support differential clock inputs
1.3	20 May, 2007	Updated Table 1 to remove pins 121-132, which do not exist but are actually GND blades. Corrected Figures 7, 9 and 10 for mounting hole position. Corrected Figures 9 and 10 for left card edge dimensions. Minor edits throughout document.
1.4	26 September, 2007	Updated Table 1 to note TX/RX pairing on pins 53, 54, 55, 56

2 INTRODUCTION

Today, FPGAs are being used in a wide range of applications, from high performance communication systems to high-volume, low-cost consumer electronics. To facilitate their use, designers are often turning to FPGA-based development boards as a way to verify and test prototype concepts. Having an easy way to connect to the user definable FPGA I/Os or interface application specific circuits to the FPGA pins is important. However, unlike processors and fixed ASSP devices, which typically conform to some fixed interface or bus standard, the FPGA interface is user defined and completely flexible. To take advantage of this flexibility, the EXP Expansion Connector Specification was developed.

This EXP Expansion Connector Specification defines the electrical and mechanical requirements for the baseboard connector and add-on daughter card. From the baseboard connectors, users can connect EXP compliant daughter cards or cables. This specification also defines the electrical and mechanical requirements for the add-on card. There are two types of add-on cards or modules; a Full EXP Module (typically referred to as an EXP Module) and a Half EXP Module.

While the EXP specification is FPGA-centric relative to the baseboard implementation, non-FPGA-based baseboards are not precluded as long as the basic conventions are followed.

2.1 EXP Specification Feedback

The EXP Expansion Connector Specification is an open standard, free of license fees or royalties. Avnet, Inc maintains the specification. All comments, suggestions, or recommendations can be submitted to technical.support@avnet.com.

The most current version of the EXP specification and listing of available EXP modules can be viewed at www.em.avnet.com/exp.

3 EXP SIGNALS

3.1 Overview

The EXP specification defines the signaling and physical placement of two mating connectors. One connector is located on a baseboard which usually contains the FPGA, and the second connector is located on an add-on card which usually plugs into the baseboard connector. Baseboards may contain multiple EXP connectors, and each connector must meet the mechanical specifications provided in this document to be EXP compliant.

There are two EXP connector formats:

Full EXP Slot – Specifies the configuration of two EXP connectors
Half EXP Slot – Specifies the configuration of one EXP connector

A baseboard may contain a Full, Half, or any combination of the two. By definition, a Full EXP Slot configuration will support a single Full EXP Module or two Half EXP Modules. However, two Half EXP Slot connectors may not necessarily support the Full specification if the mechanical requirements of the Full EXP specification are not met.

The following sections define the common features of the EXP specification. Sections 4 and 5 define the features specific to the baseboard and module formats.

3.2 EXP Connector

The EXP specification defines a 120-pin connector from Samtec (www.samtec.com). The baseboard connector is Samtec's Q Strip® QTE series and the module connector is Samtec's Q Strip® QSE series. Refer to the baseboard and module sections of this document for additional details on these connectors.

The EXP specification defines the connector pin usage as follows:

- Twenty-four (24) power pins
- Twelve (12) ground pins
- Twelve (12) ground blades
- Eighty-four (84) user signals

The EXP connector user signals are grouped in seven different categories based on FPGA pin assignments. These signal categories consist of:

1. Single-ended input/output signals
2. Differential input/output signals
3. Multi-gigabit serial I/O signals
4. Differential clock inputs
5. Single-ended clock inputs
6. Differential clock outputs
7. Single-ended clock outputs

User signals detailed in this specification shall adhere to the above definitions. However, in some cases, differential and multi-gigabit serial I/O signals may also be defined as two independent single-ended I/O signals. The EXP specification shall support the use of differential signals in the single-ended mode as long as the underlying FPGA is capable of supporting the single ended mode. Multi-gigabit serial I/O signals are special cases of the differential input/output signals and are not supported on all baseboards. For those baseboards that cannot support the multi-gigabit signals, those signal pairs default to standard differential signal type. In a similar manner, it may be possible to use the clock input and output signals as general-purpose user I/Os. Section 3.3 provides further detail on the connector signals.

The EXP specification defines dedicated power and ground pins. The twenty-four power pins are subdivided as follows:

- +3.3V - Twelve (12) pins (4000mA max)
- +2.5V - Twelve (12) pins (4000mA max)

The twelve ground pins and the twelve ground blades are connected to common ground. Figure 1 and Figure 2 depict the baseboard and module EXP connector types.

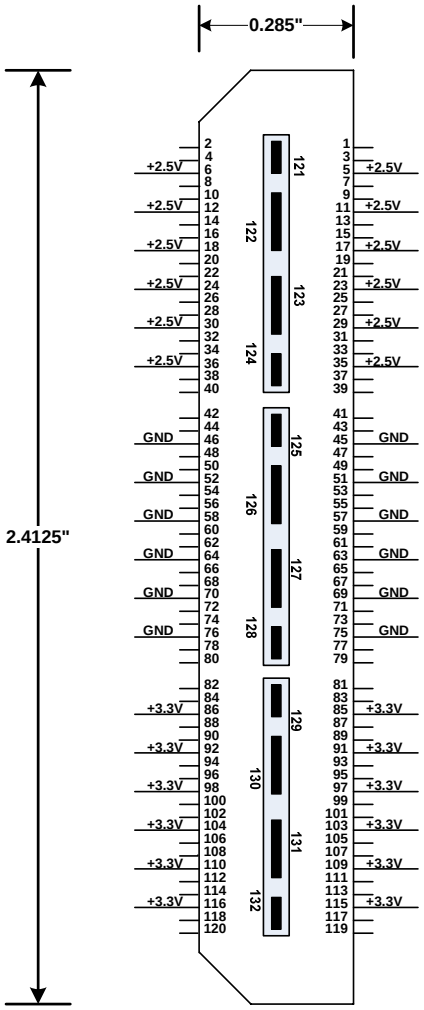


Figure 1 – Baseboard QTE Connector

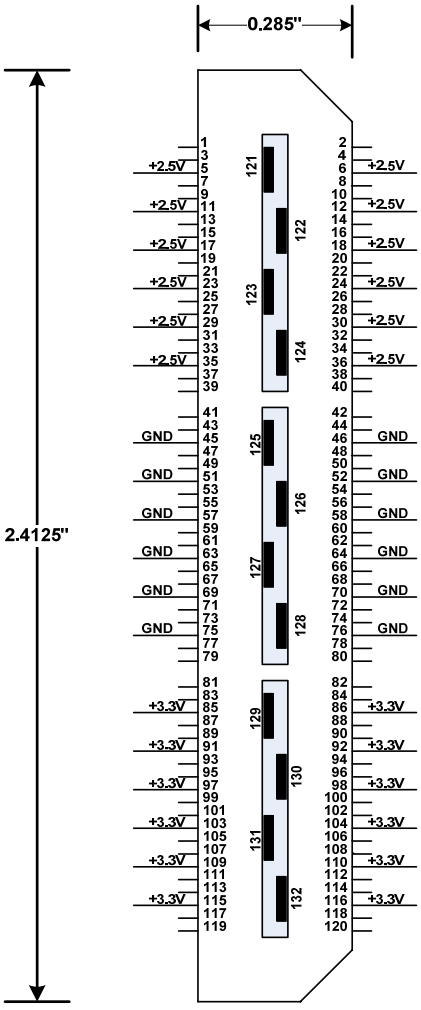


Figure 2 – Module QSE Connector

3.3 Connector Signal Definition

The baseboard and module EXP connector shall provide signals as shown in Table 1.

Table 1 – Baseboard and Module EXP Signal Definition

Signal Type	Signal Name	Pin #		Signal Name	Signal Type
Single-ended I/O	SE_IO_0	2	1	SE_IO_1	Single-ended I/O
Single-ended I/O	SE_IO_2	4	3	SE_IO_3	Single-ended I/O
Power	+2.5V	6	5	+2.5V	Power
Single-ended I/O	SE_IO_4	8	7	SE_IO_5	Single-ended I/O
Single-ended I/O	SE_IO_6	10	9	SE_IO_7	Single-ended I/O
Power	+2.5V	12	11	+2.5V	Power
Single-ended I/O	SE_IO_8	14	13	SE_IO_9	Single-ended I/O
Single-ended I/O	SE_IO_10	16	15	SE_IO_11	Single-ended I/O
Power	+2.5V	18	17	+2.5V	Power
Single-ended I/O	SE_IO_12	20	19	SE_IO_13	Single-ended I/O

Single-ended I/O	SE_IO_14	22	21	SE_IO_15	Single-ended I/O
Power	+2.5V	24	23	+2.5V	Power
Single-ended I/O	SE_IO_16	26	25	SE_IO_17	Single-ended I/O
Single-ended I/O	SE_IO_18	28	27	SE_IO_19	Single-ended I/O
Power	+2.5V	30	29	+2.5V	Power
Single-ended I/O	SE_IO_20	32	31	SE_IO_21	Single-ended I/O
Single-ended I/O	SE_IO_22	34	33	SE_IO_23	Single-ended I/O
Power	+2.5V	36	35	+2.5V	Power
Single-ended I/O	SE_IO_24	38	37	SE_IO_25	Single-ended I/O
Single-ended I/O	SE_IO_26	40	39	SE_IO_27	Single-ended I/O
Differential Clk Input (P)	DIFF_CLK_IN_p	42	41	SE_IO_28	Single-ended I/O
Differential Clk Input (N)	DIFF_CLK_IN_n	44	43	SE_CLK_IN	Single-ended Clk Input
Ground	GND	46	45	GND	Ground
Single-ended I/O	SE_IO_30	48	47	SE_IO_29	Single-ended I/O
Single-ended I/O	SE_IO_31	50	49	SE_CLK_OUT	Single-ended Clk Output
Ground	GND	52	51	GND	Ground
MGT/Differential I/O (P)	MGT_RX_DIFF_20_p	54	53	MGT_TX_DIFF_21_p	MGT/Differential I/O (P)
MGT/Differential I/O (N)	MGT_RX_DIFF_20_n	56	55	MGT_TX_DIFF_21_n	MGT/Differential I/O (N)
Ground	GND	58	57	GND	Ground
Differential I/O (P)	DIFF_18_p	60	59	SE_IO_32	Single-ended I/O
Differential I/O (N)	DIFF_18_n	62	61	SE_IO_33	Single-ended I/O
Ground	GND	64	63	GND	Ground
Differential I/O (P)	DIFF_16_p	66	65	DIFF_19_p	Differential I/O (P)
Differential I/O (N)	DIFF_16_n	68	67	DIFF_19_n	Differential I/O (N)
Ground	GND	70	69	GND	Ground
Differential Clk Out (P)	DIFF_CLK_OUT_p	72	71	DIFF_17_p	Differential I/O (P)
Differential Clk Out (N)	DIFF_CLK_OUT_n	74	73	DIFF_17_n	Differential I/O (N)
Ground	GND	76	75	GND	Ground
Differential I/O (P)	DIFF_14_p	78	77	DIFF_15_p	Differential I/O (P)
Differential I/O (N)	DIFF_14_n	80	79	DIFF_15_n	Differential I/O (N)
Differential I/O (P)	DIFF_12_p	82	81	DIFF_13_p	Differential I/O (P)
Differential I/O (N)	DIFF_12_n	84	83	DIFF_13_n	Differential I/O (N)
Power	+3.3V	86	85	+3.3V	Power
RCLK/Differential I/O (P)	RCLK_DIFF_10_p	88	87	DIFF_11_p	Differential I/O (P)
RCLK/Differential I/O(N)	RCLK_DIFF_10_n	90	89	DIFF_11_n	Differential I/O (N)
Power	+3.3V	92	91	+3.3V	Power
Differential I/O (P)	DIFF_8_p	94	93	DIFF_9_p	Differential I/O (P)
Differential I/O (N)	DIFF_8_n	96	95	DIFF_9_n	Differential I/O (N)
Power	+3.3V	98	97	+3.3V	Power
Differential I/O (P)	DIFF_6_p	100	99	DIFF_7_p	Differential I/O (P)
Differential I/O (N)	DIFF_6_n	102	101	DIFF_7_n	Differential I/O (N)
Power	+3.3V	104	103	+3.3V	Power
Differential I/O (P)	DIFF_4_p	106	105	DIFF_5_p	Differential I/O (P)
Differential I/O (N)	DIFF_4_n	108	107	DIFF_5_n	Differential I/O (N)
Power	+3.3V	110	109	+3.3V	Power
Differential I/O (P)	DIFF_2_p	112	111	DIFF_3_p	Differential I/O (P)
Differential I/O (N)	DIFF_2_n	114	113	DIFF_3_n	Differential I/O (N)
Power	+3.3V	116	115	+3.3V	Power
Differential I/O (P)	DIFF_0_p	118	117	DIFF_1_p	Differential I/O (P)
Differential I/O (N)	DIFF_0_n	120	119	DIFF_1_n	Differential I/O (N)

*GND is also connected to blade connections (121-132) along the middle strip of the connector

3.3.1 Power Signals

The EXP connector contains twenty-four (24) power pins. Twelve (12) pins supply 2.5 V at 333 mA maximum per pin (4 A total), and twelve (12) pins supply 3.3 V at 333 mA maximum per pin (4 A total). The total current rating for each of the 2.5 V and 3.3 V supplies is dependent on the baseboard power supply capabilities. Not all baseboards may be able to supply the full current rating.

3.3.2 User Signals

There are six types of user signals available on the EXP connector as described in section 3.2. On the baseboard EXP connector, the user signals are connected directly to the FPGA. Since the FPGA can support several possible voltage levels and I/O standard types, the EXP specification defines a minimum requirement, but does not limit additional capabilities that some FPGAs and baseboards may provide. Some baseboards may have limitations or constraints on voltage settings, clocking, or I/O standards. A typical baseboard shall provide user settable jumpers to select the I/O voltage standard for the corresponding FPGA I/O banks. As a recommended guideline, the following voltage banking options for the EXP user signals shall be attempted:

1) Minimum Requirement: Single-ended and differential I/Os group selectable for either 2.5 V or 3.3 V
2) Two Bank Option: Bank 1 - Single-ended I/O selectable for 2.5/3.3 V. Bank 2 – Differential I/O selectable for 2.5/3.3 V.

Trace length requirements for the various user signals are:

- Single-ended signals on one EXP connector length-matched to each other: +/- 1000 mils
- Differential pairs length-matched within each pair: +/- 25 mils
- Differential pairs on one EXP connector length-matched to each other: +/- 500 mils
- All signals on both EXP connectors length-matched to each other: +/- 3000 mils

The following sections provide details of the user signals.

3.3.2.1 Single-Ended Input and Output Signals

Single-ended input and output signals shall support signal frequencies up to the maximum limit of the FPGA I/O, or 200 MHz, whichever is lower. Proper signal routing and PCB layout practices should be followed to optimize signal integrity. Higher switching frequencies may be attained, but are not guaranteed by the specification. Performance is measured at the connector pins.

Single-ended input and output signals shall support 2.5 V or 3.3 V signal levels.

Single-ended input and output signals may specify individual voltage settings for all single-ended signals or a sub-set of single-ended signals. Voltage grouping is a function of the baseboard implementation, and not guaranteed. As a minimum, all single-ended signals shall be settable to either 2.5 or 3.3 V as a single group.

Single-ended input and output signals shall meet the I/O standards supported by the baseboard FPGA.

3.3.2.2 Single-Ended Clock Output Signals

Single-ended clock output signals shall support signal frequencies up to the maximum limit of the FPGA I/O, or 200 MHz, whichever is lower. Proper signal routing and PCB layout practices should be followed to optimize signal integrity. Higher switching frequencies may be attained, but are not guaranteed by the specification. Performance is measured at the connector pins.

Single-ended clock output signals shall support 2.5 V or 3.3 V signal levels.

Single-ended clock output signals may be tied to the voltage setting level of the other single-ended signals.

Single-ended clock output signals may be independently set, depending on the baseboard implementation.

Single-ended clock output signals may be used as general single-ended input/output.

3.3.2.3 Single-Ended Clock Input Signals

Single-ended clock input signals shall support signal frequencies up to the maximum limit of the FPGA I/O, or 200 MHz, whichever is lower. Proper signal routing and PCB layout practices should be followed to optimize signal integrity. Higher switching frequencies may be attained, but are not guaranteed by the specification. Performance is measured at the connector pins.

Single-ended clock inputs shall connect to global clock input pins on the baseboard FPGA.

Single-ended clock input signals shall support 2.5 V or 3.3 V signal levels.

Single-ended clock inputs may be tied to the voltage setting level of the other single-ended signals.

Single-ended clock input standards may be independently set, depending on the baseboard implementation.

Single-ended clock inputs may be used as general single-ended inputs or outputs, depending on the capability of the baseboard FPGA. Some FPGA clock inputs can only be used as user inputs and not outputs. Always refer to the baseboard FPGA data sheet for possible limitations on these signal types.

3.3.2.4 Differential Input and Output Signals

Differential input and output signal pairs shall support signal frequencies up to the maximum limit of the FPGA I/O, or 750 MHz, whichever is lower. Proper signal routing and PCB layout practices should be followed to optimize signal integrity. Higher switching frequencies may be attained, but are not guaranteed by the specification. Performance is measured at the connector pins.

Differential input and output signals shall support 2.5 V signal levels.

Differential input and output signals may be tied to the same voltage setting as the single-ended signals.

Differential input and output signals may be used as single-ended input/output.

Differential input and output signals may support 3.3 V levels if used as single-ended signals.

Differential input and output signals shall meet the I/O standards supported by the baseboard FPGA.

For baseboard FPGAs that have clock-capable pins, DIFF_10_p/n is defined as a regional clock (RCLK) input. For those boards without clock-capable pins, these pins are standard Diff I/O.

3.3.2.5 Differential Clock Input Signals

Differential clock input signal pairs shall support signal frequencies up to the maximum limit of the FPGA I/O, or 750 MHz, whichever is lower. Proper signal routing and PCB layout practices should be followed to optimize signal integrity. Higher switching frequencies may be attained, but are not guaranteed by the specification. Performance is measured at the connector pins.

Differential clock input signals shall support 2.5 V signal levels.

Differential clock input signals may be used as general differential inputs.

Differential clock input signals may be tied to the same voltage setting as the single-ended signals.

The (P) side of the differential clock input signal may be used as a single-ended clock input signal.

The differential clock input signals may be used as general single-ended input.

Differential clock input signals may support 3.3 V levels if used as general single-ended inputs.

For baseboard FPGAs that do not support differential clocking but do support global clock (GCLK) capable pins, these differential signals shall connect to the FPGA GCLK-pins making them capable of being either a differential I/O pair or two single-ended clock inputs. If the FPGA does not support or have GCLK-capable pins available, then these signals shall be defined as Differential Inputs and Outputs per section 3.3.2.4.

3.3.2.6 Differential clock outputs

Differential clock output signal pairs shall support signal frequencies up to the maximum limit of the FPGA I/O, or 750 MHz, whichever is lower. Proper signal routing and PCB layout practices should be followed to optimize signal integrity. Higher switching frequencies may be attained, but are not guaranteed by the specification. Performance is measured at the connector pins.

Differential clock output signals shall support 2.5 V signal levels.

Differential clock output signals may be used as general differential input/output.

Differential clock output signals may be tied to the same voltage setting as the single-ended signals.

Differential clock output signals may be used as single-ended clock output signals.

The differential clock output signals may be used as general single-ended input/output.

Differential clock output signals may support 3.3 V levels if used as general single-ended input/output.

For baseboard FPGAs that do not support differential clocking, these signals shall be defined as Differential Inputs and Outputs per section 3.3.2.4.

3.3.2.7 Multi-gigabit Serial Input and Output Signals

Multi-gigabit serial input and output signal pairs shall support serial data rates up to 3.125 Gbps. Performance is measured at the connector pins.

Multi-gigabit serial input and output signals shall support 2.5 V signal levels.

If a baseboard does not support Multi-gigabit signals, then the multi-gigabit serial input/output signal type shall default to the differential input and output signal type.

3.4 EXP Connector Mechanical Specifications

The mechanical specifications for Samtec's Q Strip® QTE and QSE Series EXP connectors are available from Samtec (www.samtec.com).

4 EXP BASEBOARD REQUIREMENTS

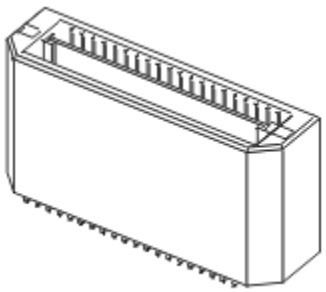
4.1 Overview

The EXP specification defines a connector configuration for both a baseboard and daughter card. This section shall provide the mechanical requirements for the baseboard connector.

4.2 Connectors

The EXP specification defines a 120-pin QTE Series connector from Samtec (www.samtec.com). The connector on the baseboard is a variable height (5 mm to 25 mm high (with QSE mated connector)), plug style connector with a part number **QTE-060- XX-F-D-A**. The "XX" denotes the connector height options (01, 02, 03, 04, 05, and 07), which is user-specified depending on the height of components underneath the area of the added plug-on EXP module. Tyco/AMP is a second source for this connector (Part number **1658055-2**).

Figure 3 shows an example of Samtec's Q Strip® QTE Series connector with the "XX" lead style height options.



QTE LEAD STYLE	A	HEIGHT WITH QSE
–01	(4,27) .168	(5,00) .198
–02	(7,26) .286	(8,00) .316
–03	(10,27) .404	(11,00) .433
–04	(15,25) .600	(16,00) .630
–05	(18,24) .718	(19,00) .748
–07	(24,24) .954	(25,00) .984

Figure 3 – Samtec's Q Strip QTE Series Connector

4.3 Baseboard Electrical Characteristics

A baseboard supporting the EXP specification shall meet the EXP electrical requirements detailed in section 3 of this document.

4.4 Baseboard Mechanical Characteristics

A baseboard that is EXP compatible shall be able to support the addition of Full EXP Modules, Half EXP Modules, or a combination of the two. An example baseboard configuration showing the support of a single Half EXP Module is shown in Figure 4. This figure shows two EXP connectors on the baseboard, but only one connector is required to support the Half EXP Module.

Figure 5 shows a baseboard configuration that supports two Half EXP Modules. In this configuration, each EXP connector supports its own Half EXP Module, independent of the other

connector. The relative placement of the second (and additional) EXP connector is not important for the support of Half Modules, but is critical if the connectors are to support a Full Module.

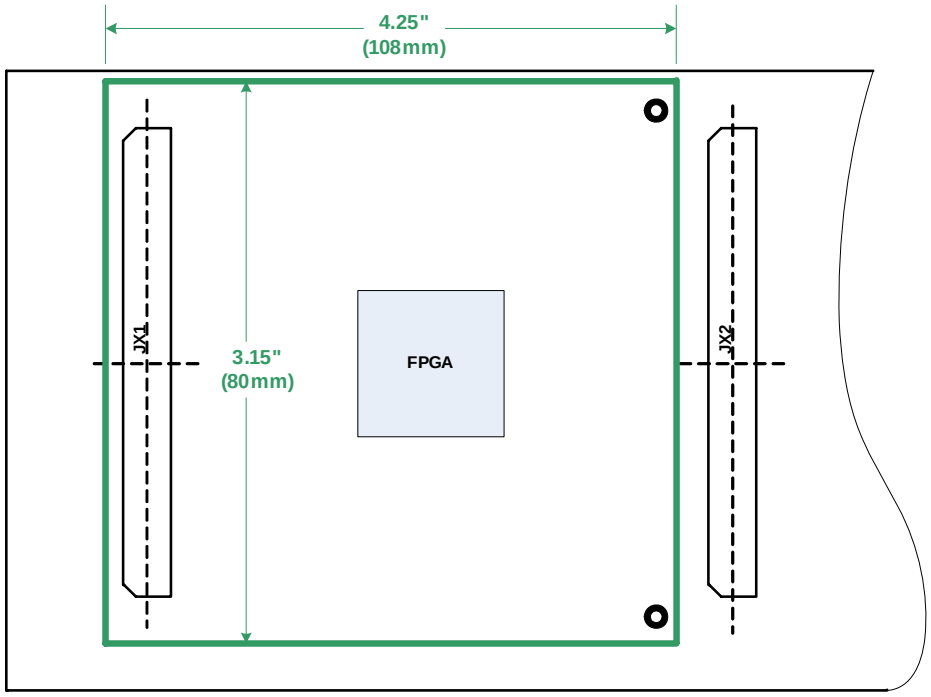


Figure 4 – Baseboard Supporting One Half EXP Module

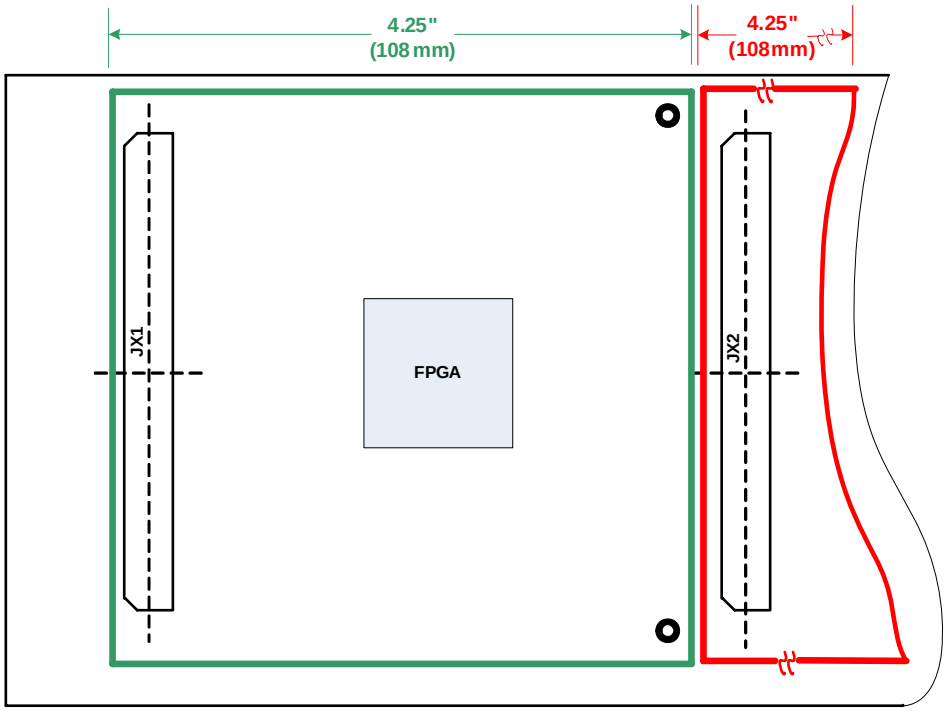


Figure 5 – Baseboard Supporting Two Half EXP Modules

Baseboards capable of supporting a Full EXP Module must contain a minimum of two EXP connectors, meeting specific physical layout constraints. Figure 6 shows an example baseboard supporting a Full EXP Module.

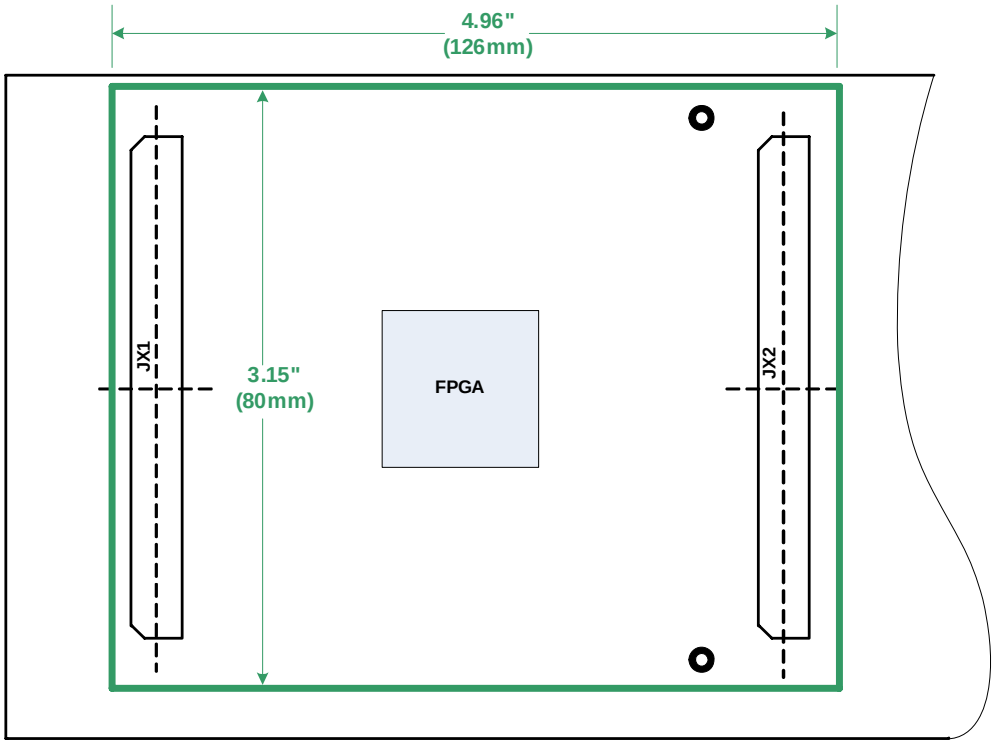


Figure 6 – Example Baseboard Supporting a Full EXP Module

Figure 7 shows the physical layout constraints that the baseboard shall meet to support Full and Half EXP Modules. Dimensions shown relative to the edge of the baseboard are reference examples and not constrained by the EXP specification.

The two connectors, JX1 and JX2 may receive a single daughter card or two separate daughter cards. Referring to connectors JX1 and JX2 on Figure 7, the center-to center spacing is 110mm (4.33”). Center-to-center spacing of JX1 to its mounting holes is 95mm (3.74”). Mounting holes for the JX2 connector are not shown on Figure 7 but they bear the same relationship as to JX1 (e.g., the center of JX2’s mounting holes are 95mm to the right of the JX2 centerline (if the baseboard is long enough to accommodate them).

The FPGA depicted in Figure 7 is shown only to illustrate that the normal “baseboard” configuration would place the FPGA between the JX1 and JX2 connectors. Actual placement may see the FPGA closer to one or the other connector. Consequently, signal routing (single-

ended and differential), while length-matched between the FPGA to JX1 and JX2, may not be the same length at both connectors.

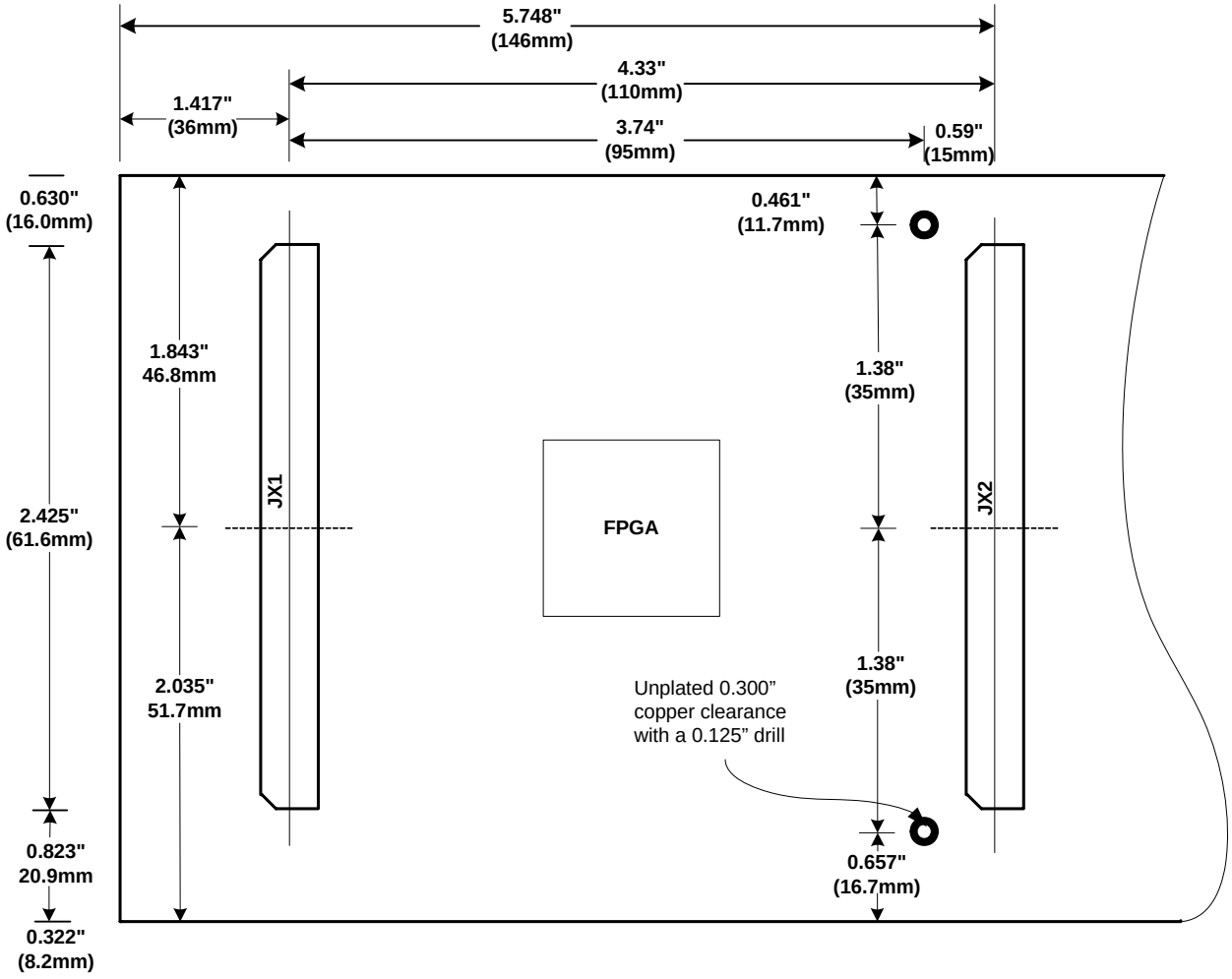


Figure 7 – Example Baseboard Physical Layout Constraints

5 EXP MODULE REQUIREMENTS

5.1 Overview

The EXP specification defines two EXP module types; a Full EXP Module (typically referred to as a Module), and a Half EXP Module. This section shall provide the electrical and mechanical requirements for the Full and Half Modules.

5.2 Connectors

The EXP specification defines a 120-pin QSE Series connector from Samtec (www.samtec.com). The connector on the module is a fixed height (3.25 mm umated, 5 mm mated), receptacle style connector with a part number **QSE-060-01-F-D-A**. Tyco/AMP is a second source for this connector (Part Number **1658052-2**).

Figure 8 shows Samtec's Q Strip® QSE Series connector.

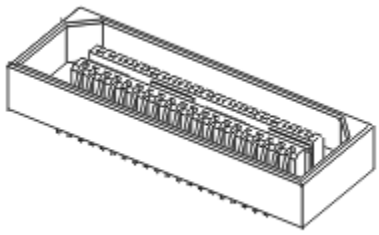


Figure 8 – QSE receptacle for the EXP Module

The Full EXP Module specifies two EXP connectors per module. The Half EXP Module specifies a single EXP connector per module. For the Full EXP Module, each connector is electrically identical, differing only in the connection to the respective baseboard FPGA I/O pins.

5.3 Module Electrical Characteristics

A module supporting the EXP specification shall meet the EXP electrical requirements detailed in section 3 of this document.

5.4 Module Mechanical Definition

5.4.1 Half EXP Modules

Half EXP Modules shall meet the physical dimensions of 108 mm x 80 mm. Half Module cards intended to plug into a single EXP connector must limit their right-most excursion to no more than 5 mm (0.197") to the right of the mounting hole center-line. Left-most excursion of the Half Module must be limited to no more than 5 mm (0.197") to the left of the EXP connector center-line. These requirements must be met to ensure that two Half EXP Module cards can be plugged onto a baseboard supporting a two connector, Full EXP Module configuration. The 80

mm module width (top to bottom) is a guaranteed size dimension for compatibility with all baseboards. Modules that exceed this size cannot be guaranteed to meet the height clearance of all baseboards.

Figure 9 shows the Half EXP Module mechanical specifications.

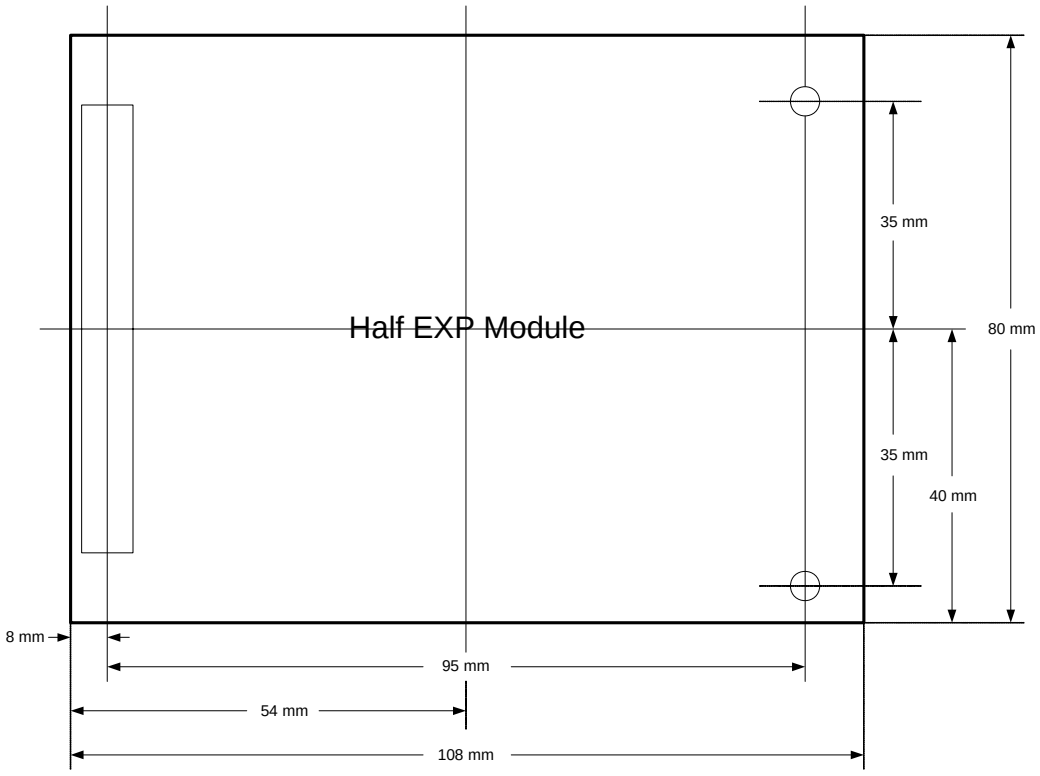


Figure 9 – Half EXP Module Mechanical Specifications

5.4.2 Full EXP Module

Full EXP Modules shall meet the physical dimensions of 126 mm x 80 mm. The 80 mm module width (top to bottom) is a guaranteed size dimension for compatibility with all baseboards. Modules that exceed this size cannot be guaranteed to meet the height clearance of all baseboards. Figure 10 shows the Full EXP Module mechanical specifications.

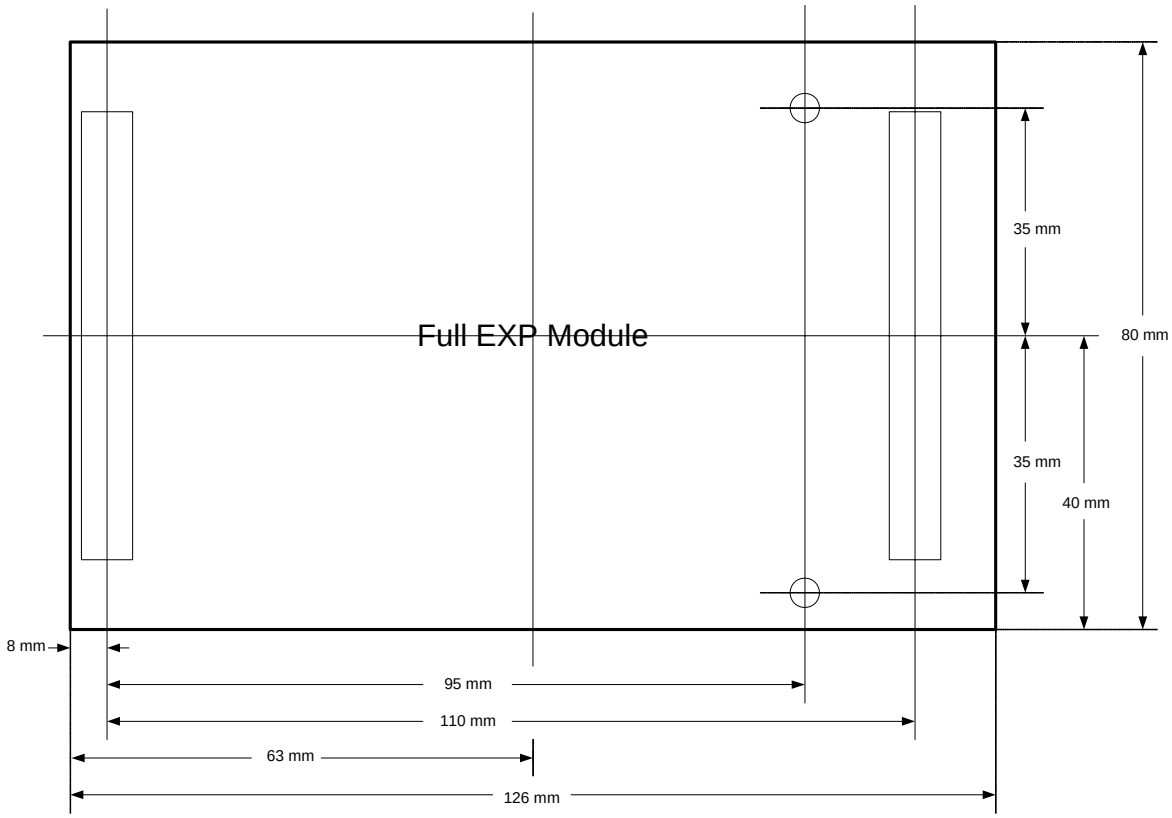


Figure 10 – Full EXP Module Mechanical Specifications

6 EXP CABLE ASSEMBLIES

The EXP specification shall allow cable assemblies to mate to the EXP connectors contained on the baseboard and the modules. These cables shall allow connection of external circuit cards to the FPGA I/O signals, or the remote connection of an EXP Module to the baseboard. Samtec provides a Data Rate EQCD micro coax high speed cable assemblies that will mate with either the Baseboard Samtec Q Strip® QTE Series connectors or the Module Samtec Q Strip ® QSE Series connectors. Cable assemblies can be ordered with QTE-to-QTE style ends, QSE-to-QSE style ends, or QTE-to-QSE style ends. Figure 11 shows an example of a QTE-to-QSE style cable. Refer to Samtec (www.samtec.com) for additional information on these Data Rate high speed cable assemblies.

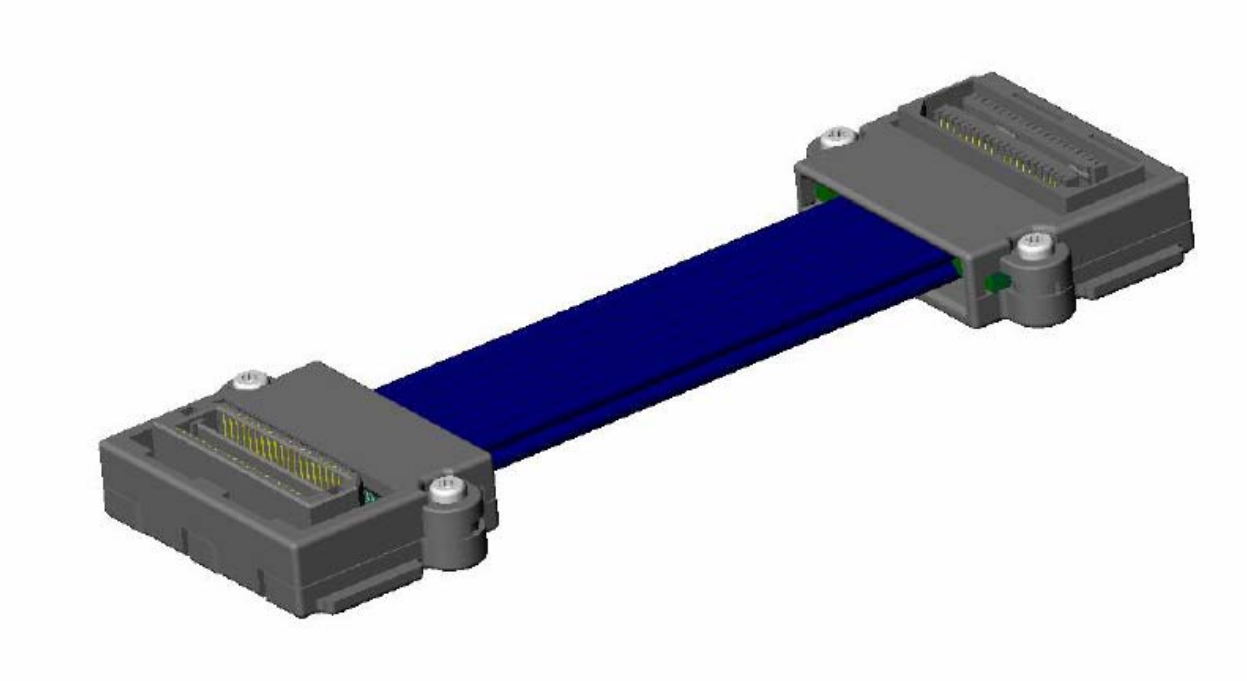


Figure 11 – EXP Cable Assembly Example