All nets ending in _P or _N are differential pairs;
from what I can tell, the H* stuff is meant for
higher-speed; the L* stuff can be used differentially
or single-ended. I have routed everything differentially,
so, for single-ended use, you would tie the _N line to GND.

I managed to balance all of the differential pairs
to 3.3" (3300mil) to a tolerance of 25mil
so you can run you busses however you need
to without the adapter adding time skew.
This tolerance is based on the DDR2 spec.

Bypass capacitors at ingress and
egress of each power rail. Probably
overkill, but my though is to avoid
coupling in noise from the environment,
bugs in the board, or between the devices.

EXP2_HDQ

The +3v3 rail is present on both EXT connectors and
the FMC connector. I have tied them all together and added
bypass capacitance in strategic places.

+3V3

3P3V_1 3P3V_2 3P3V_3 3P3V_4

+2V5 +3V3

VCC_3P3V

VCC_2P5V

EXP1_HDP

Values are nominal; board sized for 0805 SMD.
3v3 bypass at: EXT1/EXT2 termination,
FMC termination, and off-board connection.

+3V3

C5 10u C6 10n C7 10u C8 10n C1 10u C2 10n C3 10u C4 10n

GND GND GND GND GND

2v5 bypass at EXT1/EXT2 termination

+2V5

C9 10u C10 10n C11 10u C12 10n

GND

JA1

LA21_LA29

LA00_LA20

LA00_LA20

LA21_LA29

GND

GND

GND

3.2mm mounting holes, tied to ground plane.

H1 MOUNT-PAD-ROUND3.2

H2 MOUNT-PAD-ROUND3.2

H3 MOUNT-PAD-ROUND3.2

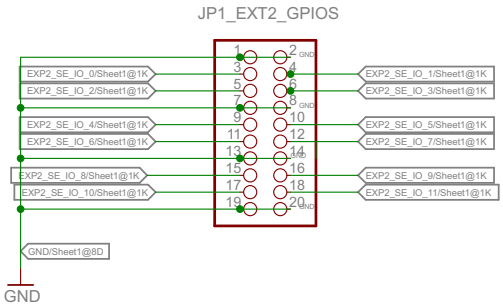
Remaining, non-differential IOs on the EXT sockets
are brought out to 0.1" pin headers for use as GPIOs.

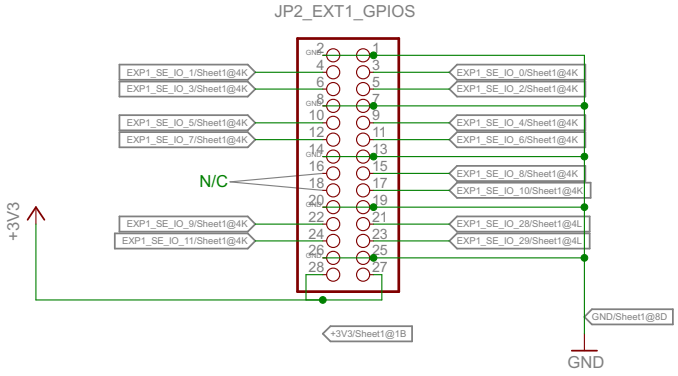
I couldn't find any more useful pins on the FMC that Xilinx
typically ties into... and I'm not sure I can get much more on
board without adding another layer.

Although they are not specifically rated for differential
use, I routed the GPIOs differentially based on the adjacent
pinouts on the EXT2 connectors and with ground guards at
the 0.1" connectors.

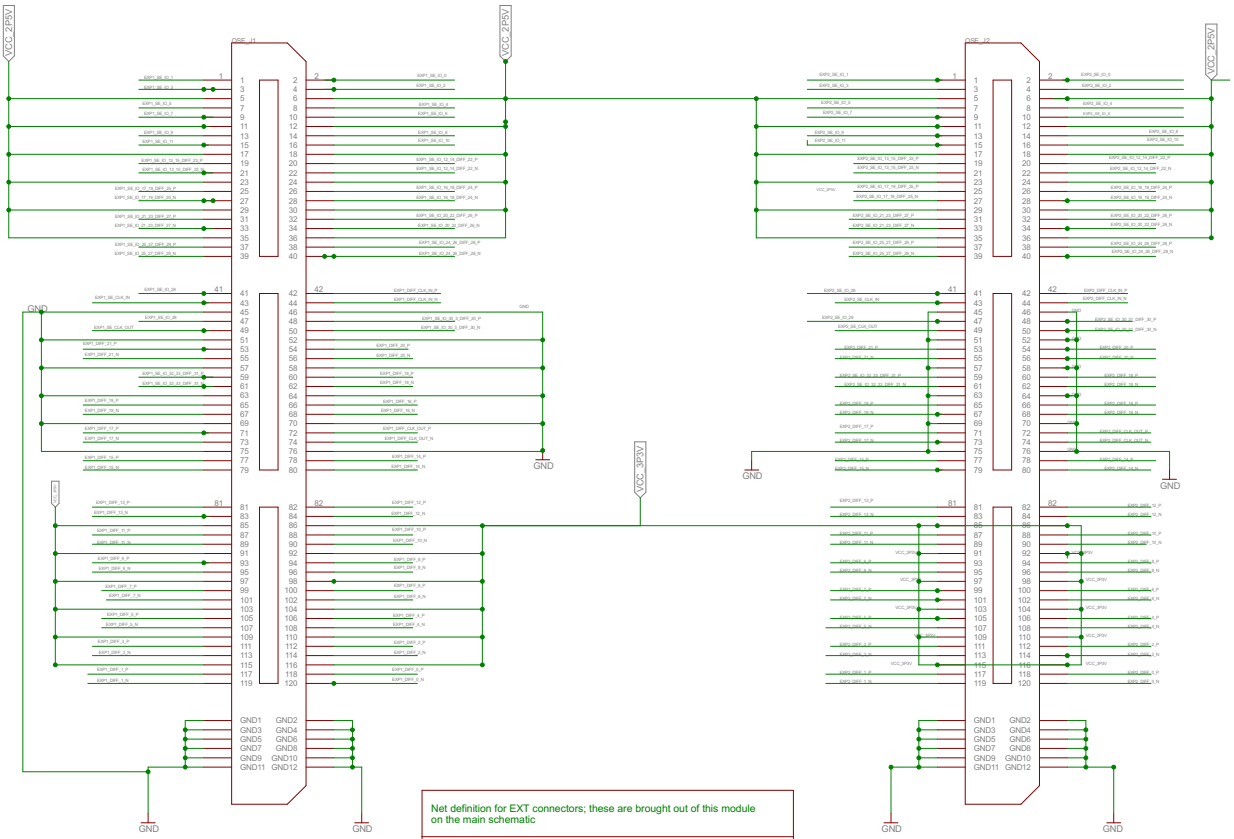
Connections between EXT1 and EXT2 QST connectors and FMC connector.
Also present are two 100mil headers bringing out the remaining
GPIOs from the EXT connectors.

TITLE: 20150104_QSE_to_FMC_6Layer_R3.1	
Document Number:	REV:
Date: 1/4/2015 7:42:13 PM	Sheet: 1/2





Auxiliary connections for GPIOs		
TITLE: 20150104_QSE_to_FMC_6Layer_R3.1		
Document Number:		REV:
Date: 1/4/2015 7:42:13 PM	Sheet: 2/2	

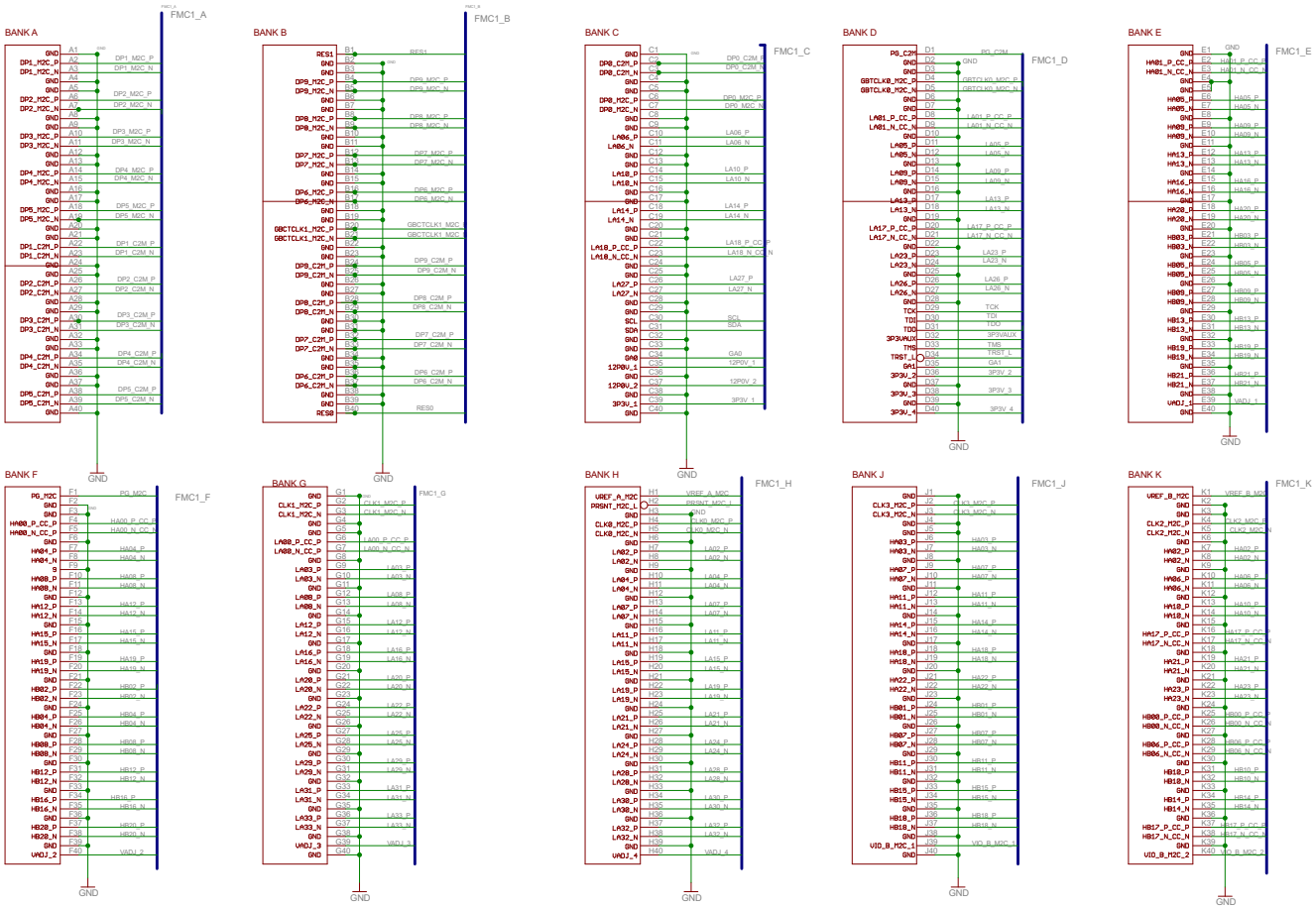


Net definition for EXT connectors; these are brought out of this module on the main schematic

TITLE: 20150104_QSE_to_FMC_6Layer_R3.1	
Document Number:	REV:
Date: 1/4/2015 7:42:13 PM	Sheet: 1/1

These pinouts are based on my inspection of several Xilinx board schematics. The actual FMC connector specification is not publicly-available. I have specifically not used certain nets, such as DP* because Xilinx does not seem to use them (these are meant for AC-coupled applications, anyhow).

FMC1



Netouts for FMC connector

TITLE: 20150104_QSE_to_FMC_6Layer_R3.1

REV:

Document Number:

Sheet: 1/1

Date: 1/4/2015 7:42:13 PM