

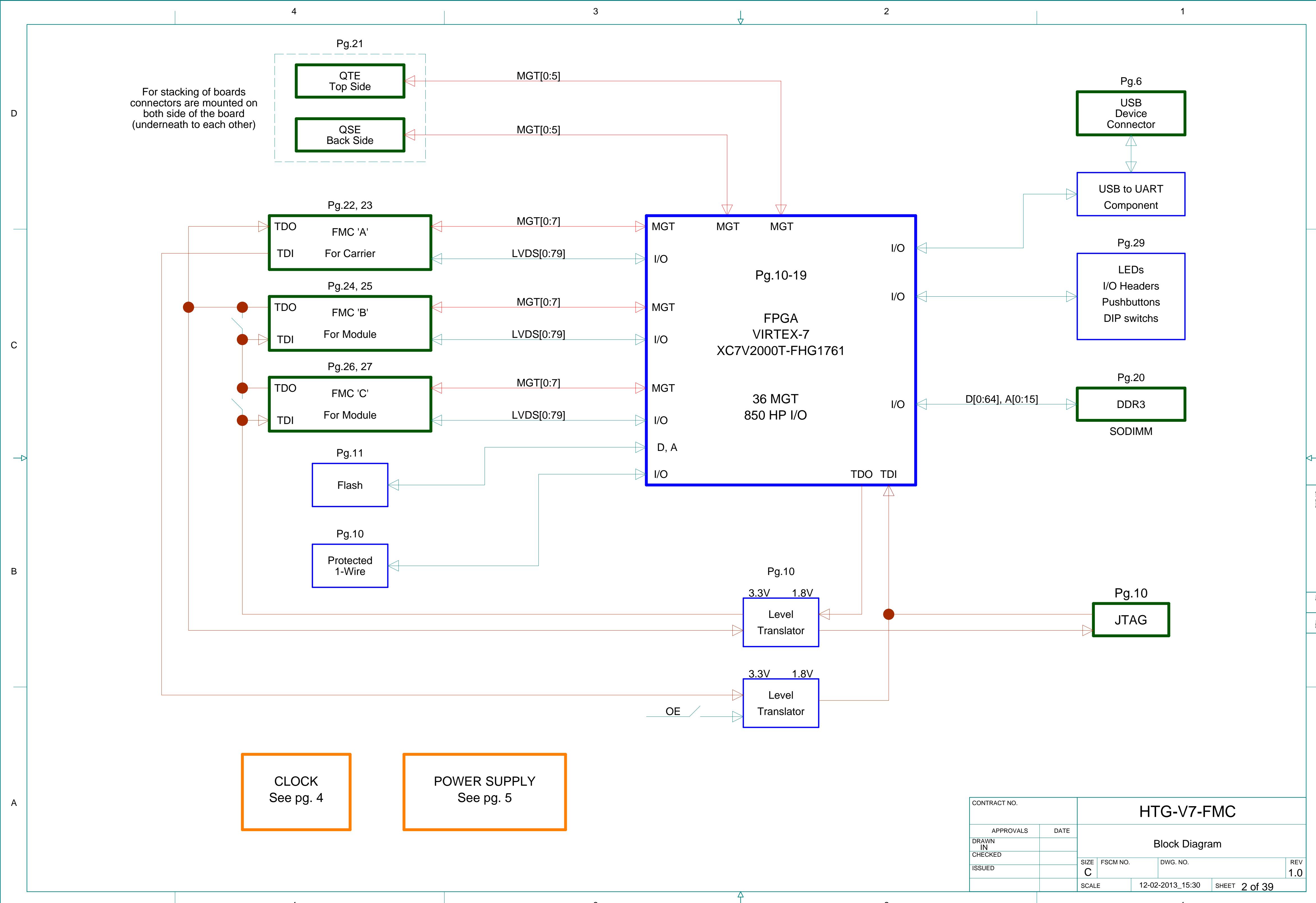
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FINAL VERSION REV. 1.0

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CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	Note Page		
DRAWN IN CHECKED	ISSUED			
SIZE	FSCM NO.	DWG. NO.	REV 1.0	
C			SCALE	06-03-2013_15:59
			SHEET	1 of 39



D

D

C

C

→

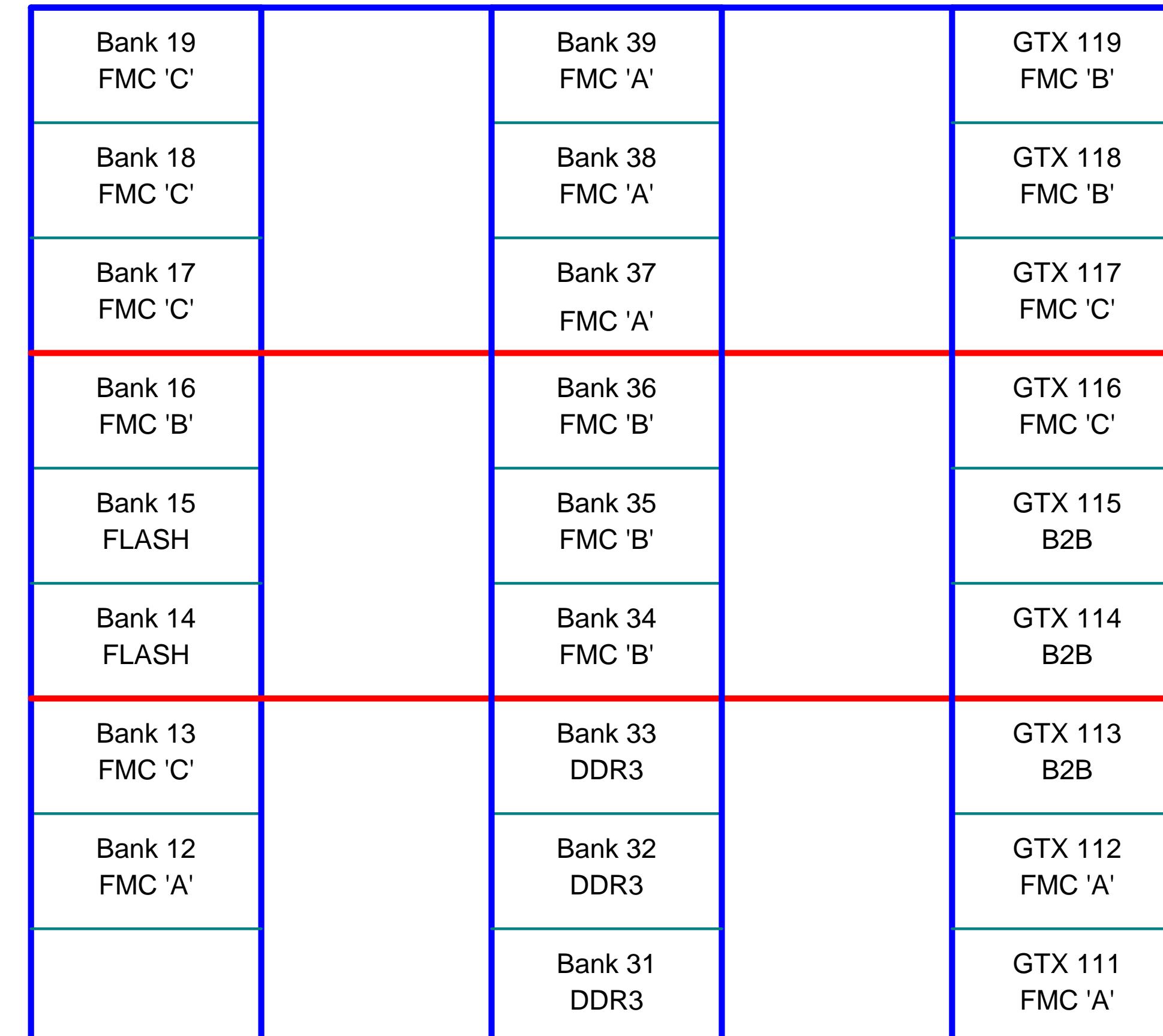
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B

B

A

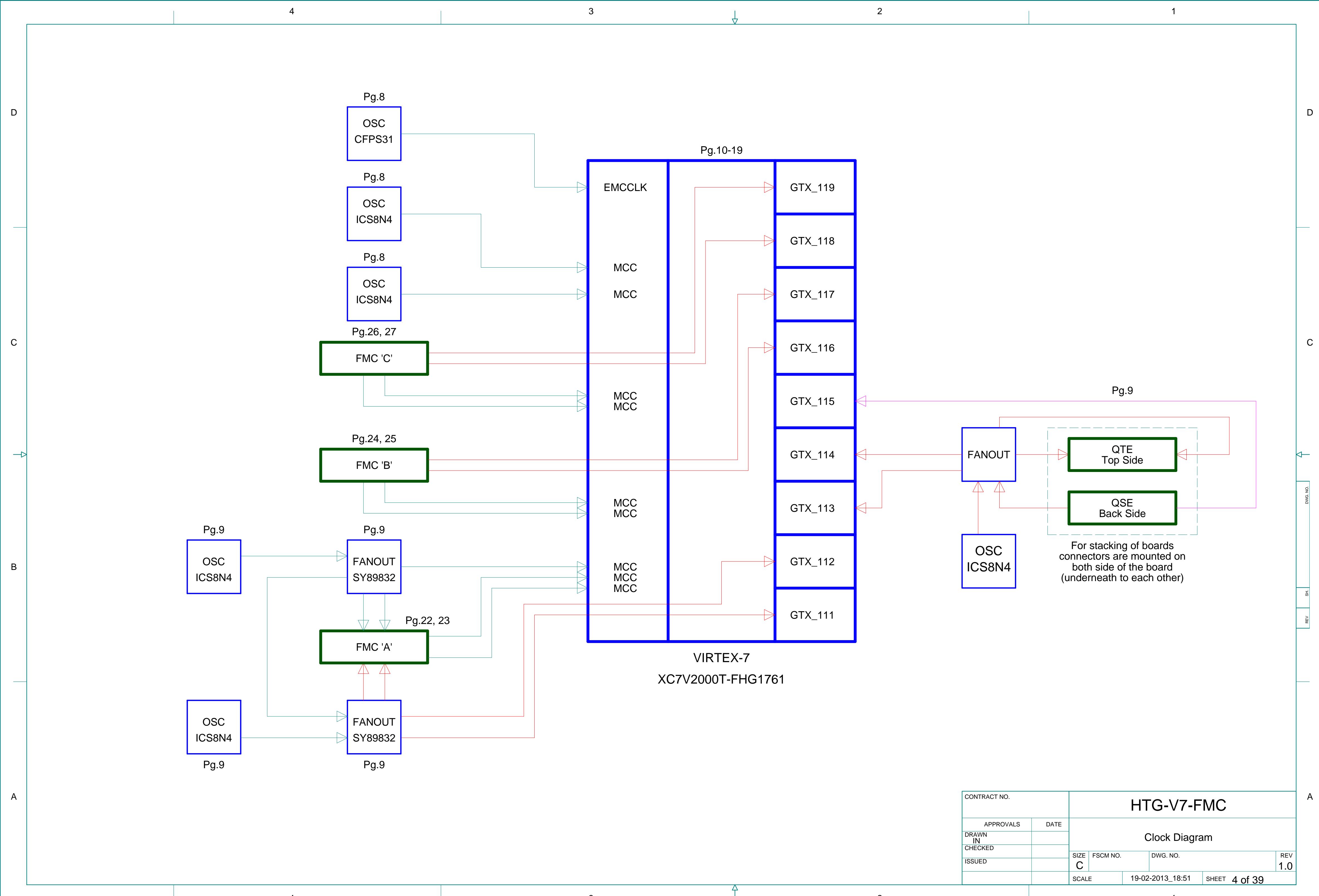
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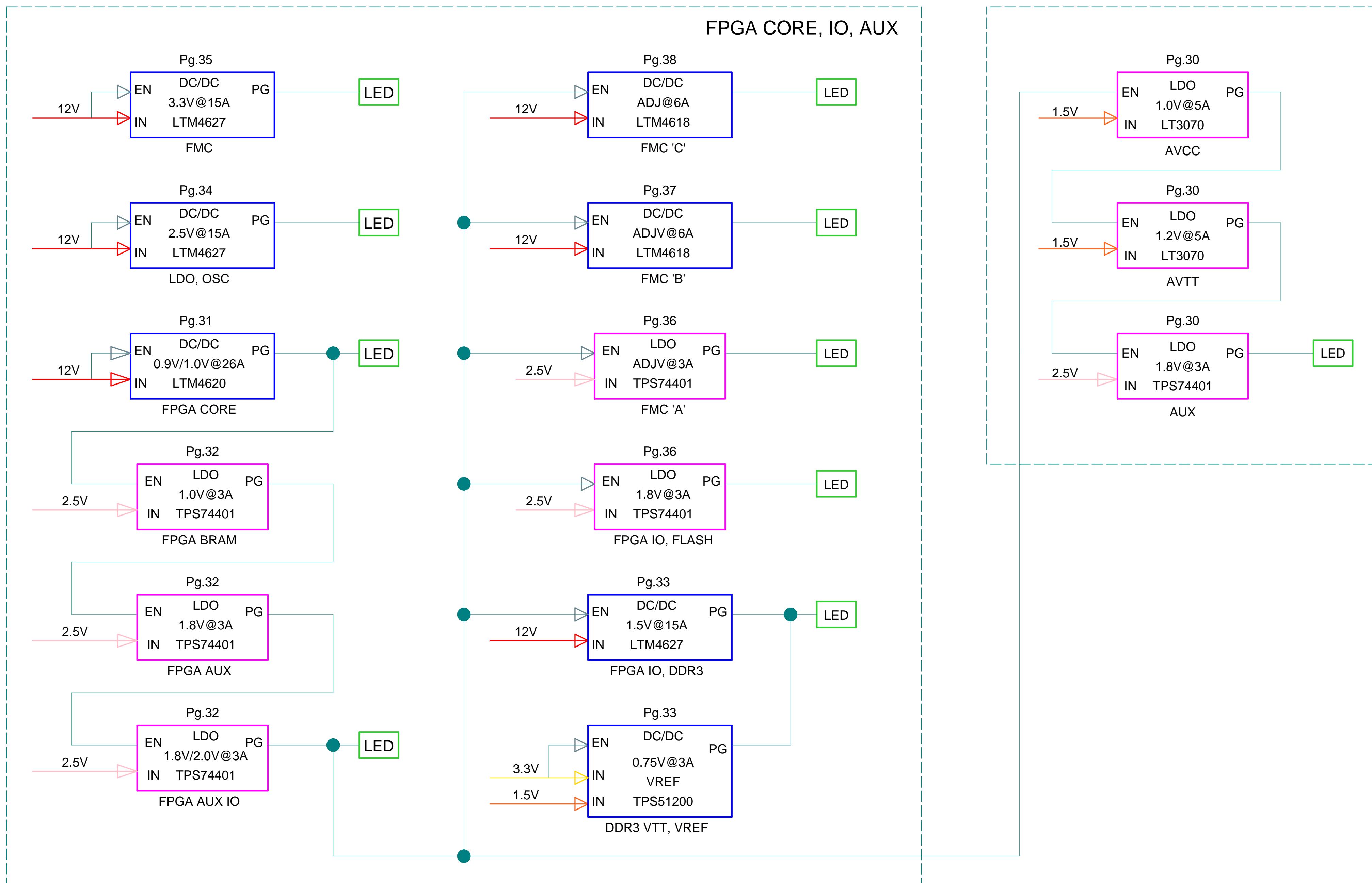


## DIE VIEW

XC7V2000T-FHG1761

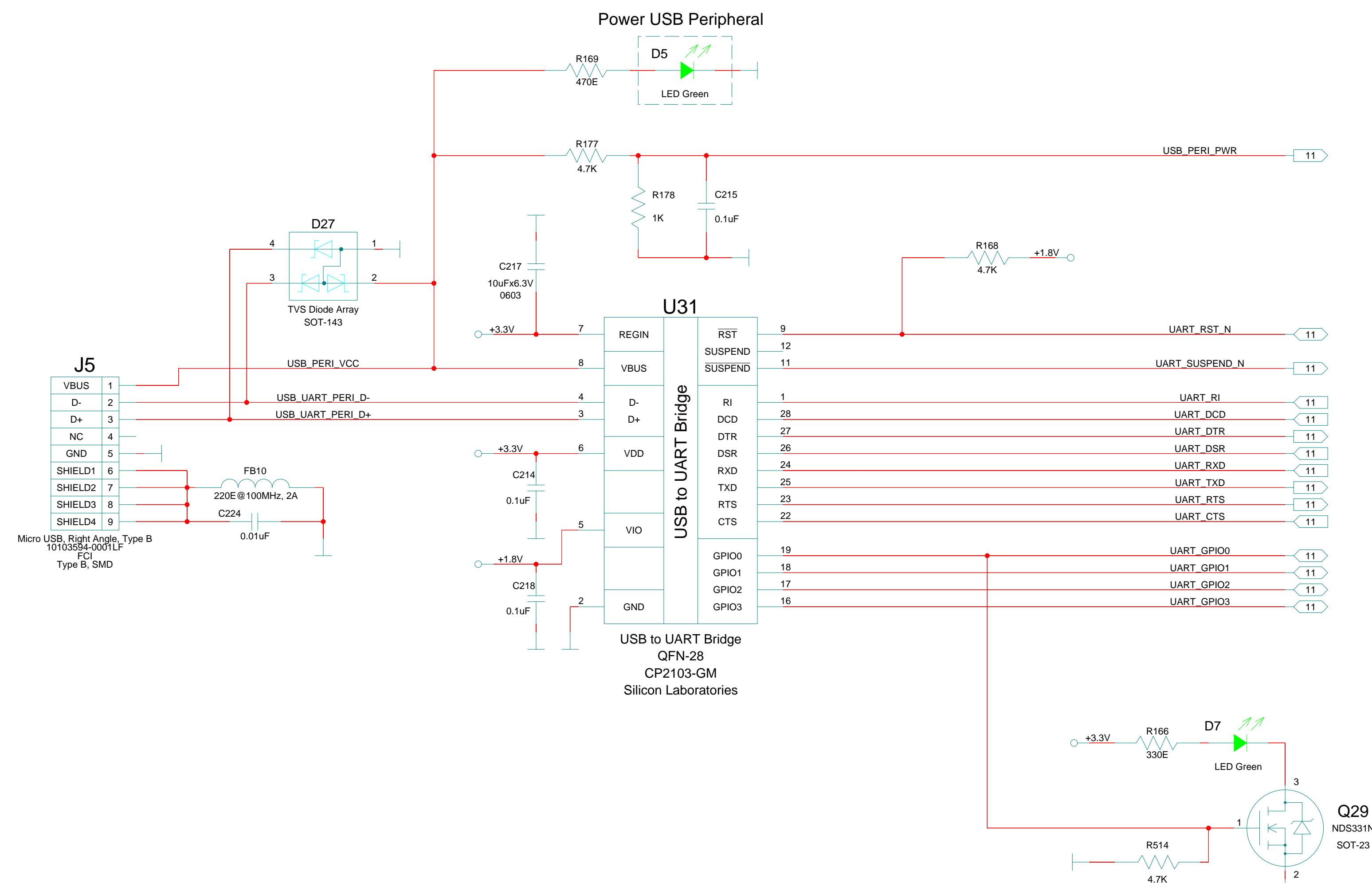
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APPROVALS	DATE	FPGA Diagram		
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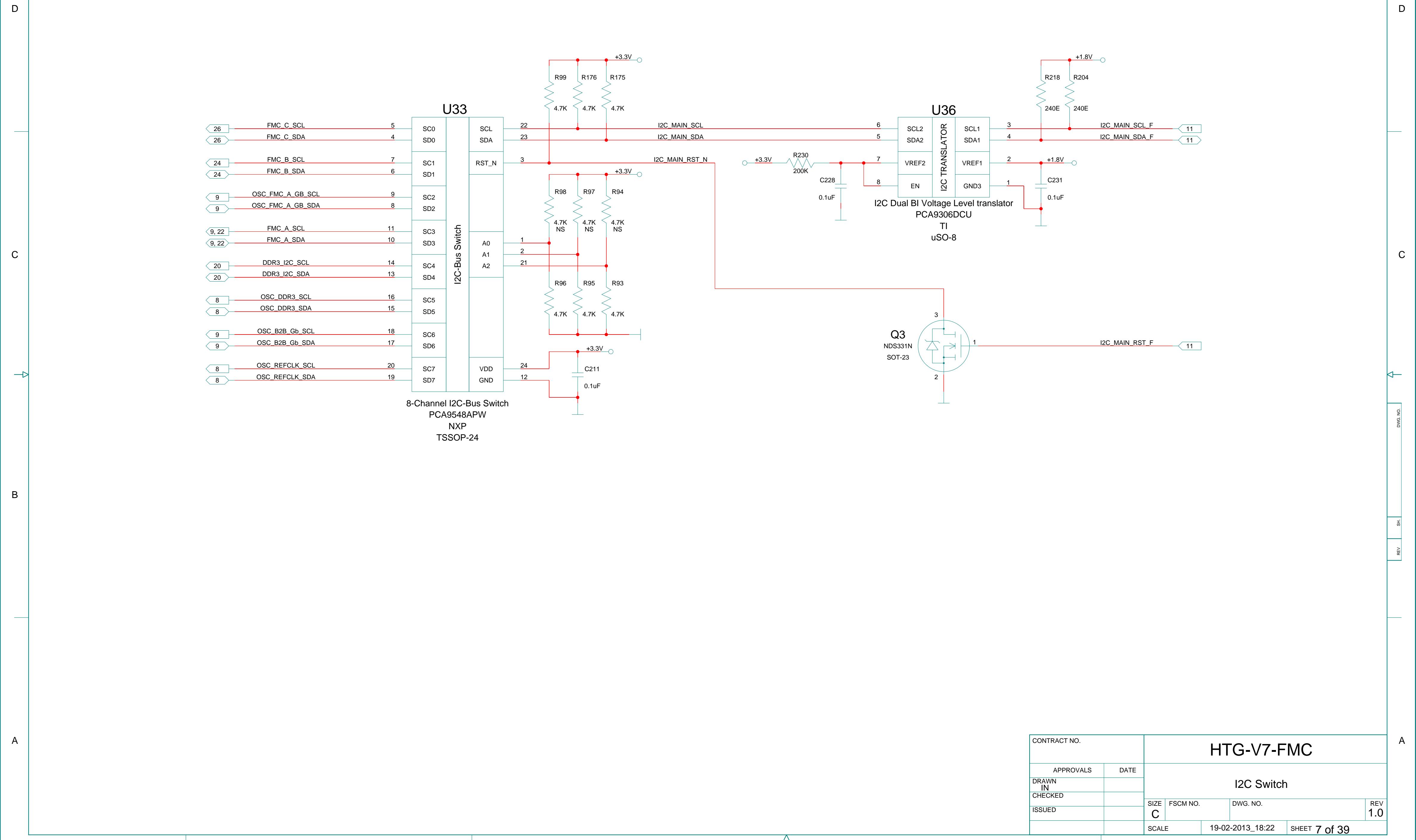


- 1) Power-on sequence for Virtex-7 devices is: VCCINT, VCCBRAM, VCCAUX, VCCAUX\_IO, and VCOO  
See 'Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics'
- 2) VCCAUX\_IO is 1.8V or 2.0V
- 4) For -1L devices: Core is 0.9V

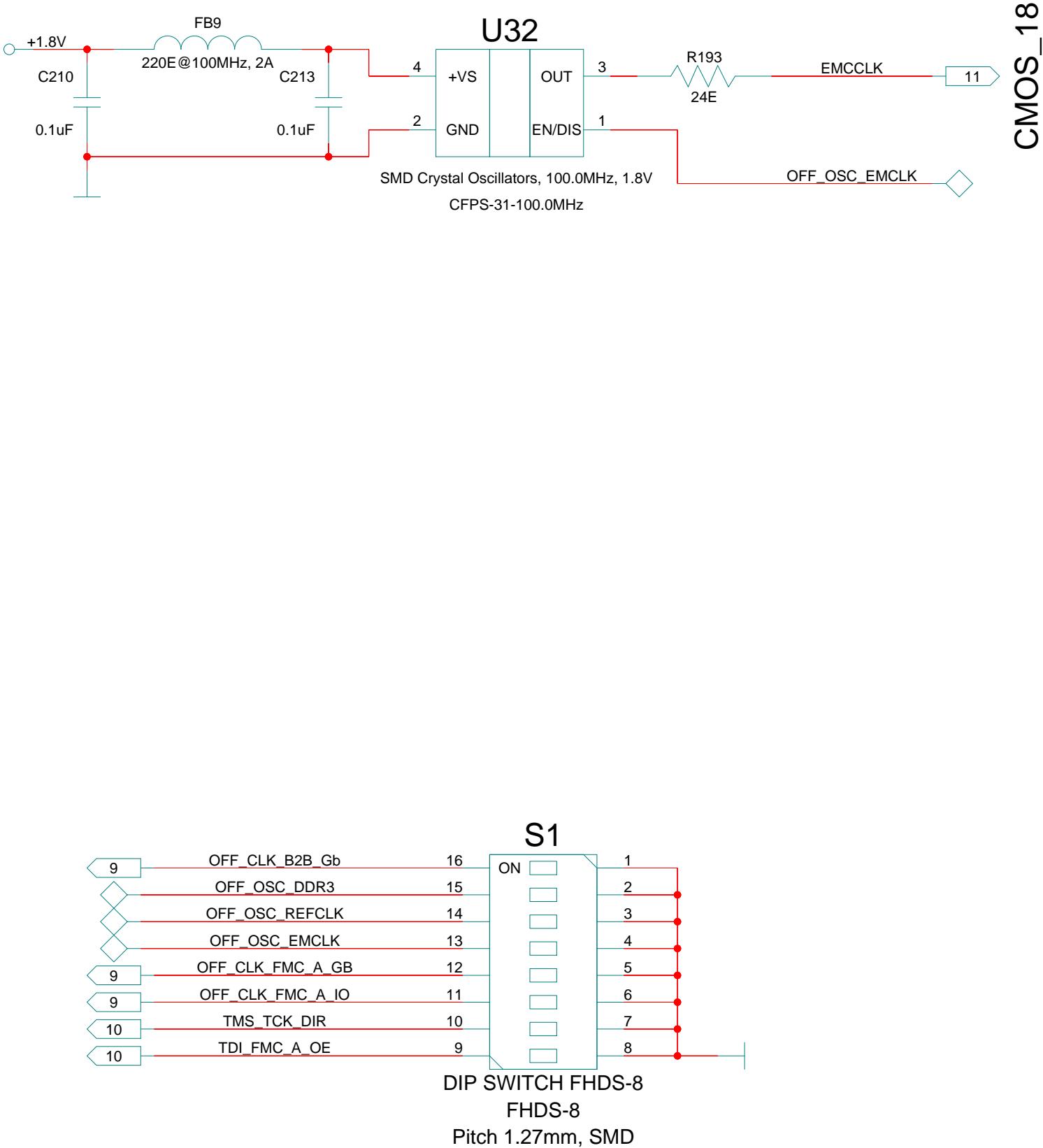
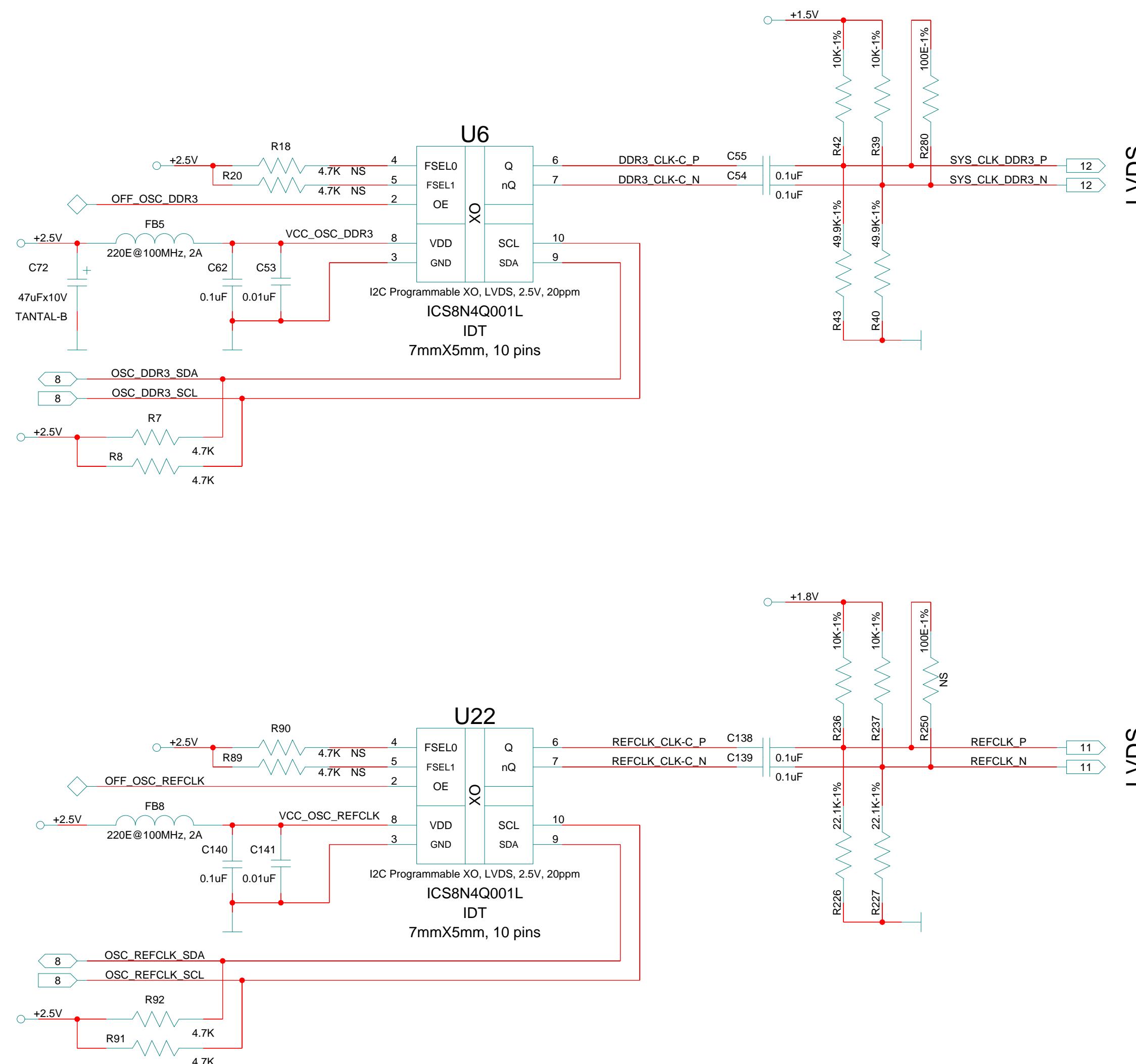
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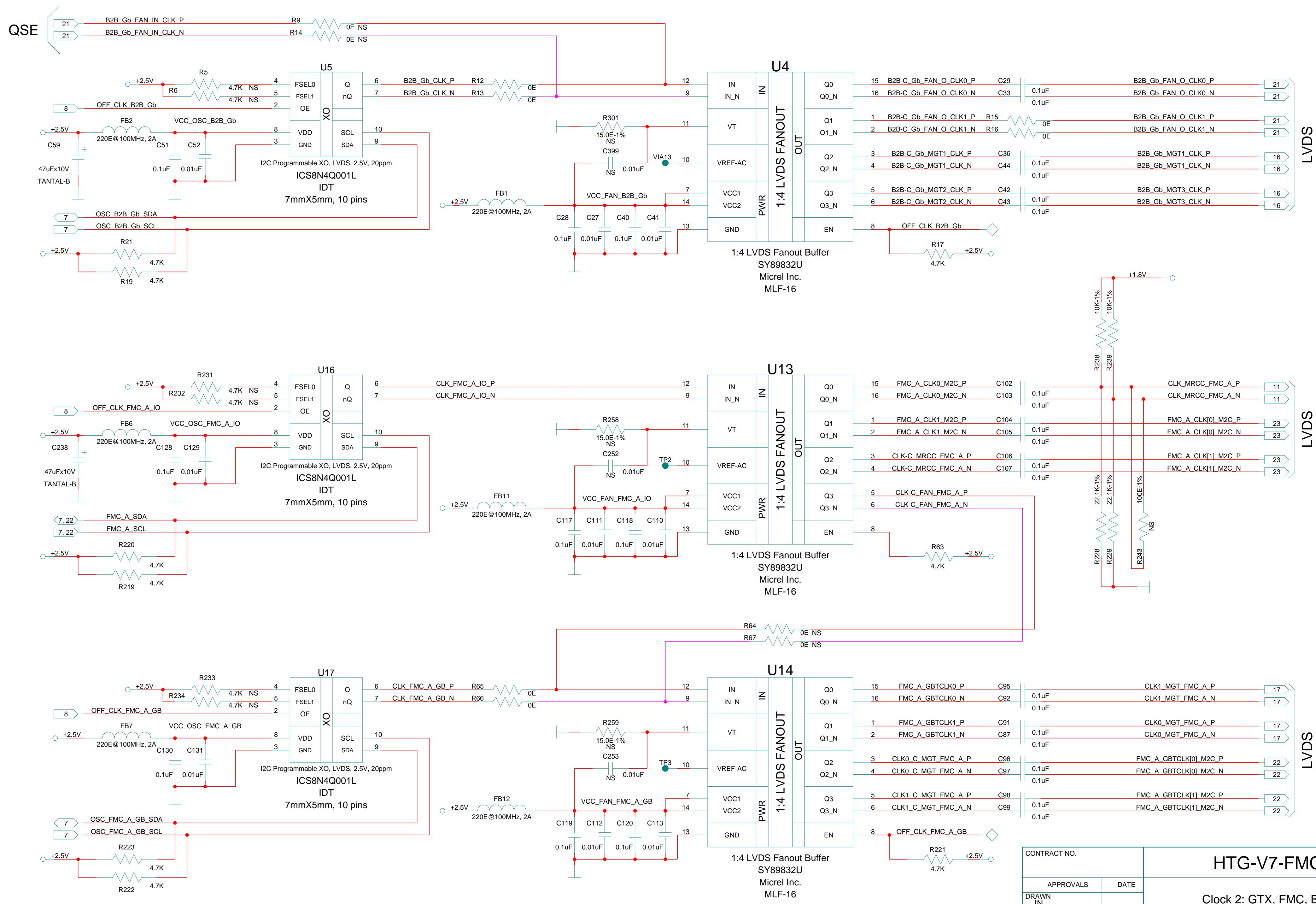
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CHECKED				
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CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	I2C Switch		
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CHECKED				
ISSUED				
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		REV	1.0	



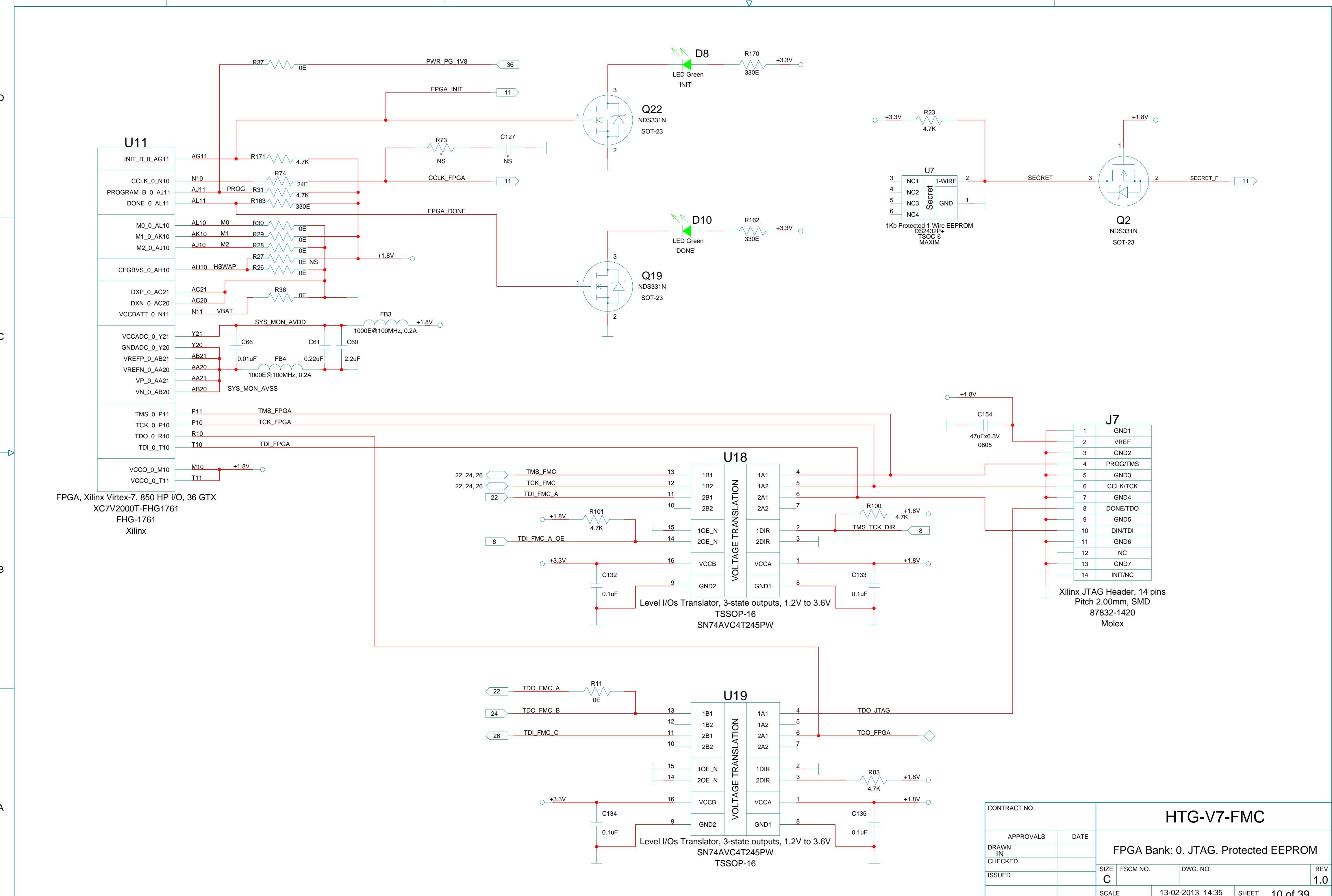
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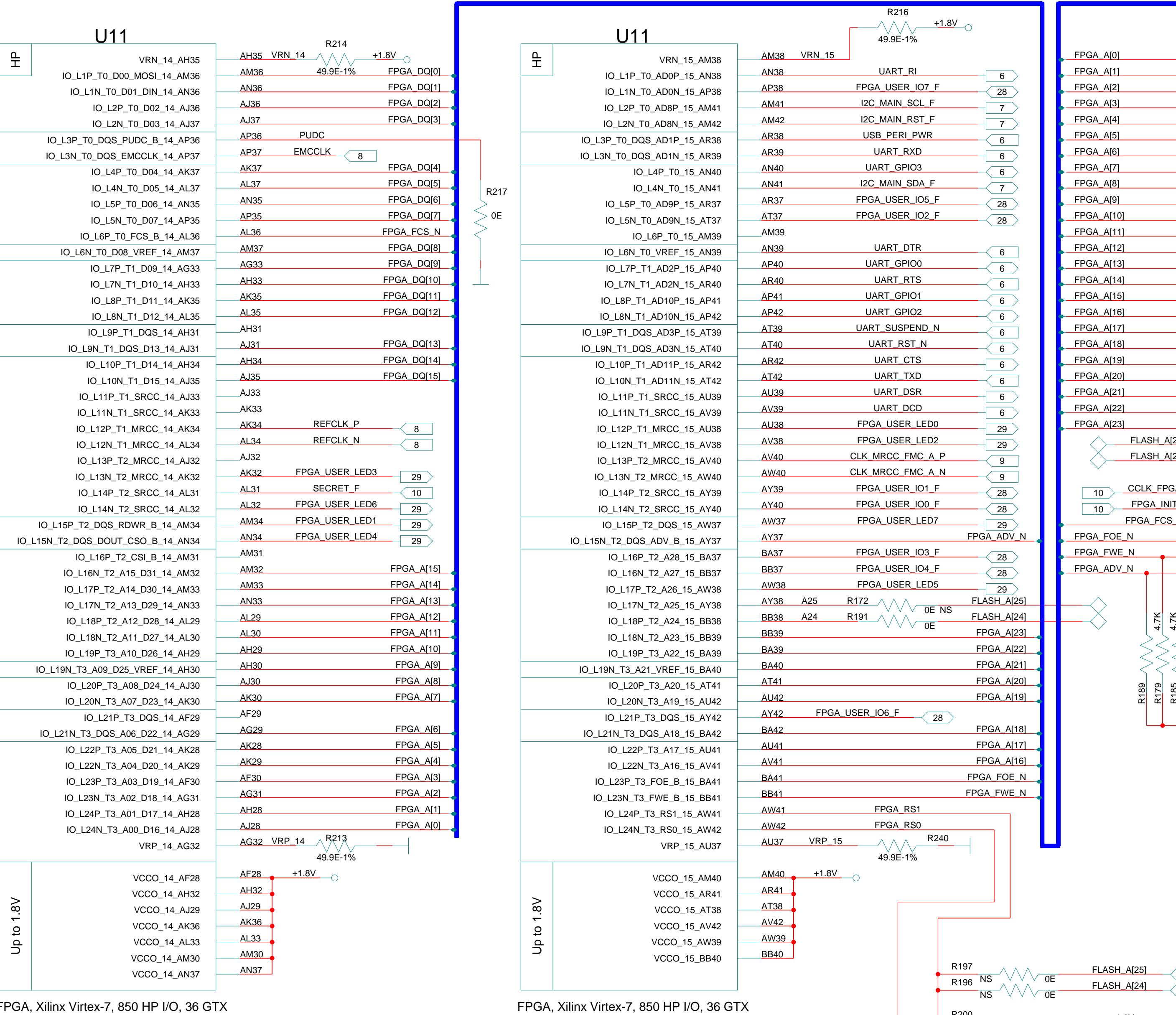


HTC V7 EMC

## Clock 2: GTX, FMC, B2B

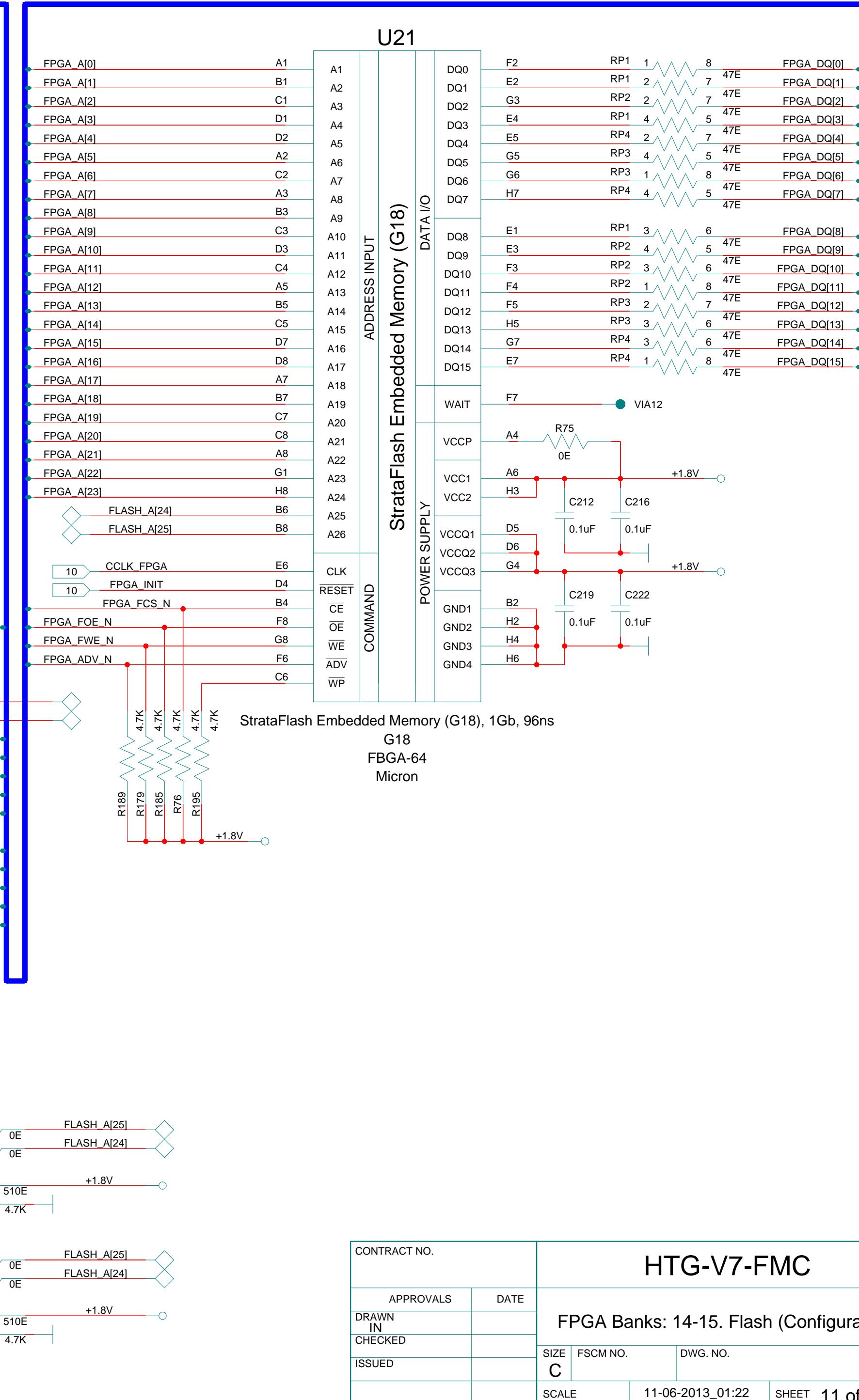
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APPROVALS	DATE	Clock 2: GTX, FMC, B2B					
DRAWN IN							
CHECKED		SIZE C	FSCM NO.		DWG. NO.		REV 1.0
ISSUED							
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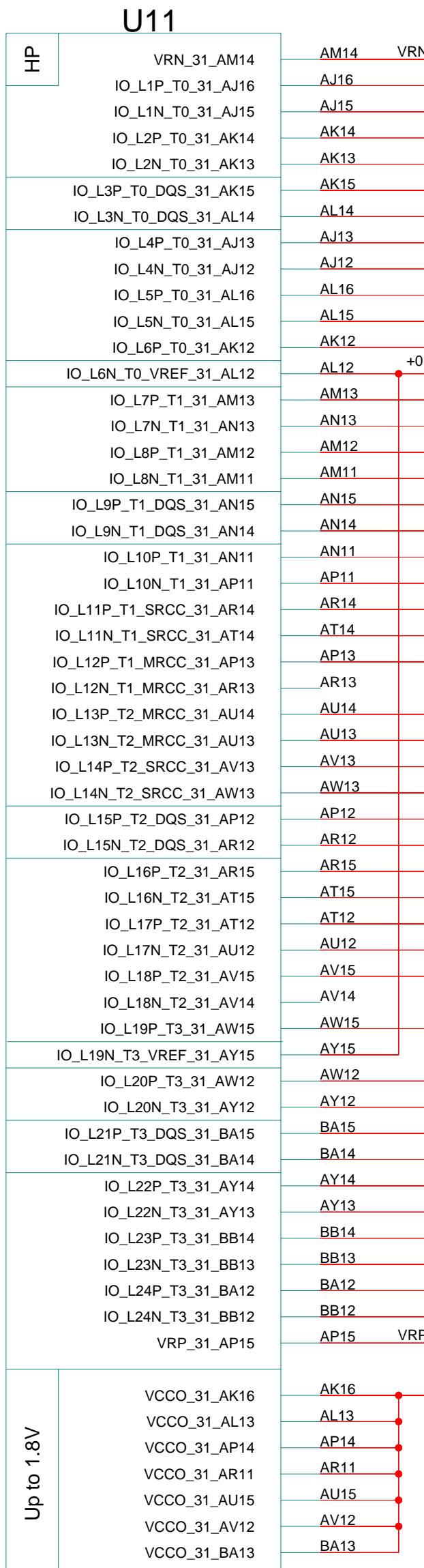




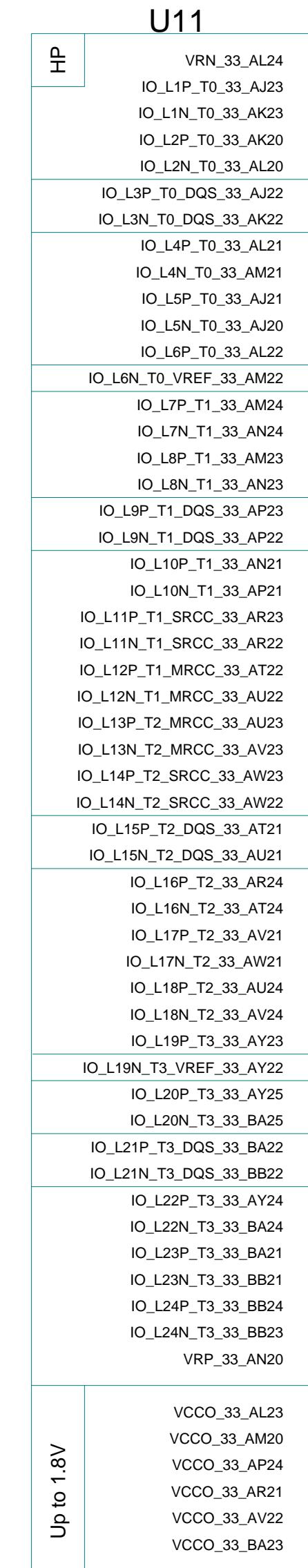
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XC7V2000T-FHG1761  
FHG-1761

FPGA, Xilinx Virtex-7, 850 HP I/O, 36 GTX  
XC7V2000T-FHG1761  
FHG-1761

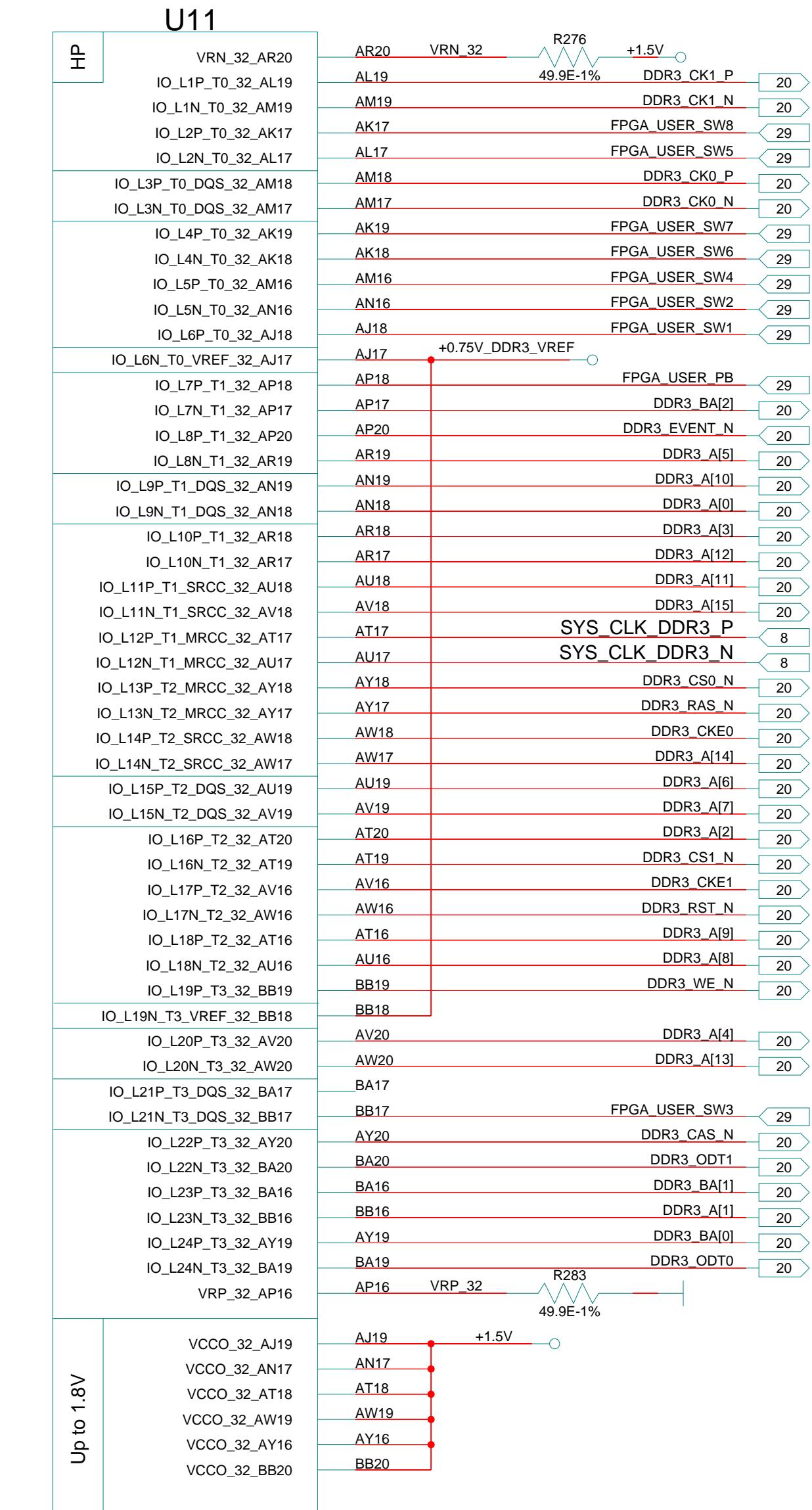




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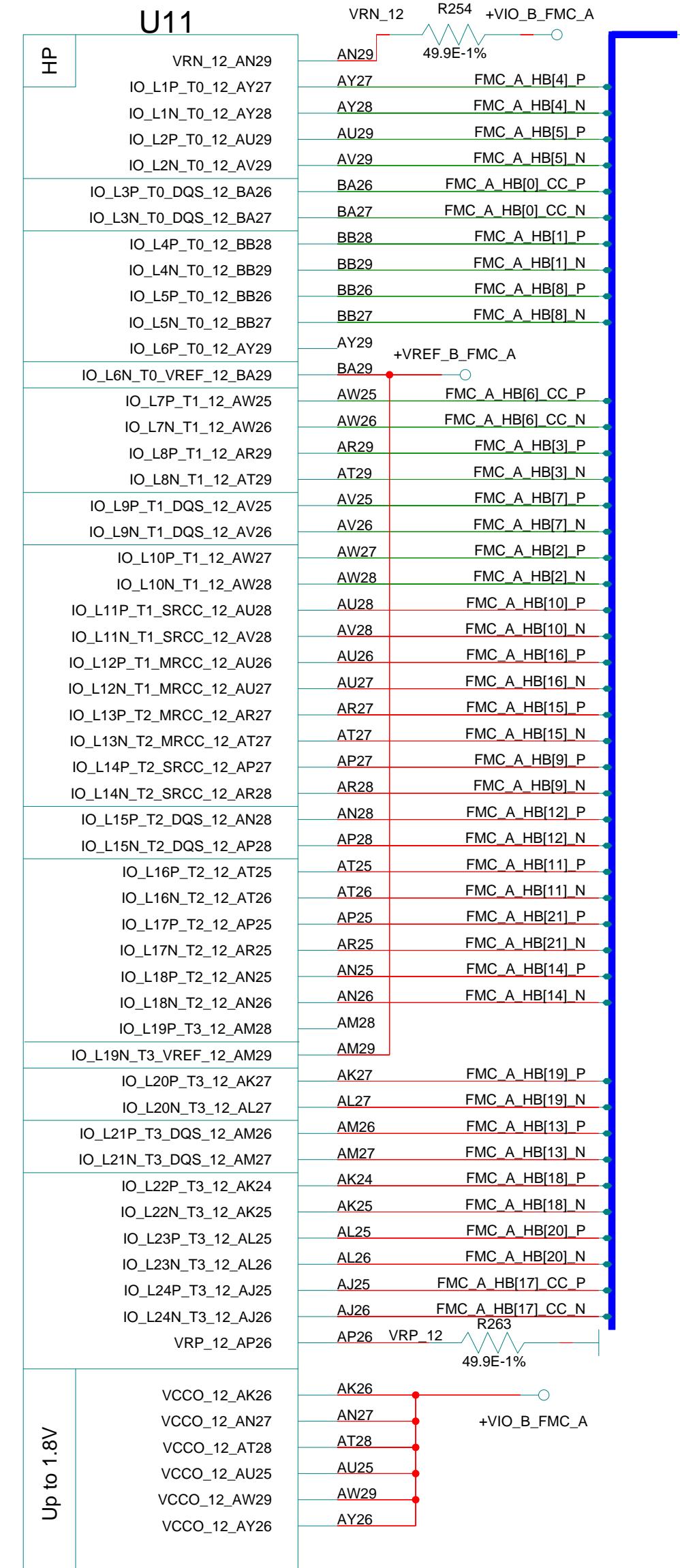
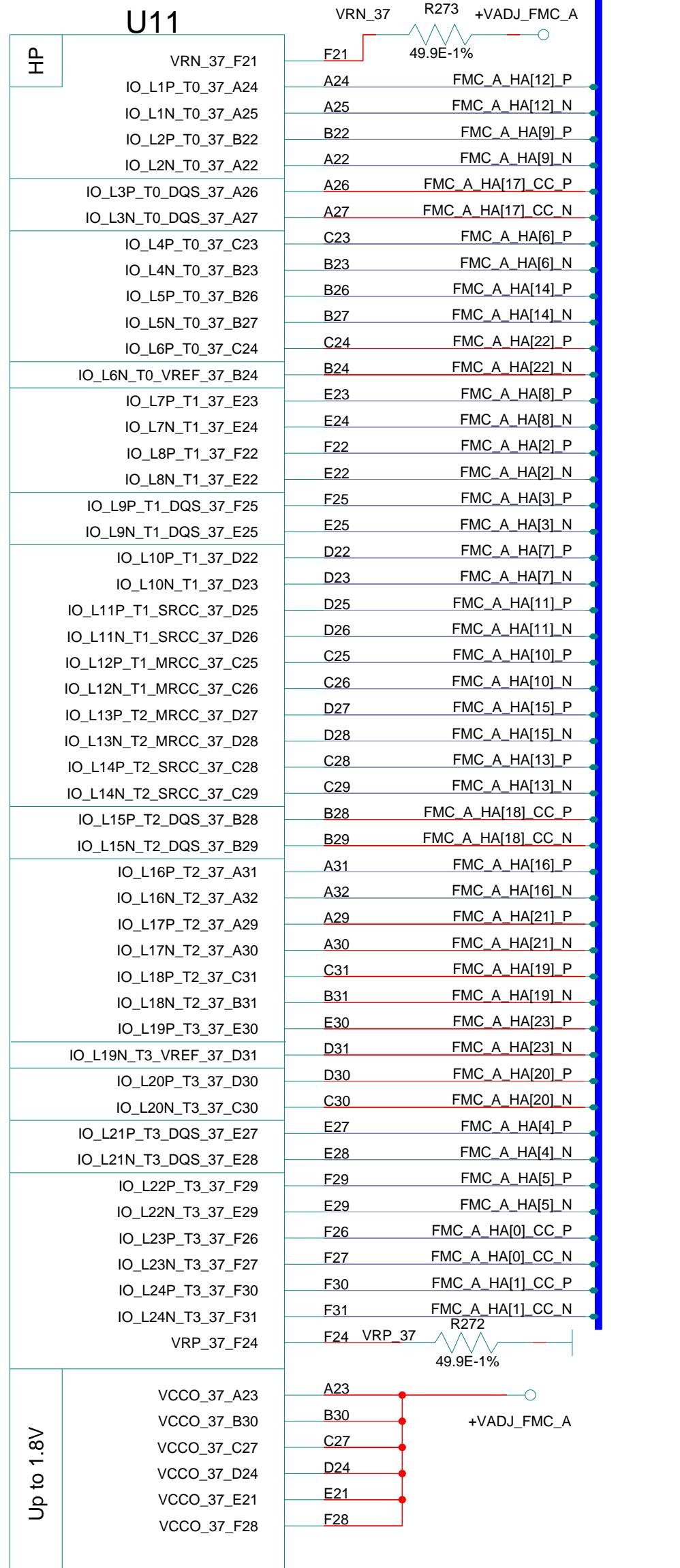
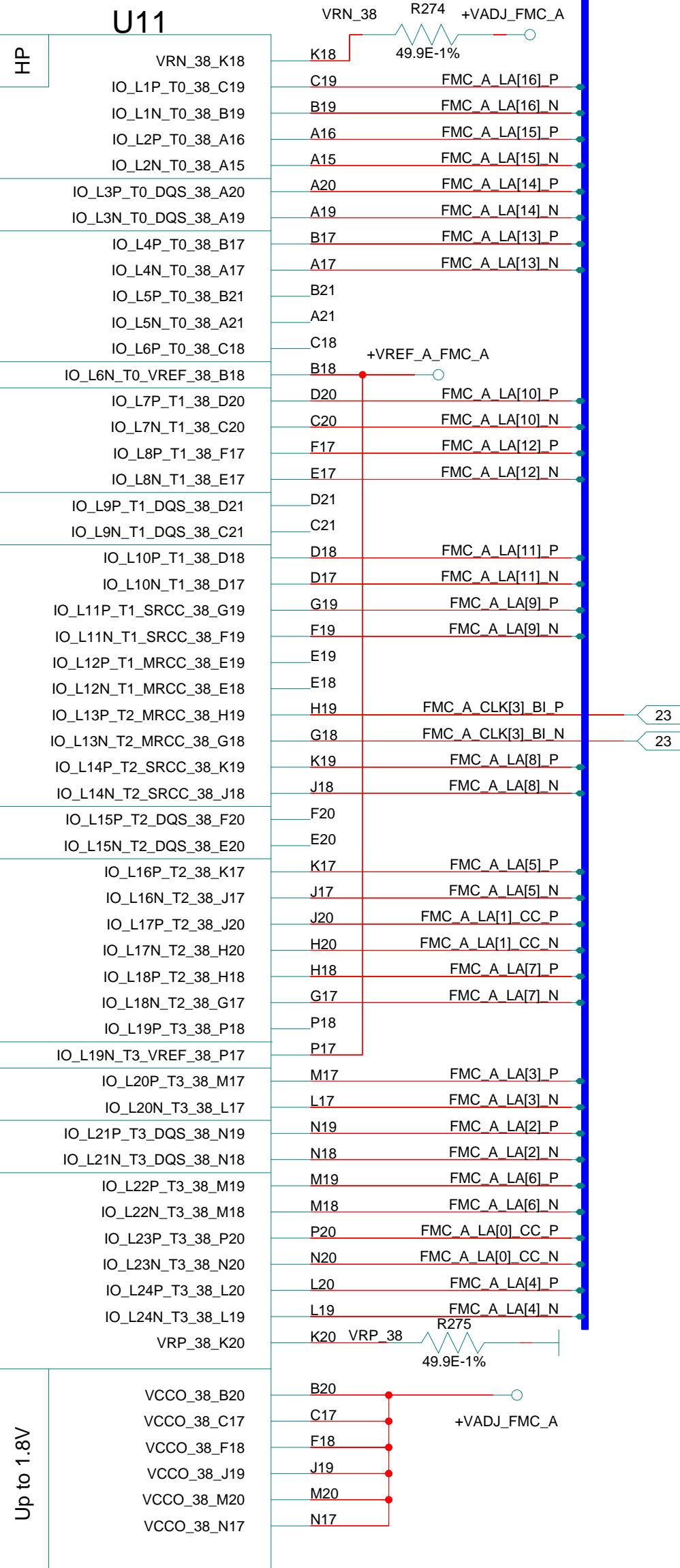
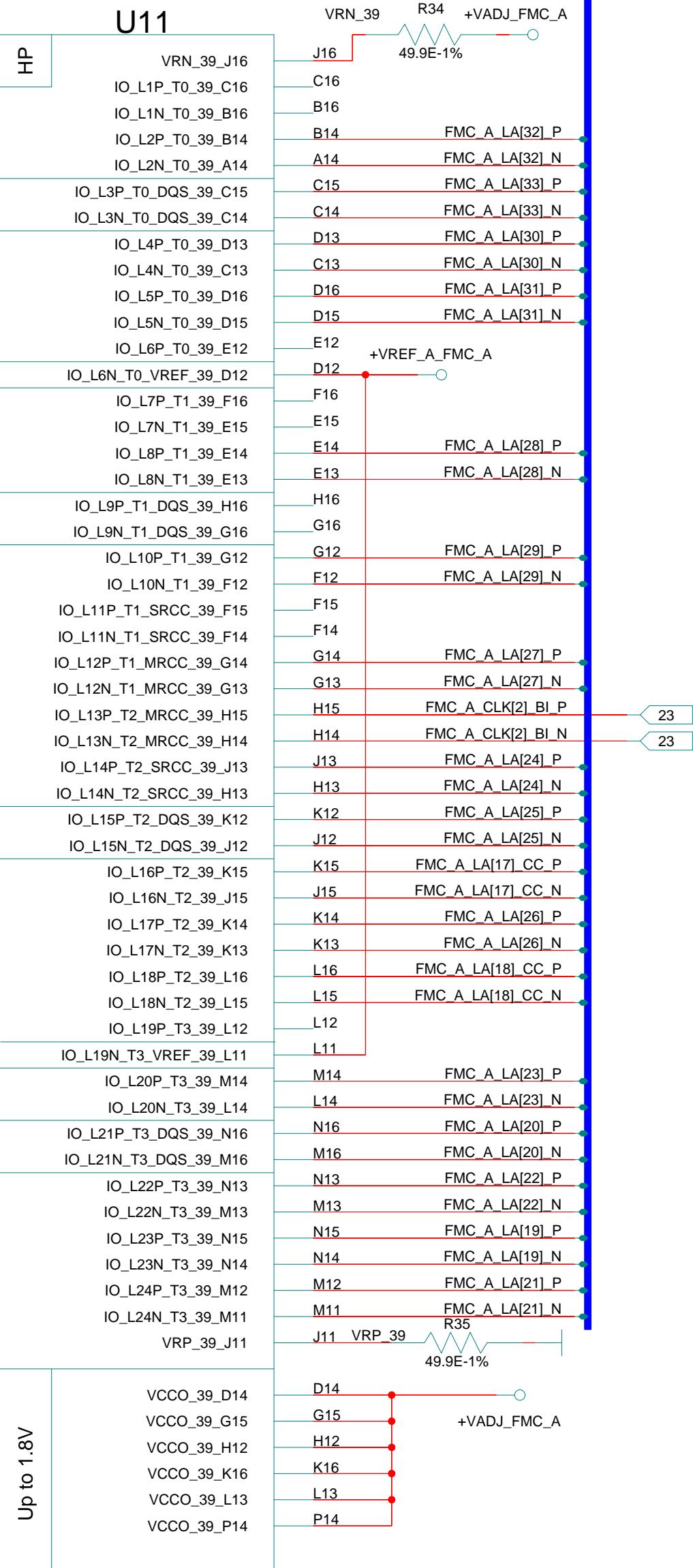


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FHG-1761



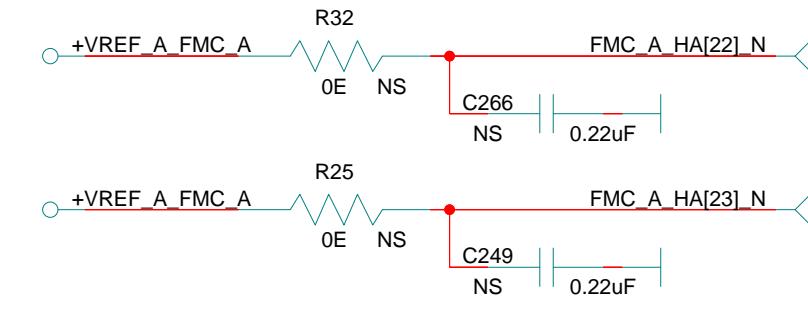
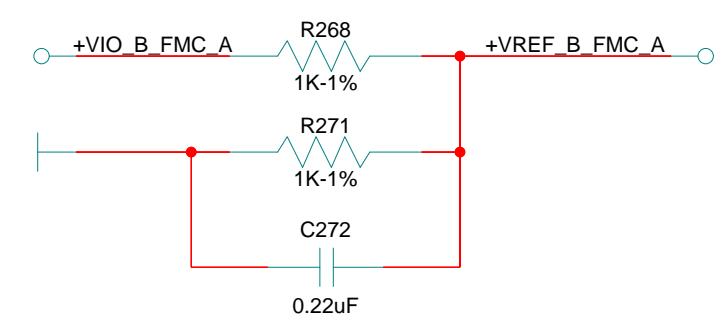
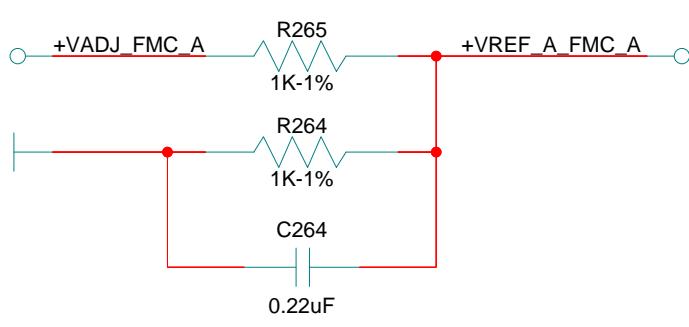
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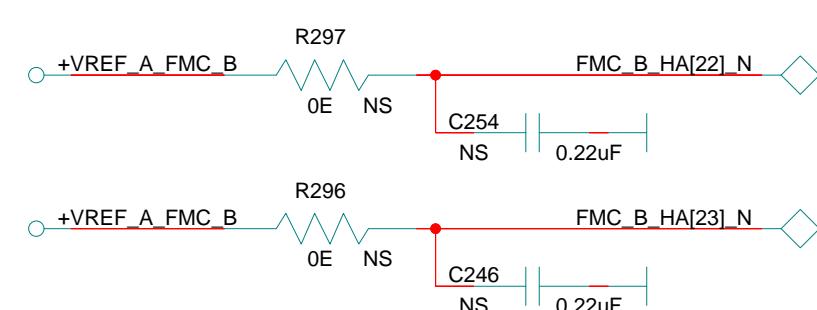
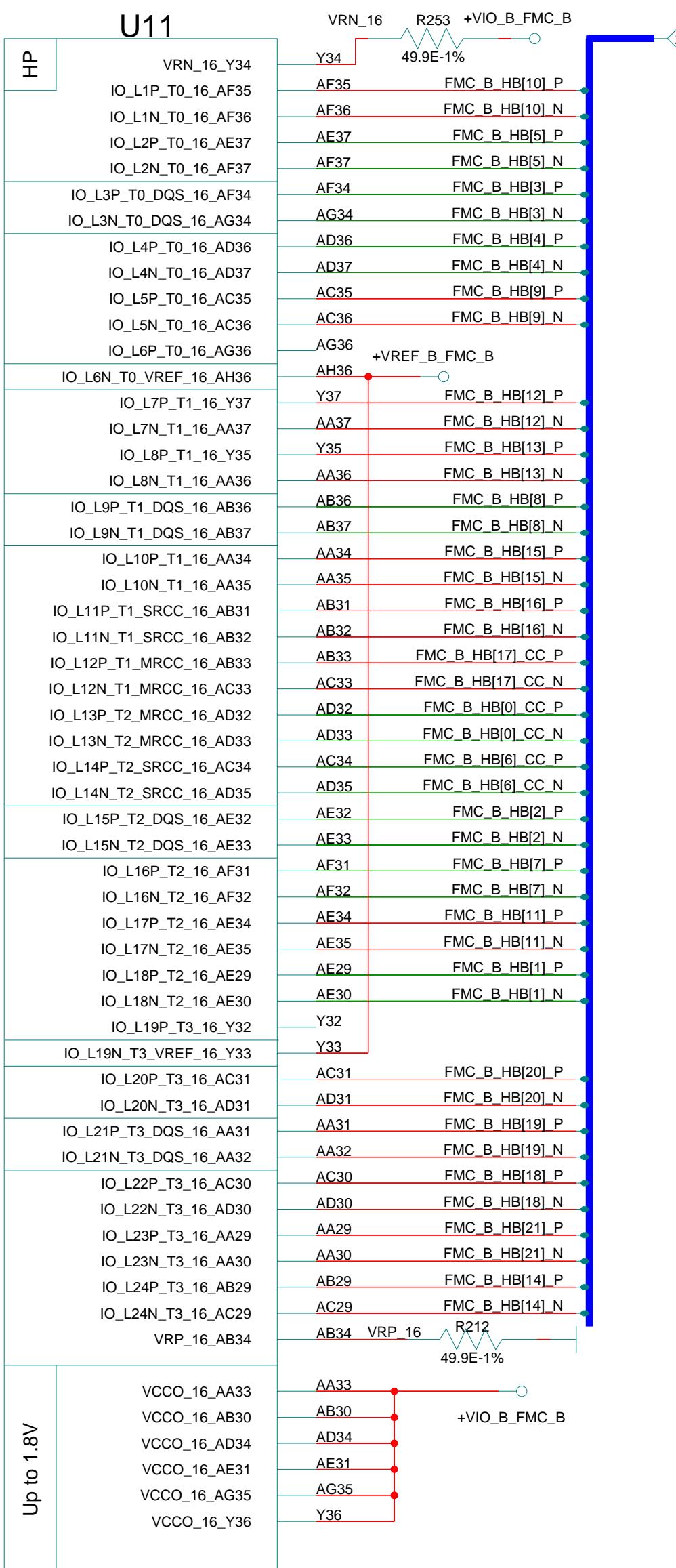
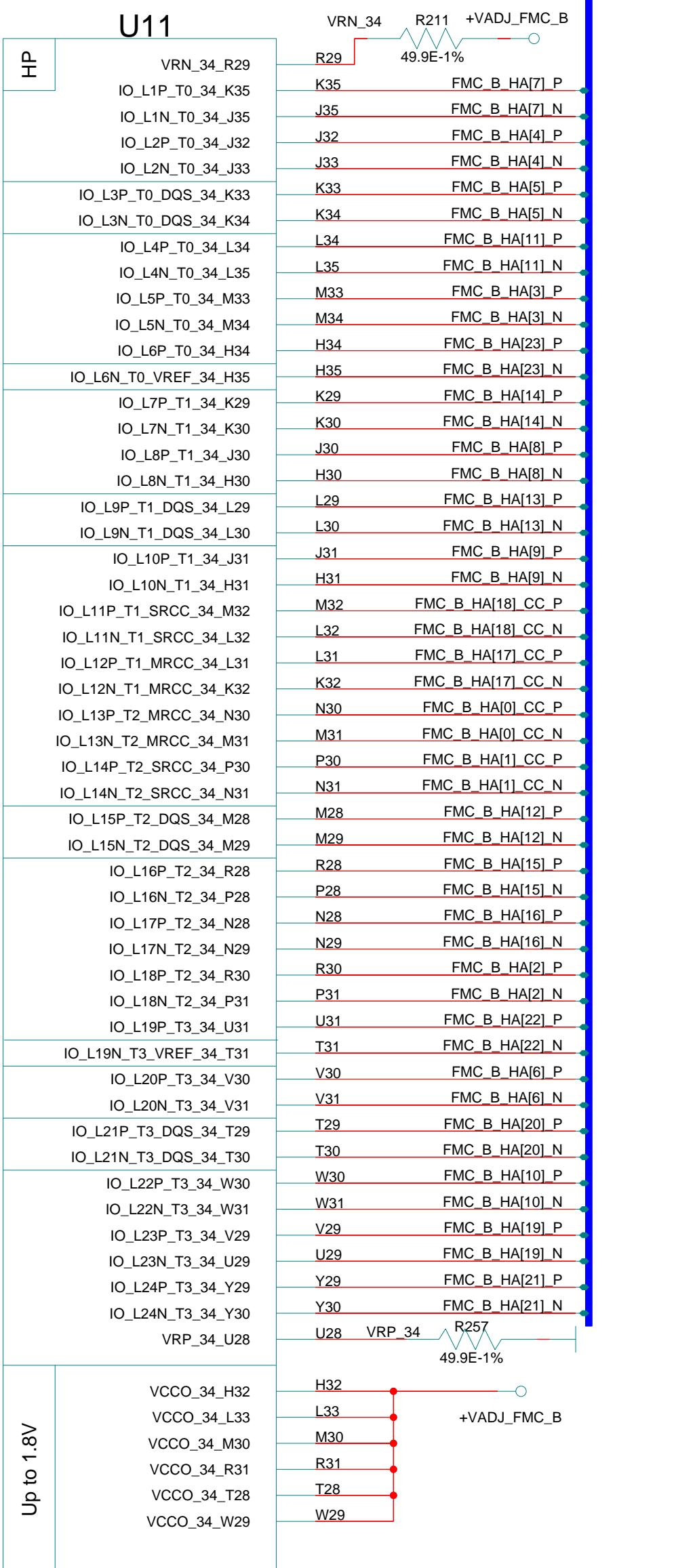
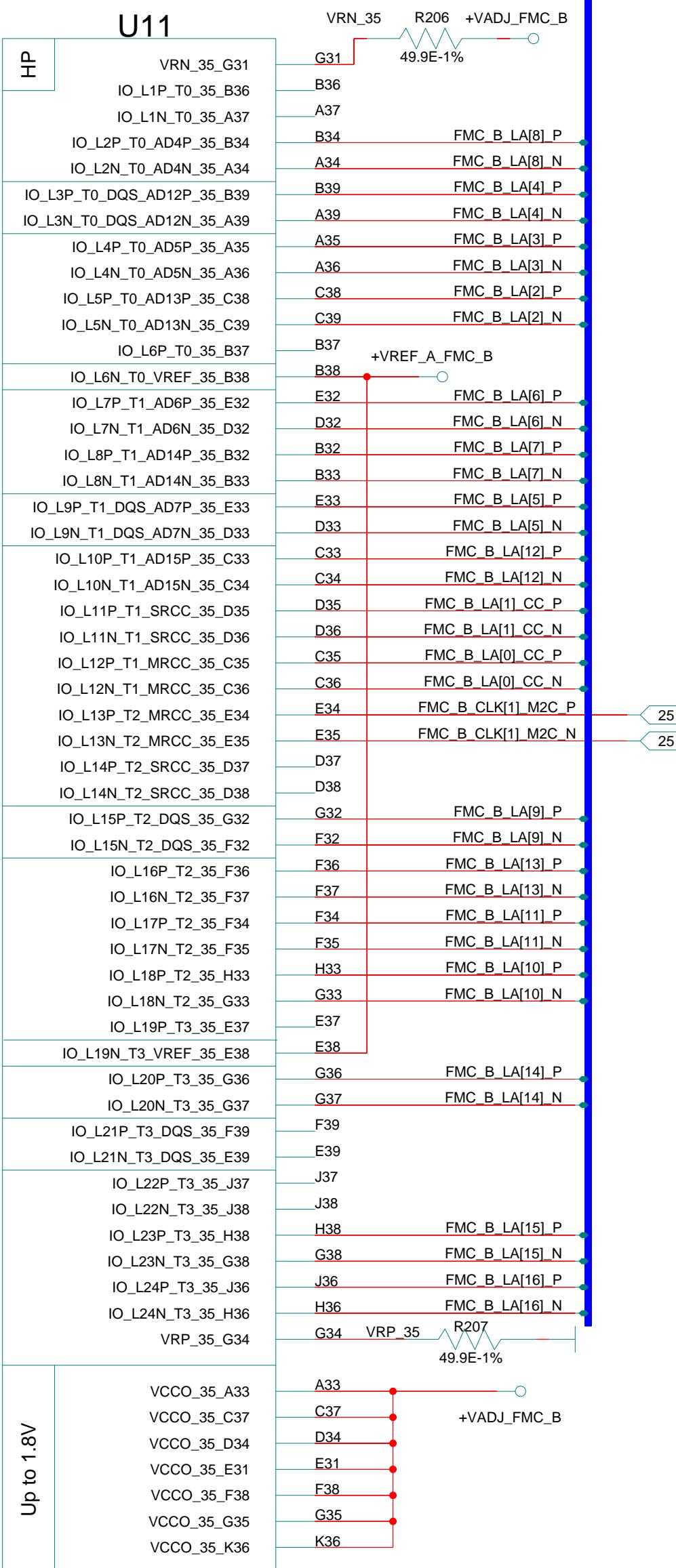
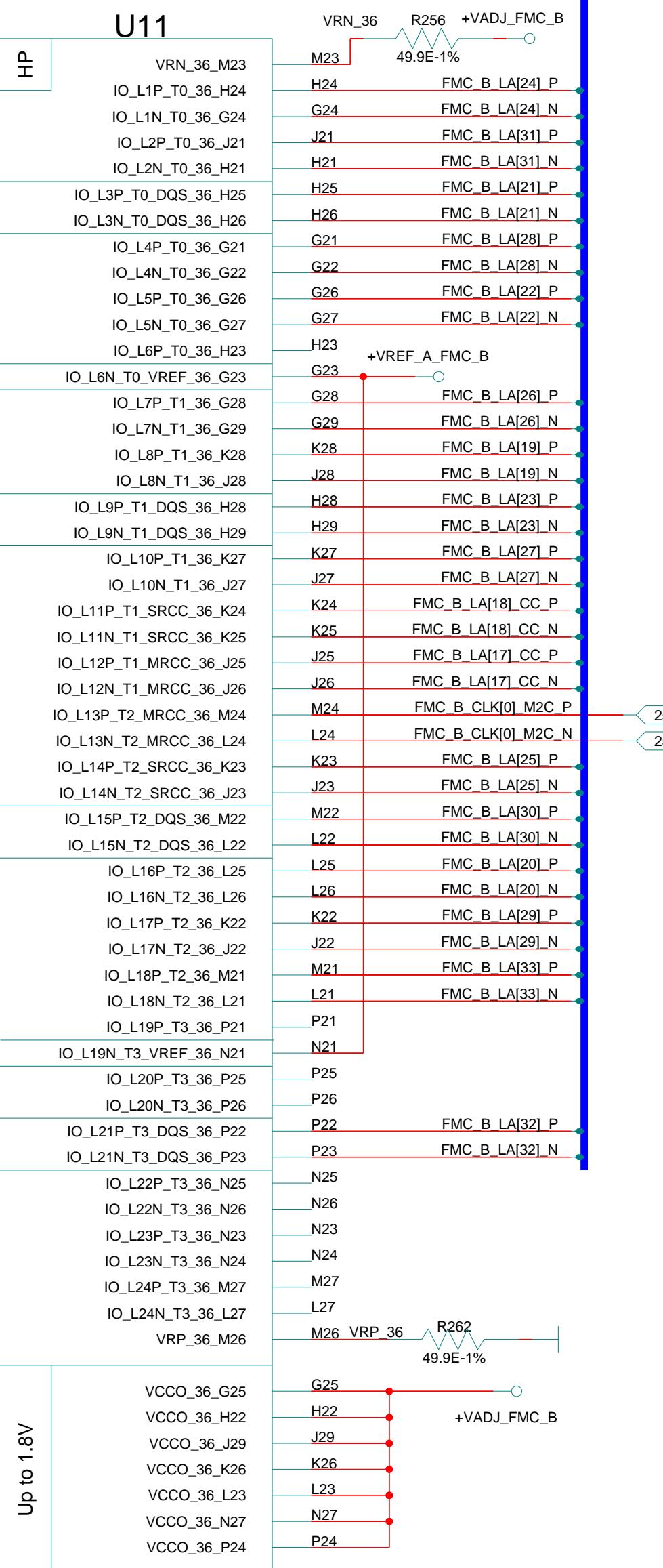
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ISSUED		C			1.0
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XC7V2000T-FHG1761  
FHG-1761

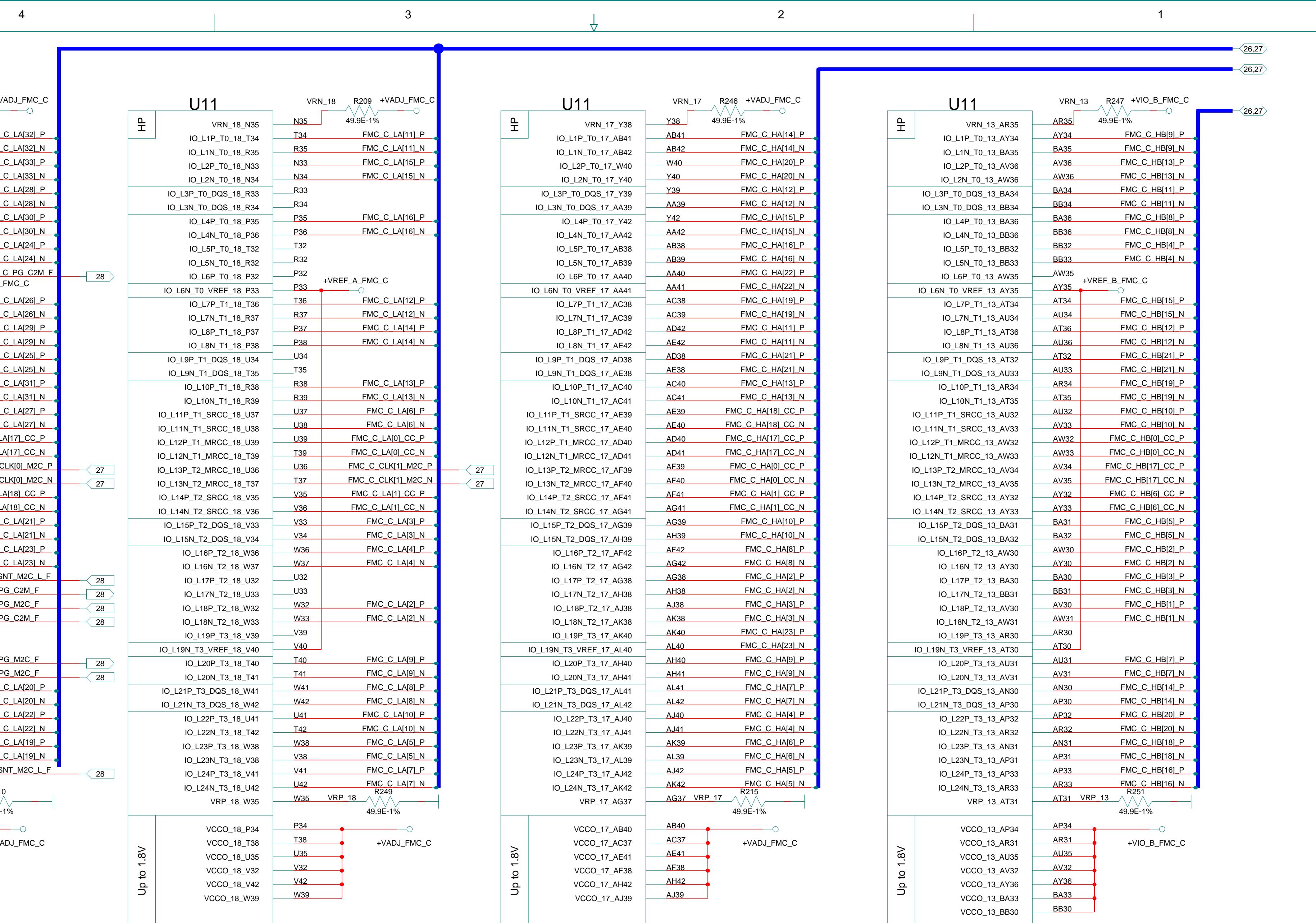
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SH					
DWG. NO.					



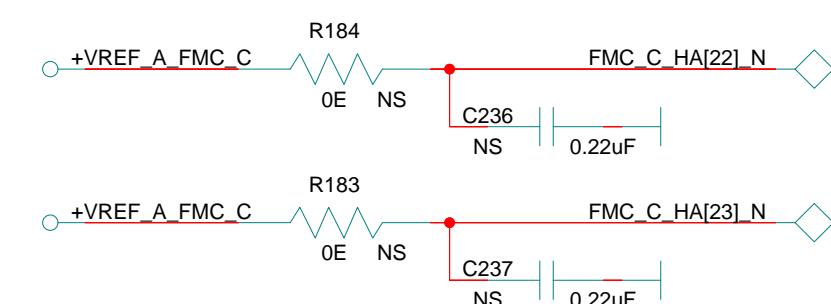


FPGA, Xilinx Virtex-7, 850 HP I/O, 36 GTX  
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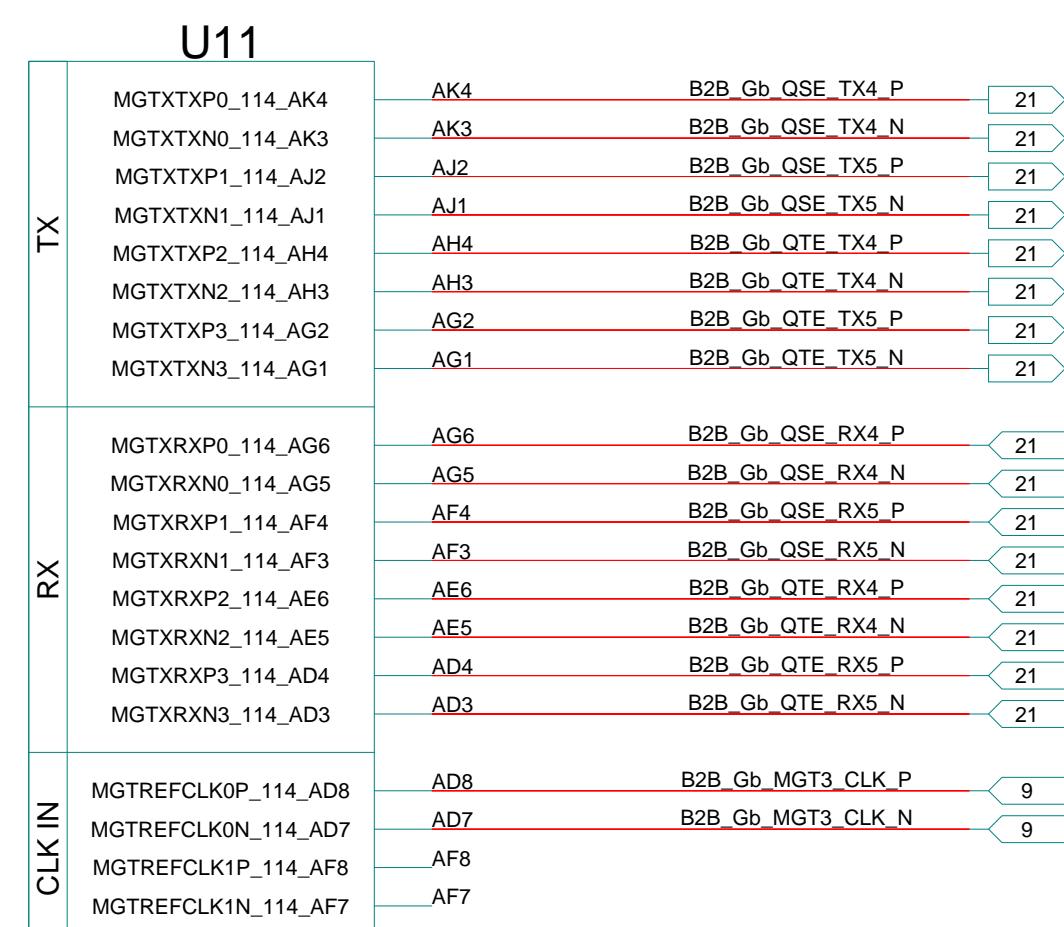
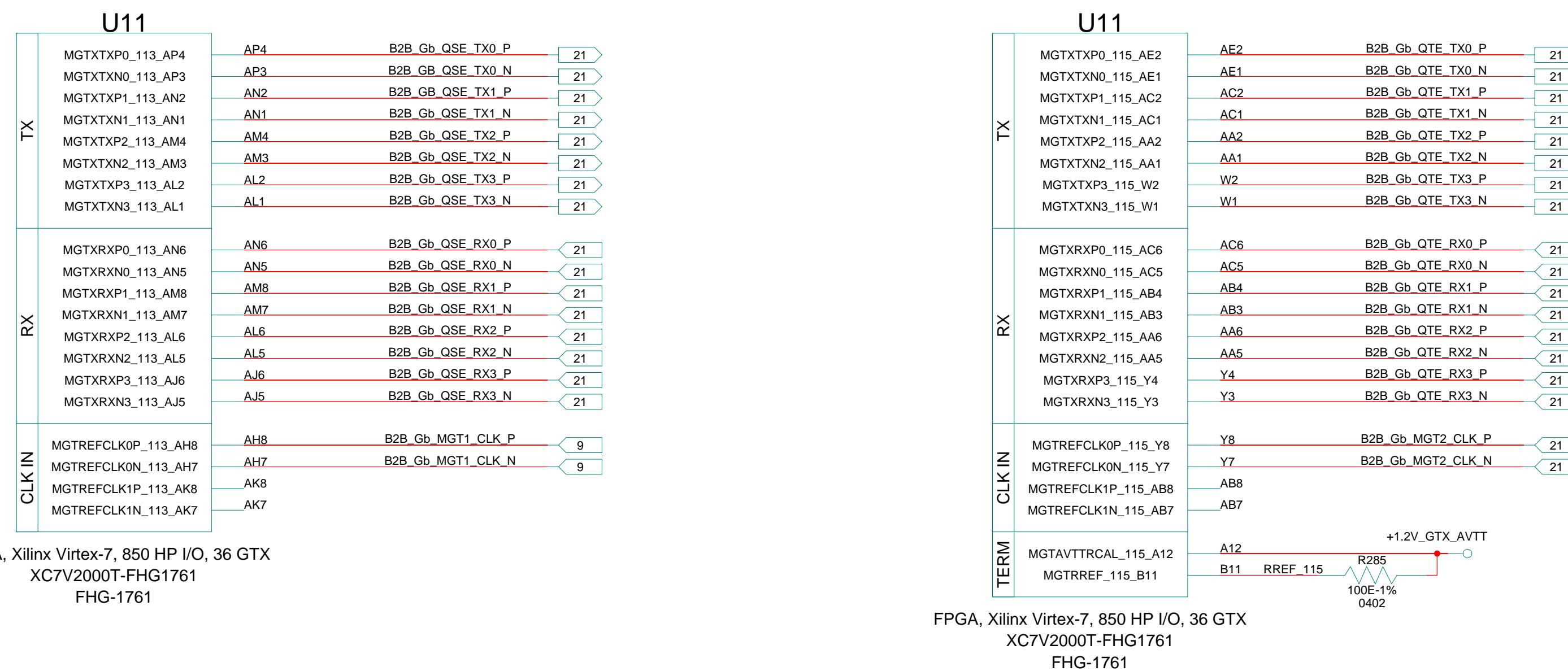
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ISSUED					
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FPGA, Xilinx Virtex-7, 850 HP I/O, 36 GTX  
XC7V2000T-FHG1761  
FHG-1761



CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	FPGA Banks: 13, 17-19 (FMC 'C' LVDS IO)		
DRAWN IN				
CHECKED				
ISSUED		SIZE	FSCM NO.	DWG. NO.
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XC7V2000T-FHG1761  
FHG-1761

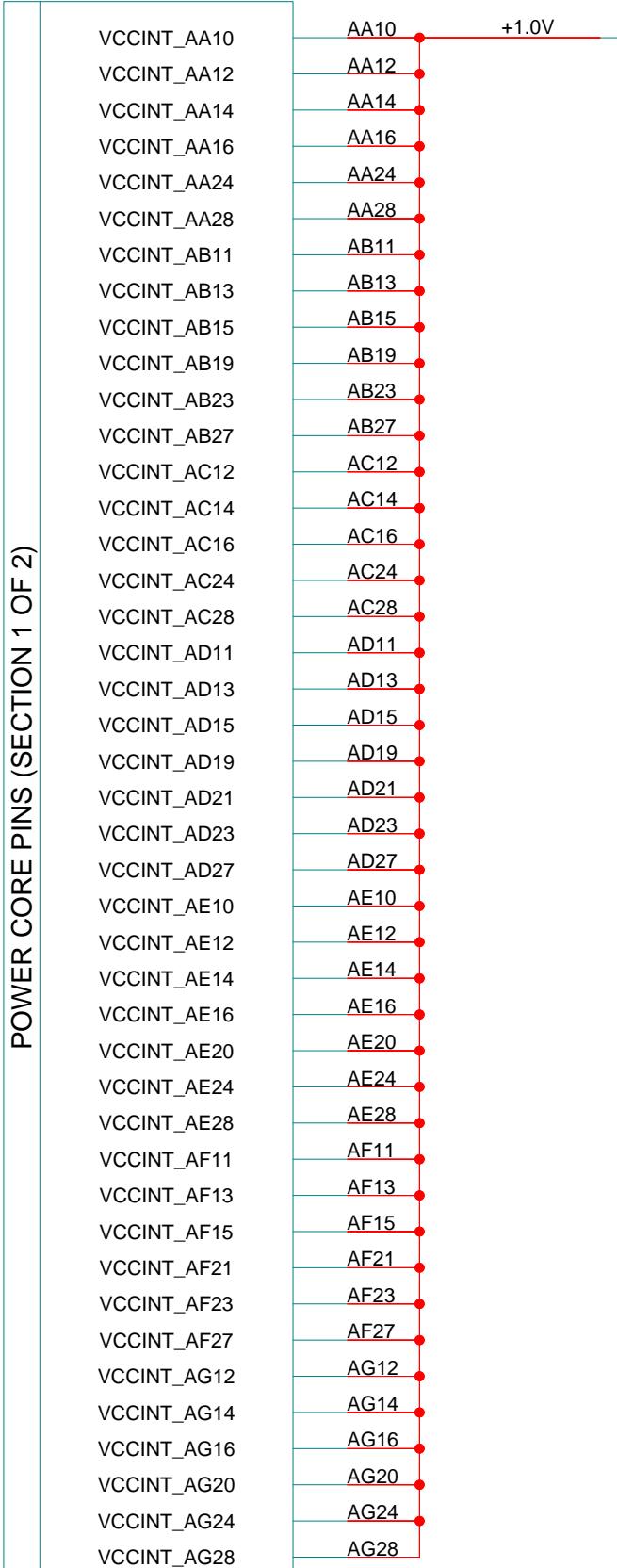
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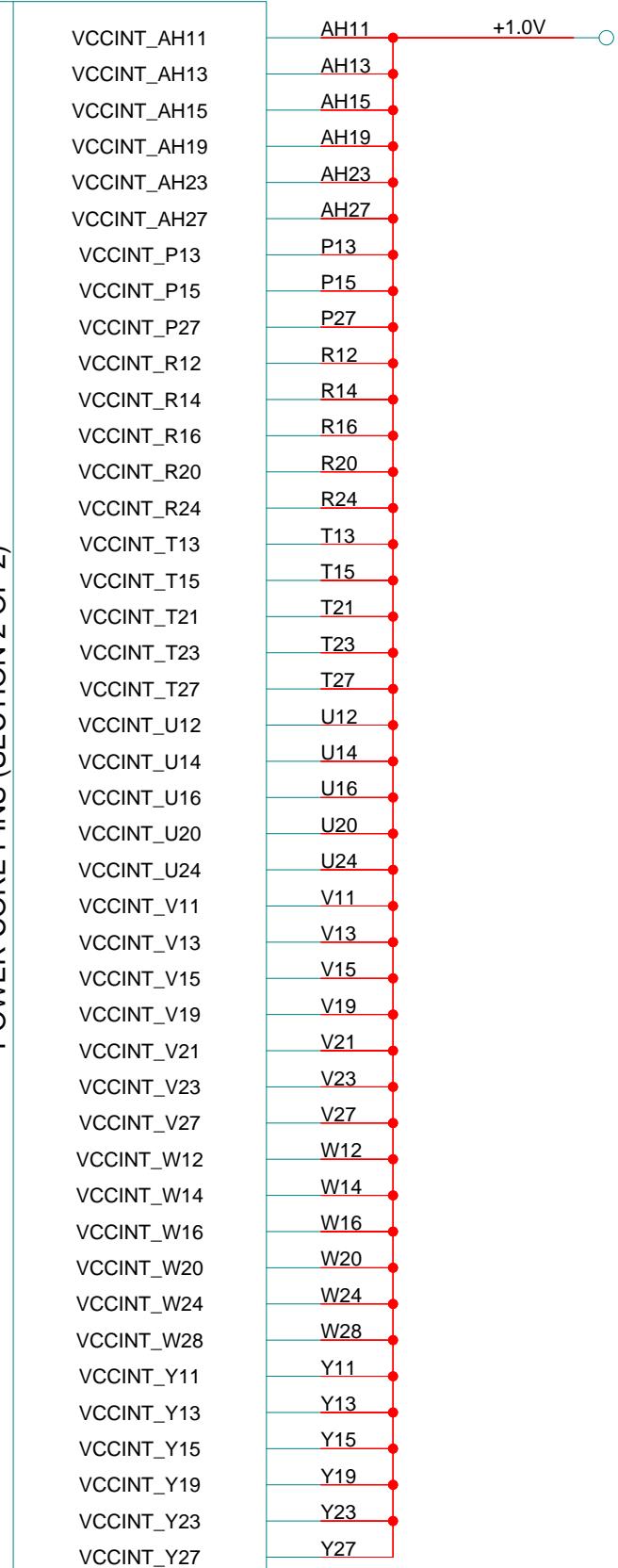
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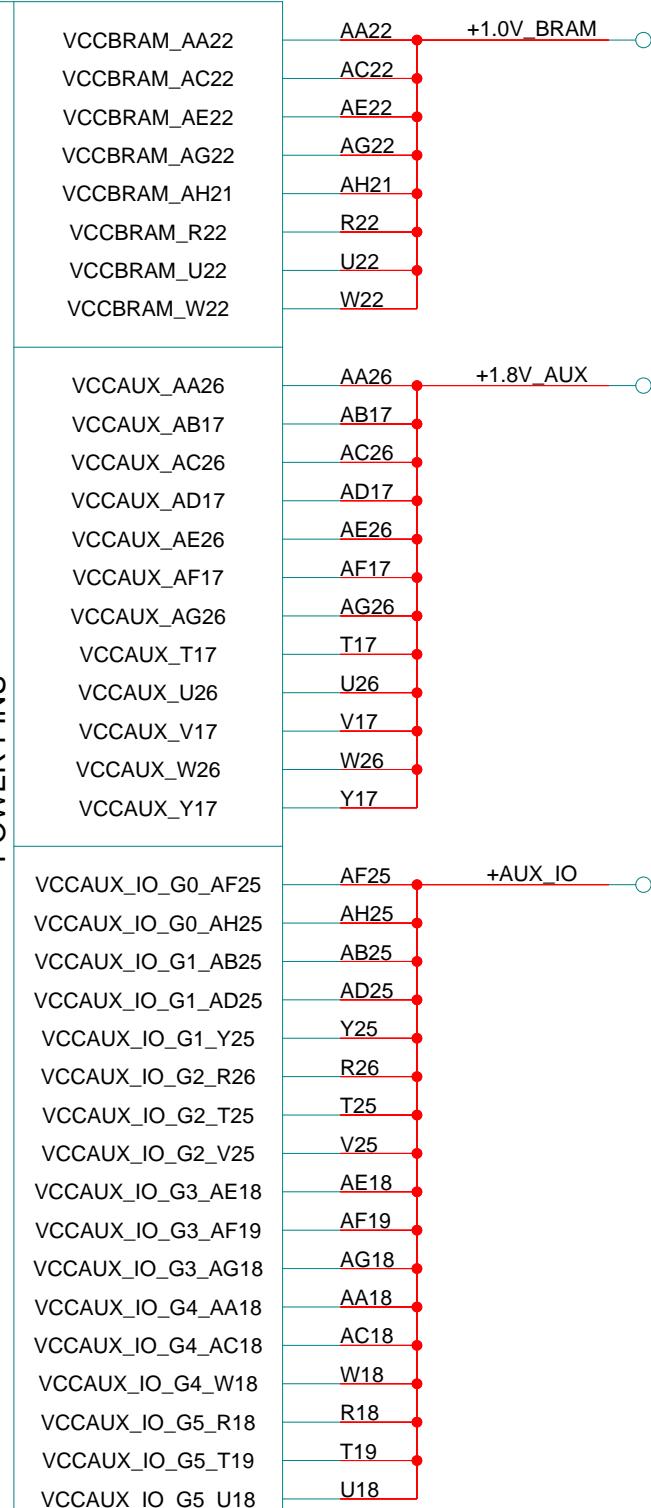
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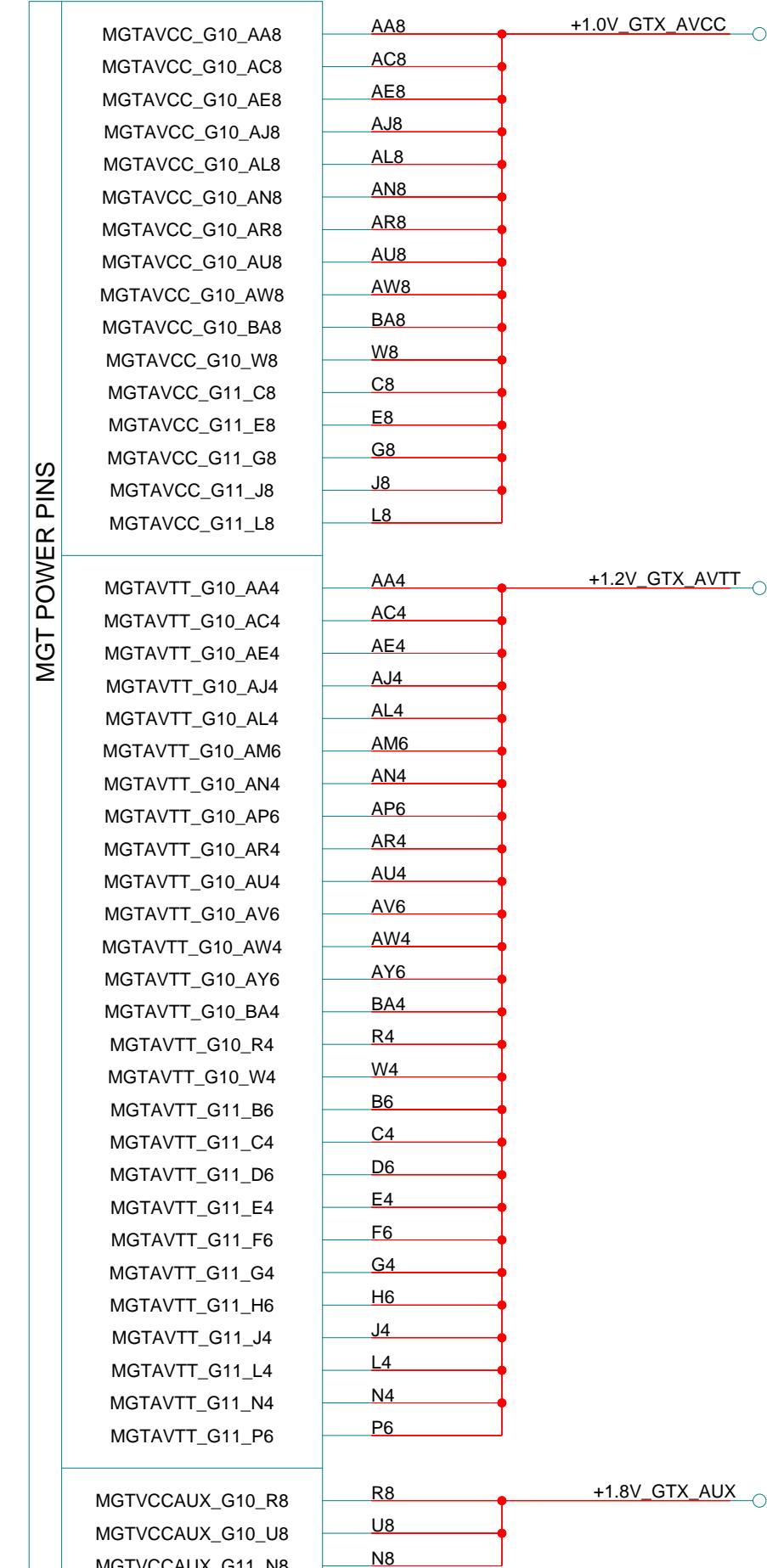
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XC7V2000T-FHG1761  
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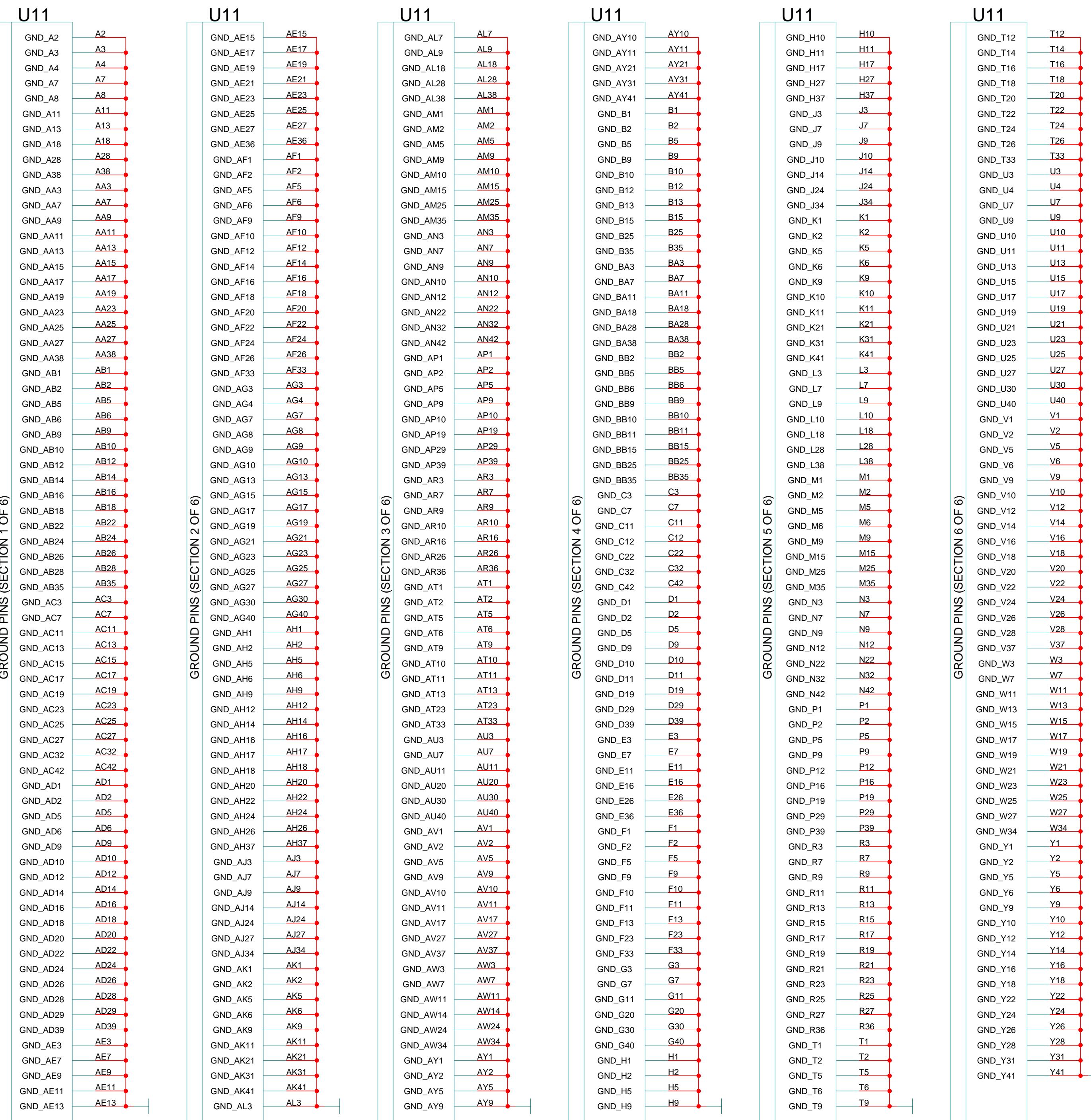
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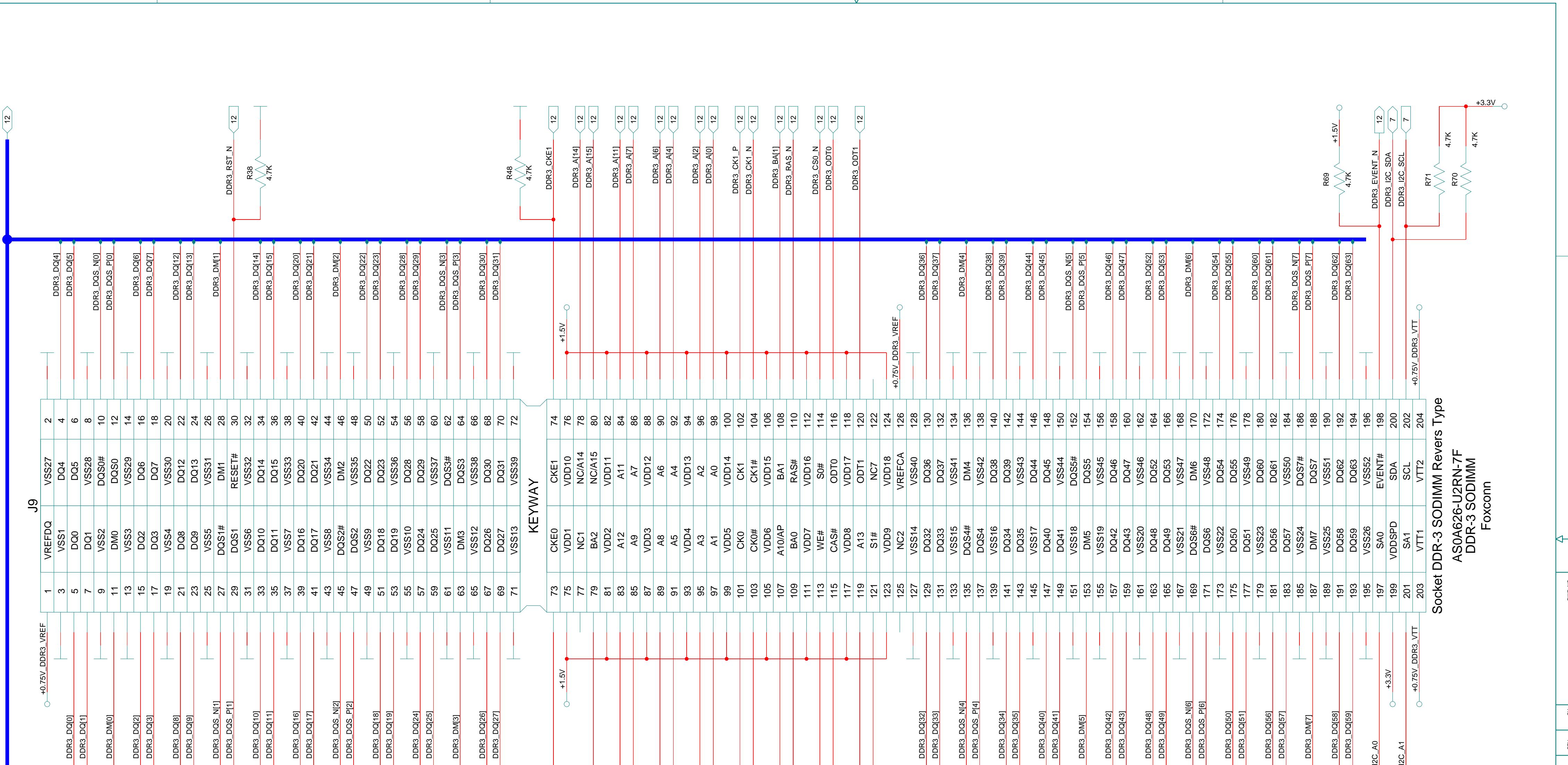
HTG-V7-FMC

FPGA Banks: PWR

APPROVALS	DATE	DRAWN IN	CHECKED	ISSUED	SIZE	FSCM NO.	DWG. NO.	REV

SCALE 12-02-2013\_15:43 SHEET 18 of 39





Socket DDR-3 SODIMM Revers Type  
AS0A626-U2RN-7F  
DDR-3 SODIMM  
Foxconn

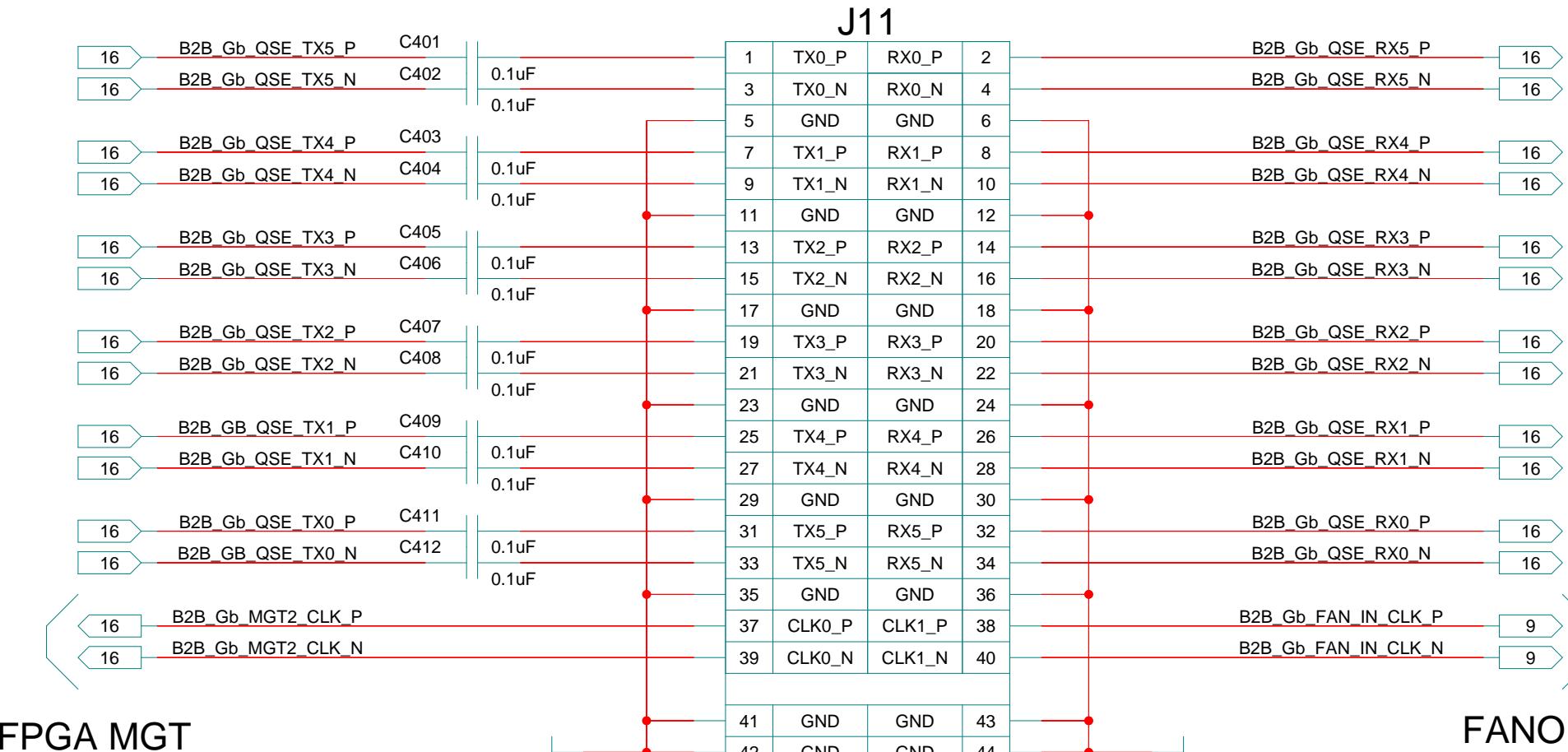
HTG-V7-FMC

DDR3-SODIMM

CONTRACT NO.		HTG-V7-FMC			
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CHECKED		SIZE C	FSCM NO.	DWG. NO.	REV 1.0
ISSUED					
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D

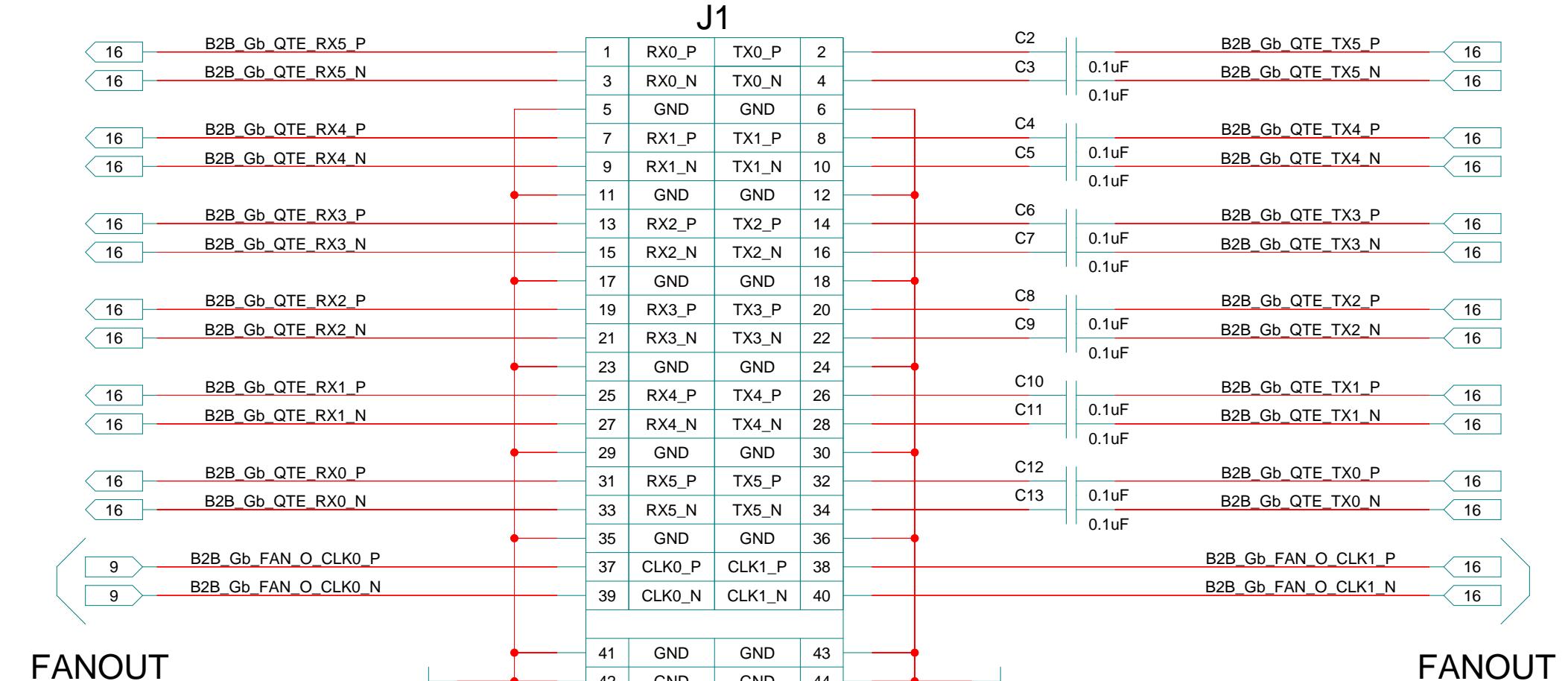
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High Speed Socket, QSE Series  
40 Pins, Pitch 0.8mm  
QSE-020-01-F-D-A  
Samtec

MOUNTED ON BACK SIDE

FANOUT

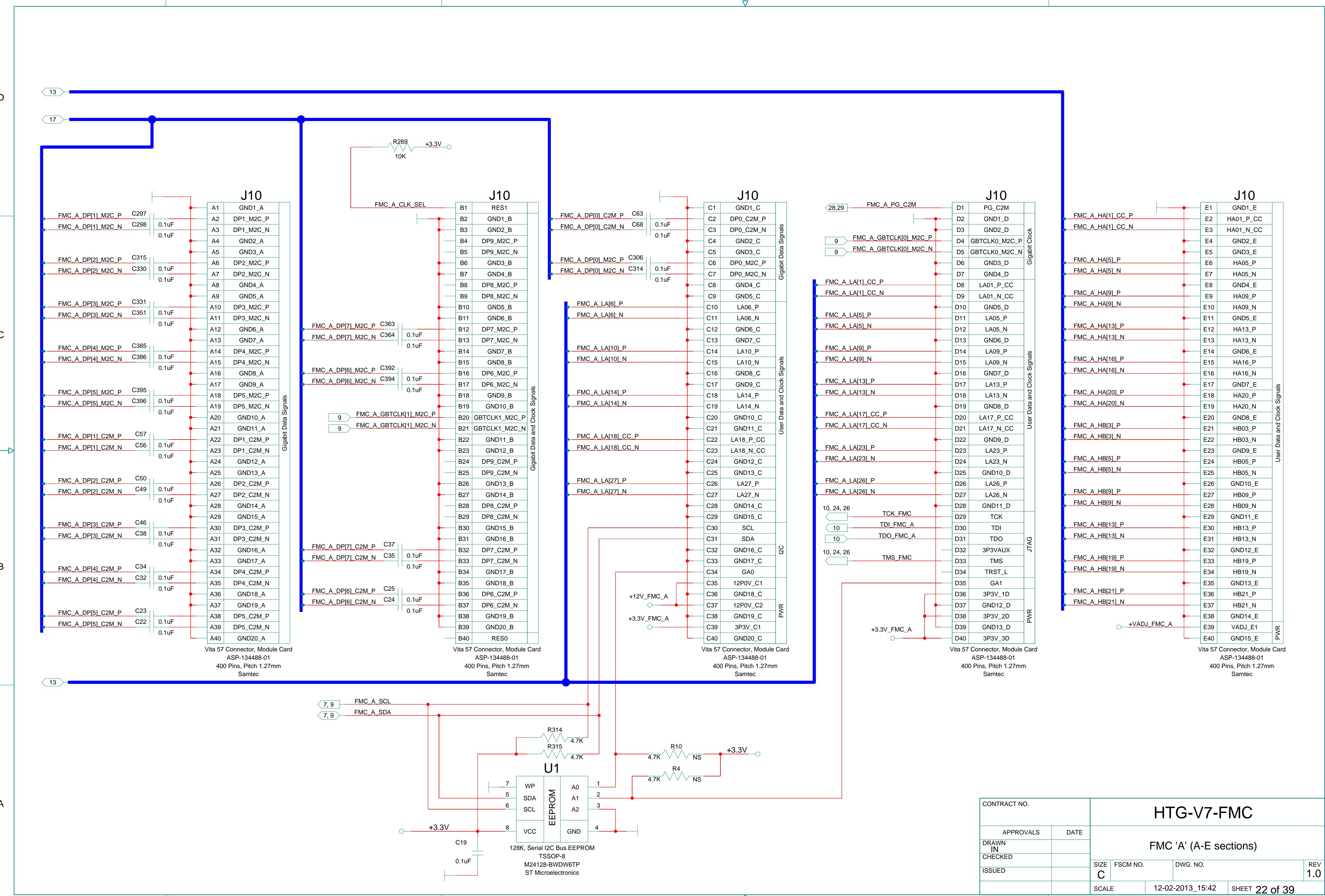


High Speed Header, QTE Series  
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QTE-020-01-F-D-A  
Samtec

MOUNTED ON TOP SIDE

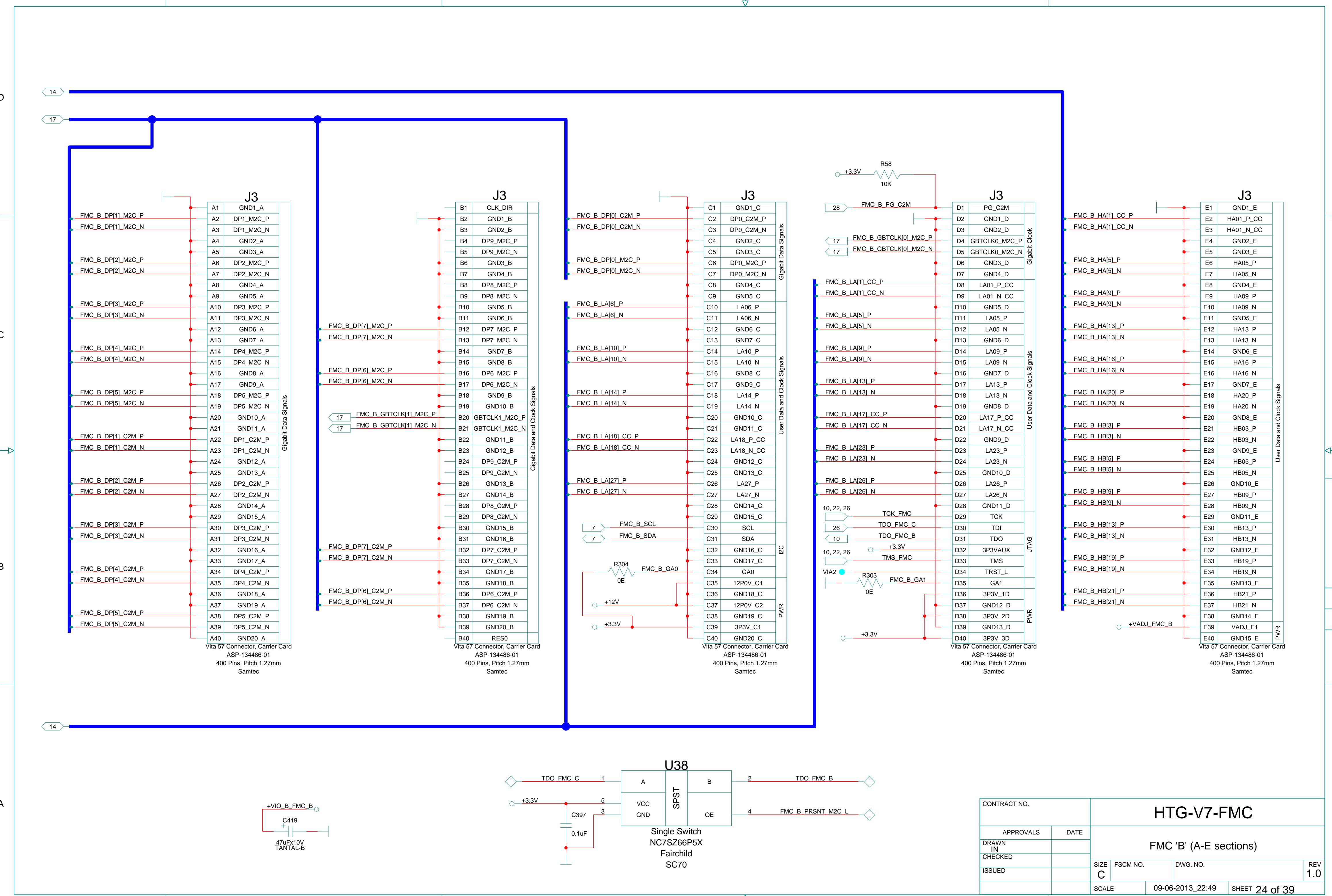
FANOUT

CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	B2B connectors (QSE and QTE)		
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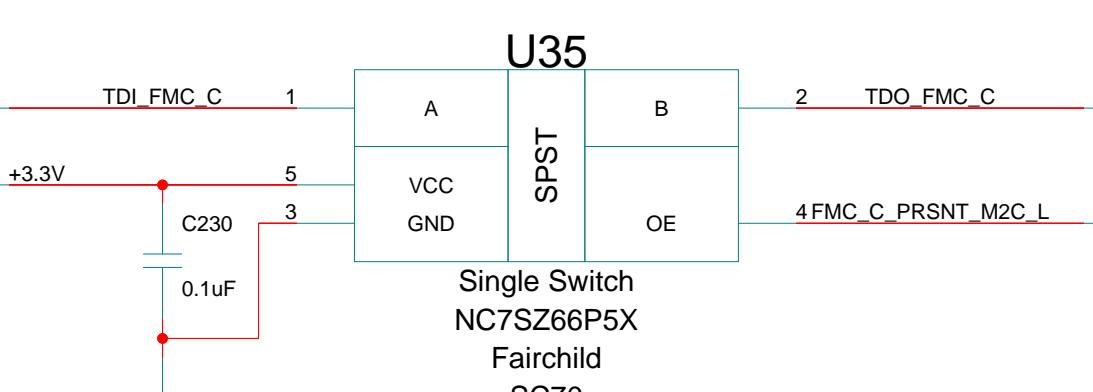
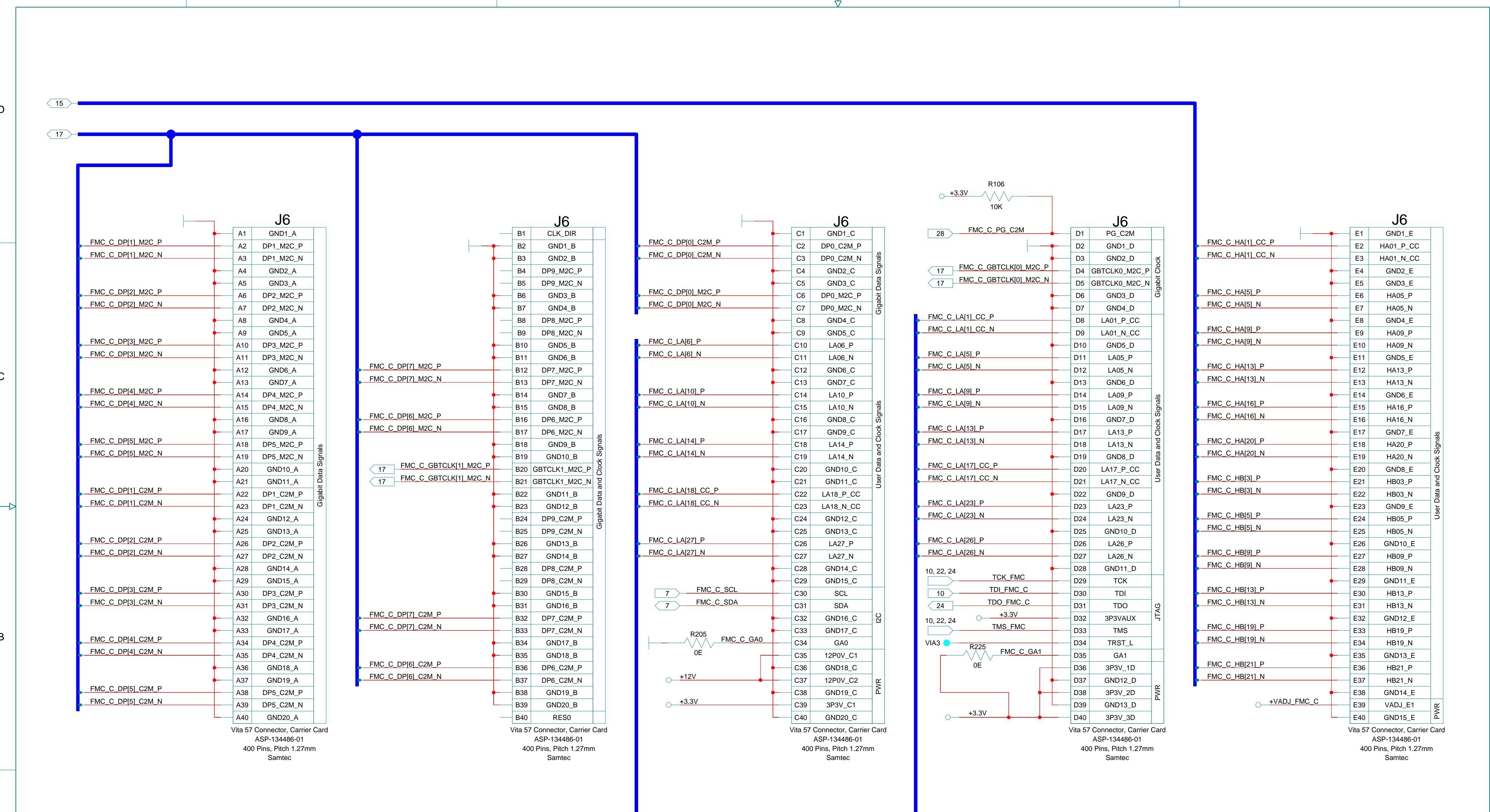


CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	FMC 'A' (F-K sections)		
DRAWN IN CHECKED		SIZE	FSCM NO.	DWG. NO.
ISSUED		C		REV 1.0
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CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	FMC 'B' (F-K sections)		
DRAWN IN CHECKED		SIZE	FSCM NO.	DWG. NO.
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CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	FMC 'C' (A-E sections)		
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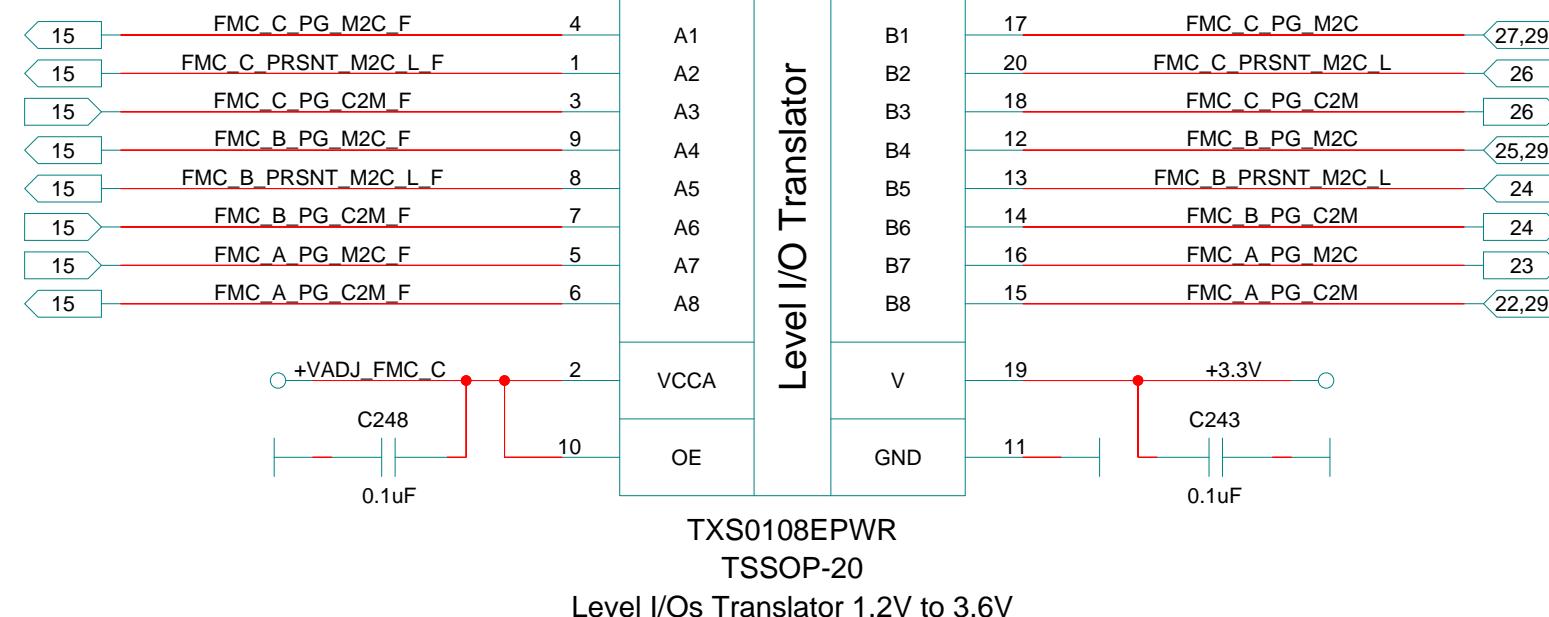


CONTRACT NO.		HTG-V7-FMC		
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D

D

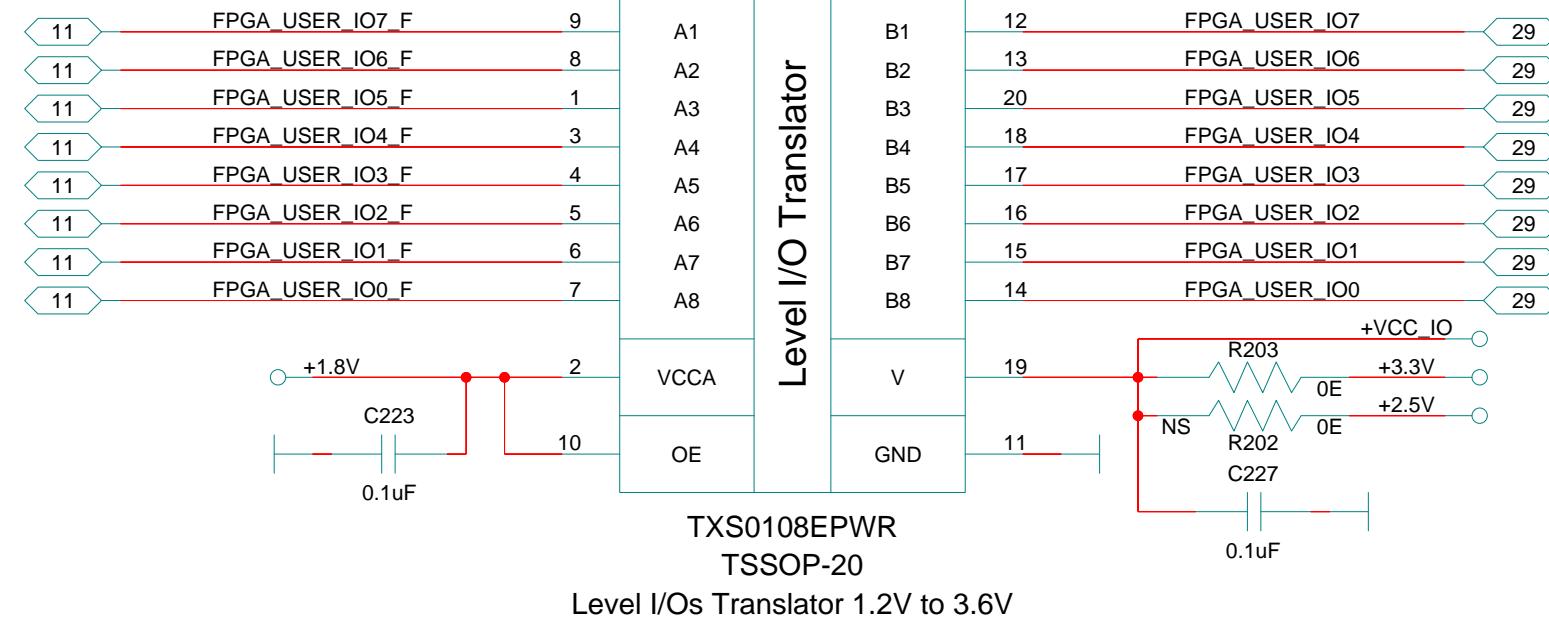
U37



C

C

U34



B

B

CONTRACT NO.

HTG-V7-FMC

APPROVALS

DRAWN

IN

CHECKED

ISSUED

DATE

Level I/O Translators

SIZE

FSCM NO.

DWG. NO.

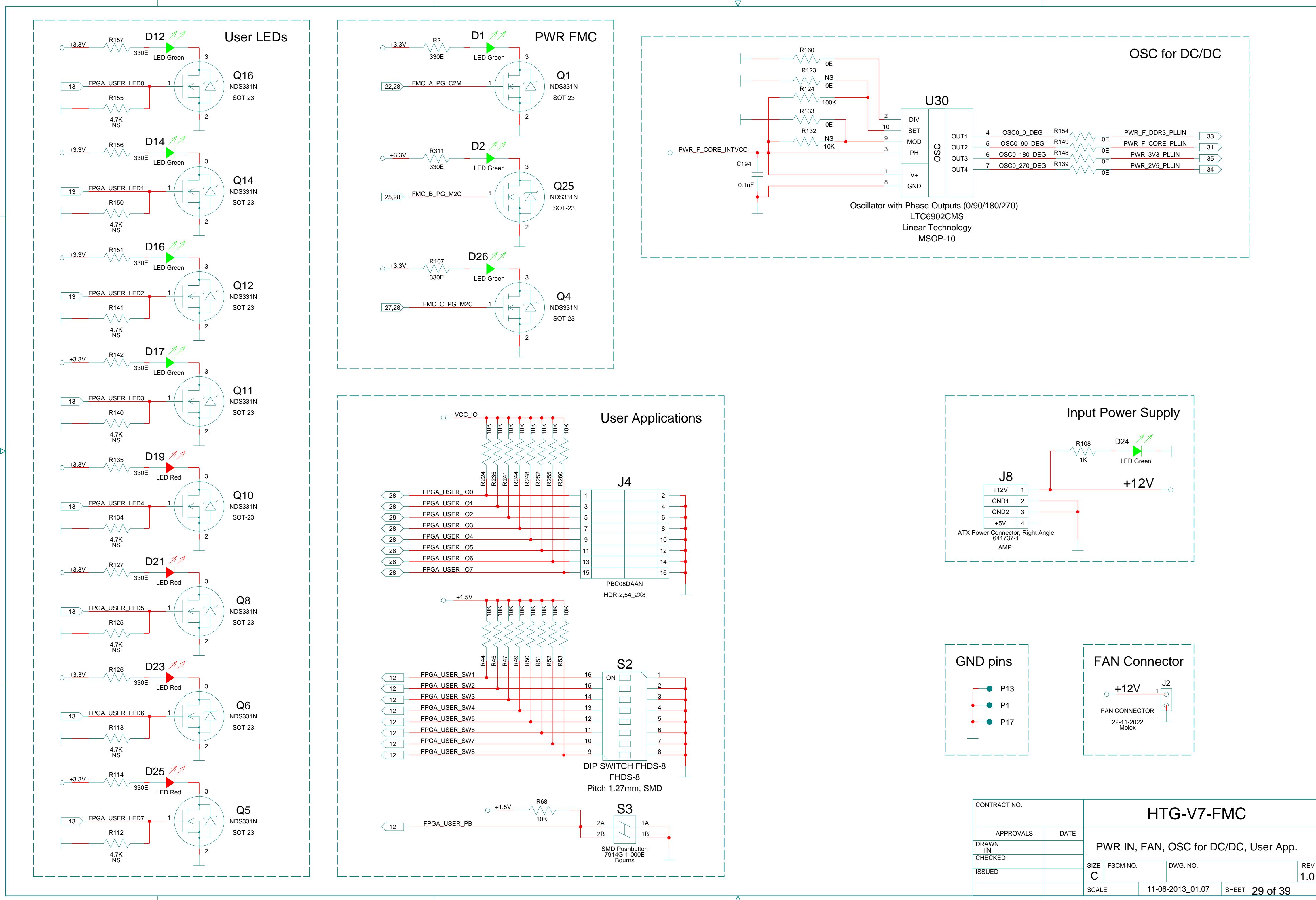
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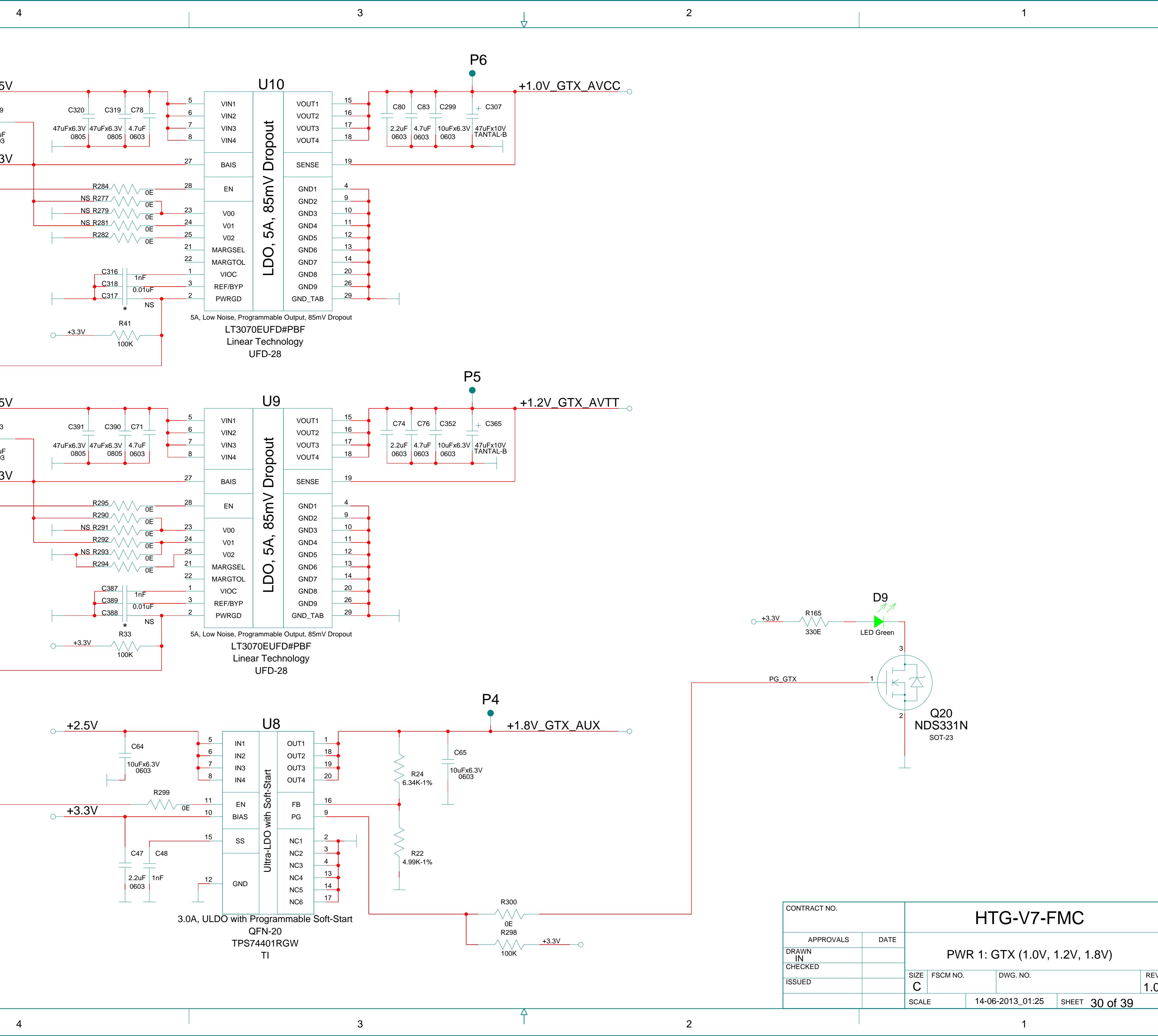
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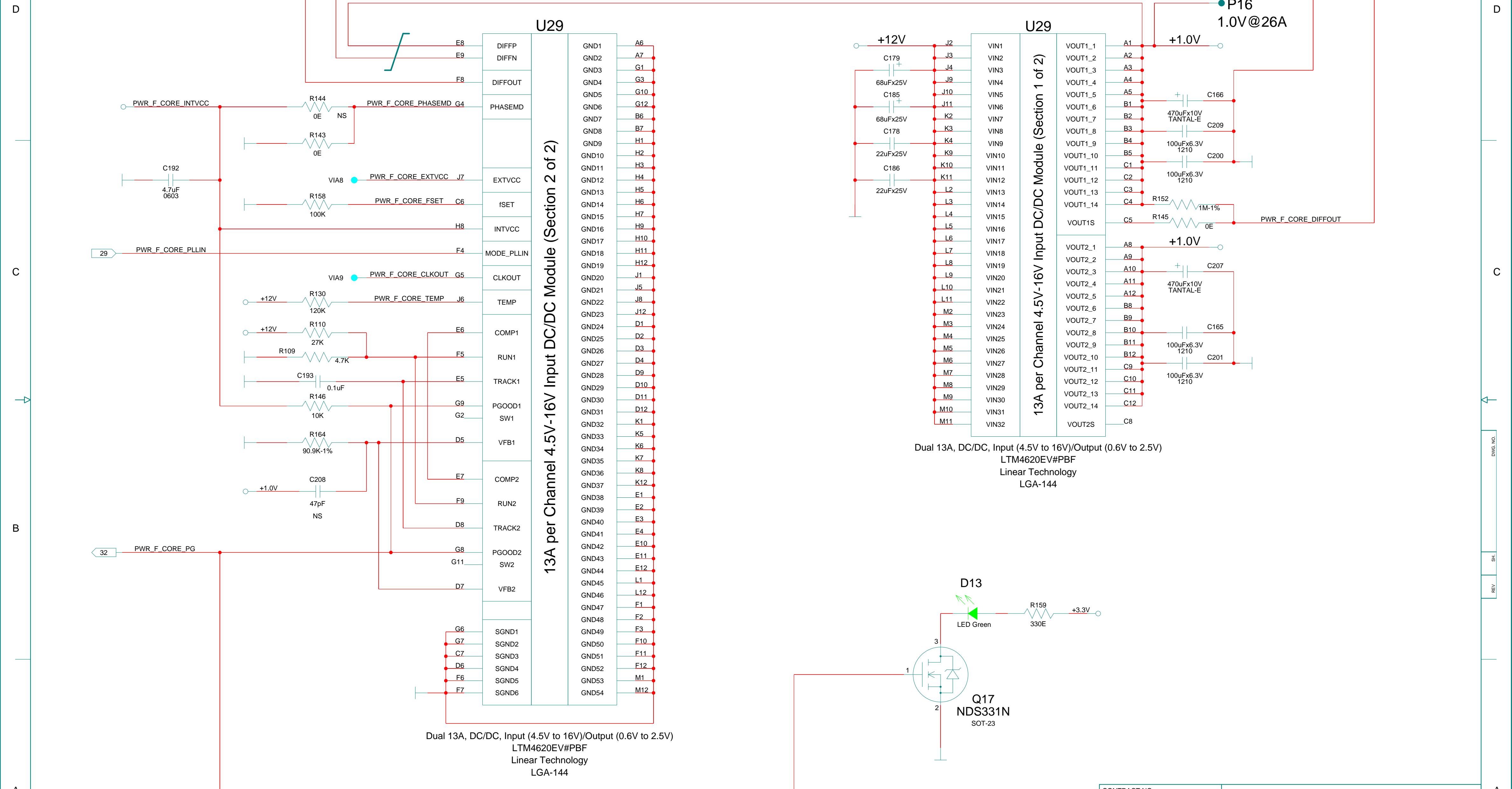
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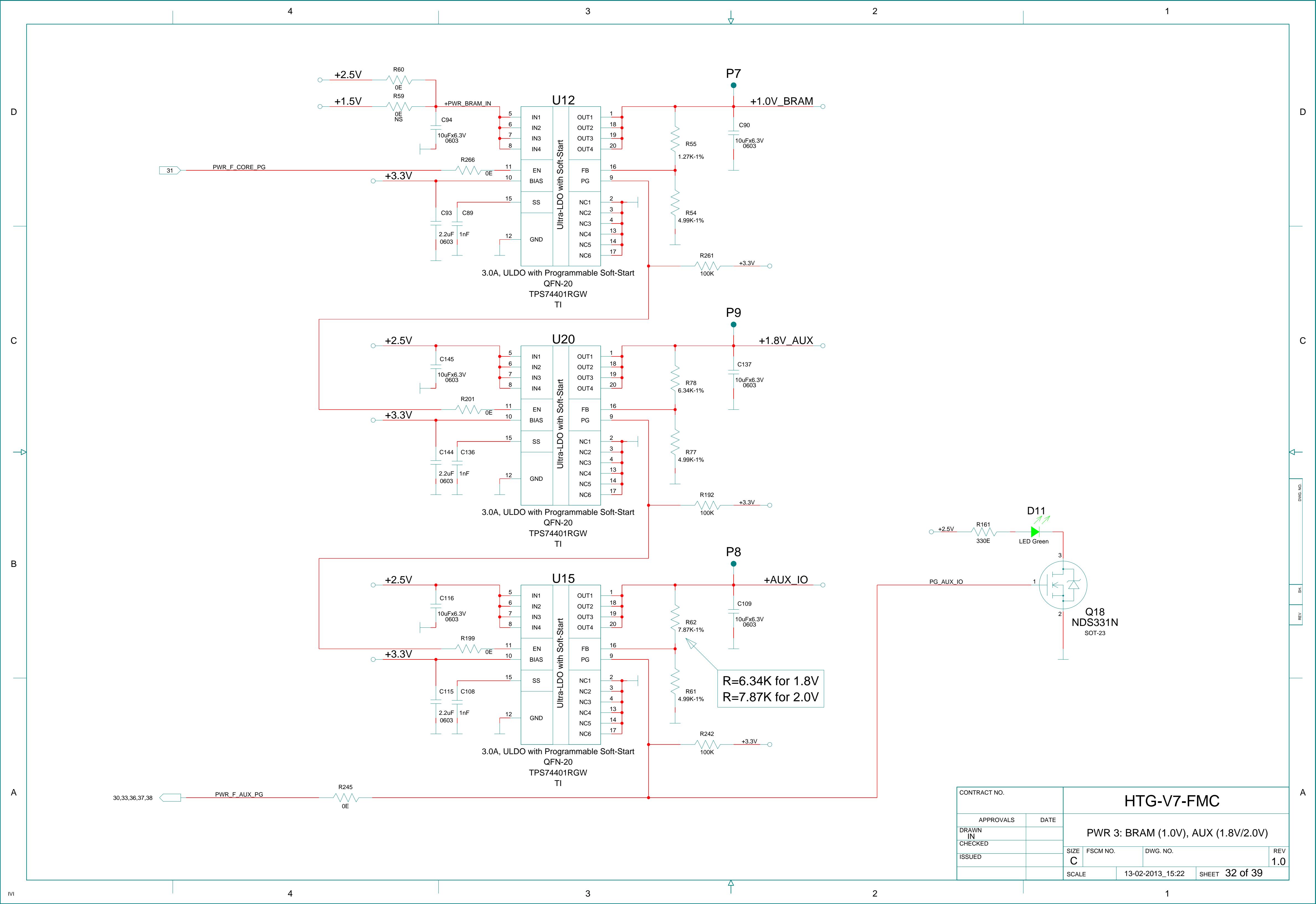
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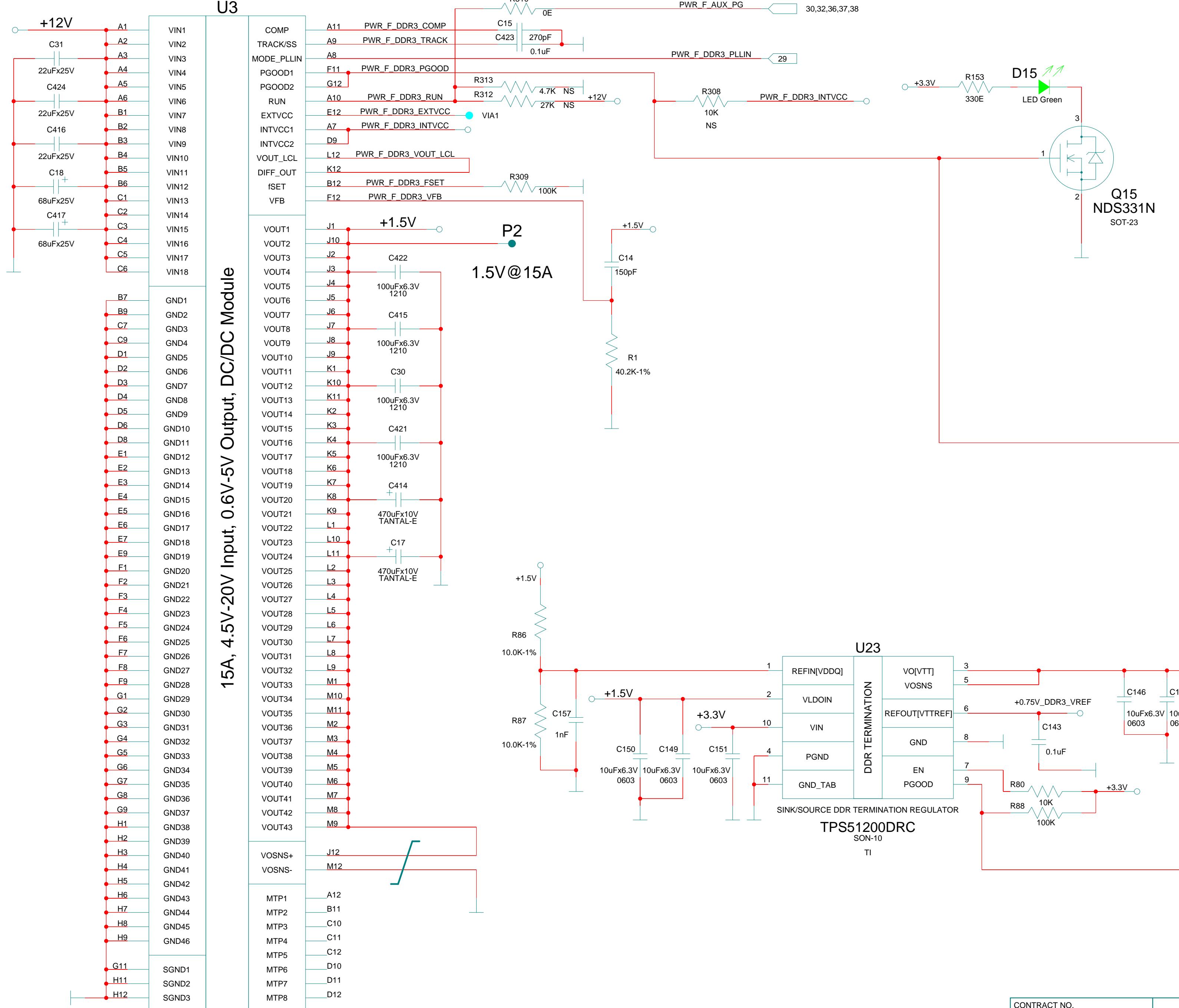






CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	PWR 2: FPGA Core (0.9V/1.0V)		
DRAWN IN	CHECKED	SIZE FSCM NO. DWG. NO. REV		
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SCALE		06-03-2013_16:01	SHEET	31 of 39

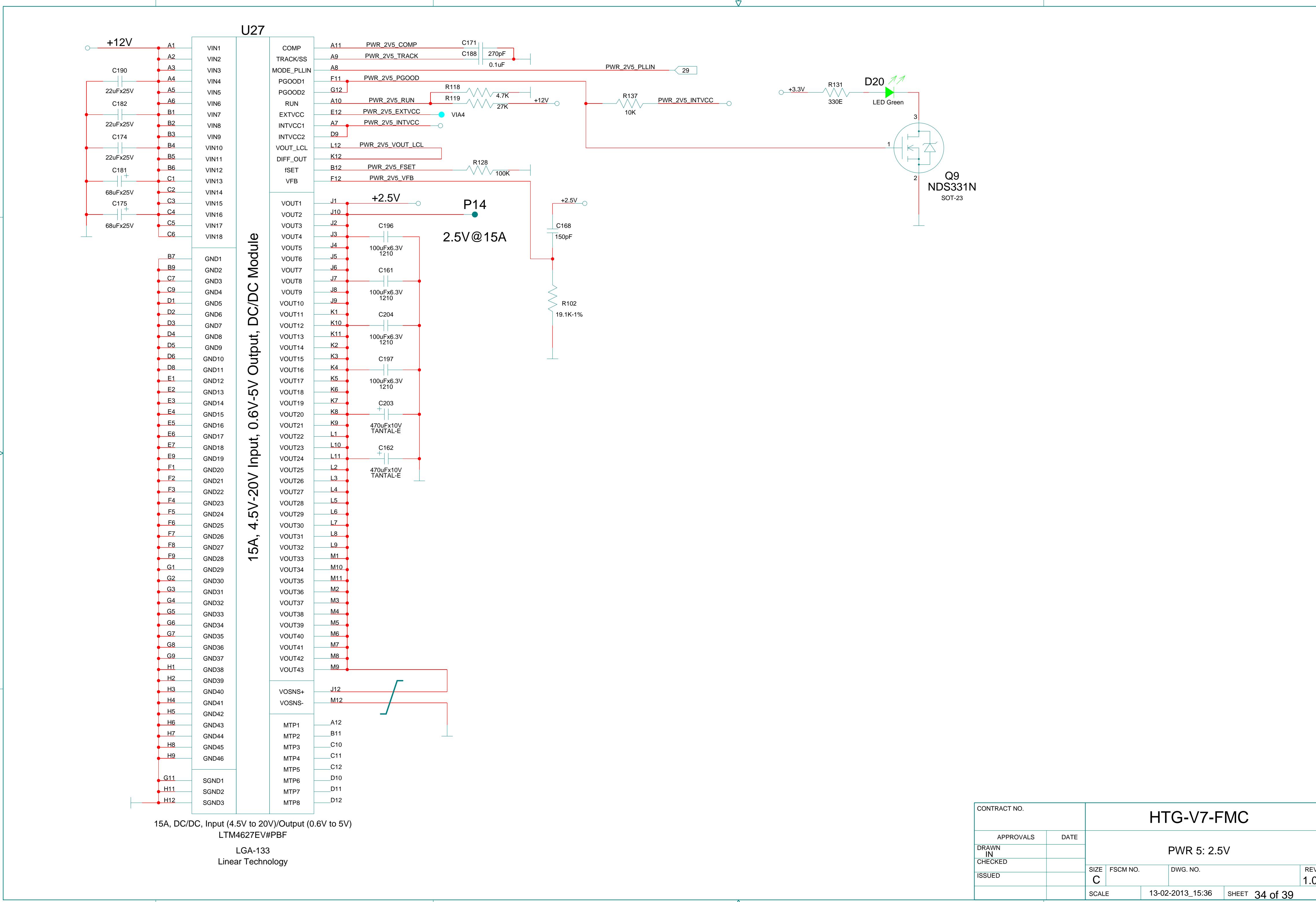


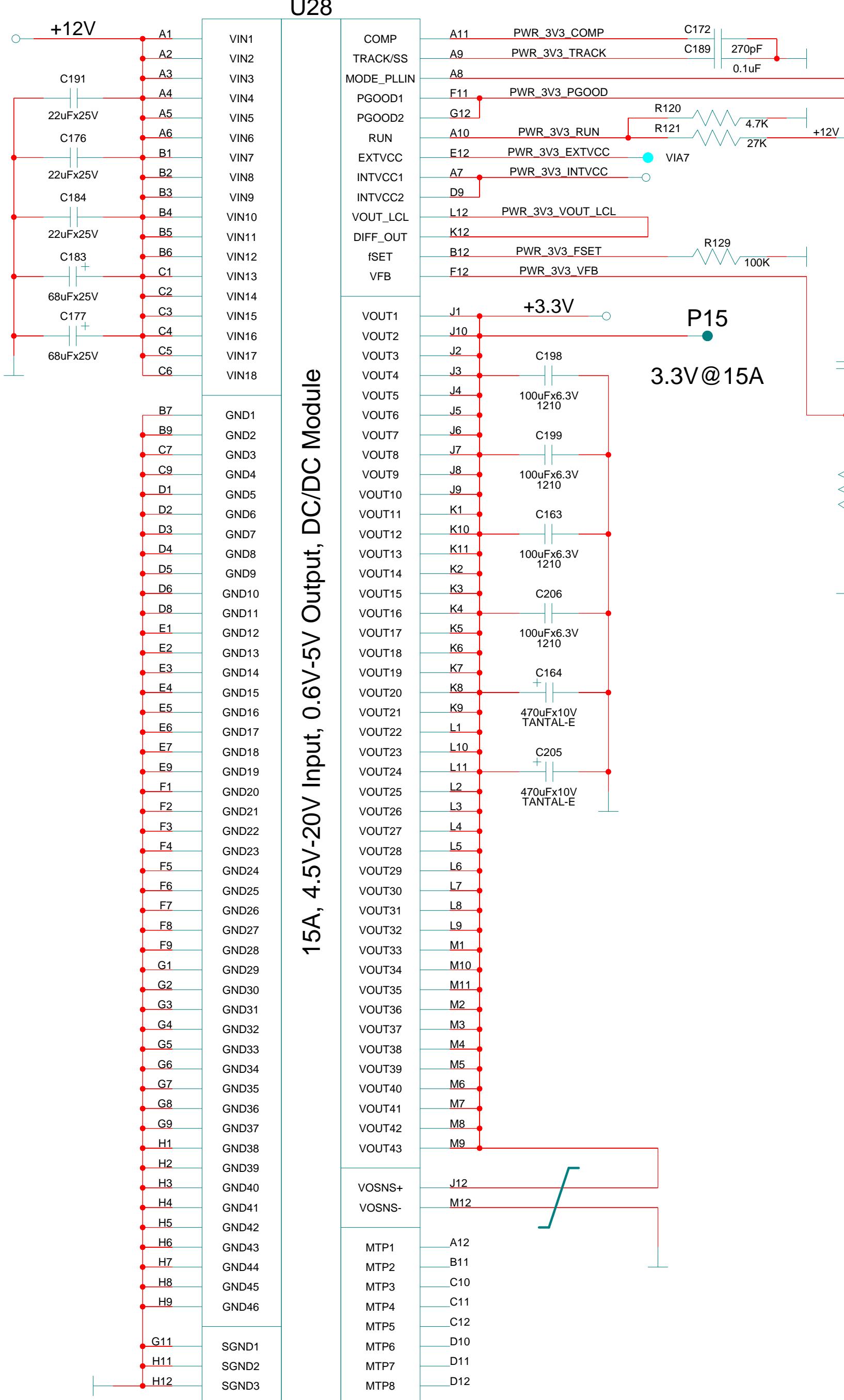


15A, DC/DC, Input (4.5V to 20V)/Output (0.6V to 5V)

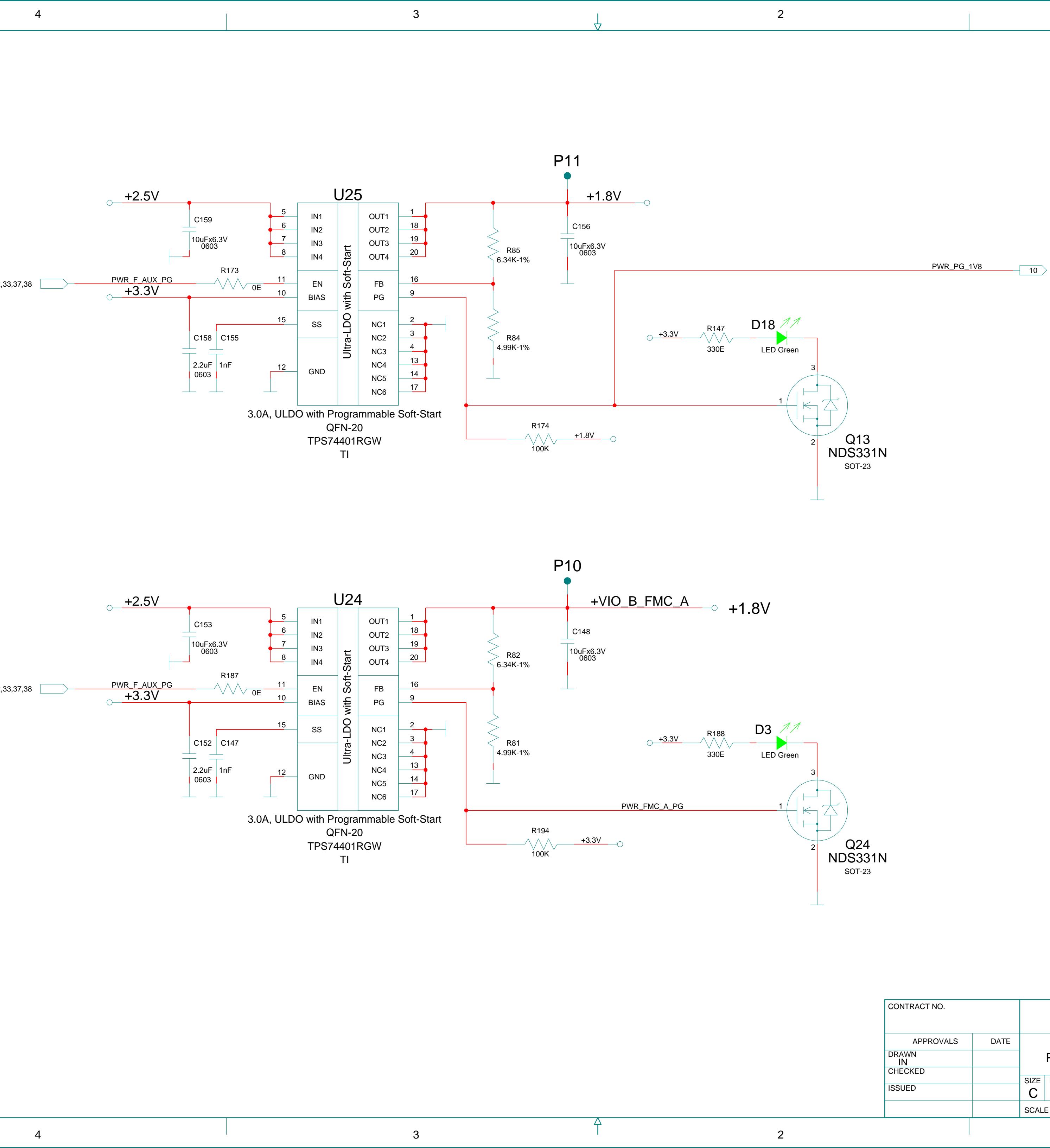
LGA-133  
Linear Technology

CONTRACT NO.		HTG-V7-FMC			
APPROVALS	DATE	PWR 4: 1.5V, DDR3 Termination and Ref			
DRAWN IN					
CHECKED					
ISSUED					
		SIZE <b>C</b>	FSCM NO.	DWG. NO.	REV <b>1.0</b>
		SCALE		13-02-2013_15:36	SHEET <b>33 of 39</b>

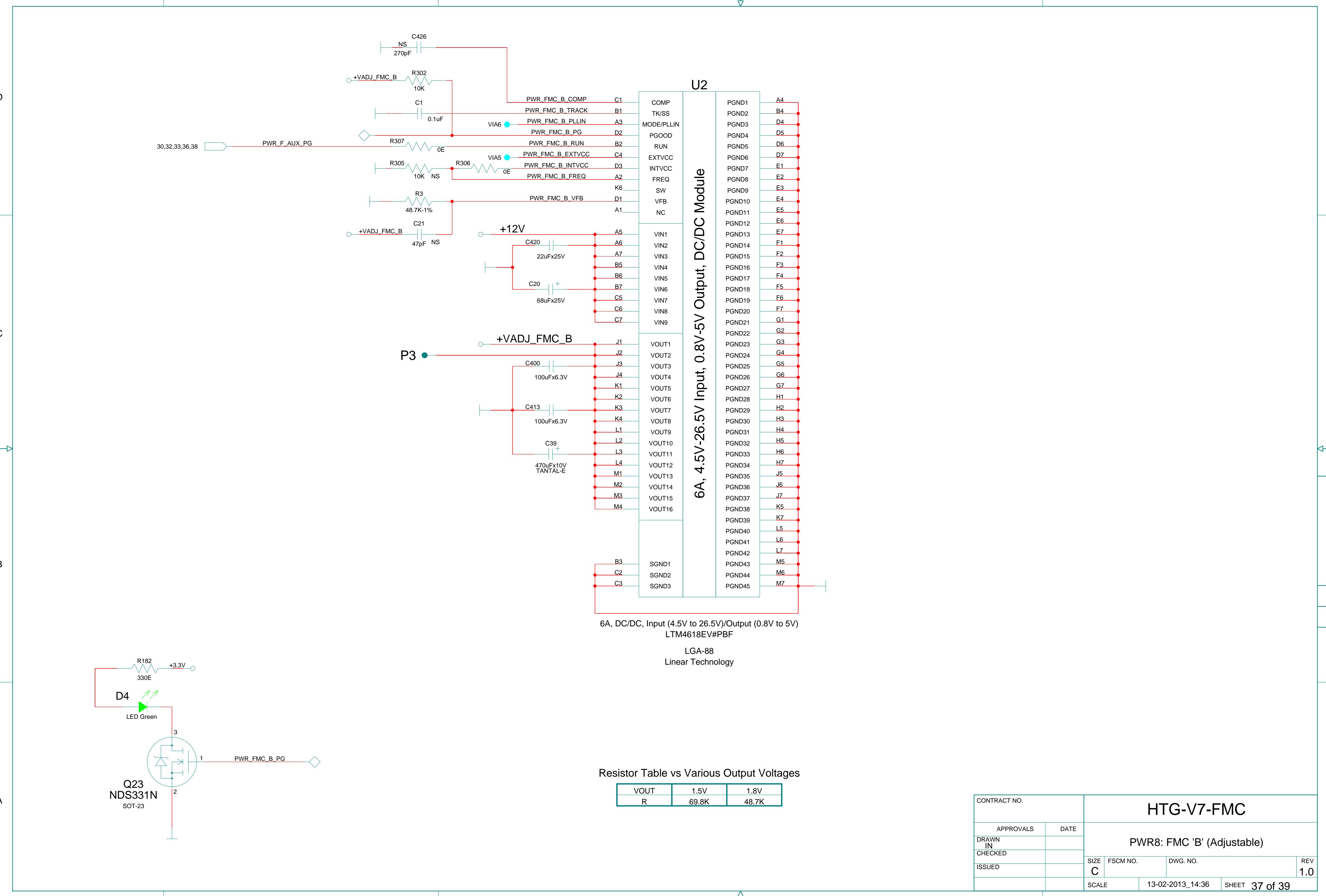


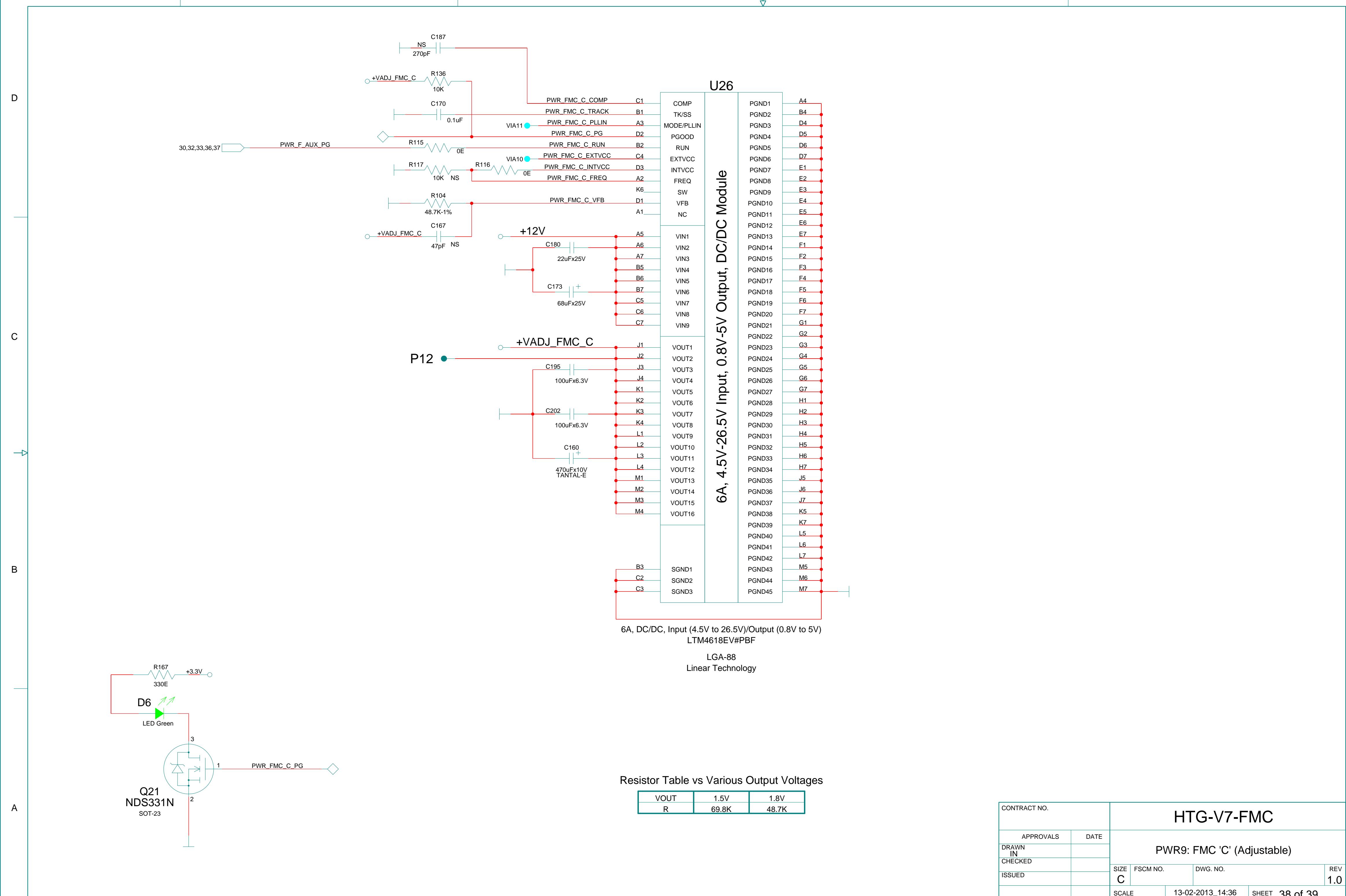


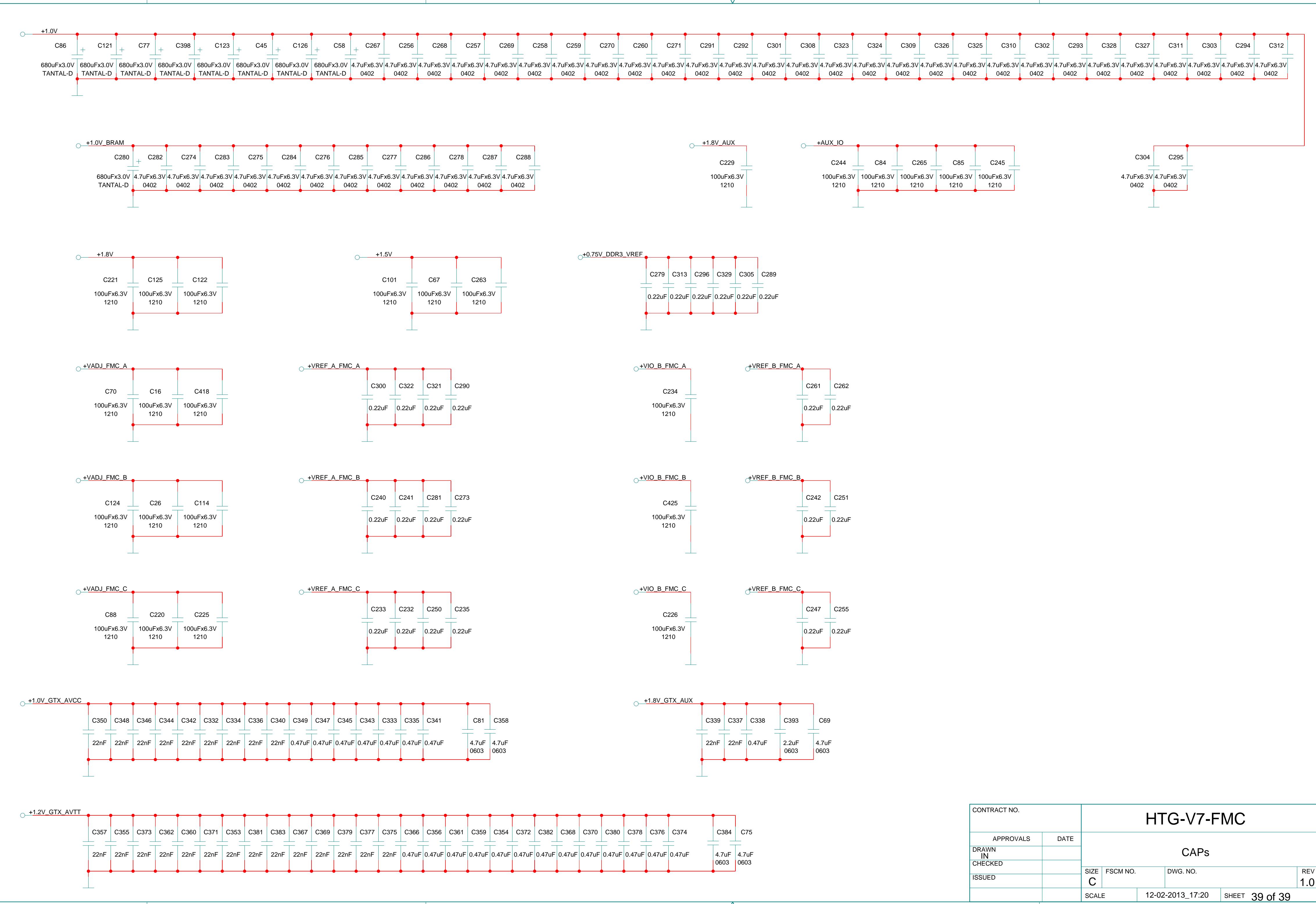
CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	PWR 6: 3.3V		
DRAWN IN	CHECKED			
ISSUED				
		SIZE	FSCM NO.	DWG. NO.
		C		REV 1.0
		SCALE	13-02-2013_15:37	SHEET 35 of 39



CONTRACT NO.		HTG-V7-FMC		
APPROVALS	DATE	PWR 7: FMC 'A' (Adjustable) and 1.8V		
DRAWN IN CHECKED				
ISSUED				
		SIZE	FSCM NO.	DWG. NO.
		C		REV 1.0
		SCALE	13-02-2013_15:25	SHEET 36 of 39







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