HW-V7T-VC7215
VIRTEX-7 FFG1927
MGT CHARACTERIZATION BOARD

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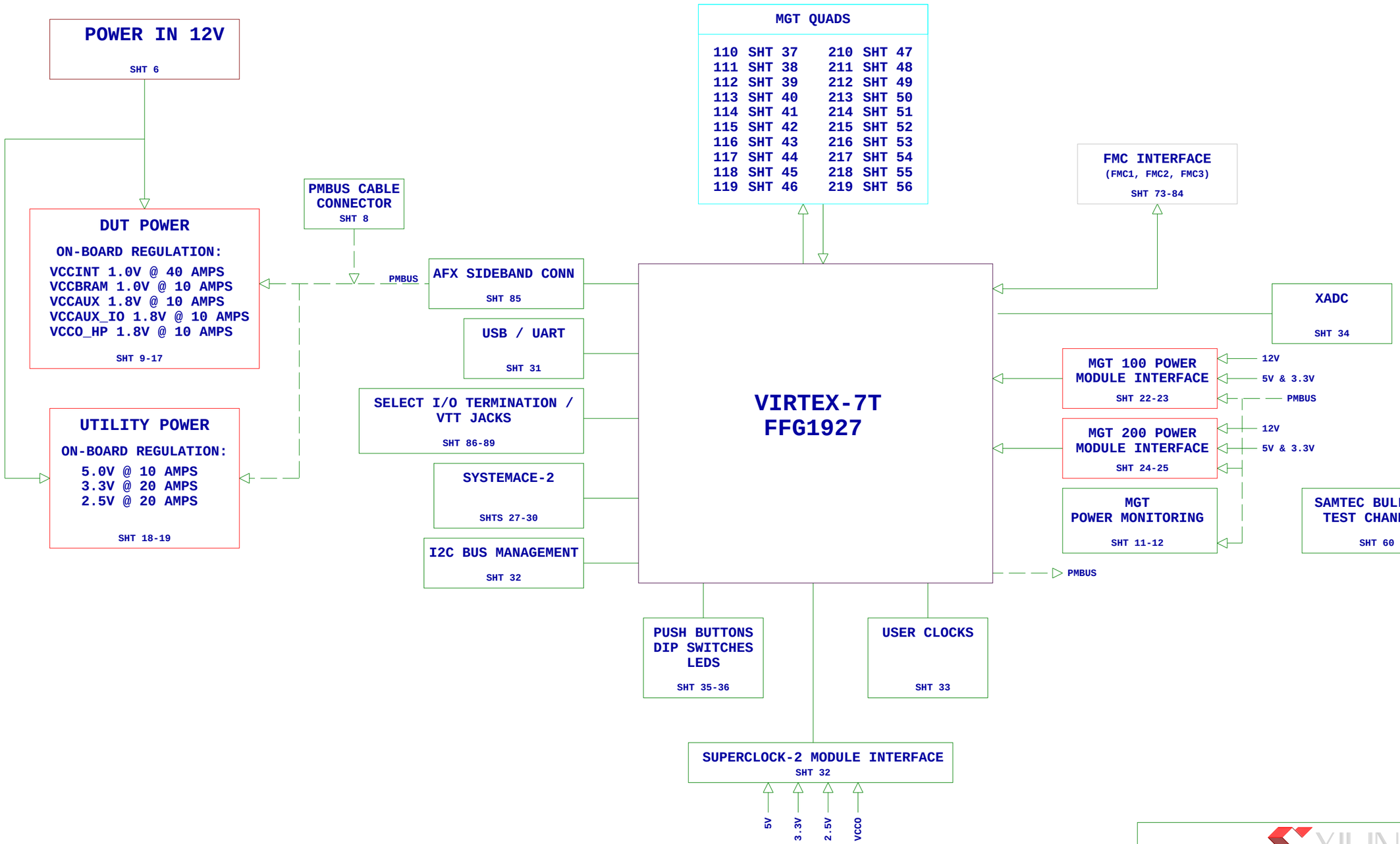
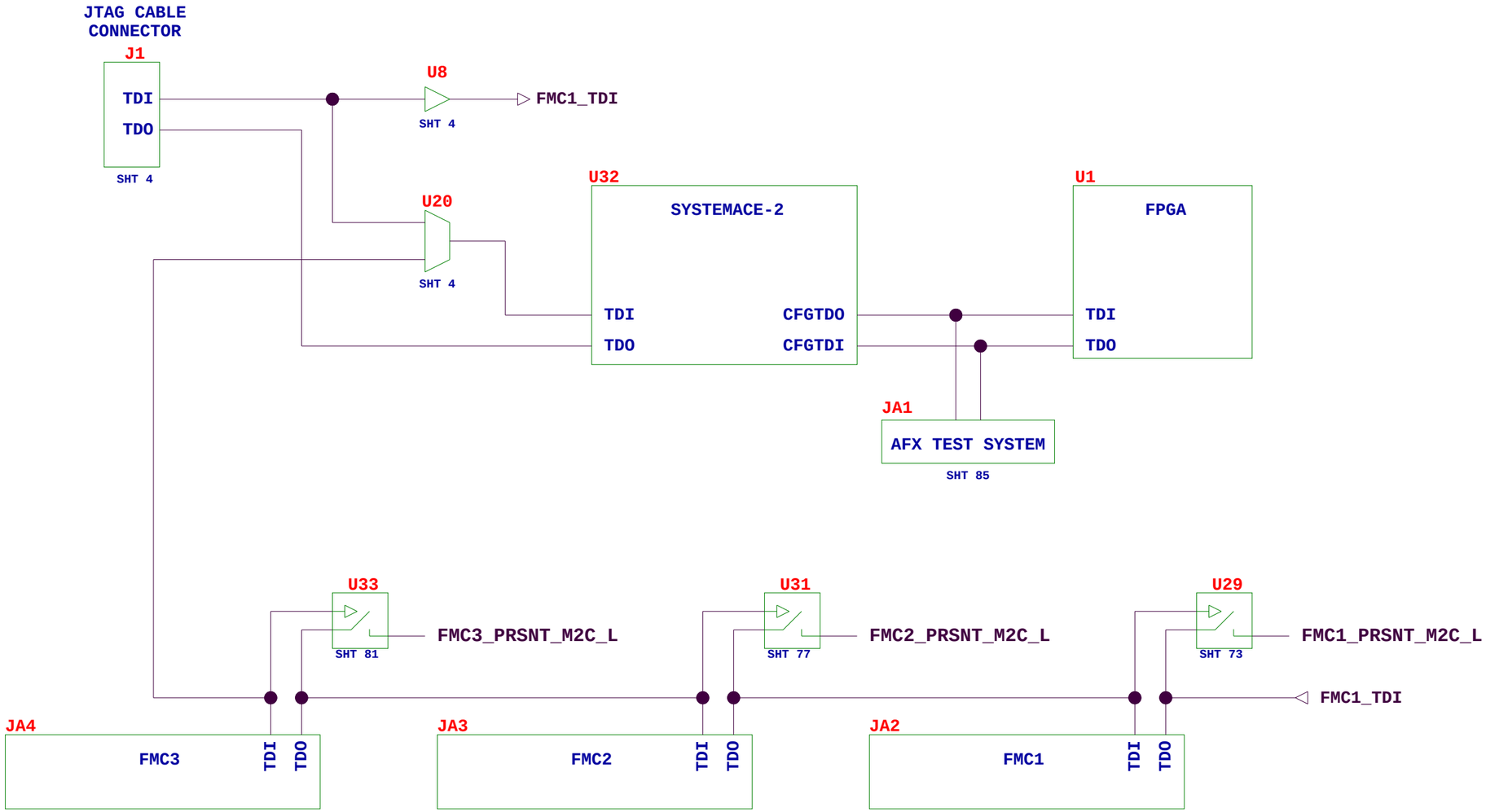
XILINX

Title: COVER SHEET SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 1 of 90	Drawn By RN



Title: BLOCK DIAGRAM SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:01	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 2 of 90	Drawn By RN



XILINX

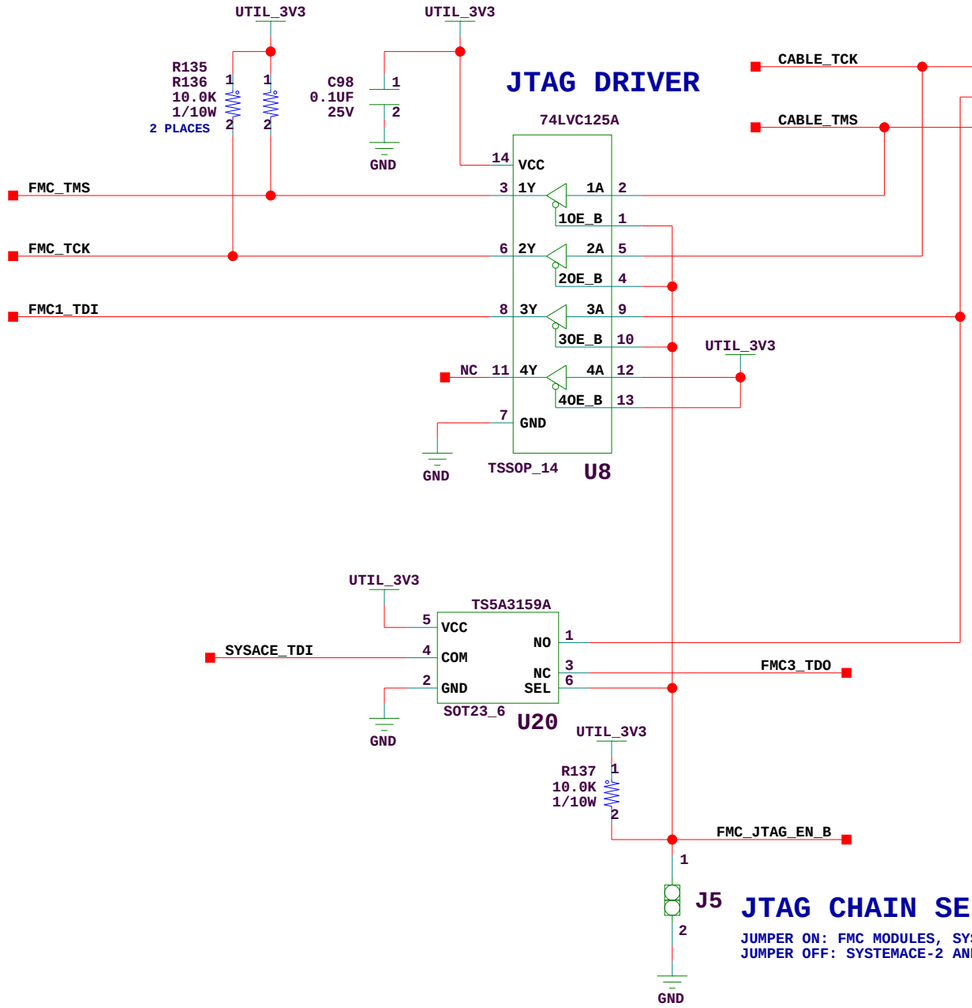
Title: JTAG CHAIN
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 3 of 90	Drawn By RN

EMBEDDED USB TO JTAG INTERFACE / EXTERNAL JTAG HEADER

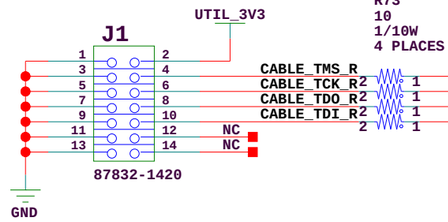
JTAG DRIVER



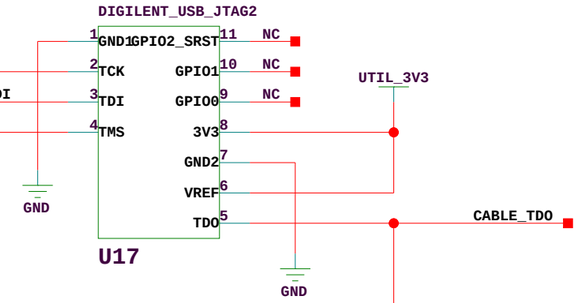
JTAG CHAIN SELECTION

JUMPER ON: FMC MODULES, SYSTEMACE-2 AND FPGA
JUMPER OFF: SYSTEMACE-2 AND FPGA ONLY

JTAG HEADER

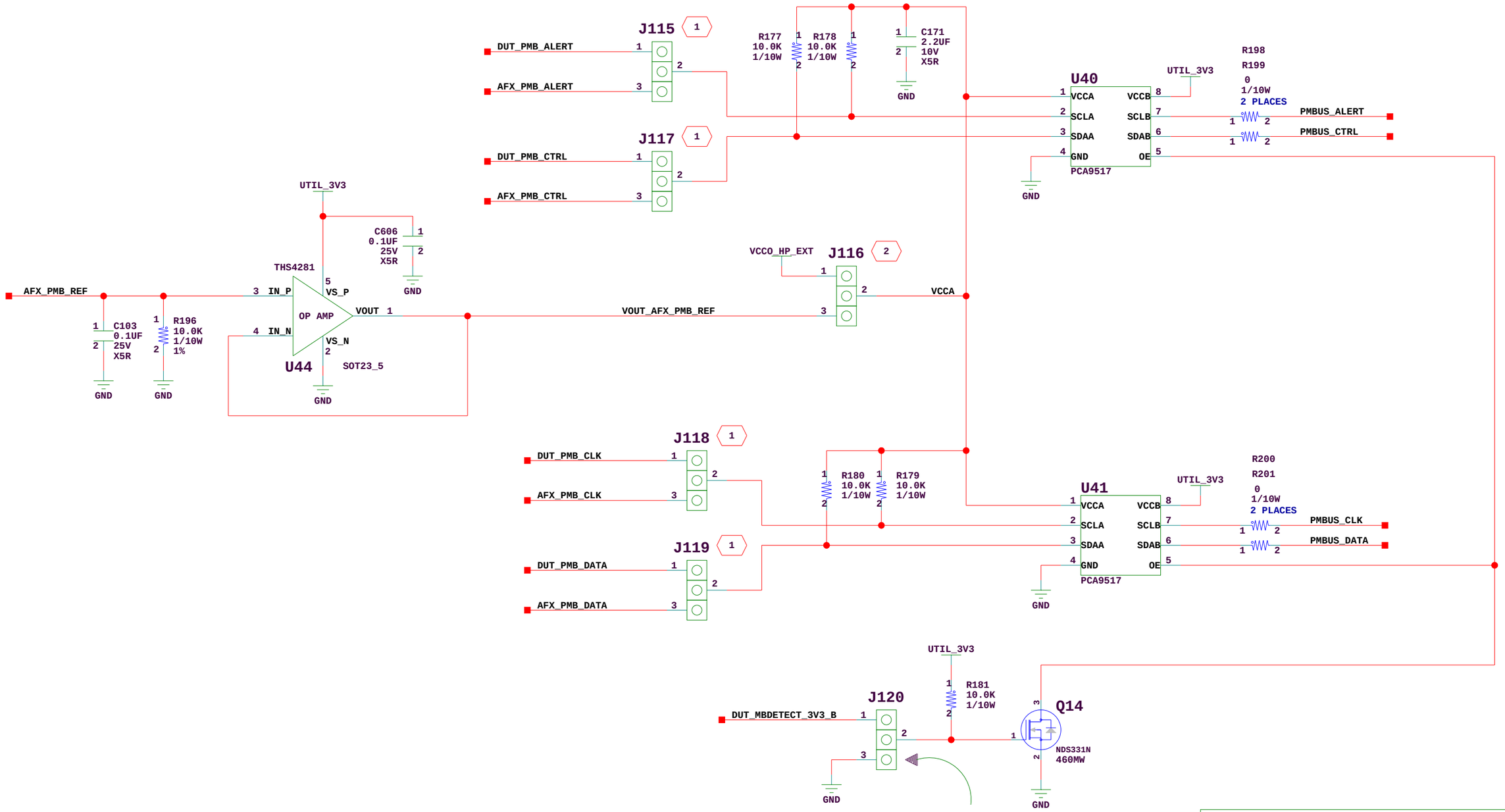


EMBEDDED USB-JTAG MODULE



Title: USB / JTAG CONNECTORS & DRIVERS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 4	of 90	Drawn By RN	

PMBUS LEVEL TRANSLATION



PMBUS MASTER SELECT #1

POS 1-2: AFX OR CABLE
POS 2-3: AFX (MANUAL) OR DUT

1 **PMBUS MASTER SELECT #2**

POS 1-2:DUT IS PMBUS MASTER
POS 2-3:AFX IS PMBUS MASTER

2 **VOLTAGE TRANSLATOR REF VOLTAGE SELECT**

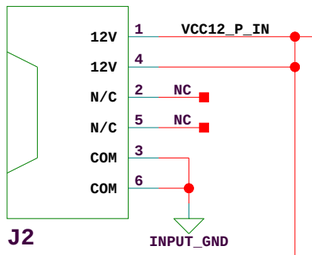
POS 1-2: REFERENCED TO AFX
POS 2-3: REFERENCED TO VCCO

XILINX

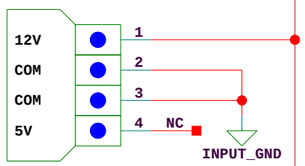
Title: PMBUS LEVEL TRANSLATION SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 5 of 90	Drawn By RN

INPUT POWER CONNECTORS / POWER SUPERVISORY

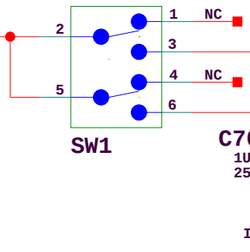
6-PIN MINI-FIT AC ADAPTER (BRICK)



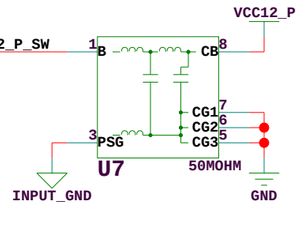
ATX 4-PIN MINI-FIT



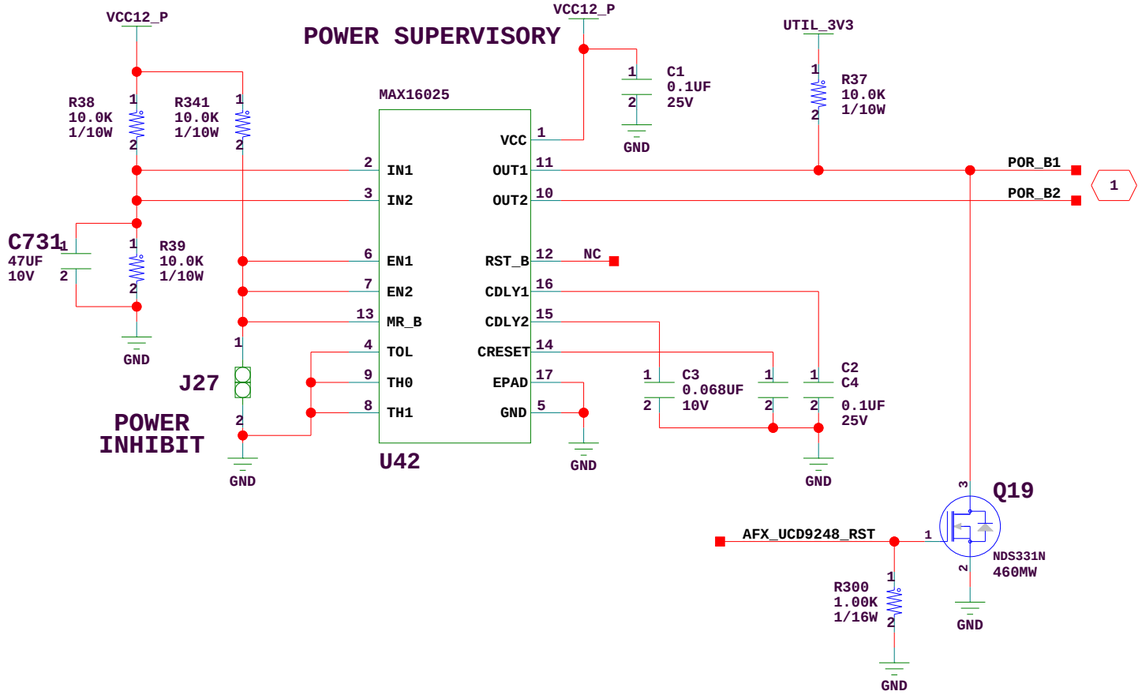
POWER-ON SLIDE SWITCH



NOISE SUPPRESSION FILTER

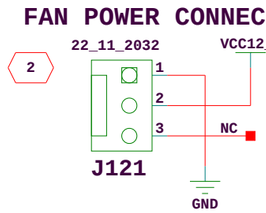


POWER SUPERVISORY



FPGA INPUT POWER (EURO-MAG)

FAN POWER CONNECTOR

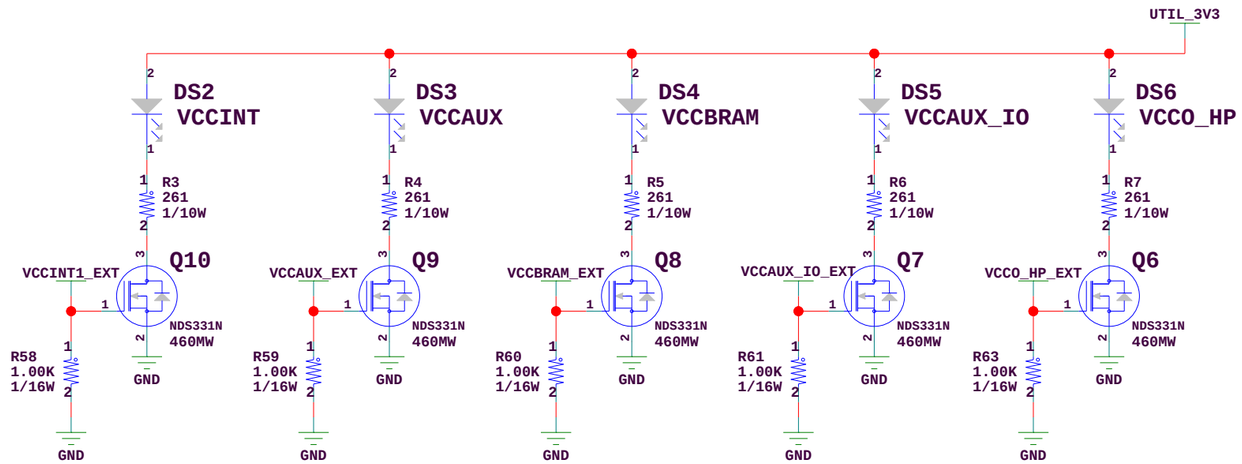


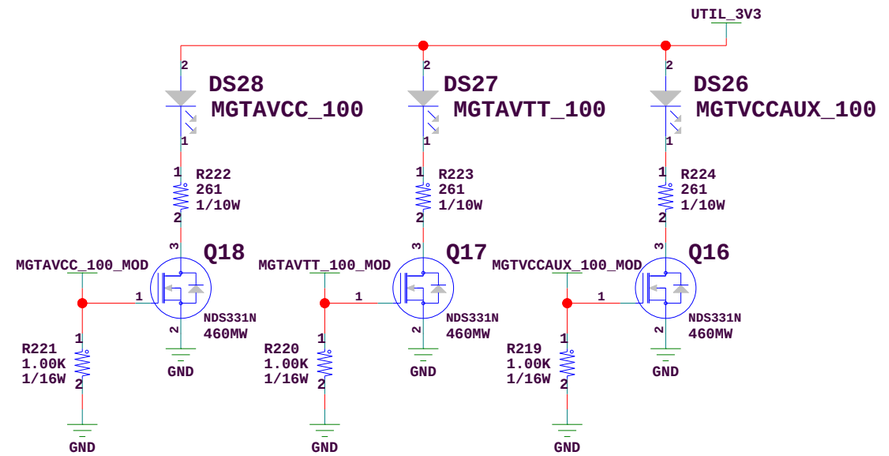
1. POR_B1 USED BY UCD9248 POWER CONTROLLERS AND REGULATORS
   POR_B2 USED BY UTILITY REGULATORS (VCC5V0, VCC3V3, VCC2V5)
2. PLACE FAN POWER CONNECTOR WITHIN 9-INCHES OF DUT

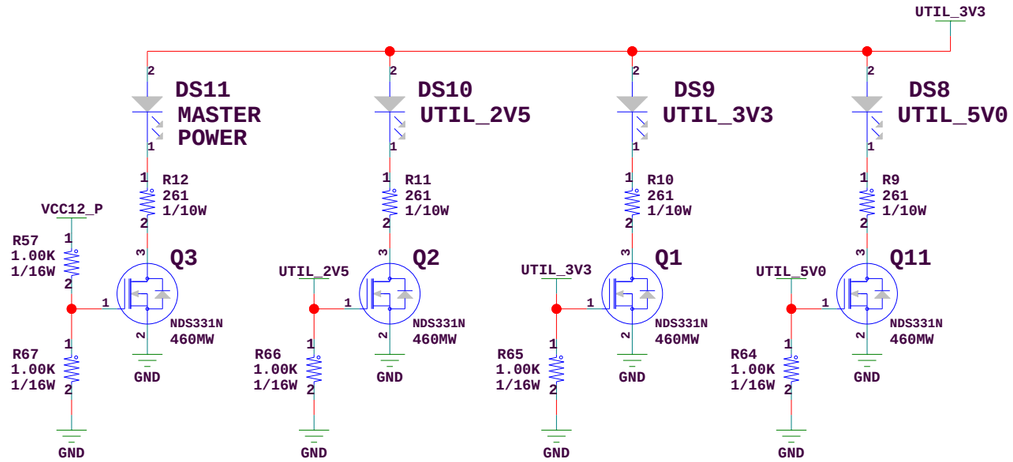
XILINX

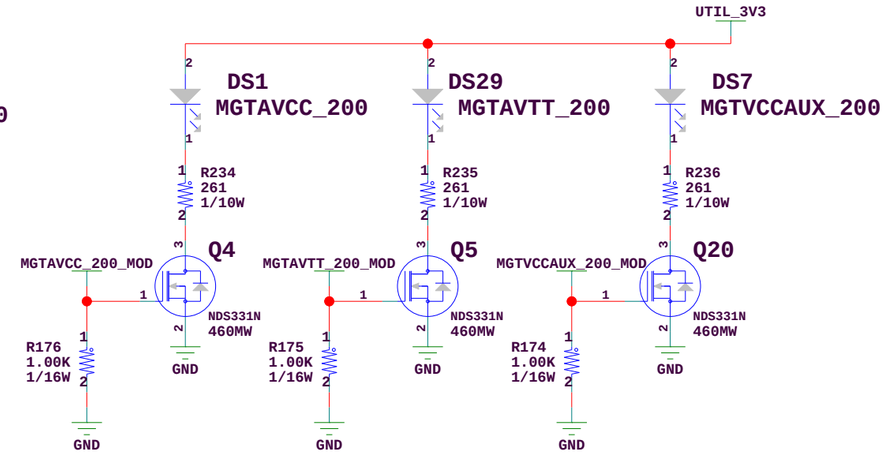
Title: 12V MAIN POWER IN SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 6 of 90	Drawn By RN

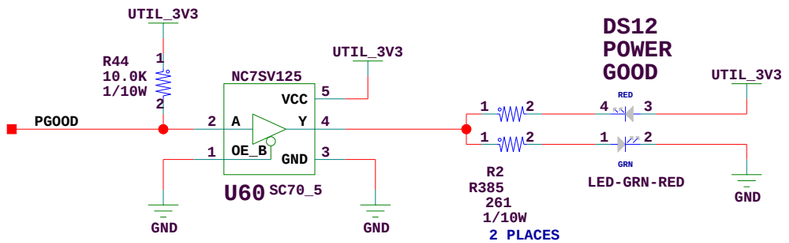
POWER STATUS LEDS







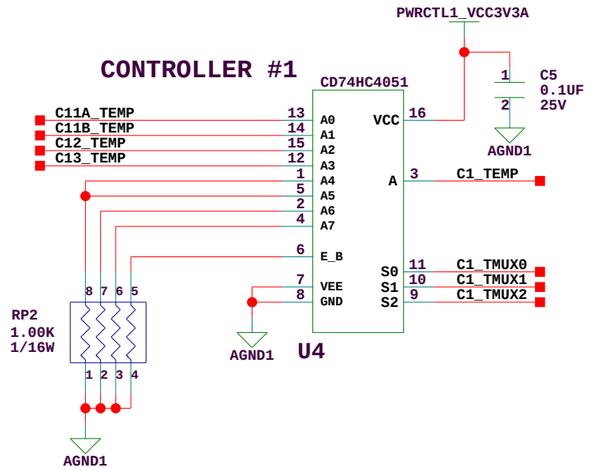


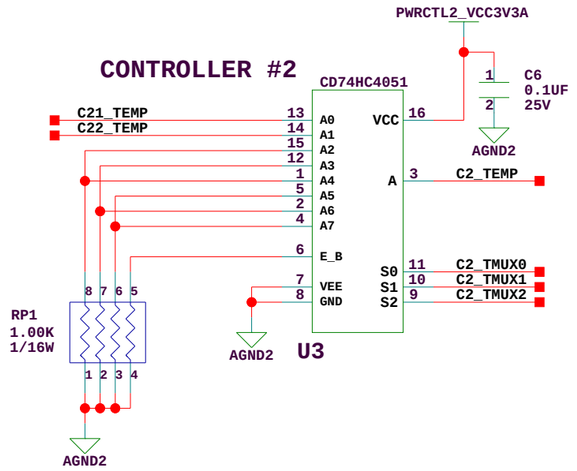


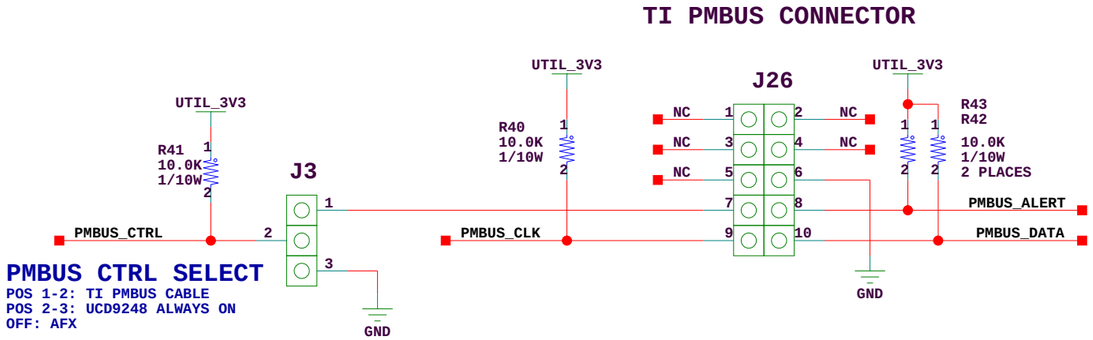
XILINX

Title: POWER STATUS LEDS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 7 of 90		Drawn By RN	

TEMPERATURE SENSOR MULTIPLEXERS / TI PMBUS CONNECTOR



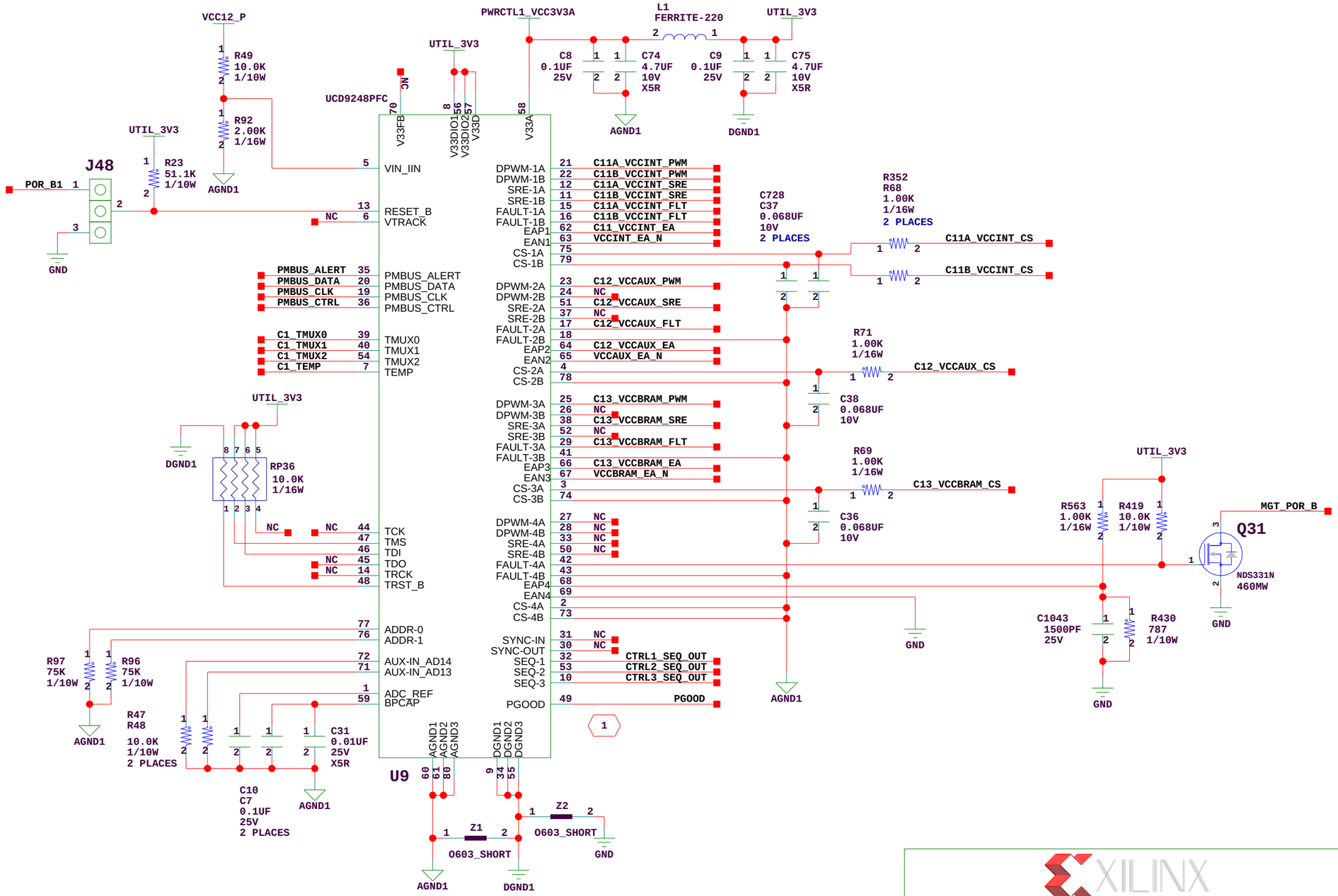




Title: TEMP SENSOR MUX / TI PMBUS CONNECTOR SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 8 of 90	Drawn By RN

PWM SYSTEM CONTROLLER #1

PMBUS ADDRESS	
HEX	DECIMAL
0x34	52



1 ALL PGOOD OUTPUTS WILL BE OPEN-DRAIN AND WIRE-ORED

XILINX

Title: PWM SYSTEM CONTROLLER #1 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
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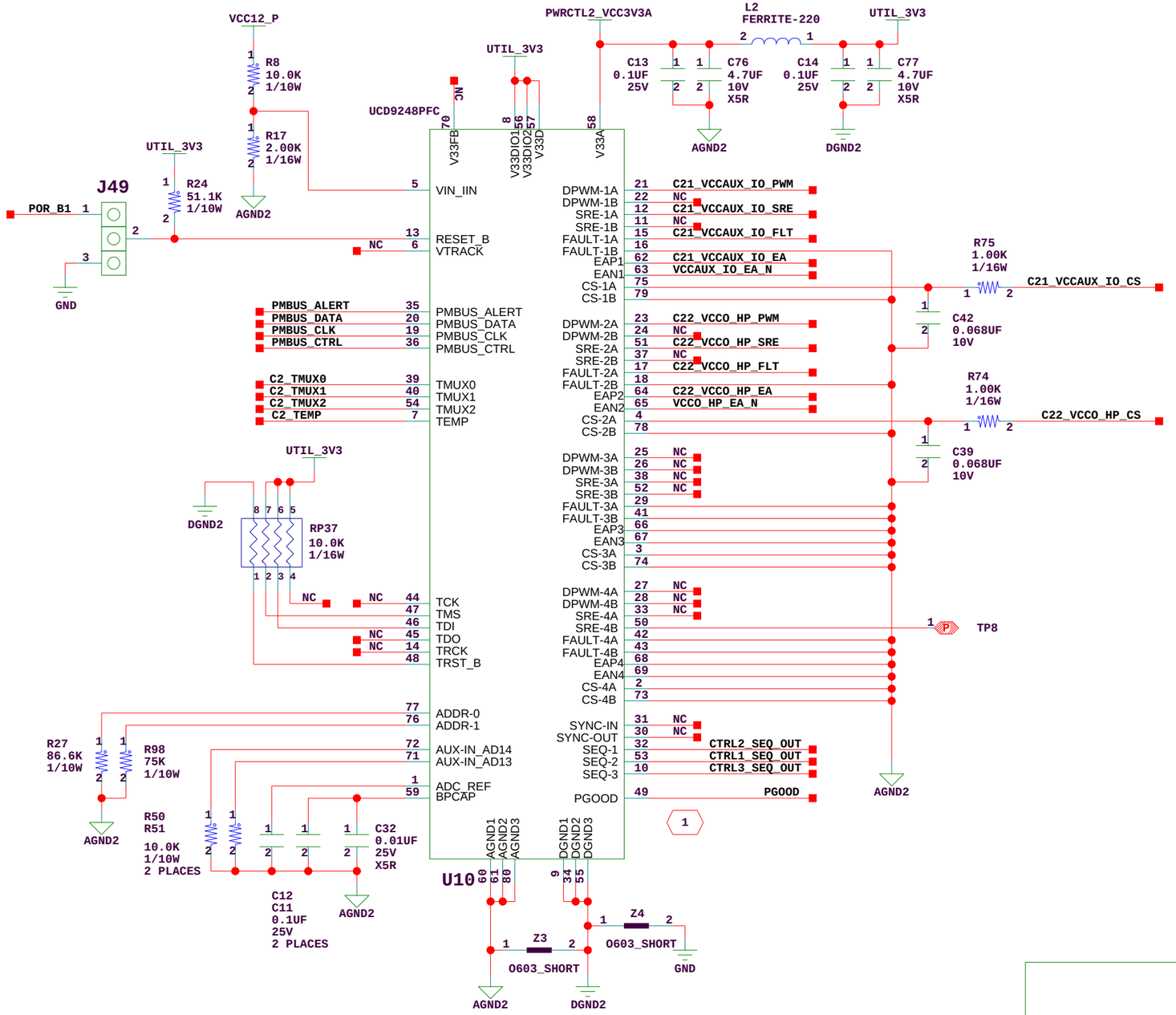
PWM SYSTEM CONTROLLER #2

PMBUS ADDRESS	
HEX	DECIMAL
0x35	53



1 ALL PGOOD OUTPUTS WILL BE OPEN-DRAIN AND WIRE-ORED

XILINX

Title: PWM SYSTEM CONTROLLER #2 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
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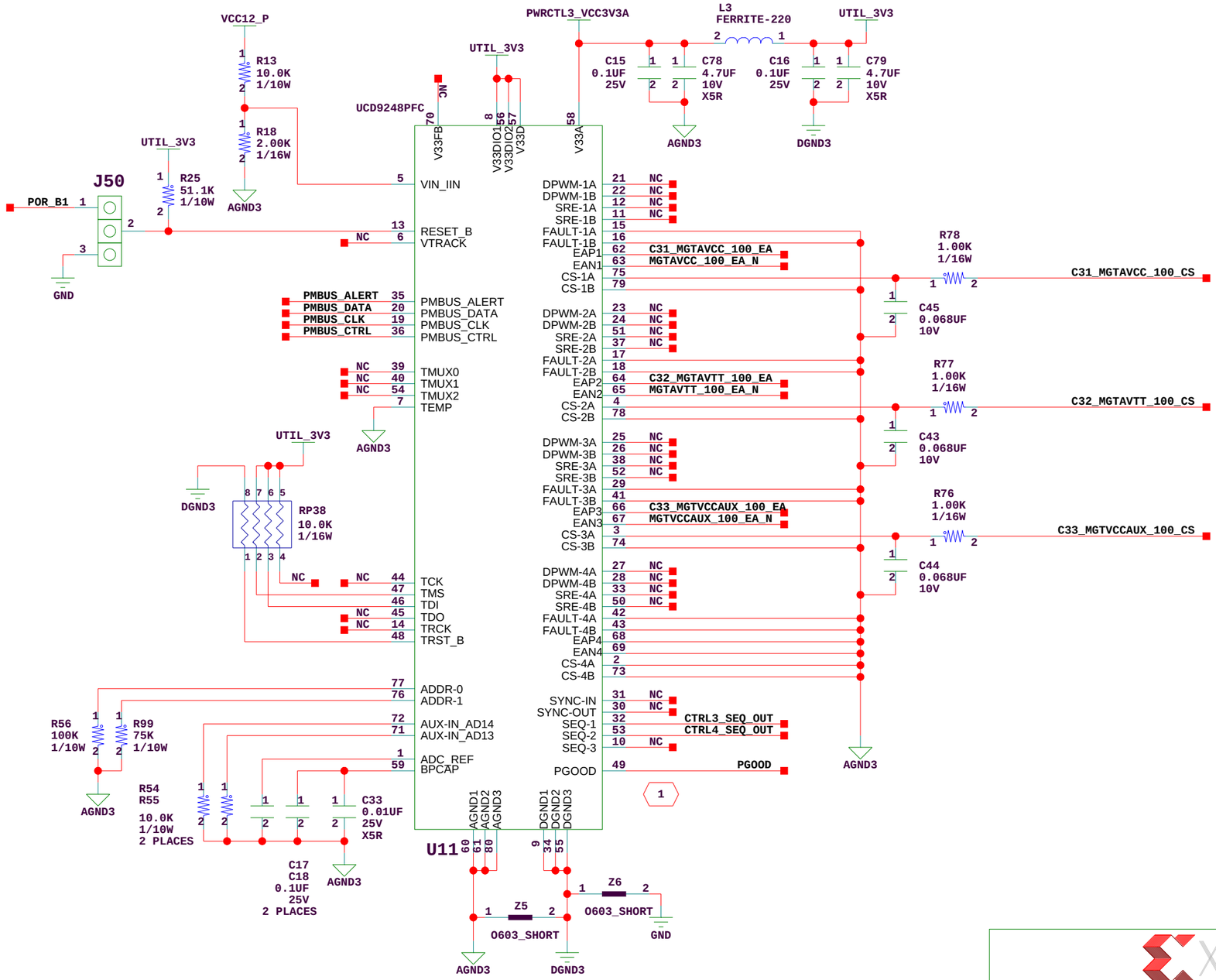
PWM SYSTEM CONTROLLER #3

PMBUS ADDRESS	
HEX	DECIMAL
0x36	54



1 ALL PGOOD OUTPUTS WILL BE OPEN-DRAIN AND WIRE-ORED

Title: PWM SYSTEM CONTROLLER #3 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
Sheet Size: B	Rev: 01
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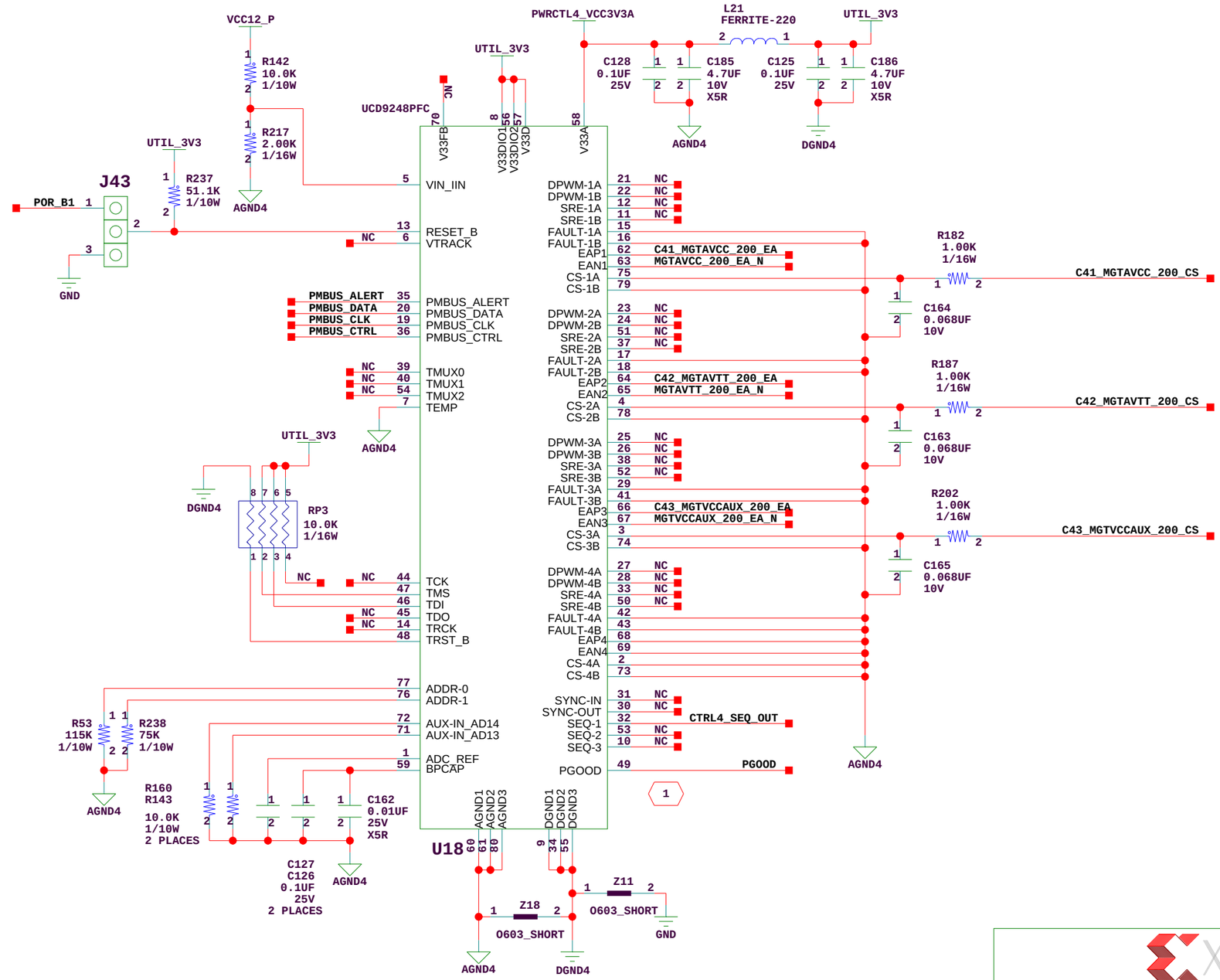
PWM SYSTEM CONTROLLER #4

PMBUS ADDRESS	
HEX	DECIMAL
0x37	55



1 ALL PGOOD OUTPUTS WILL BE OPEN-DRAIN AND WIRE-ORED

Title: PWM SYSTEM CONTROLLER #4 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
Sheet Size: B	Rev: 01
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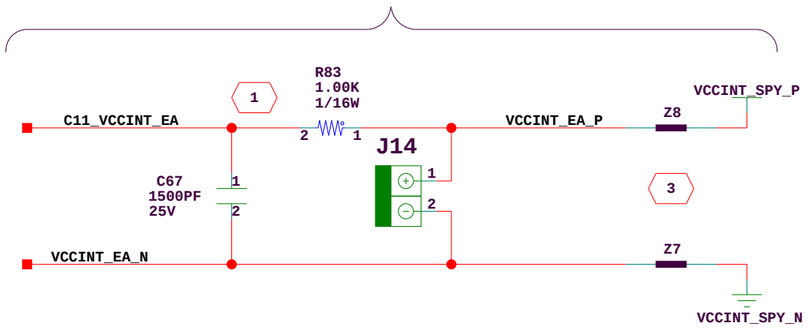
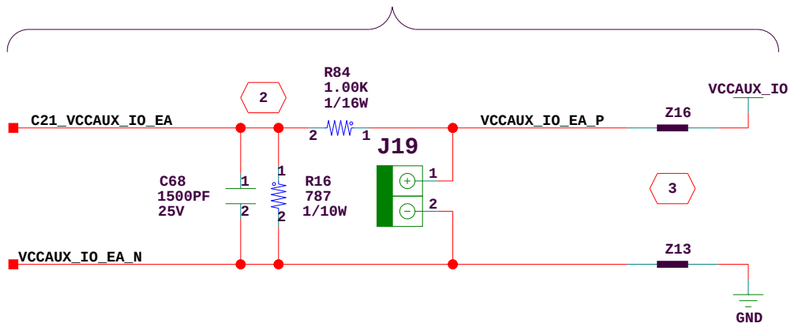
REMOTE VOLTAGE SENSE LOW-PASS FILTERS

CONTROLLER #1 RAILS



CONTROLLER #2 RAILS



1. PLACE LOW-PASS FILTER COMPONENTS ADJACENT TO CONTROLLER #1
2. PLACE LOW-PASS FILTER COMPONENTS ADJACENT TO CONTROLLER #2
3. ROUTE AS 100 OHM DIFFERENTIAL PAIR FROM LOAD SENSE POINT TO CONTROLLER

XILINX

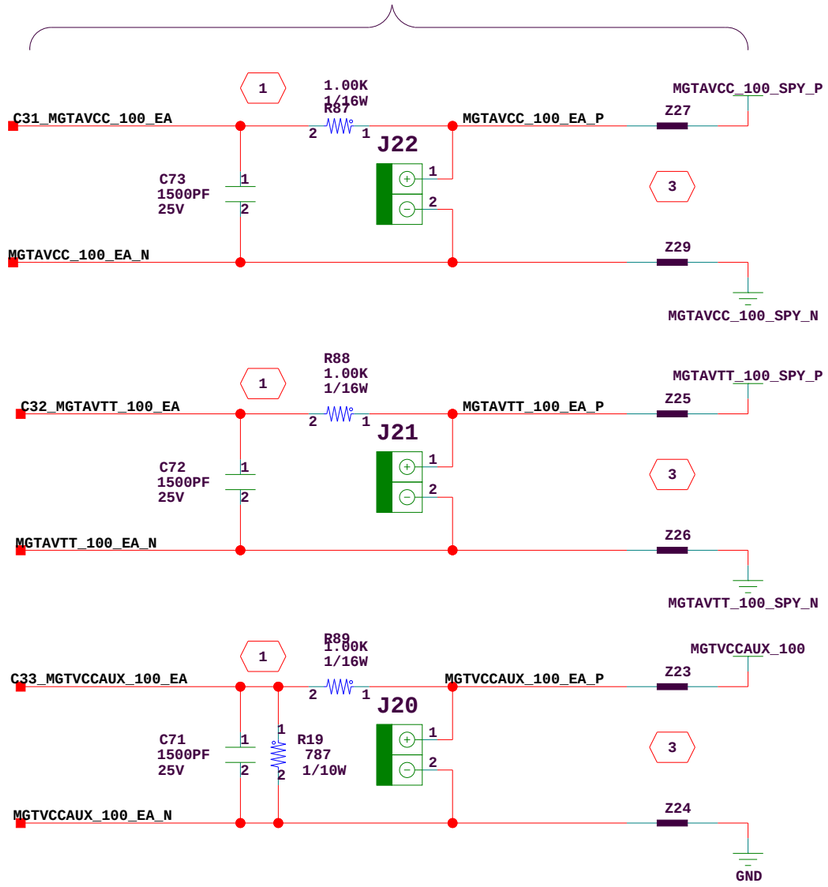
Title: REMOTE VOLTAGE SENSE LOW-PASS FILTERS
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

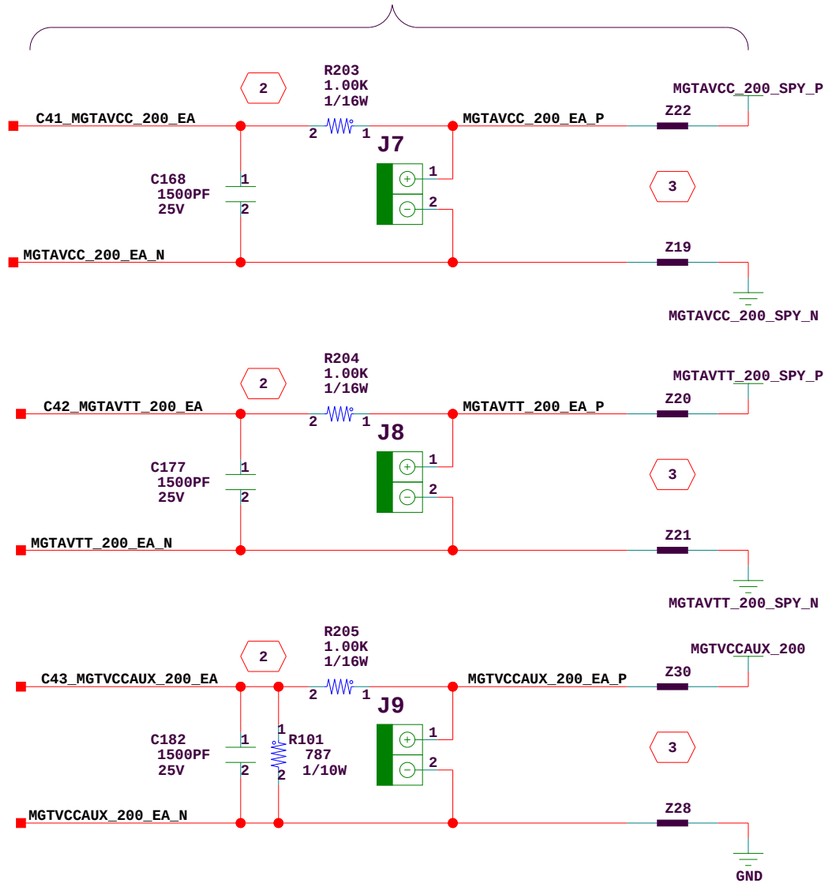
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 13 of 90	Drawn By RN

REMOTE VOLTAGE SENSE LOW-PASS FILTERS

CONTROLLER #3 RAILS



CONTROLLER #4 RAILS



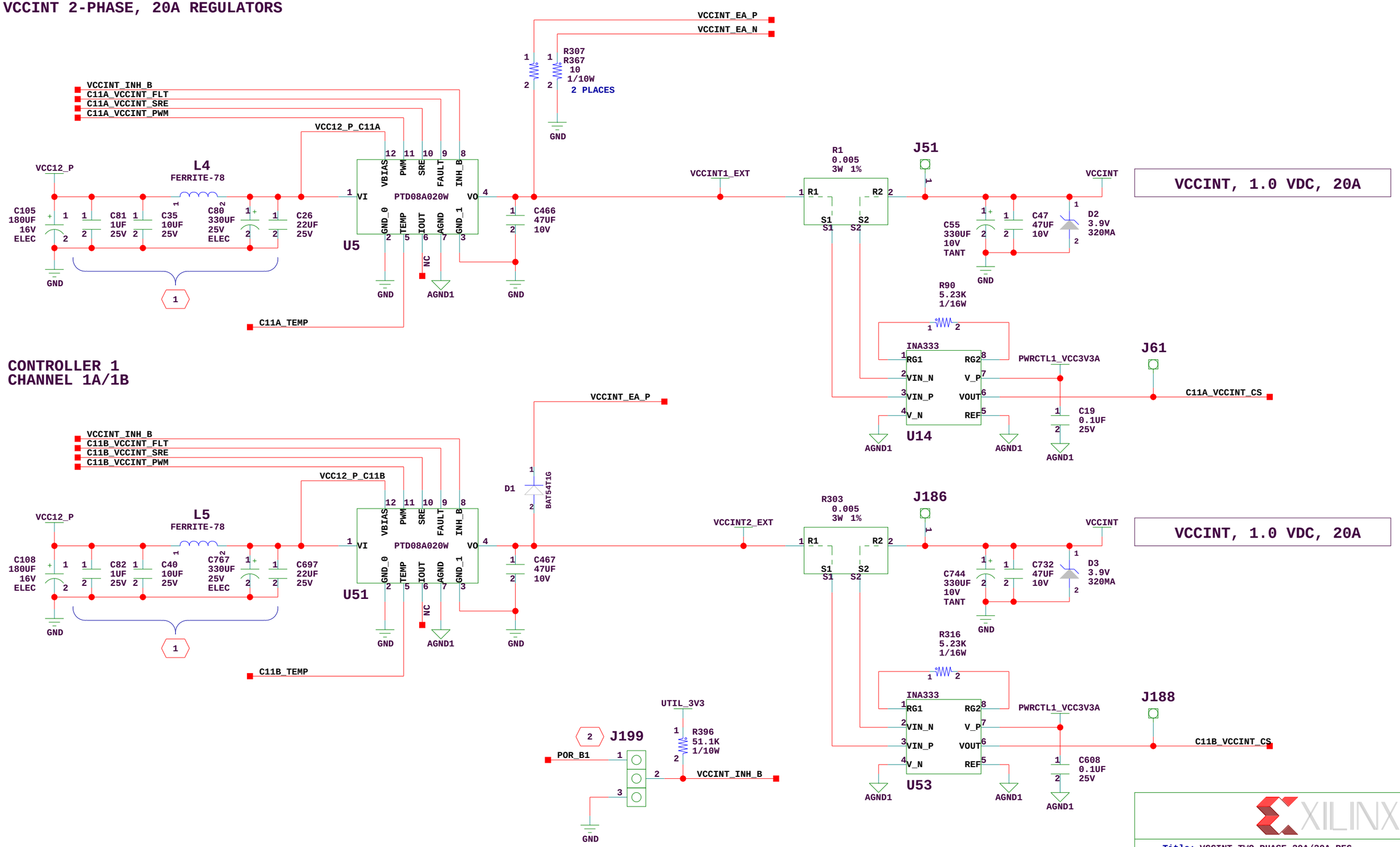
1. PLACE LOW-PASS FILTER COMPONENTS ADJACENT TO CONTROLLER #3
2. PLACE LOW-PASS FILTER COMPONENTS ADJACENT TO CONTROLLER #4
3. ROUTE AS 100 OHM DIFFERENTIAL PAIR FROM LOAD SENSE POINT TO CONTROLLER

XILINX

Title:	REMOTE VOLTAGE SENSE LOW-PASS FILTERS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N:	0431676
		PCB P/N:	1280597
		SCH P/N:	0381429
		TEST P/N:	TSS0XXX
Date:	4-11-2013_18:23	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	14 of 90	Drawn By	RN

VCCINT 2-PHASE, 20A REGULATORS

CONTROLLER 1
CHANNEL 1A/1B



VCCINT, 1.0 VDC, 20A

VCCINT, 1.0 VDC, 20A

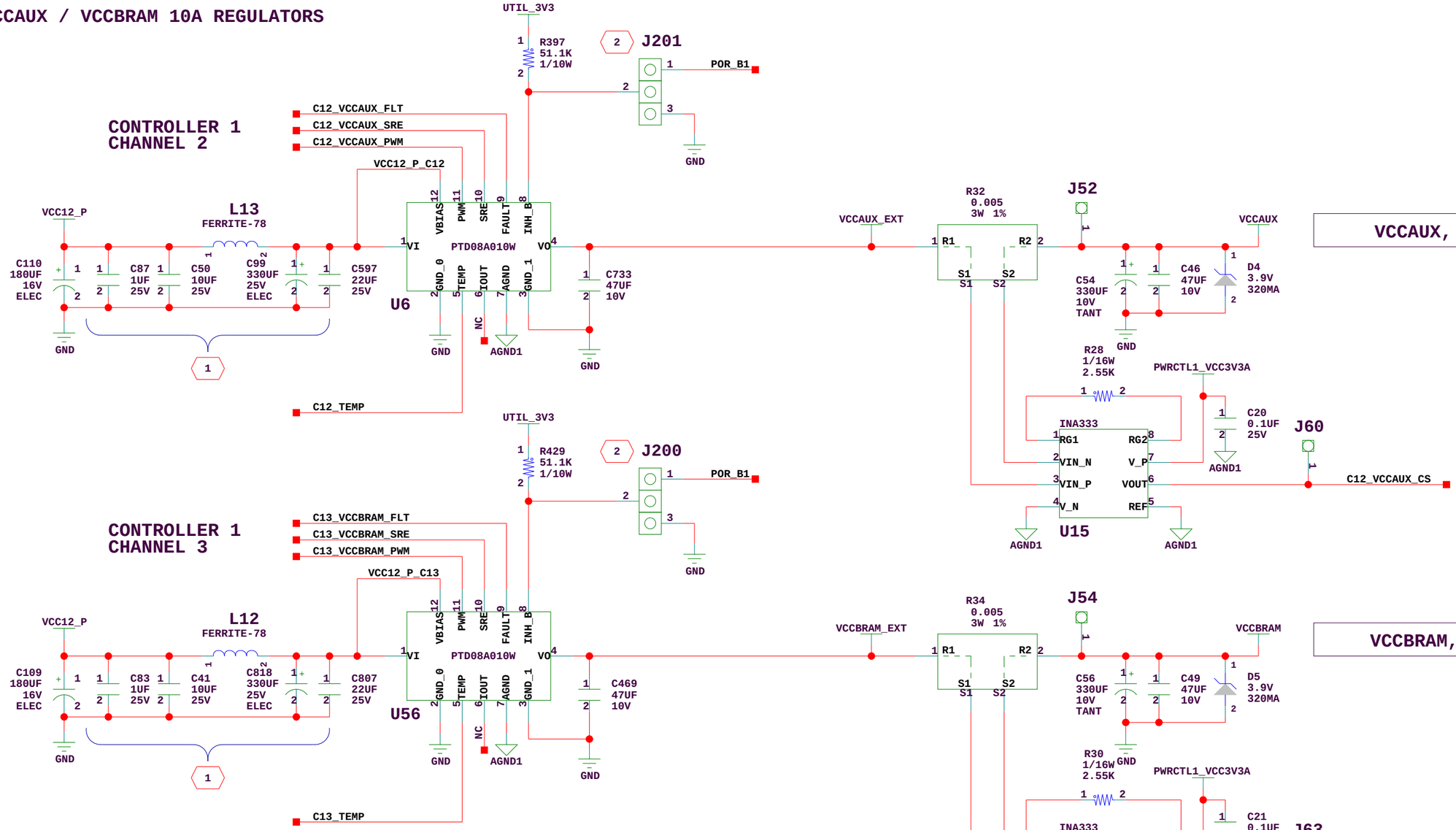
1. PLACE COMPONENTS AS CLOSE AS POSSIBLE TO VI PIN ON REGULATOR
2. CAUTION: TO AVOID DAMAGE PLACE THE REGULATORS IN RESET (POSITION 2-3) WHEN USING EXTERNAL SUPPLIES TO SOURCE THIS RAIL

XILINX

Title: VCCINT TWO PHASE 20A/20A REG SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 15 of 90	Drawn By RN

VCCAUX / VCCBRAM 10A REGULATORS

CONTROLLER 1 CHANNEL 2



VCCAUX, 1.8 VDC, 10A

CONTROLLER 1 CHANNEL 3

VCCBRAM, 1.0 VDC, 10A

1. PLACE COMPONENTS AS CLOSE AS POSSIBLE TO VI PIN ON REGULATOR
2. CAUTION: TO AVOID DAMAGE PLACE THE REGULATORS IN RESET (POSITION 2-3) WHEN USING EXTERNAL SUPPLIES TO SOURCE THIS RAIL

XILINX

Title: VCCAUX / VCCBRAM 10A REG SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-12-2013_11:36		Ver: 1.0	
Sheet Size: B		Rev: 01	
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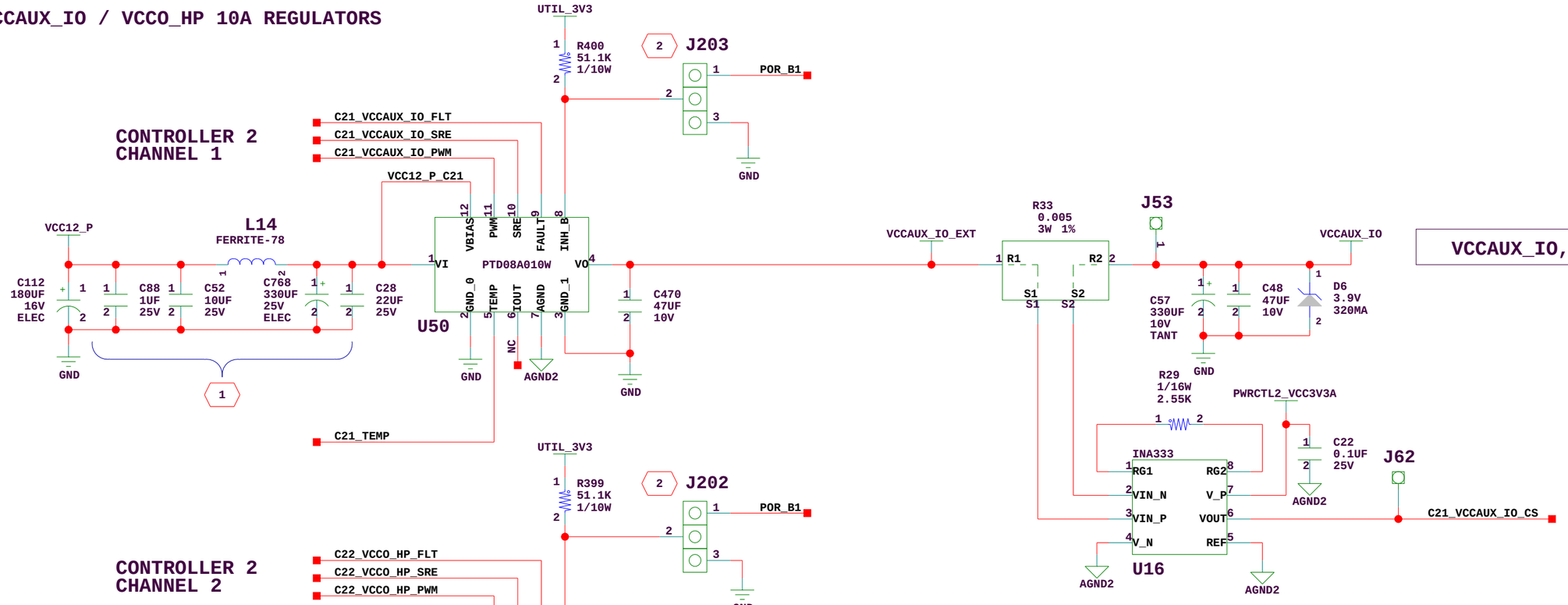
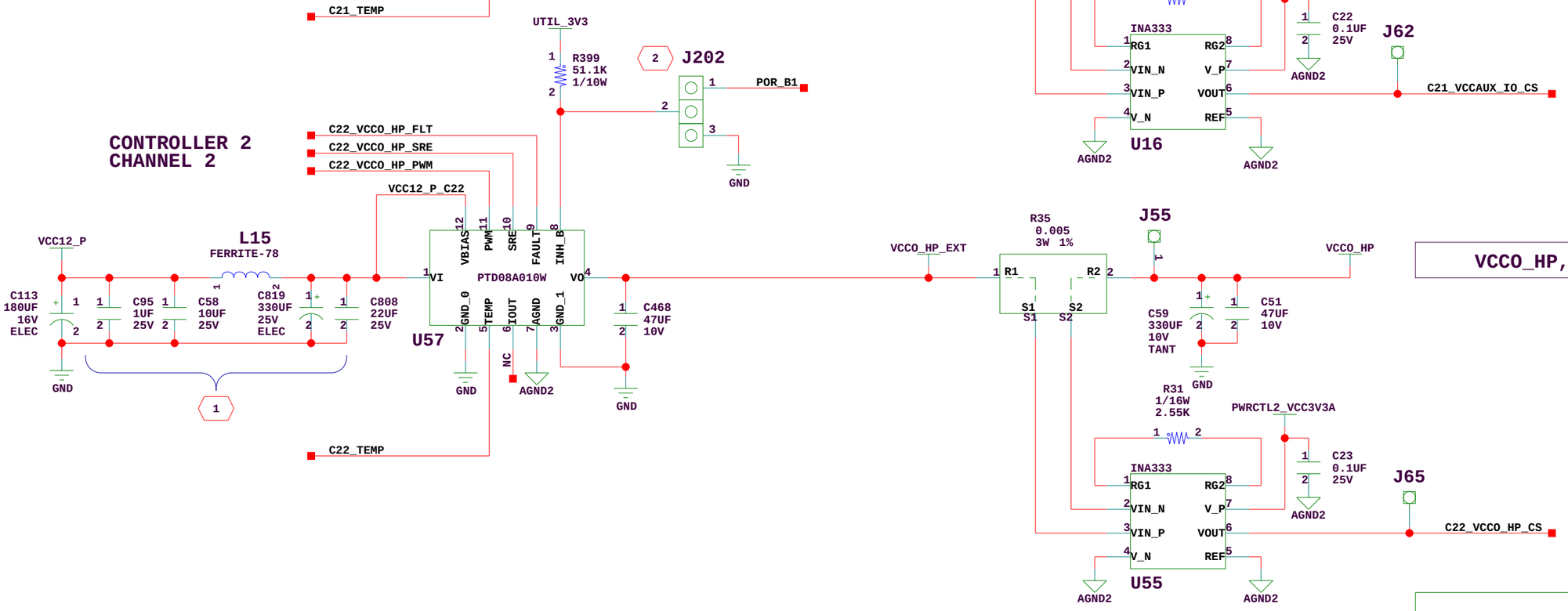
VCCAUX_IO / VCCO_HP 10A REGULATORS

CONTROLLER 2 CHANNEL 1



CONTROLLER 2 CHANNEL 2

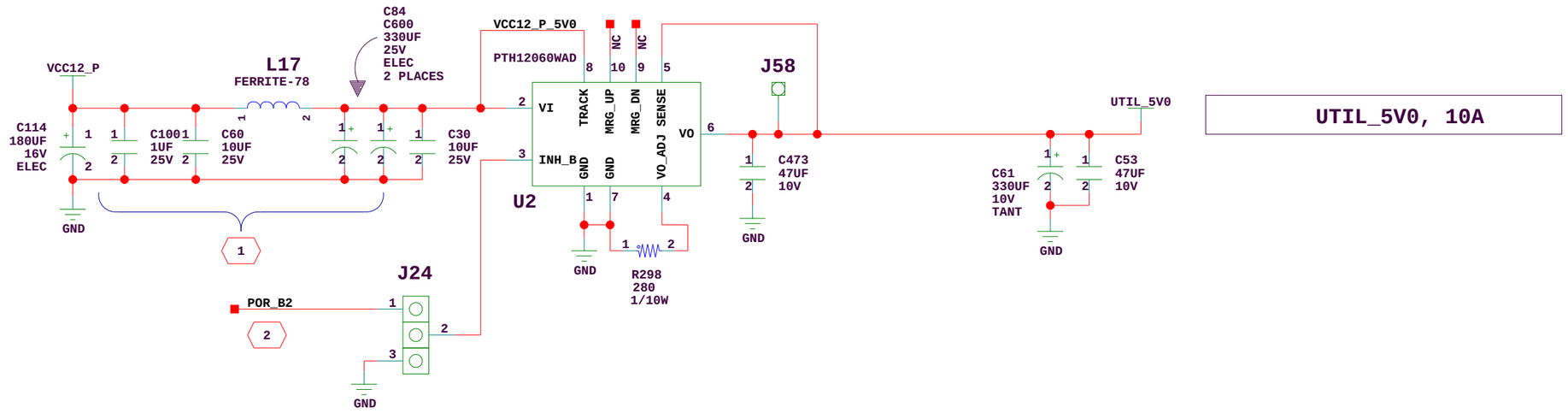


1. PLACE COMPONENTS AS CLOSE AS POSSIBLE TO VI PIN ON REGULATOR
2. CAUTION: TO AVOID DAMAGE PLACE THE REGULATORS IN RESET (POSITION 2-3) WHEN USING EXTERNAL SUPPLIES TO SOURCE THIS RAIL

XILINX

Title: VCCAUX_IO / VCCO_HP 10A REG SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 17 of 90	Drawn By RN

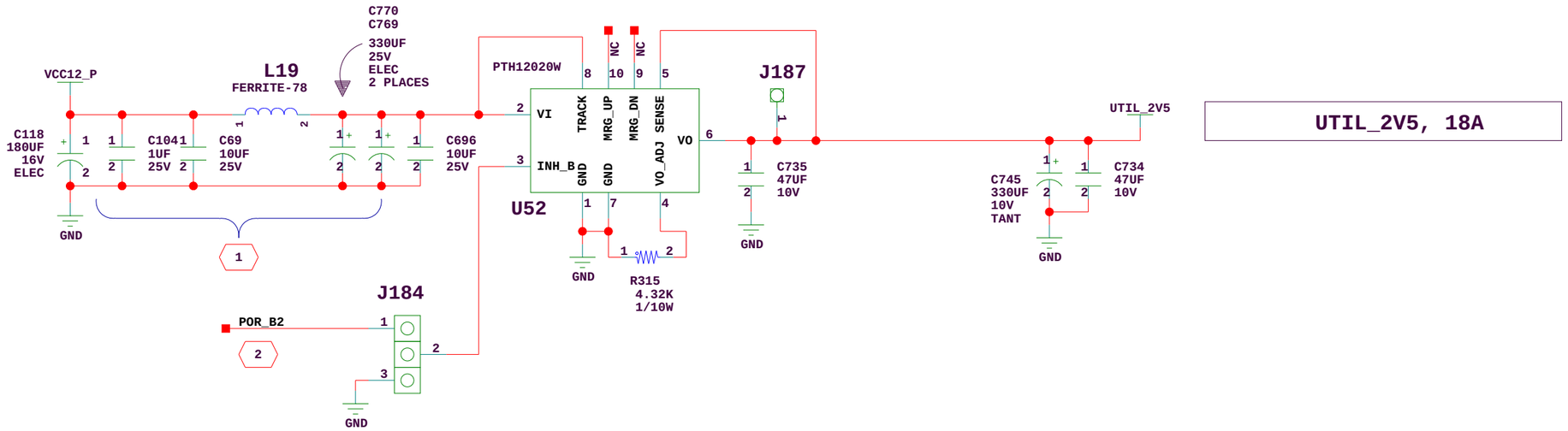
UTIL_5V0 10A FIXED OUTPUT REGULATOR / UTIL_3V3 18A FIXED OUTPUT REGULATOR



1. PLACE COMPONENTS AS CLOSE AS POSSIBLE TO VI PIN ON REGULATOR
2. POR_B2 IS AN OPEN-DRAIN DRIVER

Title: UTIL_5V0 / UTIL_3V3 REGULATORS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 18 of 90	Drawn By RN

UTIL_2V5 18A FIXED OUTPUT REGULATOR

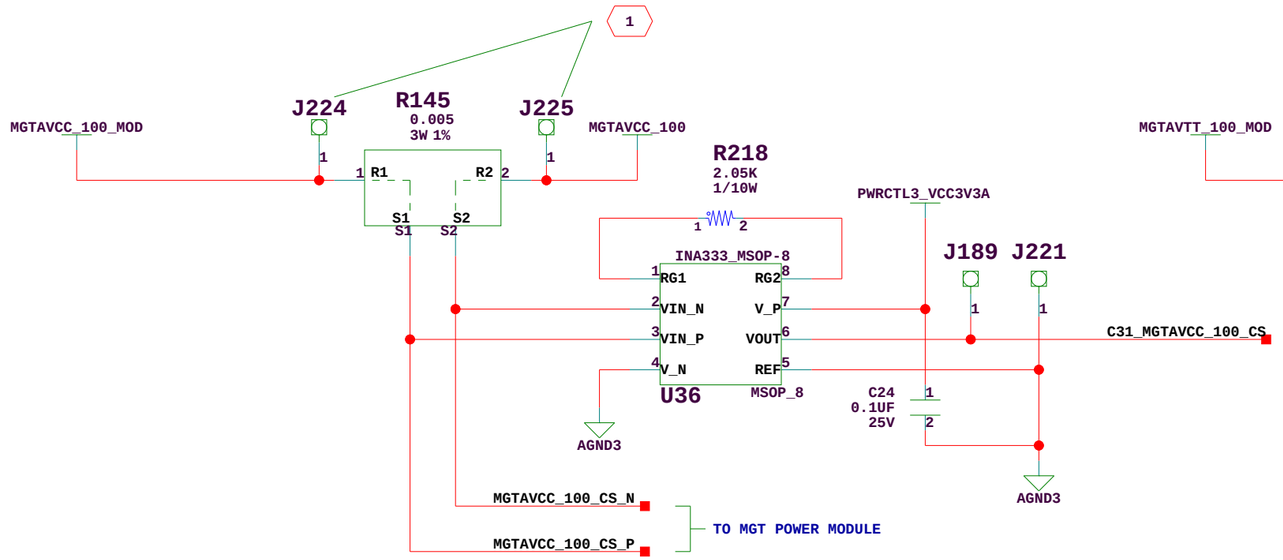


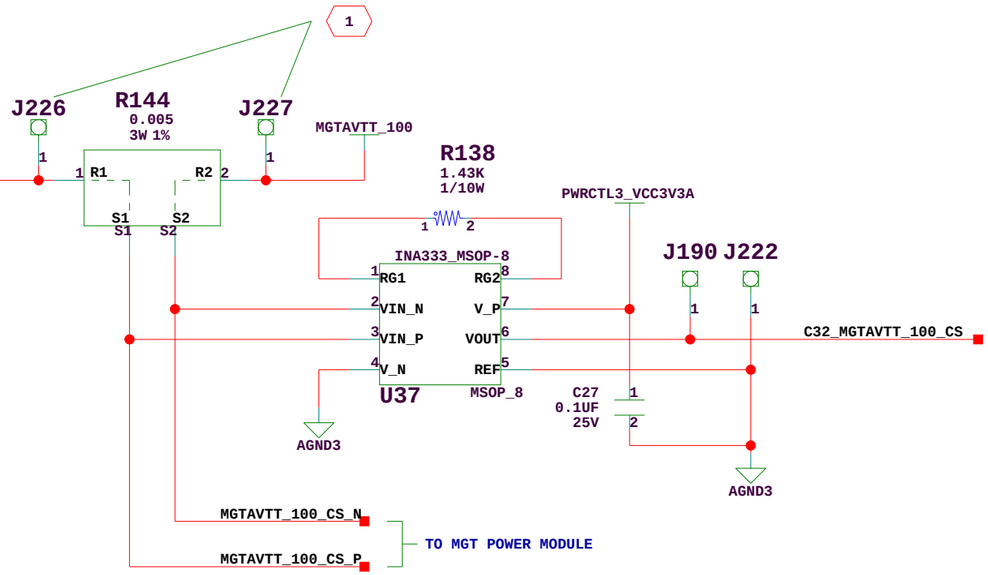
UTIL_2V5, 18A

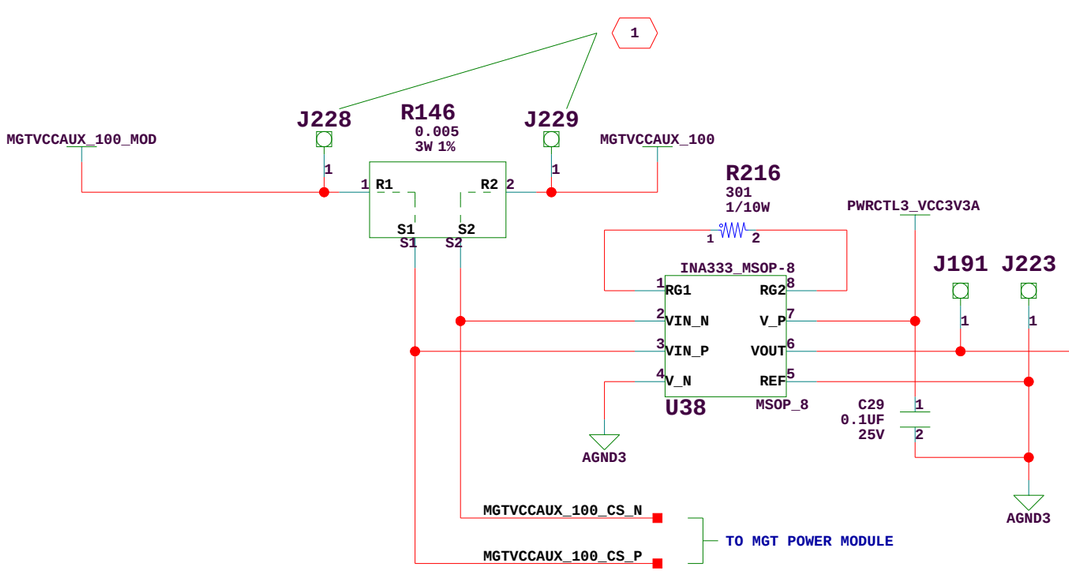
1. PLACE COMPONENTS AS CLOSE AS POSSIBLE TO VI PIN ON REGULATOR
2. POR_B2 IS AN OPEN-DRAIN DRIVER

Title: UTIL_2V5 REGULATOR SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 19 of 90	Drawn By RN

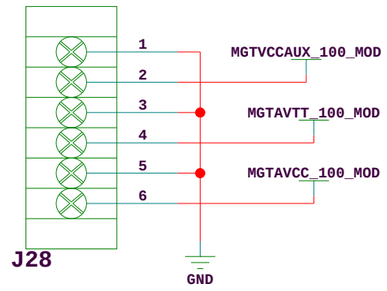
MGTAVCC_100, MGTAVTT_100 AND MGTVCCAUX_100 CURRENT SENSE AND EXT POWER JACKS







MGT 100 INPUT POWER (EURO-MAG)

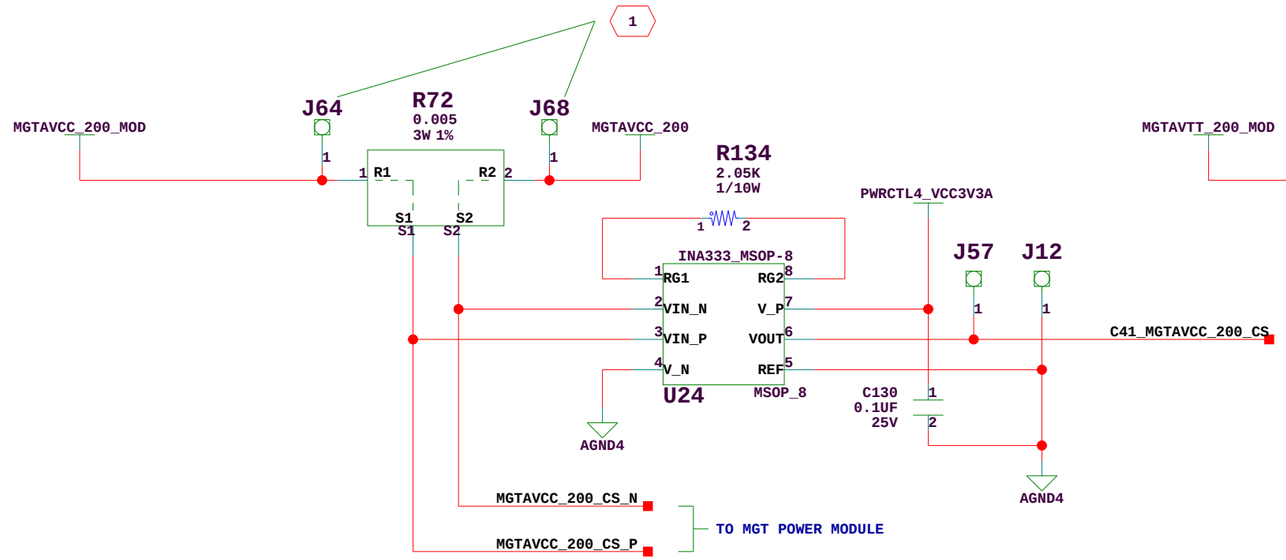


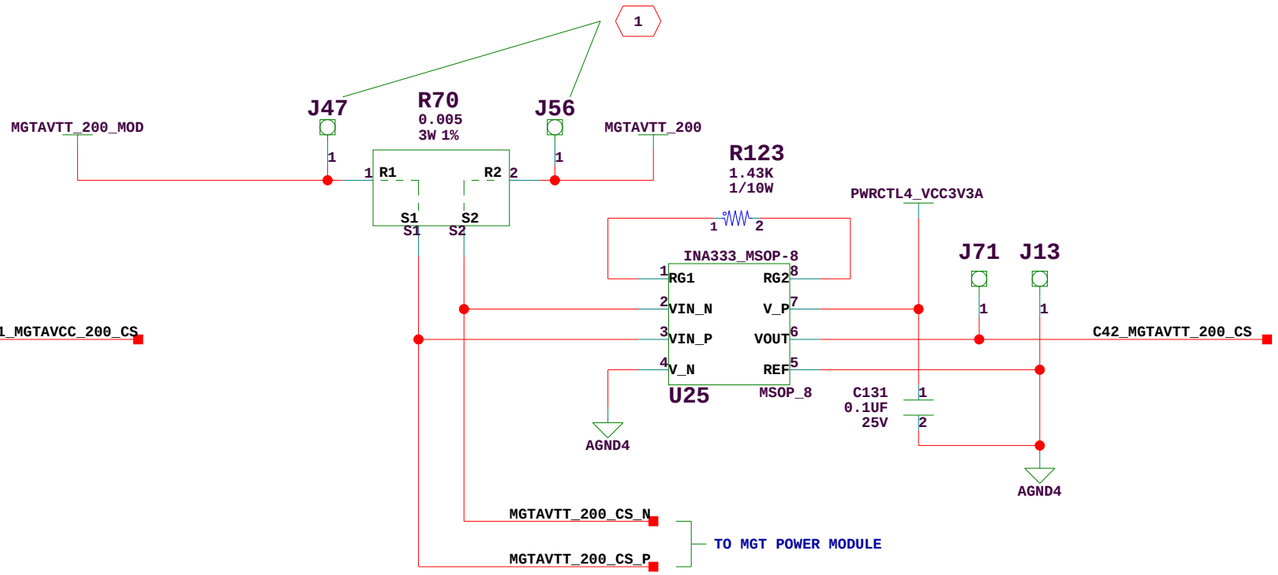
1 PLACE TEST POINTS AS CLOSE AS POSSIBLE TO SENSE RESISTOR

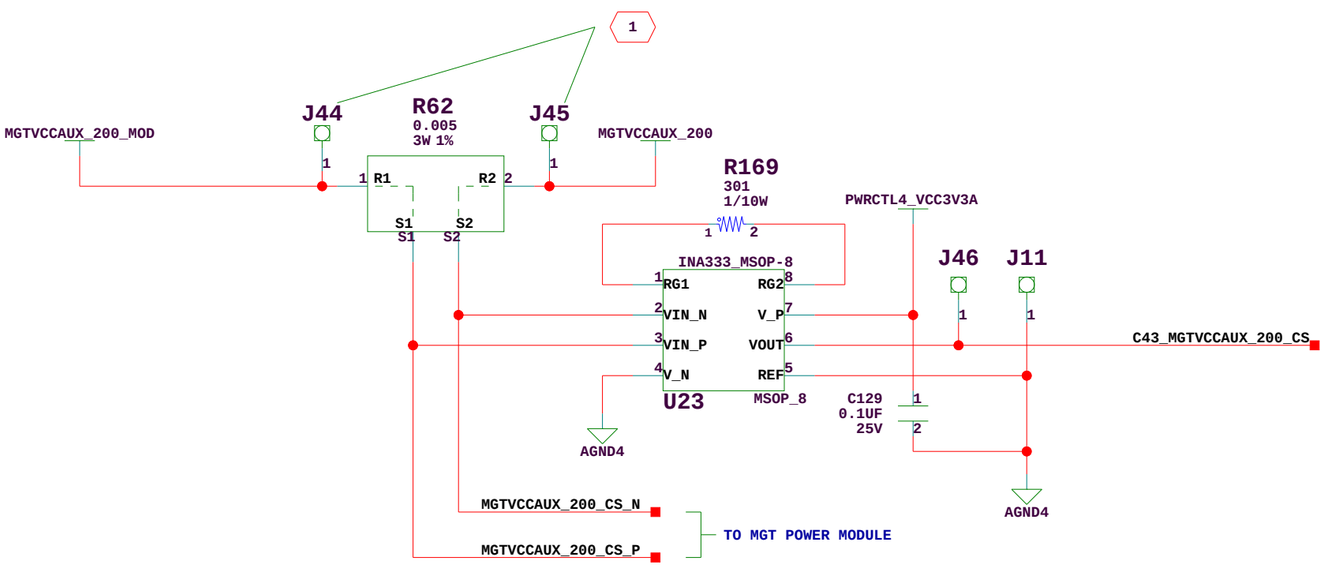
XILINX

Title: MGT 100 CURR SNS, EXT PWR JACKS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 20 of 90	Drawn By RN

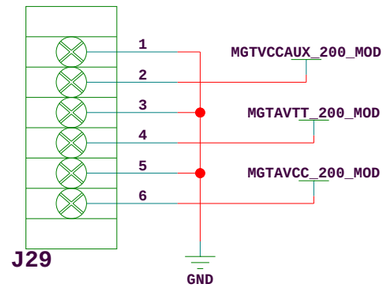
MGTAVCC_200, MGTAVTT_200 AND MGTVCCAUX_200 CURRENT SENSE AND EXT POWER JACKS







MGT 200 INPUT POWER (EURO-MAG)



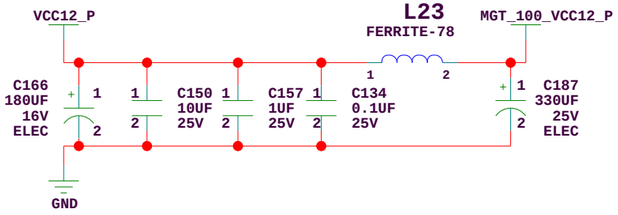
1 PLACE TEST POINTS AS CLOSE AS POSSIBLE TO SENSE RESISTOR

XILINX

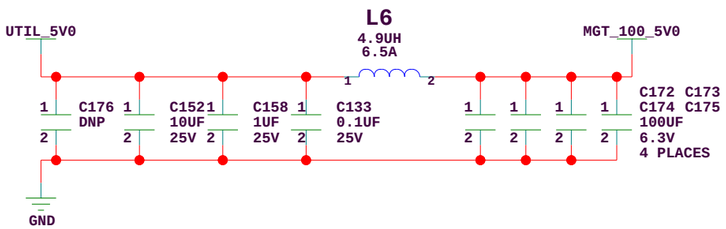
Title: MGT 200 CURR SNS, EXT PWR JACKS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 21 of 90	Drawn By RN

MGT POWER MODULE INTERFACE - BANKS 1XX - POWER CONNECTOR

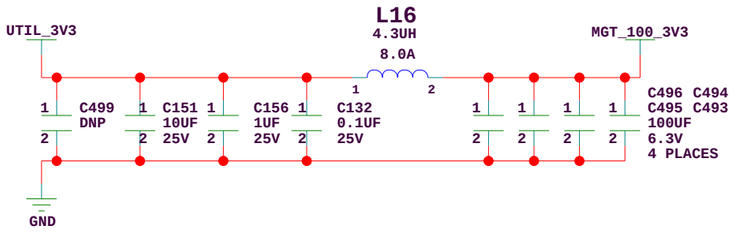
12V INPUT FILTER (1)

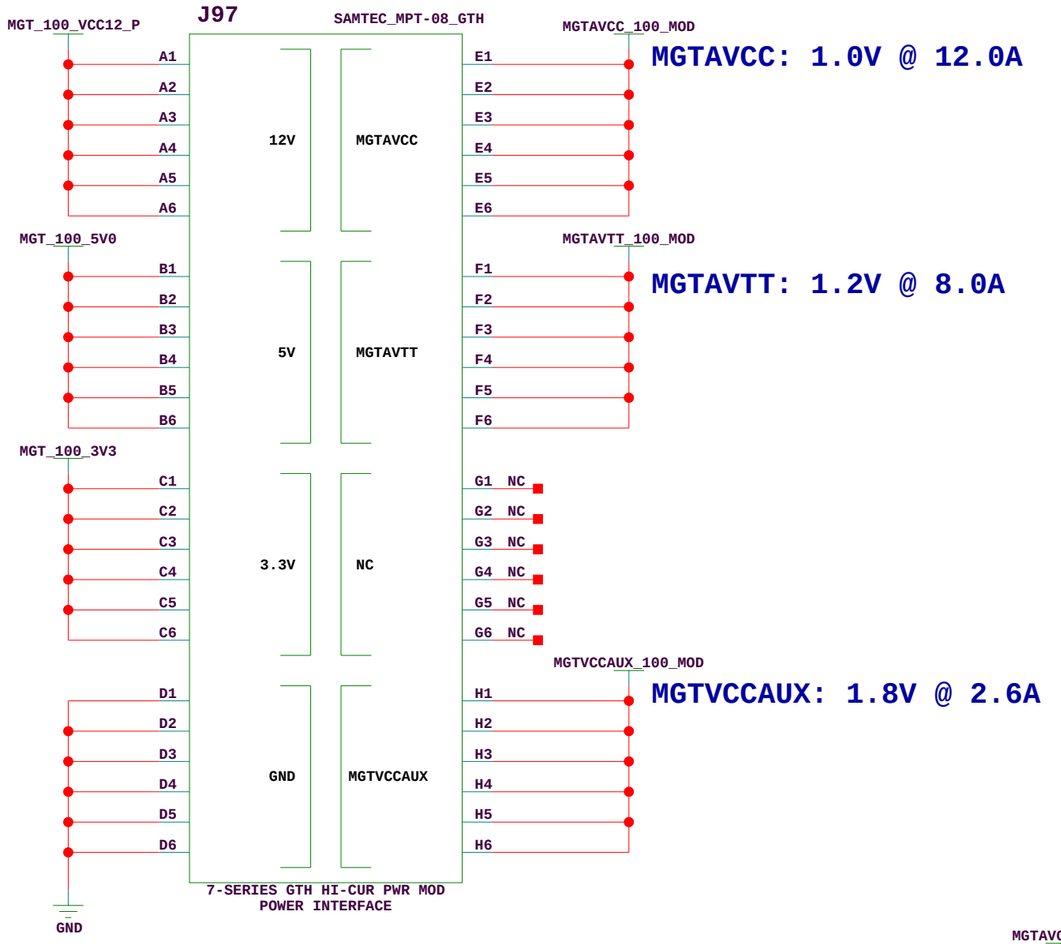


5V INPUT FILTER (1)

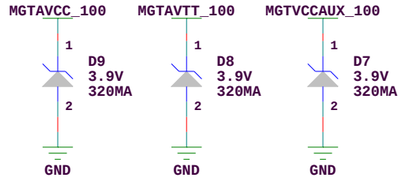


3.3V INPUT FILTER (1)





PROTECTION DIODES

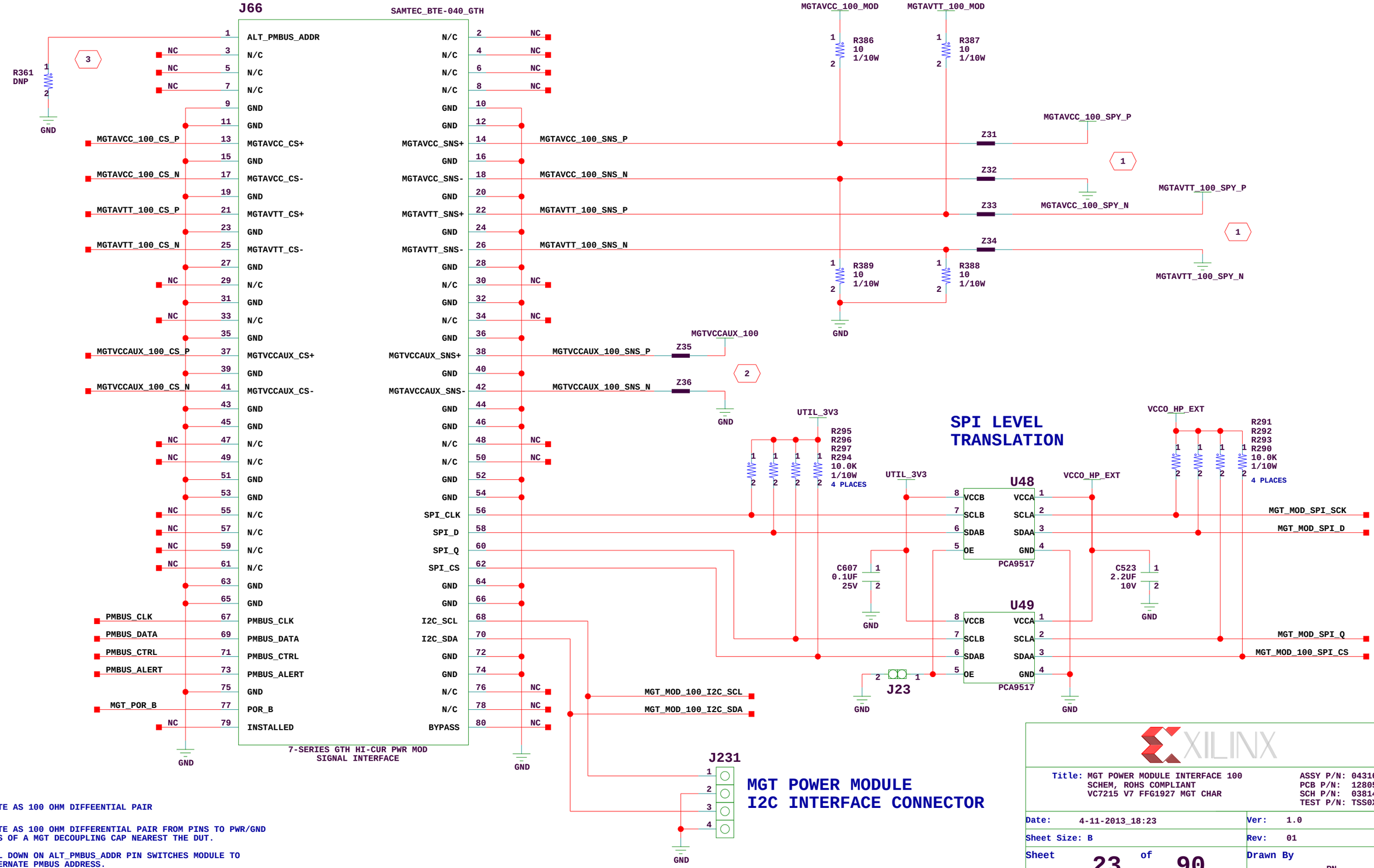


(1) PLACE ALL FILTER COMPONENTS AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE PIN ON THE POWER CONNECTOR.

XILINX

Title: MGT POWER MODULE INTERFACE 100 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 22 of 90	Drawn By RN

MGT POWER MODULE INTERFACE - BANKS 1XX - SIGNAL CONNECTOR



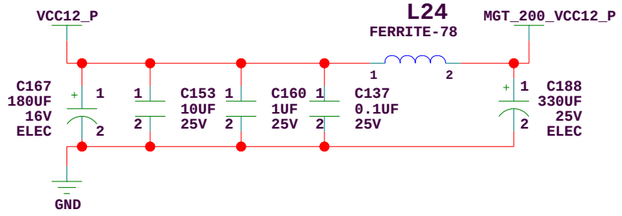
1. ROUTE AS 100 OHM DIFFEENTIAL PAIR
2. ROUTE AS 100 OHM DIFFERENTIAL PAIR FROM PINS TO PWR/GND PINS OF A MGT DECOUPLING CAP NEAREST THE DUT.
3. PULL DOWN ON ALT_PMBUS_ADDR PIN SWITCHES MODULE TO ALTERNATE PMBUS ADDRESS.

XILINX

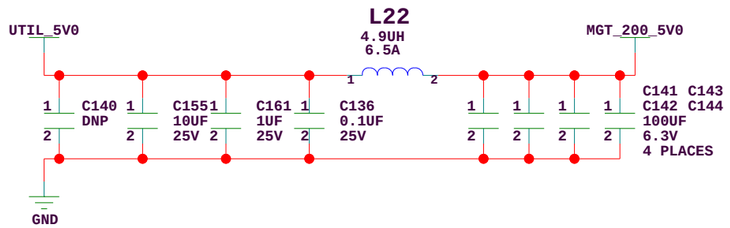
Title: MGT POWER MODULE INTERFACE 100 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 23 of 90	Drawn By RN

MGT POWER MODULE INTERFACE - BANKS 2XX - POWER CONNECTOR

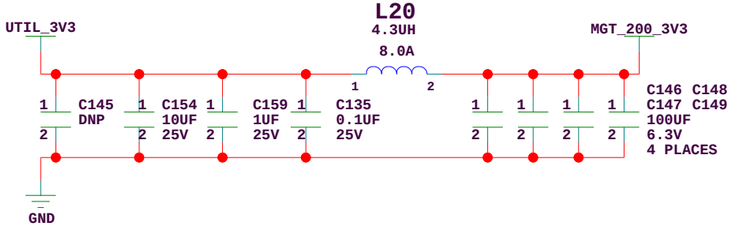
12V INPUT FILTER (1)

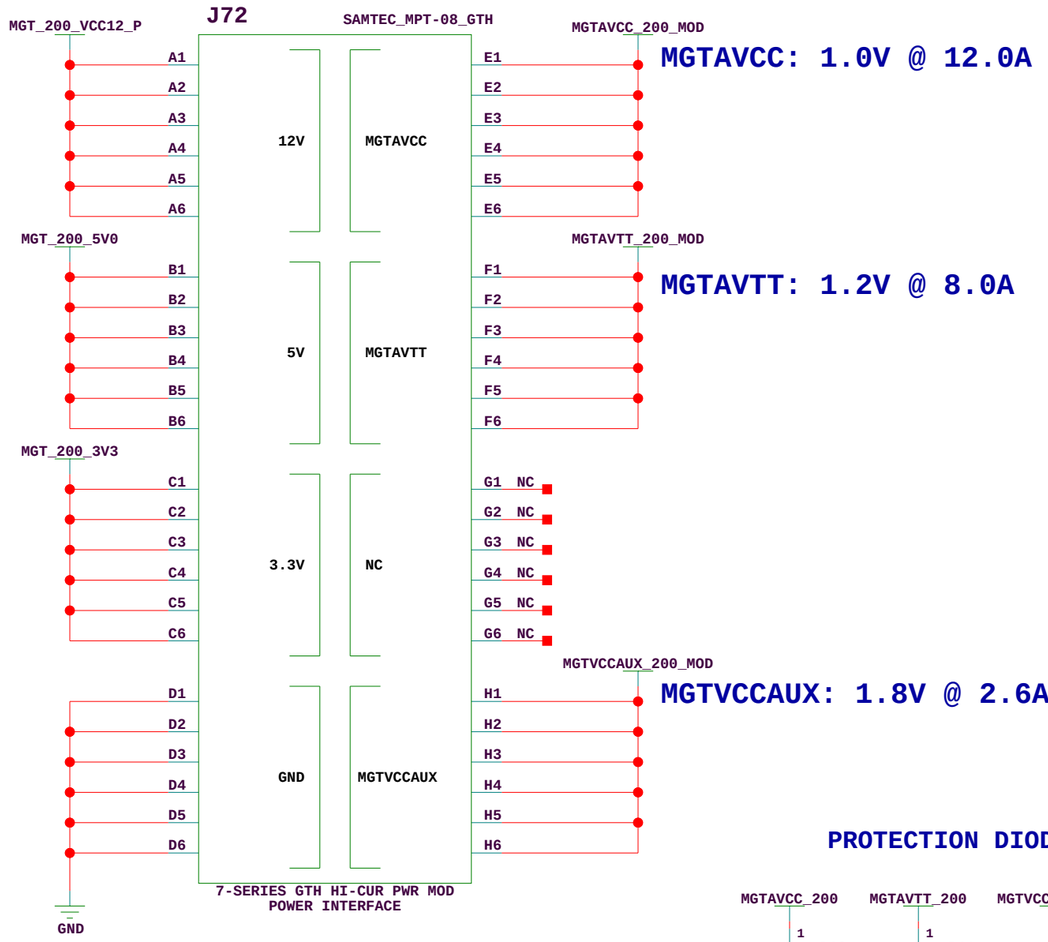


5V INPUT FILTER (1)

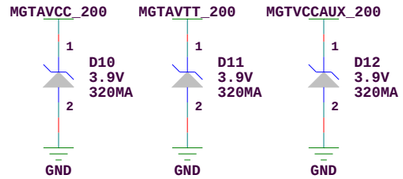


3.3V INPUT FILTER (1)





PROTECTION DIODES

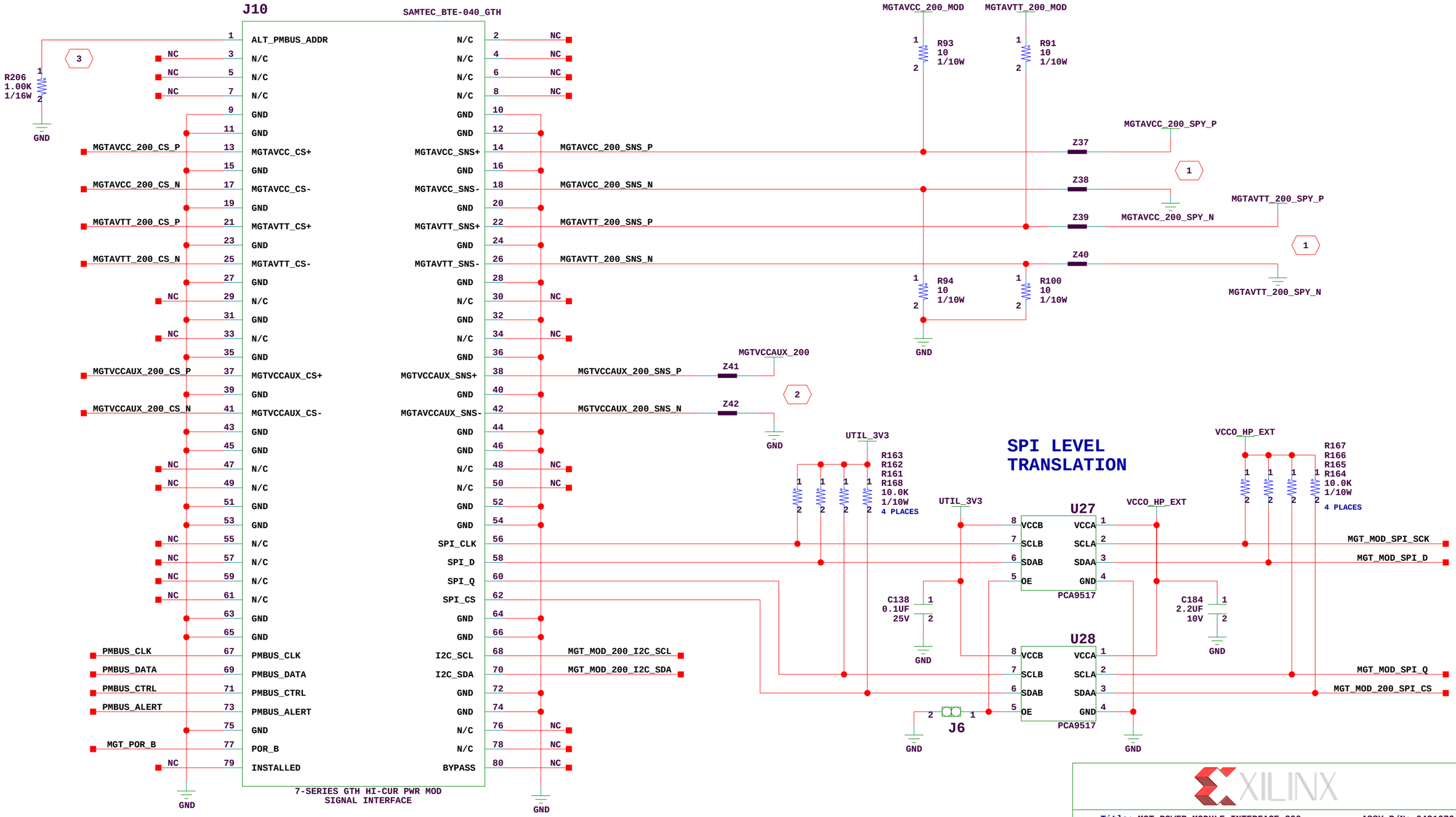


(1) PLACE ALL FILTER COMPONENTS AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE PIN ON THE POWER CONNECTOR.

XILINX

Title: MGT POWER MODULE INTERFACE 200 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_18:23		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 24 of 90		Drawn By RN	

MGT POWER MODULE INTERFACE - BANKS 2XX - SIGNAL CONNECTOR



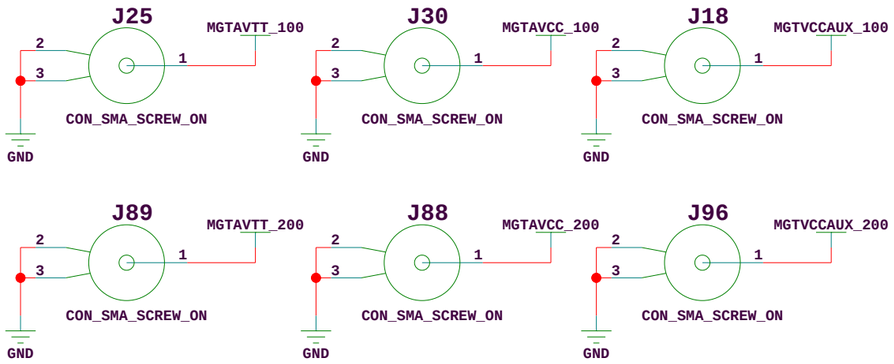
1. ROUTE AS 100 OHM DIFFEENTIAL PAIR
2. ROUTE AS 100 OHM DIFFERENTIAL PAIR FROM PINS TO PWR/GND PINS OF A MGT DECOUPLING CAP NEAREST THE DUT.
3. PULL DOWN ON ALT_PMBUS_ADDR PIN SWITCHES MODULE TO ALTERNATE PMBUS ADDRESS.

XILINX

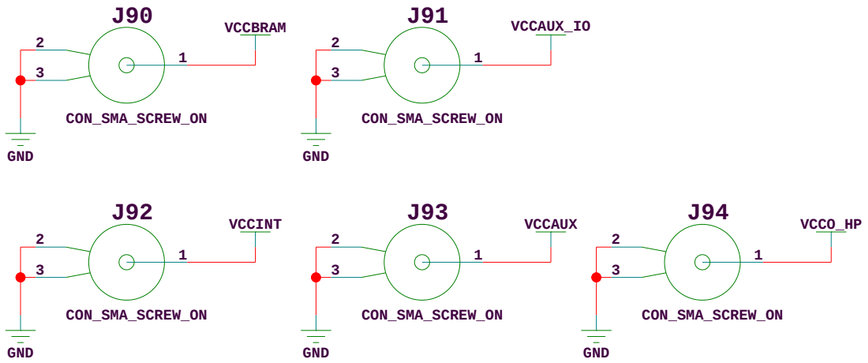
Title:	MGT POWER MODULE INTERFACE 200 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N:	0431676
		PCB P/N:	1280597
		SCH P/N:	0381429
		TEST P/N:	TSS0XXX
Date:	4-11-2013_18:23	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	25 of 90	Drawn By	RN

POWER PROBE CHANNELS

MGT POWER PROBE CHANNELS 1



DUT POWER PROBE CHANNELS 1

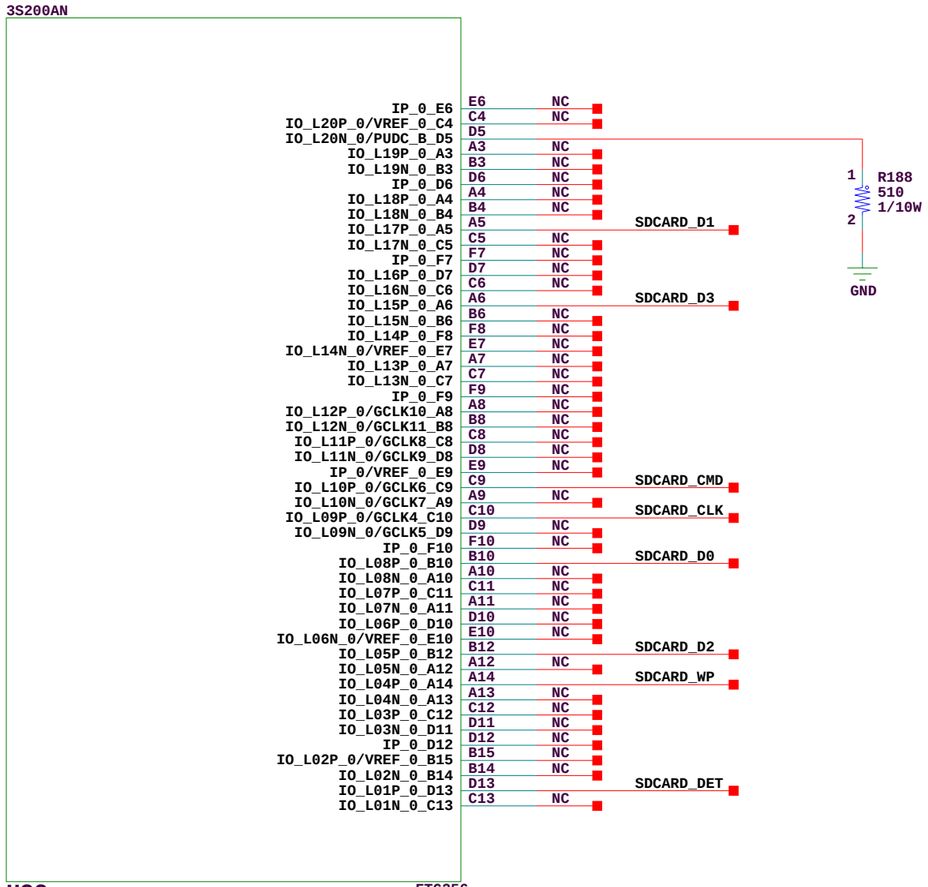


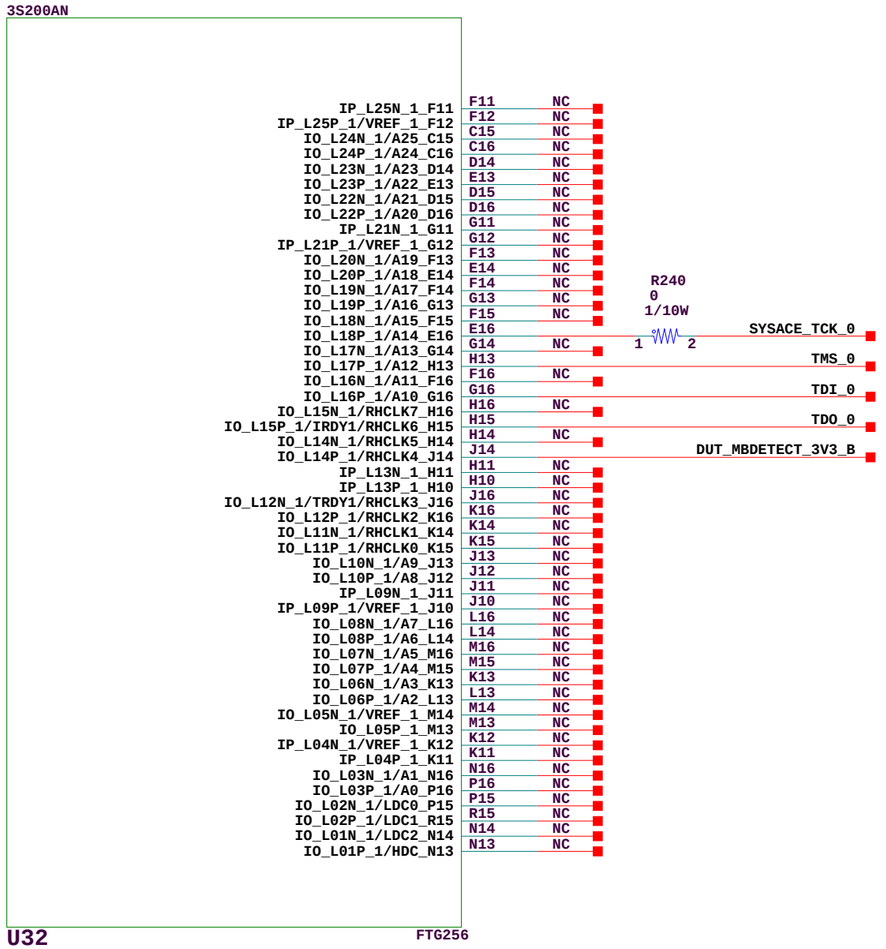
1 PLACE POWER PROBE CHANNELS AS CLOSE AS POSSIBLE TO THE DUT

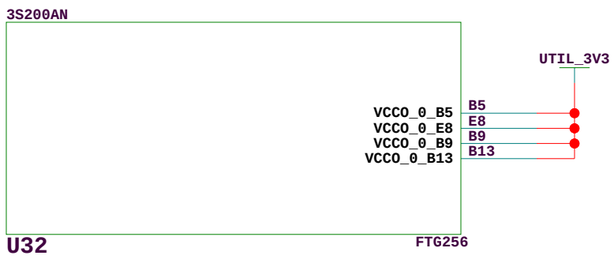
XILINX

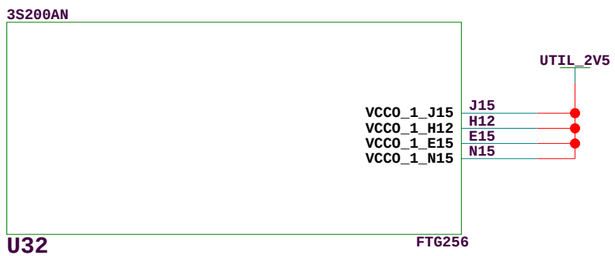
Title: POWER PROBE CHANNELS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 26 of 90	Drawn By RN

SYSTEMACE-2 - S3AN FPGA BANKS 0, 1









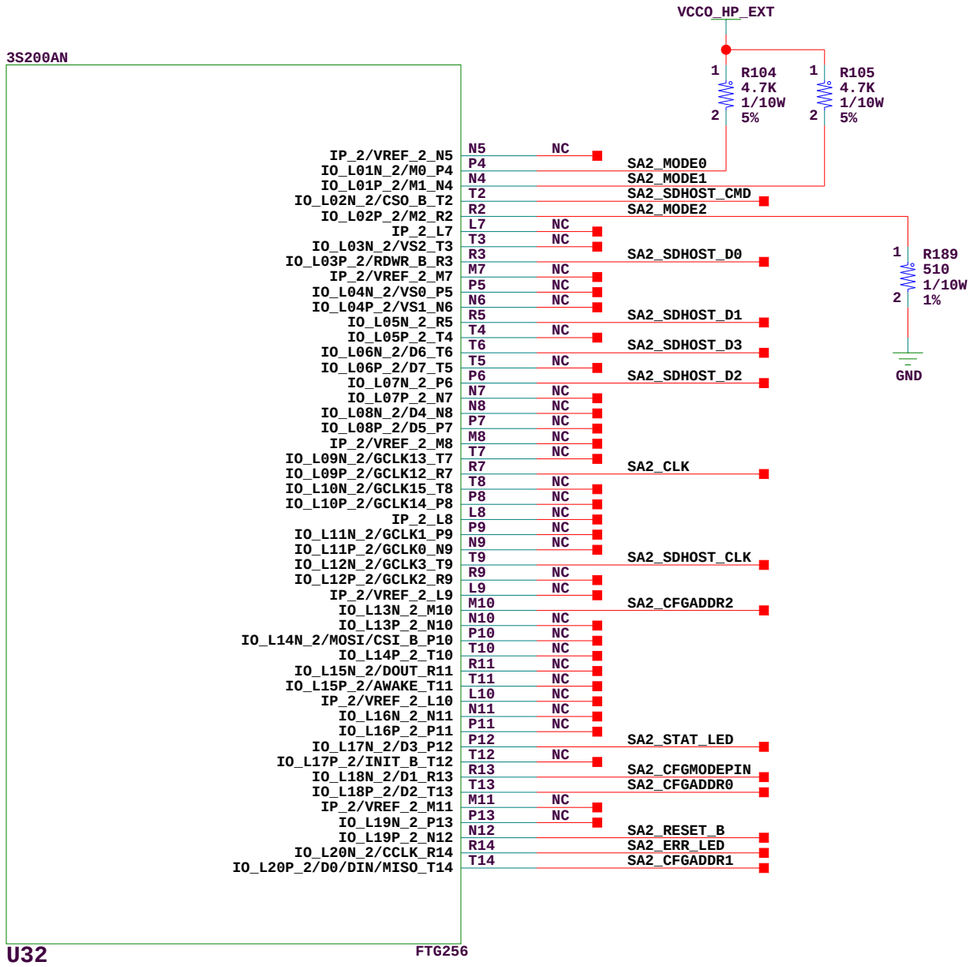
XILINX

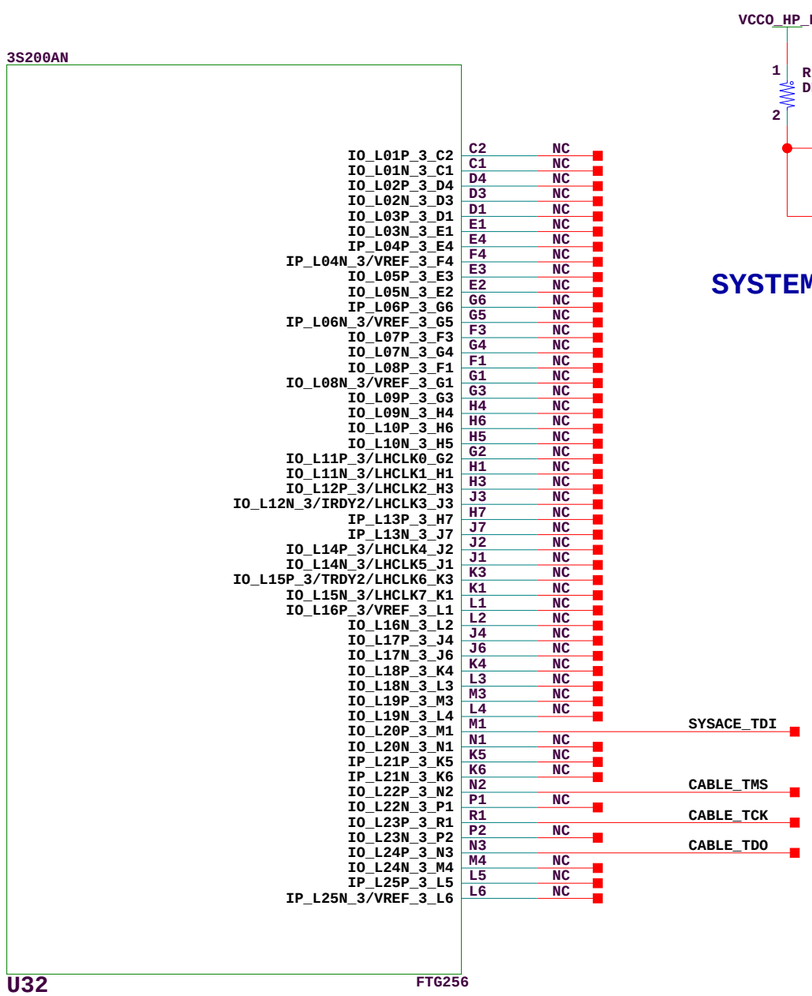
Title: SYSTEMACE-2 S3AN BANKS 0, 1
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

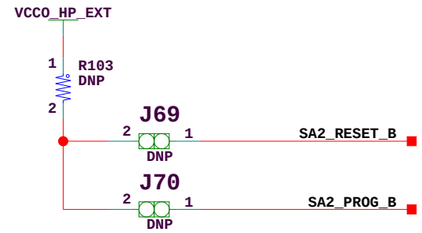
ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-18-2013_16:12	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 27 of 90	Drawn By RN

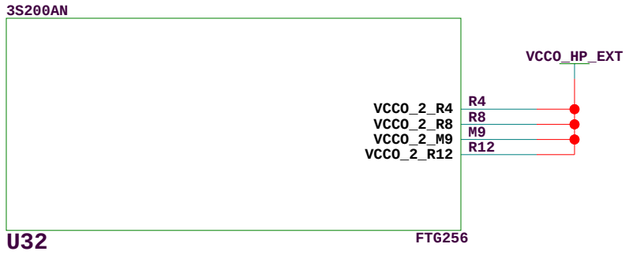
SYSTEMACE-2 - S3AN FPGA BANKS 2, 3

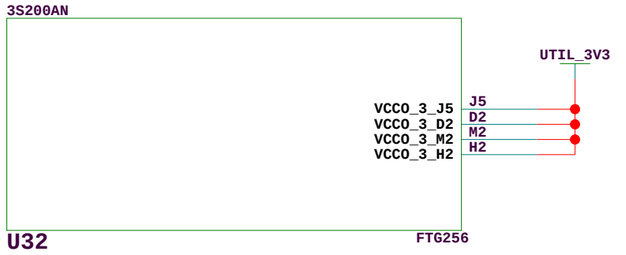






SYSTEMACE-2 FAILSAFE MODE JUMPERS





XILINX

Title: SYSTEMACE-2 S3AN BANKS 2, 3
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-18-2013_16:12
Ver: 1.0
Sheet Size: B
Rev: 01
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Drawn By RN

SYSTEMACE-2 - S3AN FPGA CONFIGURATION, PWR/GND

3S200AN

VCCAUX_E11 E11
VCCAUX_F5 F5
VCCAUX_L12 L12
VCCAUX_M6 M6

UTIL_3V3

U32 FTG256

3S200AN

VCCINT_J9 J9
VCCINT_H8 H8
VCCINT_G7 G7
VCCINT_G9 G9
VCCINT_K8 K8
VCCINT_K10 K10

VCC1V2

U32 FTG256

3S200AN

GND_J8 J8
GND_R10 R10
GND_M12 M12
GND_A16 A16
GND_A1 A1
GND_K9 K9
GND_T1 T1
GND_L11 L11
GND_F2 F2
GND_G15 G15
GND_K2 K2
GND_G8 G8
GND_C3 C3
GND_H9 H9
GND_P3 P3
GND_G10 G10
GND_E5 E5
GND_B11 B11
GND_M5 M5
GND_E12 E12
GND_F6 F6
GND_C14 C14
GND_R6 R6
GND_L15 L15
GND_B7 B7
GND_T16 T16
GND_K7 K7
GND_P14 P14

GND

U32 FTG256

1 ADD SILKSCREEN TEXT "3AN DONE" BESIDE LED

3S200AN

DONE_T15 T15
PROG_B_A2 A2
SUSPEND_R16 R16
TCK_A15 A15
TDI_B1 B1
TDO_B16 B16
TMS_B2 B2

SA2_PROG_B
SA2_TCK
SA2_TDI
SA2_TDO
SA2_TMS

DEDICATED SYSTEMACE-2 JTAG

U32 FTG256

UTIL_3V3

R147 330 1/10W 5%

DS22 LED-GRN-SMT

R197 0 1/10W 5%

R102 27.4 1/10W 1%

GND

UTIL_2V5

C823 0.01UF 25V X5R
C94 0.01UF 25V X5R
C822 1UF 25V X5R
C825 470UF 6.3V TANT

GND

UTIL_3V3

C202 0.01UF 25V X5R
C205 0.01UF 25V X5R
C203 0.01UF 25V X5R
C204 0.01UF 25V X5R
C206 0.01UF 25V X5R
C207 0.01UF 25V X5R
C208 0.01UF 25V X5R
C91 0.1UF 25V X5R
C92 0.1UF 25V X5R

GND

VCCO_HP_EXT

C595 0.01UF 25V X5R
C596 0.01UF 25V X5R
C500 1UF 25V X5R
C501 470UF 6.3V TANT

GND

UTIL_3V3

C96 0.1UF 25V X5R
C93 0.1UF 25V X5R
C180 1UF 25V X5R
C179 1UF 25V X5R
C310 470UF 6.3V TANT

GND

VCC1V2

C209 0.01UF 25V X5R
C210 0.01UF 25V X5R
C211 0.01UF 25V X5R
C89 0.1UF 25V X5R
C90 0.1UF 25V X5R
C178 1UF 25V X5R
C312 470UF 6.3V TANT

GND

J207

UTIL_3V3

C169 10UF 25V X5R

ADP123
VIN VOUT
GND
EN ADJ
TSOT_5

U21

R139 6.81K 1/10W 1%

R141 4.7K 1/10W 5%

VCC1V2

C170 10UF 25V X5R

GND

GND

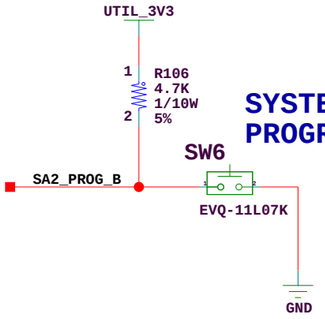
XILINX

Title: SYSTEMACE-2 S3AN CONFIG, PWR/GND
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

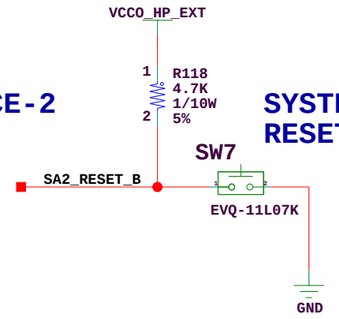
ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-18-2013_16:12	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 29 of 90	Drawn By RN

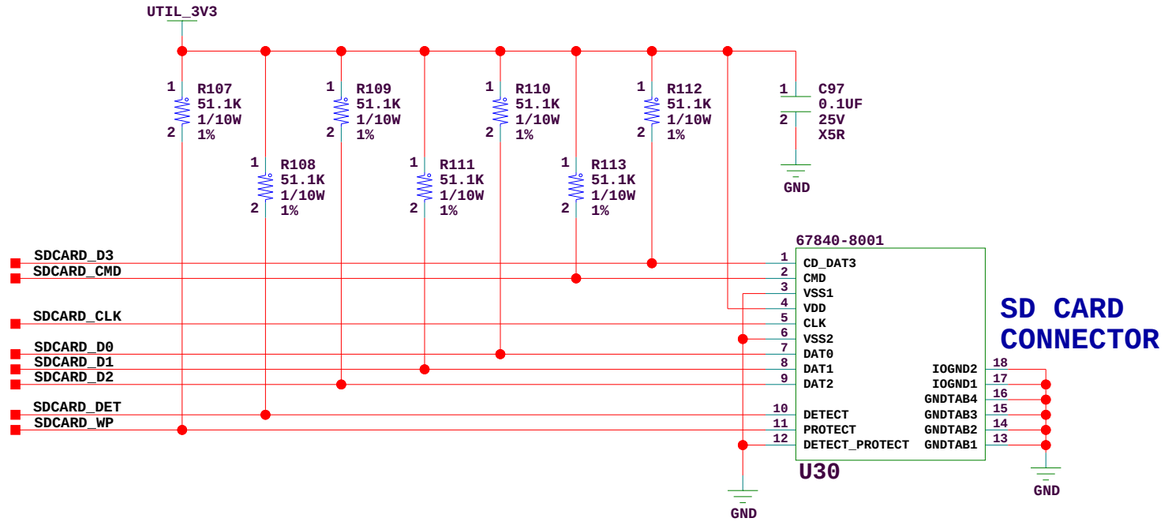
SYSTEMACE-2 - USER INTERFACE



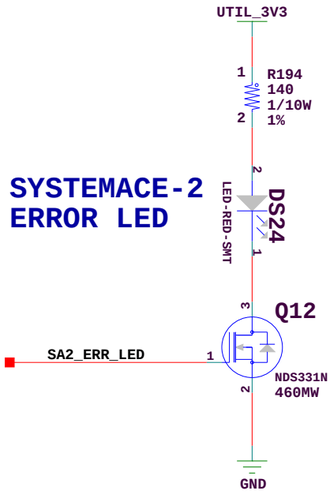
SYSTEMACE-2 PROGRAM



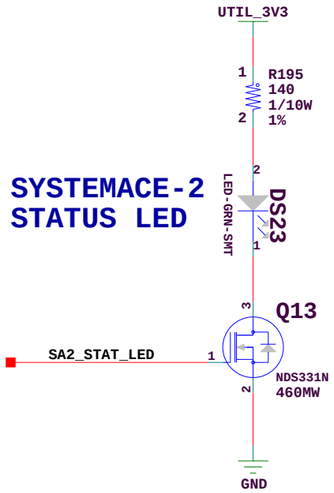
SYSTEMACE-2 RESET



SD CARD CONNECTOR

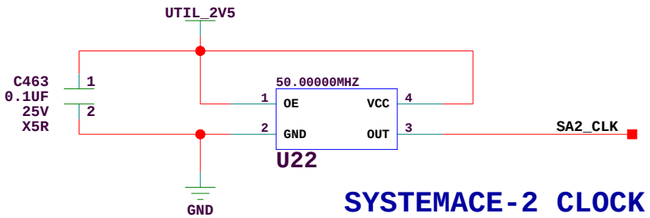


SYSTEMACE-2 ERROR LED

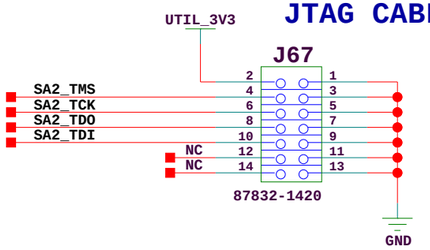


SYSTEMACE-2 STATUS LED

SYSTEMACE-2 CONFIG ADDRESS DIP SWITCH



SYSTEMACE-2 CLOCK



DEDICATED SYSTEMACE-2 JTAG CABLE CONNECTOR

XILINX

Title: SYSTEMACE-2 USER INTERFACE SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
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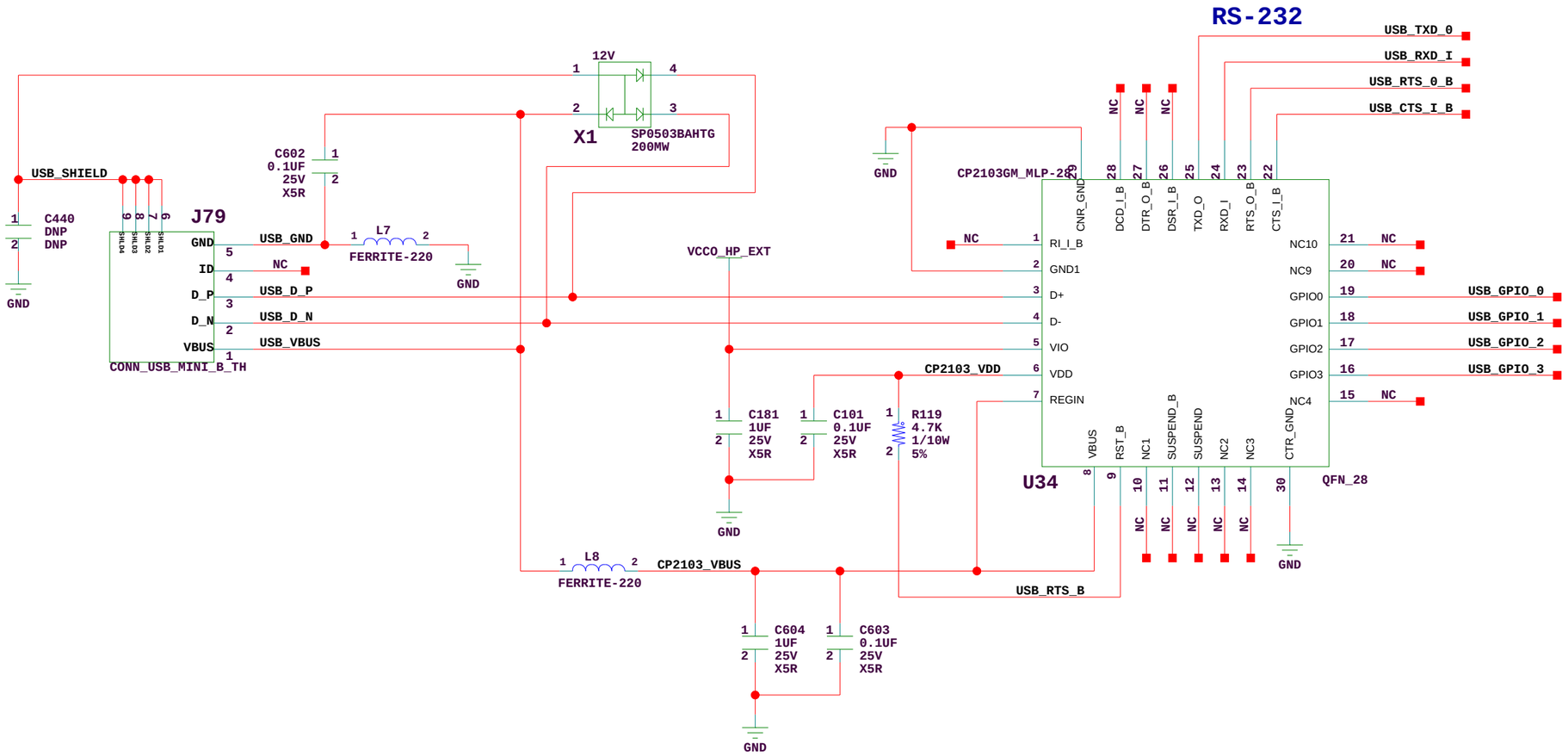
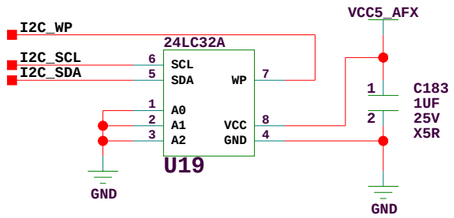
USB/UART BRIDGE

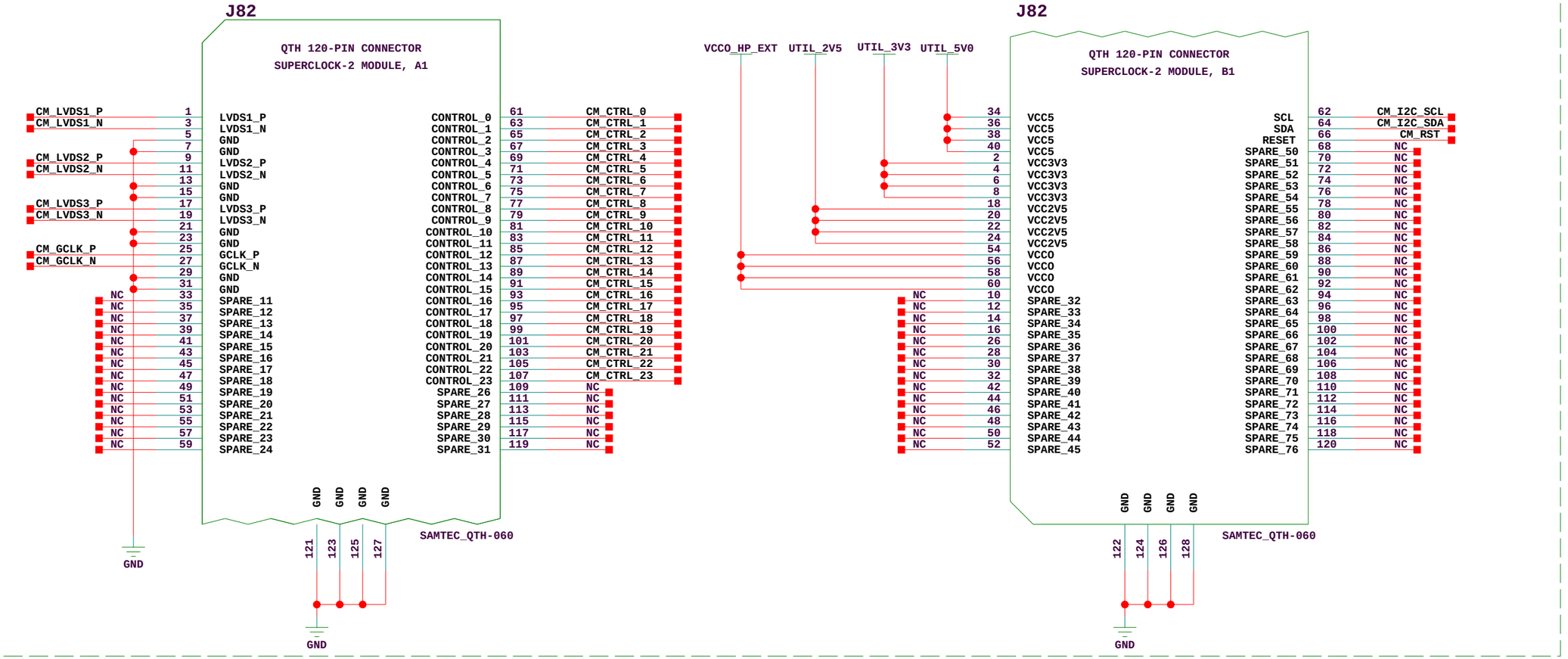


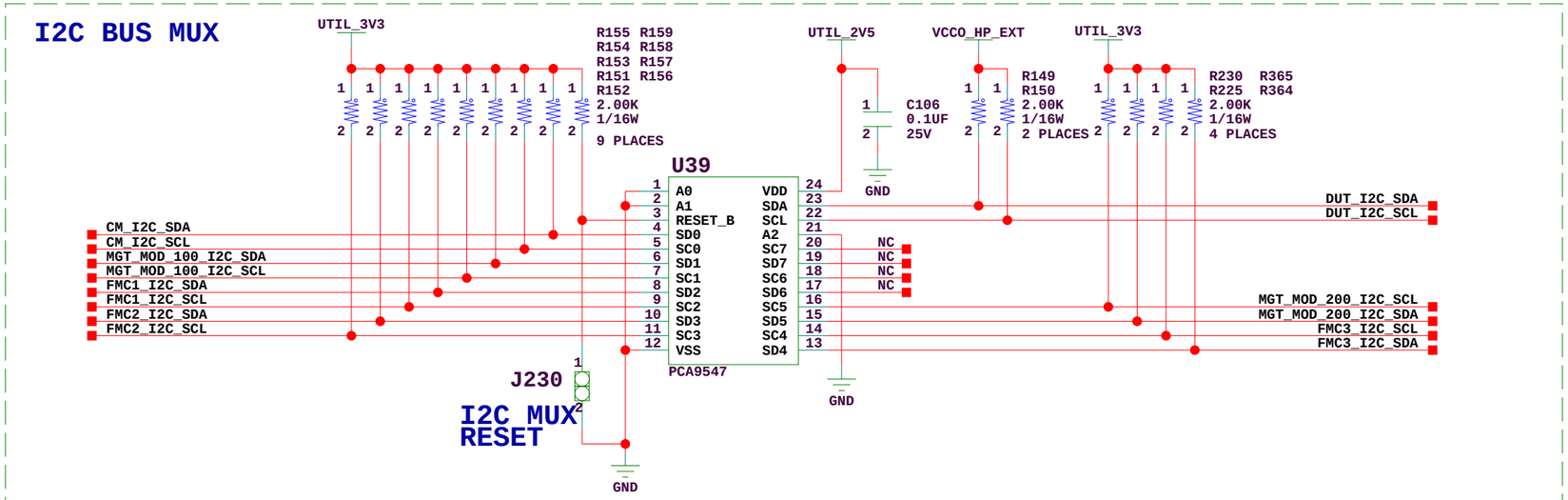
AFX I2C EEPROM



Title: USB/UART, AFX EEPROM SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 31 of 90	Drawn By RN

SUPERCLOCK-2 MODULE INTERFACE

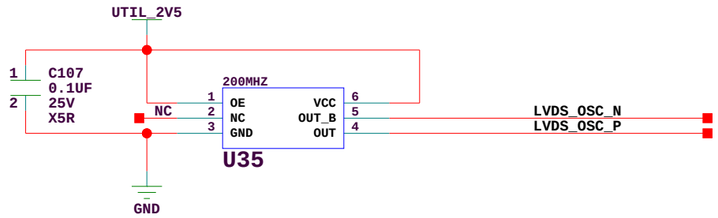




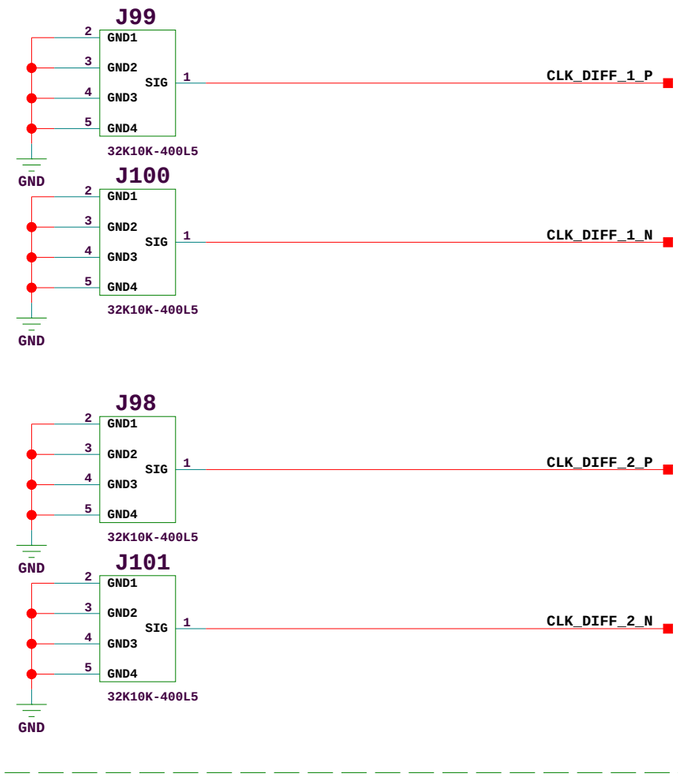
XILINX

Title:	SUPERCLOCK-2 MODULE, I2C BUS MUX SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N:	0431676
		PCB P/N:	1280597
		SCH P/N:	0381429
		TEST P/N:	TSS0XXX
Date:	4-11-2013_15:40	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	32 of 90	Drawn By	RN

200MHz LVDS CLOCK



DIFFERENTIAL SMA CLOCKS



XILINX

Title: USER CLOCKS
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
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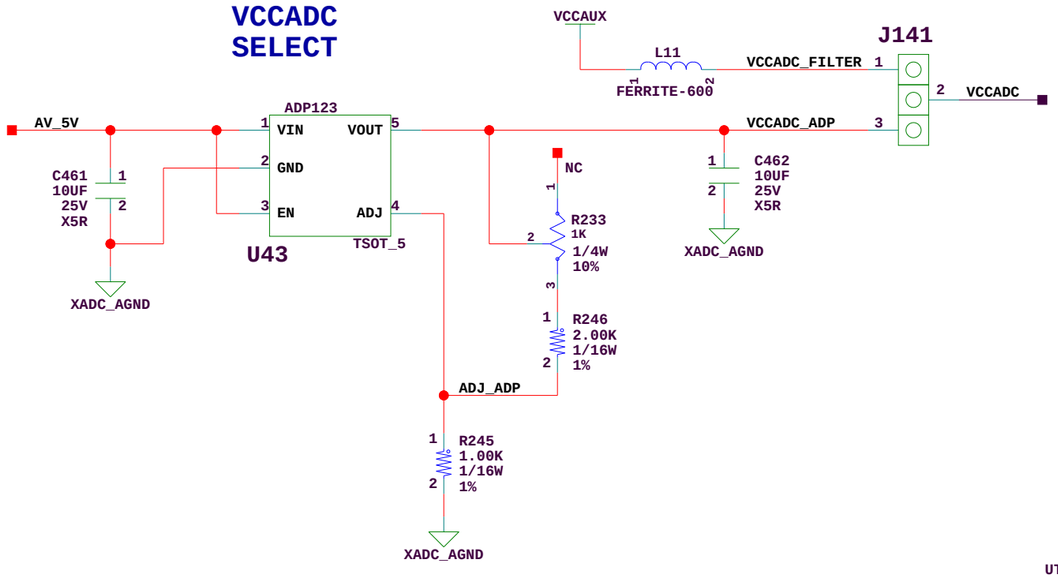
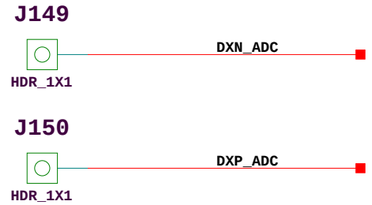
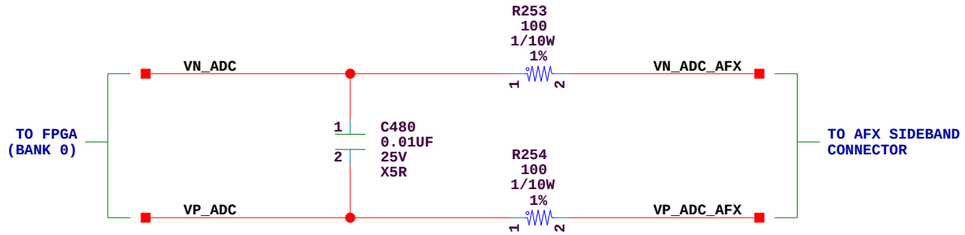
XADC TEST INTERFACE

VCCADC SELECT

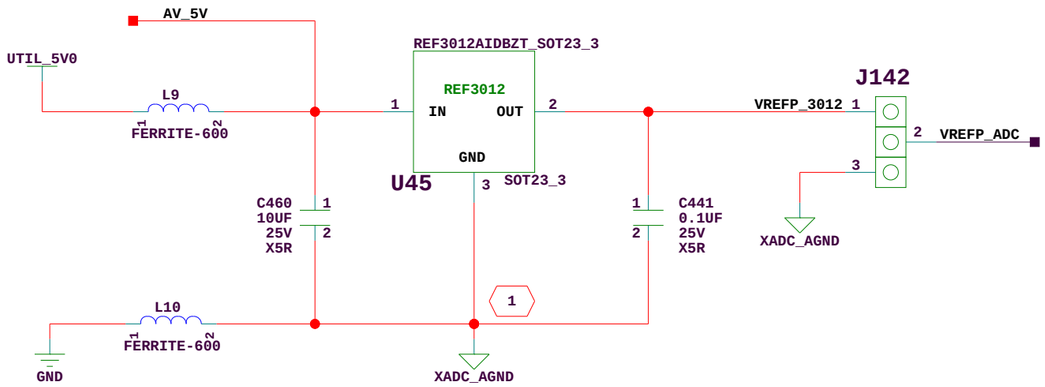


DUT THERMAL DIODE TEST POINTS





VREF SELECT



1 STAR CONNECTION, SEE XADC

XILINX

Title: XADC INTERFACE SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
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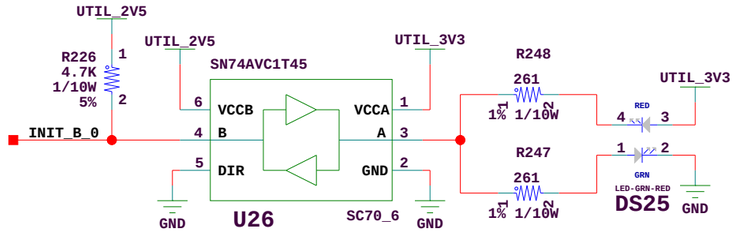
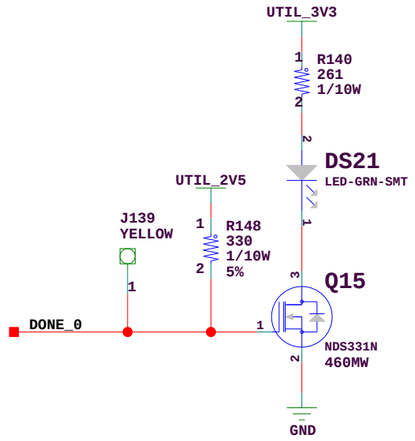
CONFIGURATION AND USER I/O

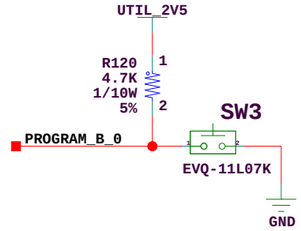
INIT_B LED



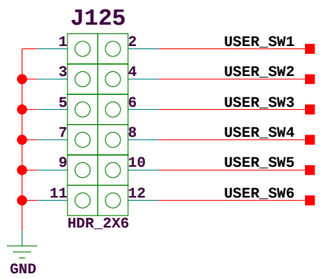
DONE LED



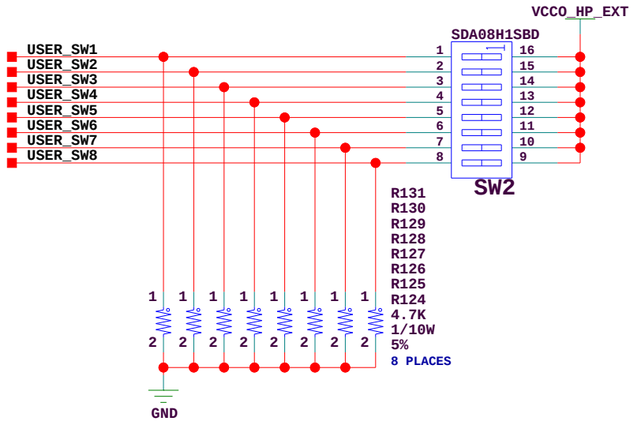
PROG_B PUSH BUTTON



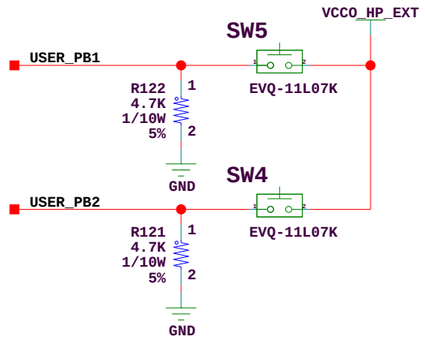
I/O HEADER



USER SWITCHES



USER PUSH BUTTONS



XILINX

Title:	CONFIG AND USER I/O SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: PCB P/N: SCH P/N: TEST P/N:	0431676 1280597 0381429 TSS0XXX
Date:	4-11-2013_15:40	Ver:	1.0
Sheet Size:	B	Rev:	01
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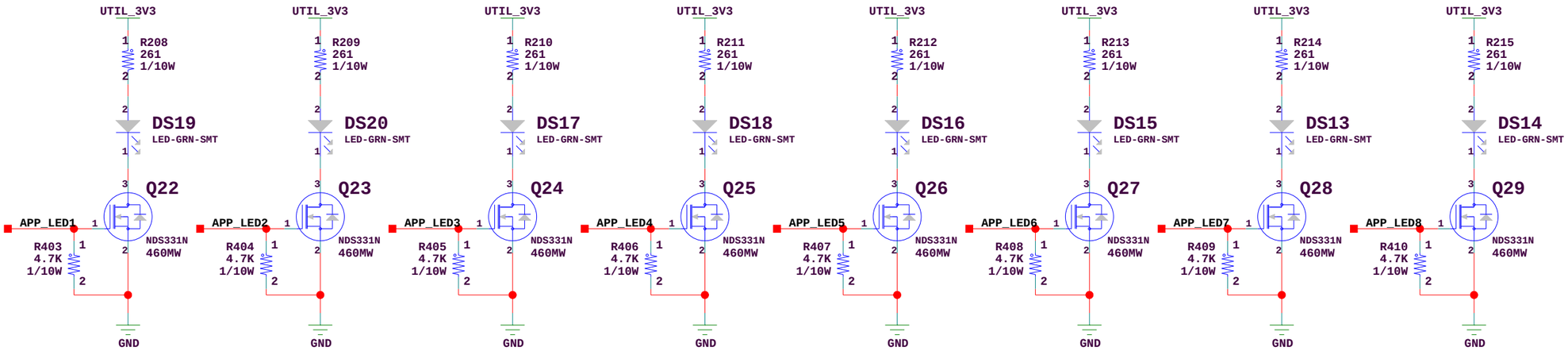
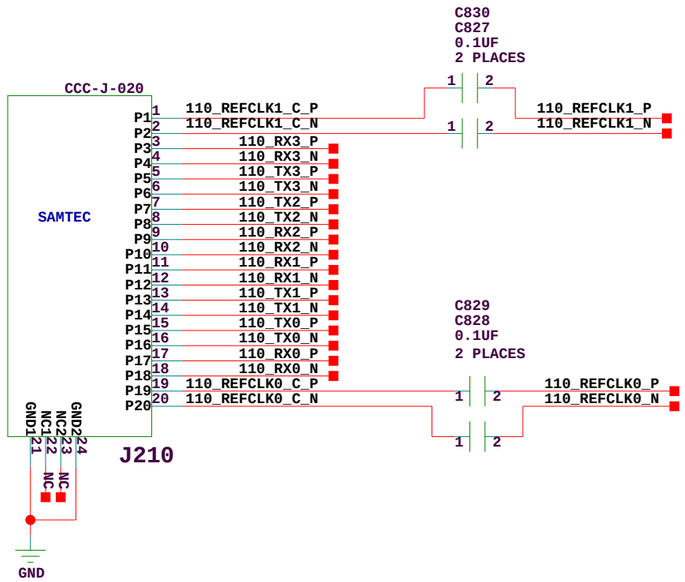
USER APPLICATION LEDS

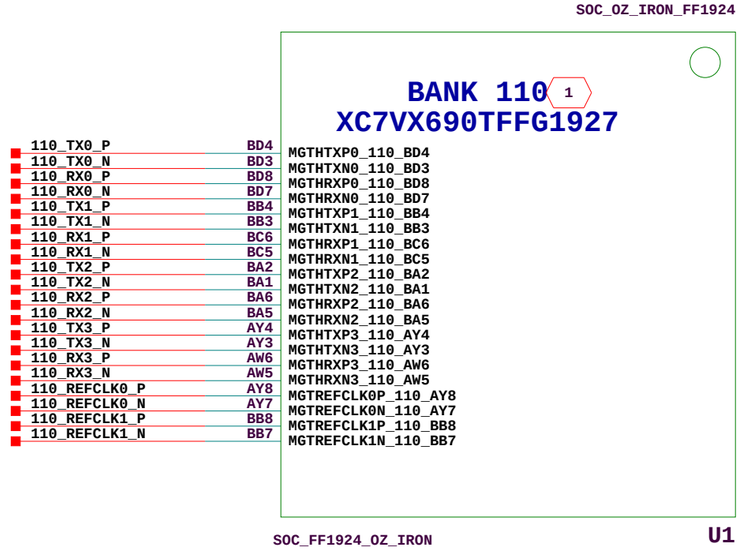


XILINX

Title: USER APPLICATION LEDS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40		Ver: 1.0
Sheet Size: B		Rev: 01
Sheet 36 of 90		Drawn By RN

MGT BANK 110



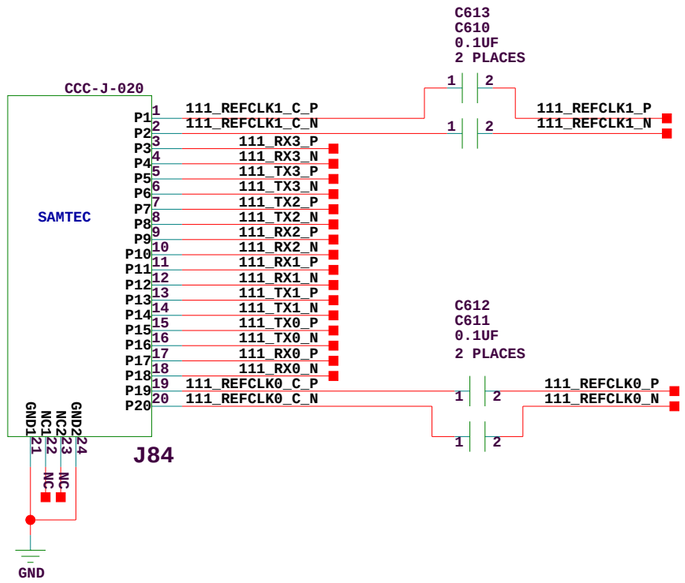


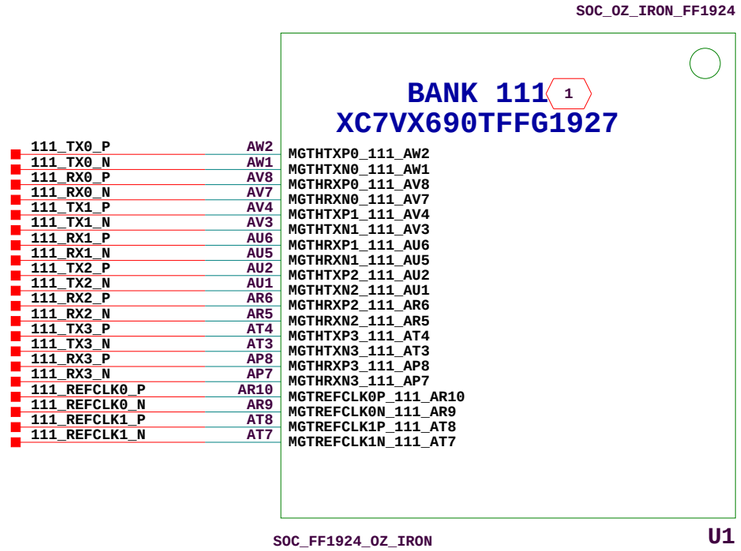
1 THIS QUAD IS NOT AVAILABLE IN THE X485T AND X415T DEVICES.

XILINX

Title: MGT BANK 110 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 37 of 90	Drawn By RN

MGT BANK 111



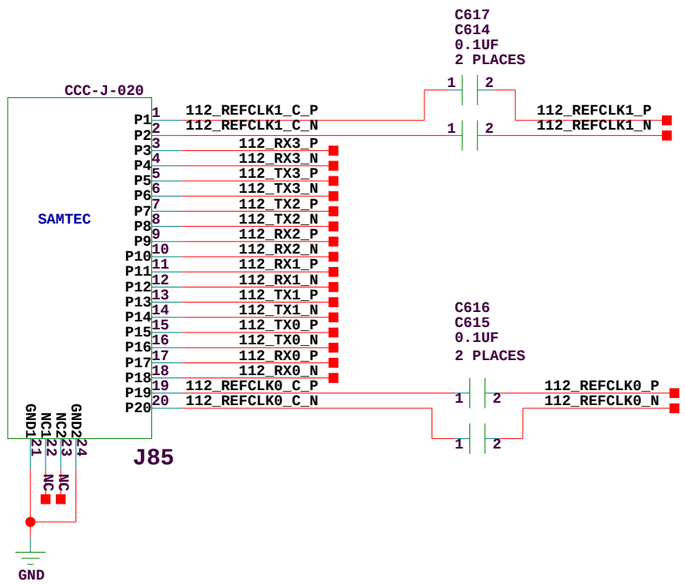


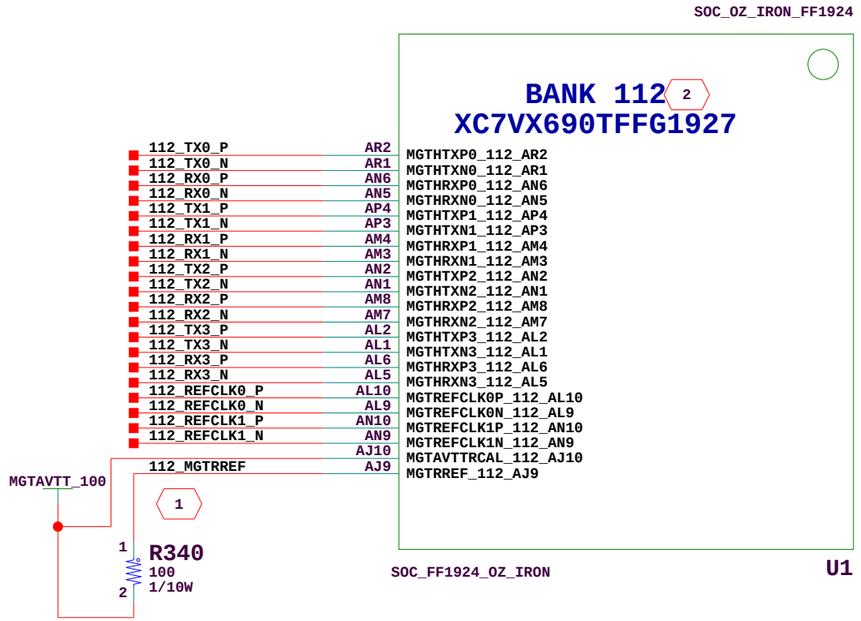
1 THIS QUAD IS NOT AVAILABLE IN THE X485T AND X415T DEVICES.

XILINX

Title: MGT BANK 111 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 38 of 90	Drawn By RN

MGT BANK 112



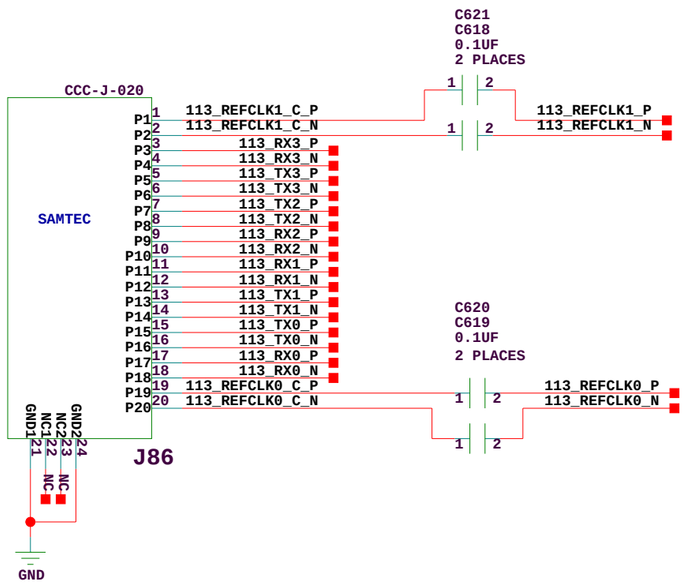


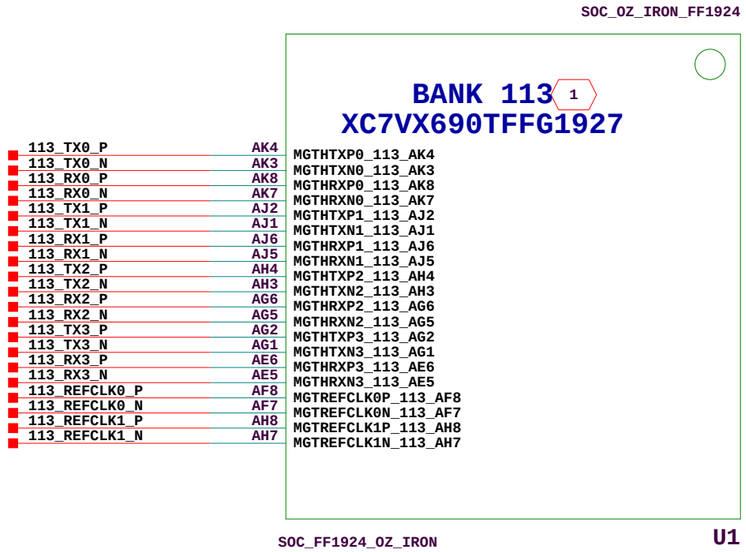
1. TRACE LENGTH FROM RESISTOR PINS TO FPGA PINS MGTRREF AND MGTAVTTRCAL MUST BE OF EQUAL LENGTH AND GEOMETRY.
2. THIS QUAD IS NOT AVAILABLE IN THE X485T AND X415T DEVICES.

XILINX

Title: MGT BANK 112 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 39 of 90	Drawn By RN

MGT BANK 113



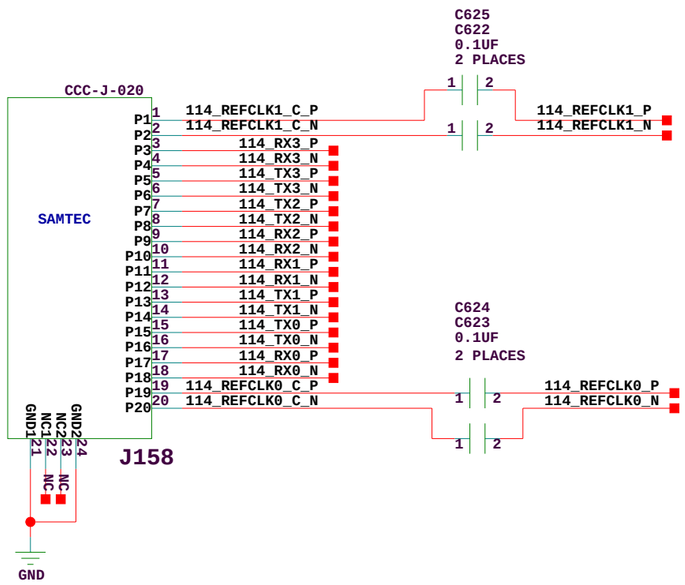


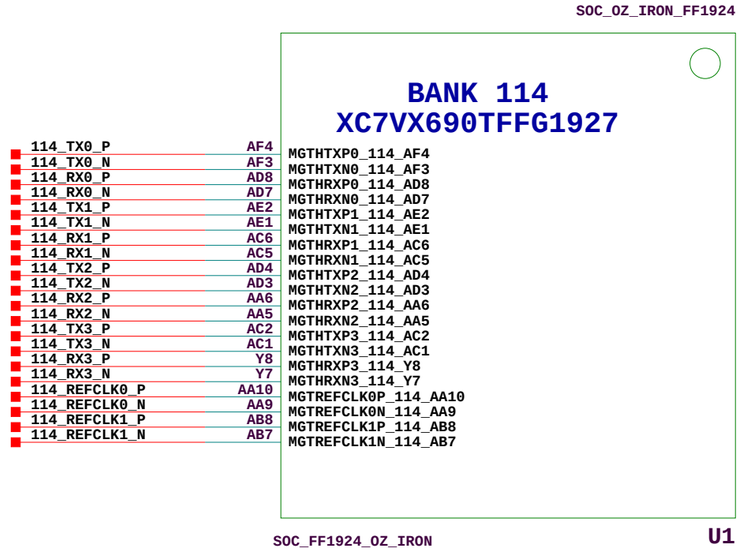
1 THIS QUAD IS NOT AVAILABLE IN THE X415T DEVICE.

XILINX

Title: MGT BANK 113 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 40 of 90	Drawn By RN

MGT BANK 114

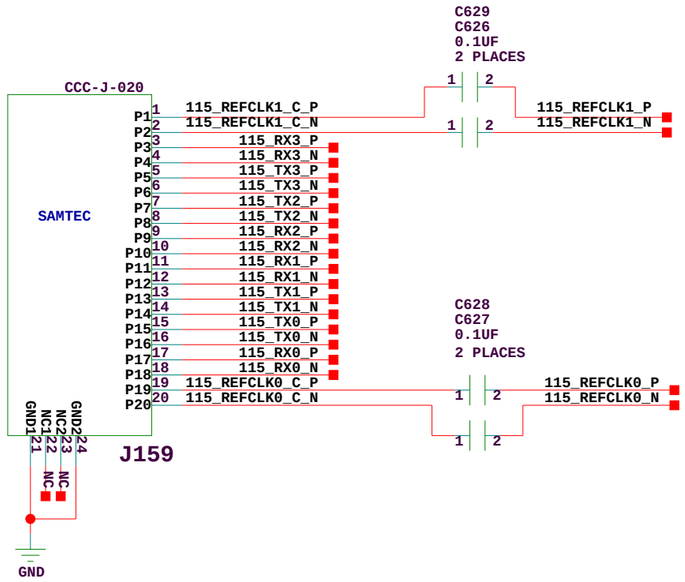


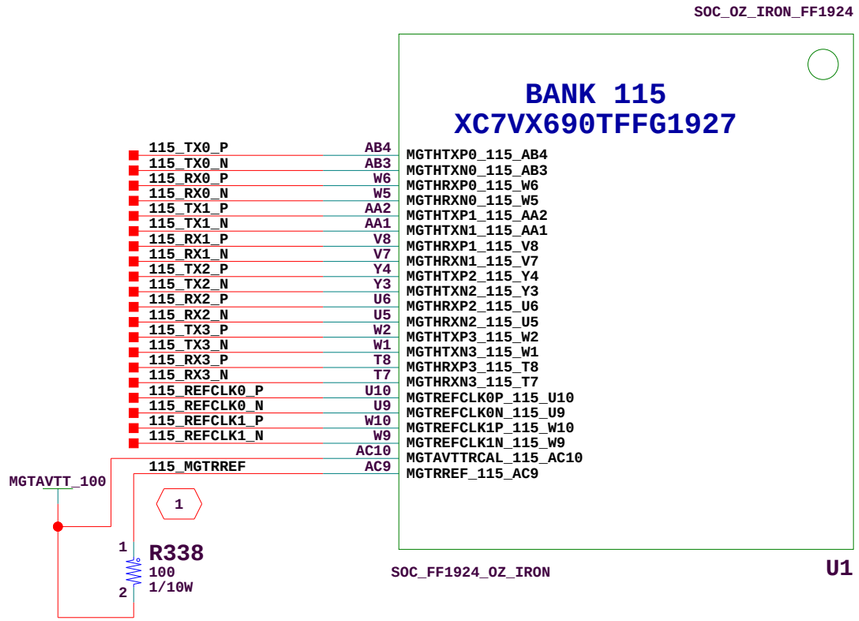


XILINX

Title: MGT BANK 114 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 41 of 90		Drawn By RN	

MGT BANK 115



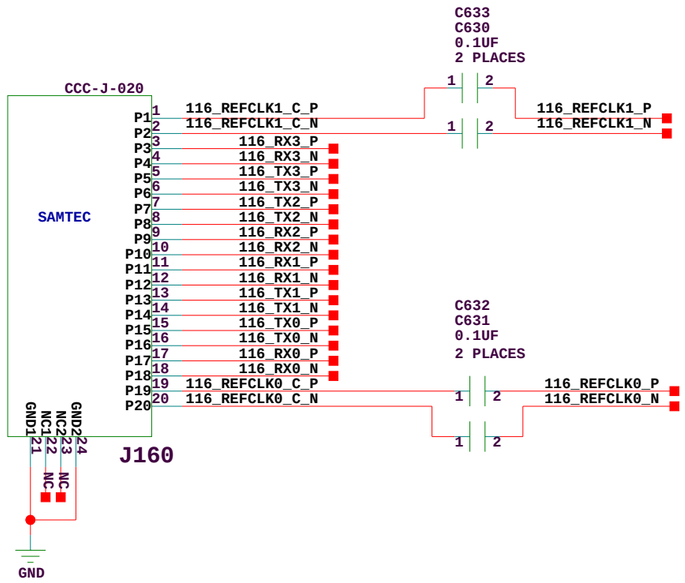


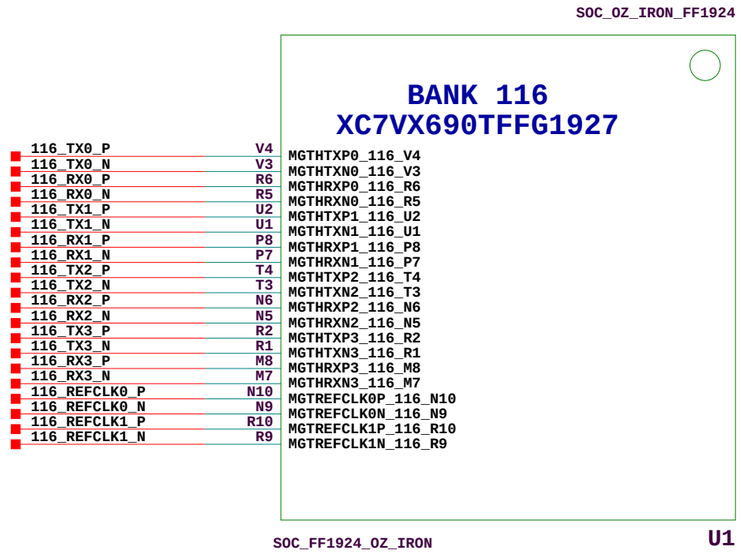
1 TRACE LENGTH FROM RESISTOR PINS TO FPGA PINS MGTRREF AND MGTAVTTRCAL MUST BE OF EQUAL LENGTH AND GEOMETRY.

XILINX

Title: MGT BANK 115 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 42 of 90	Drawn By RN

MGT BANK 116

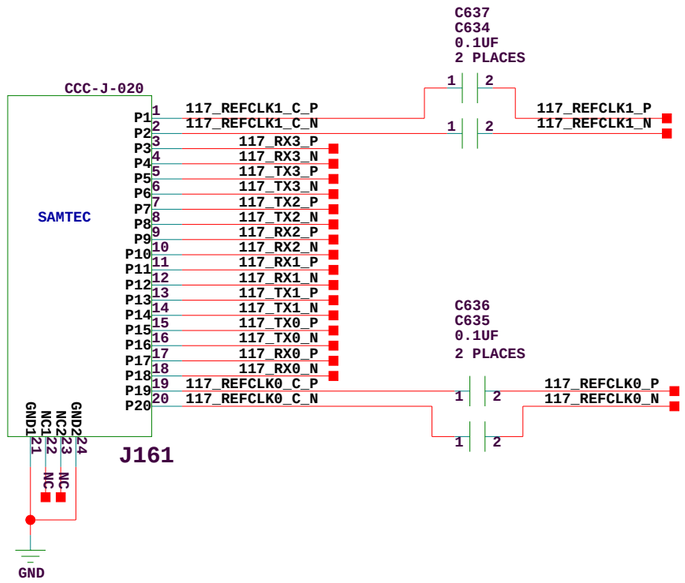


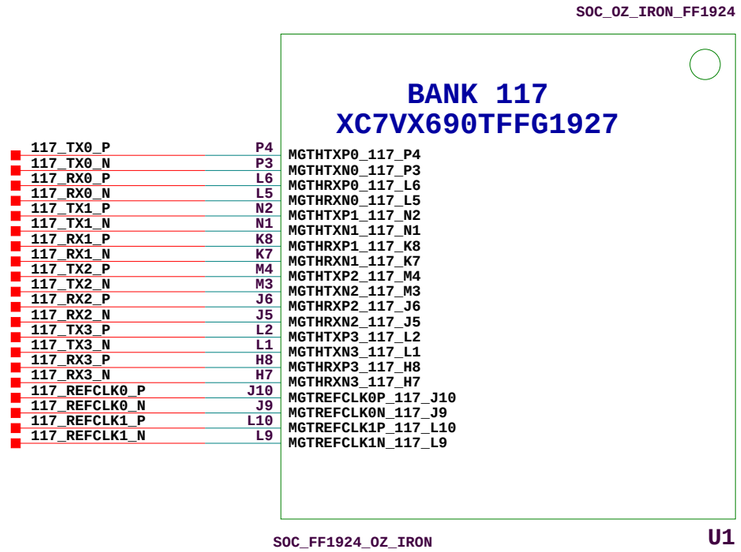


XILINX

Title: MGT BANK 116 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 43 of 90		Drawn By RN	

MGT BANK 117

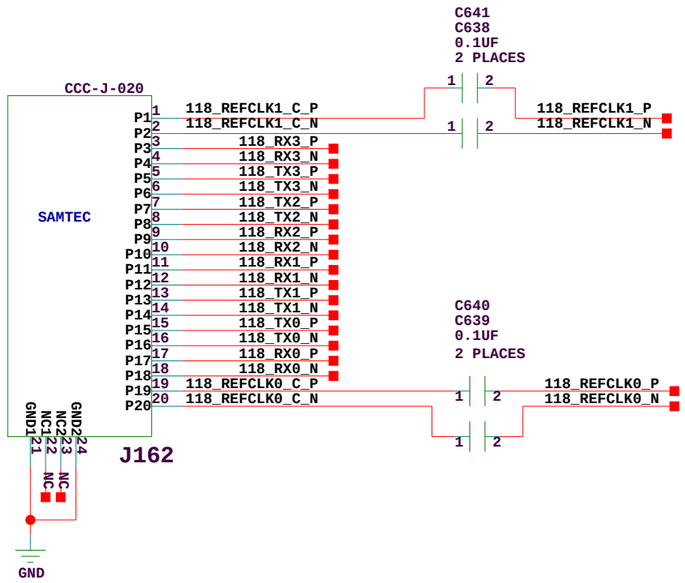


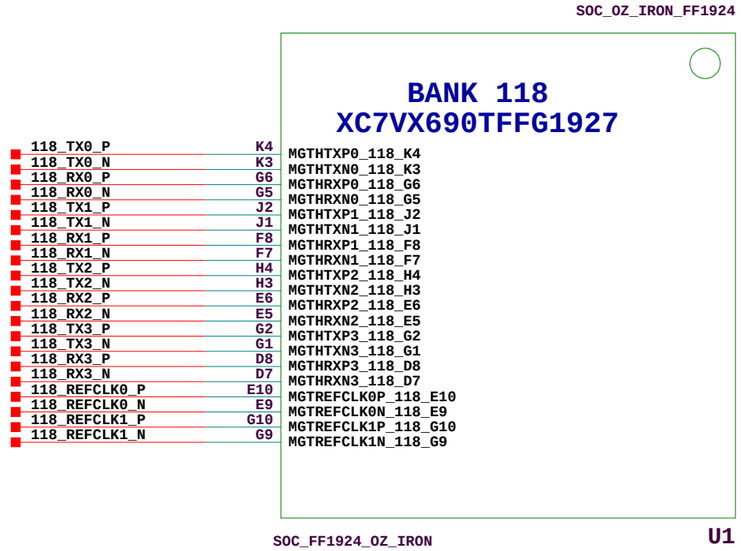


XILINX

Title: MGT BANK 117 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 44 of 90		Drawn By RN	

MGT BANK 118

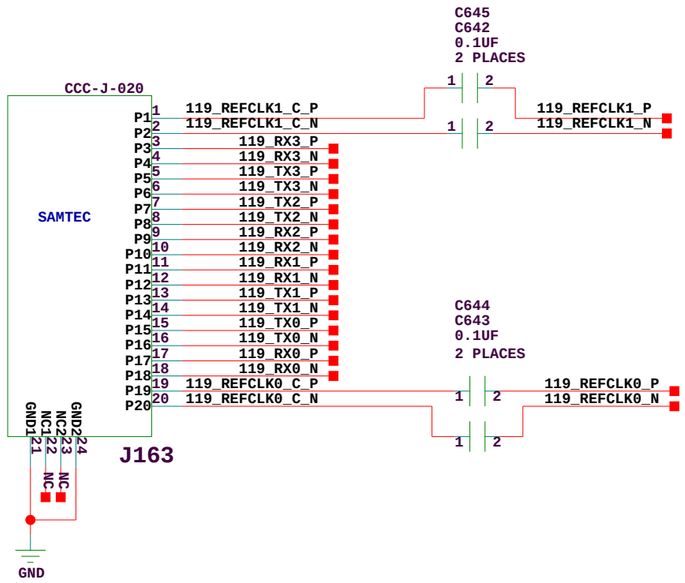


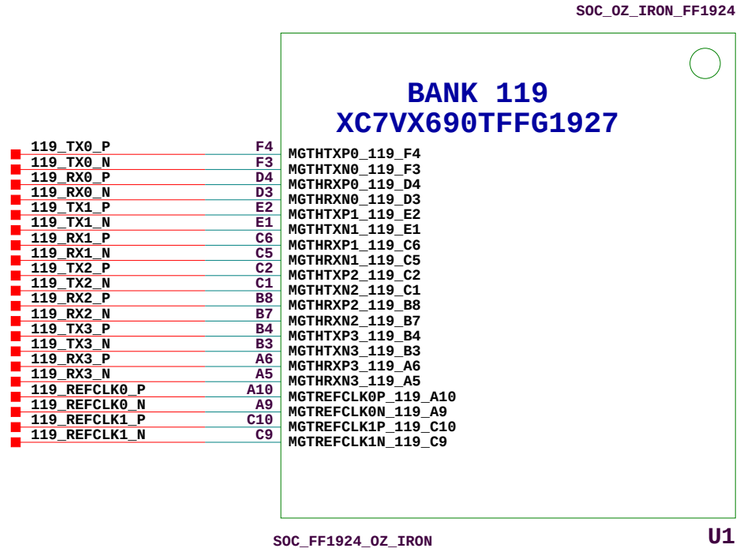


XILINX

Title: MGT BANK 118 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 45	of 90	Drawn By RN	

MGT BANK 119

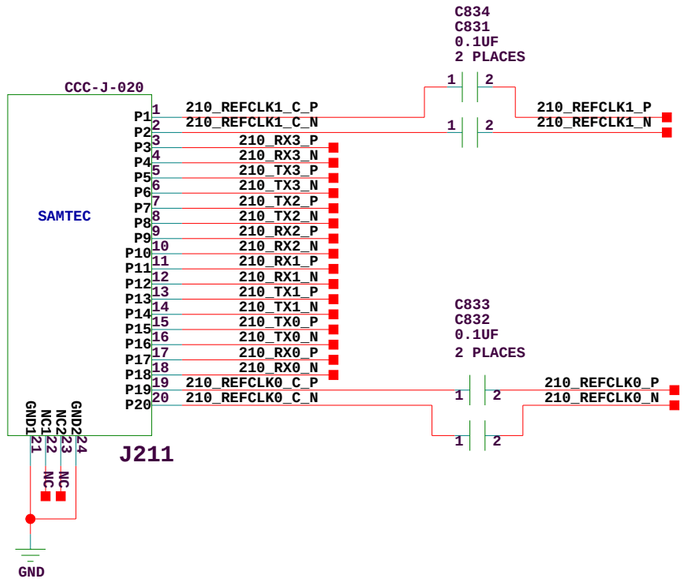


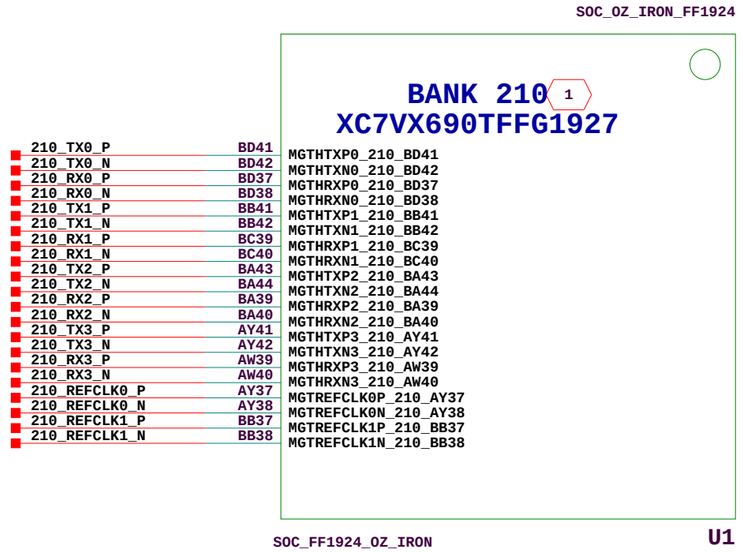


XILINX

Title: MGT BANK 119 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 46 of 90		Drawn By RN	

MGT BANK 210



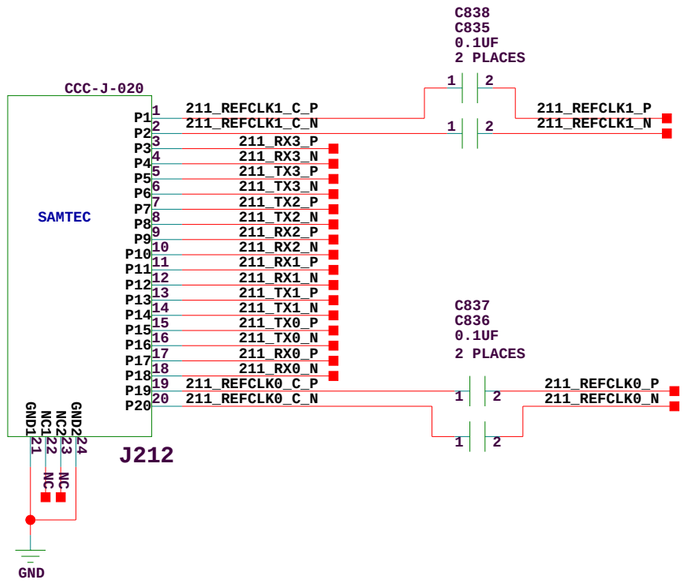


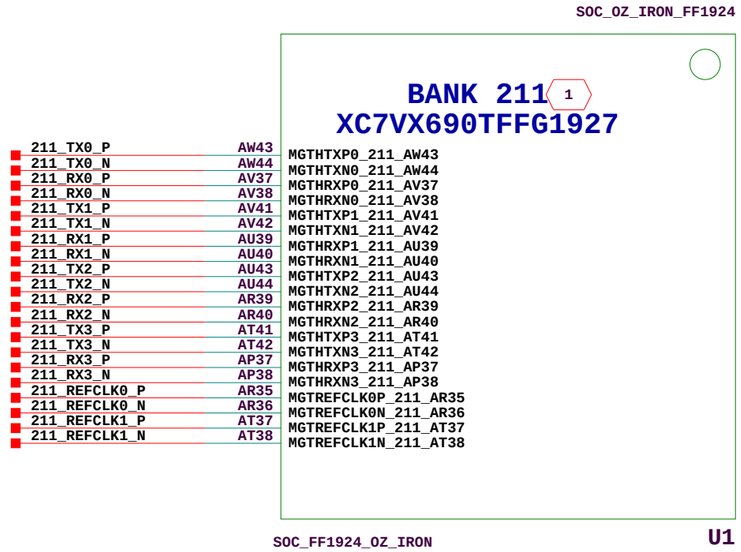
1 THIS QUAD IS NOT AVAILABLE IN THE X485T AND X415T DEVICES.

XILINX

Title: MGT BANK 210 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 47 of 90	Drawn By RN

MGT BANK 211





1 THIS QUAD IS NOT AVAILABLE IN THE X485T AND X415T DEVICES.

XILINX

Title: MGT BANK 211 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
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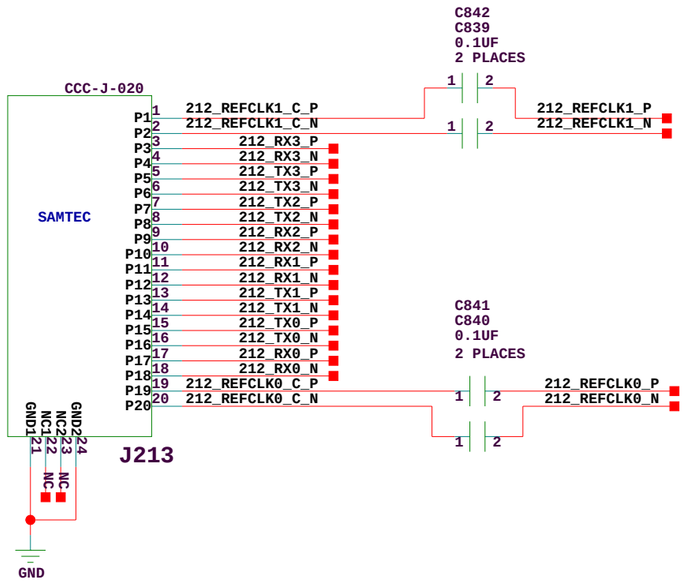
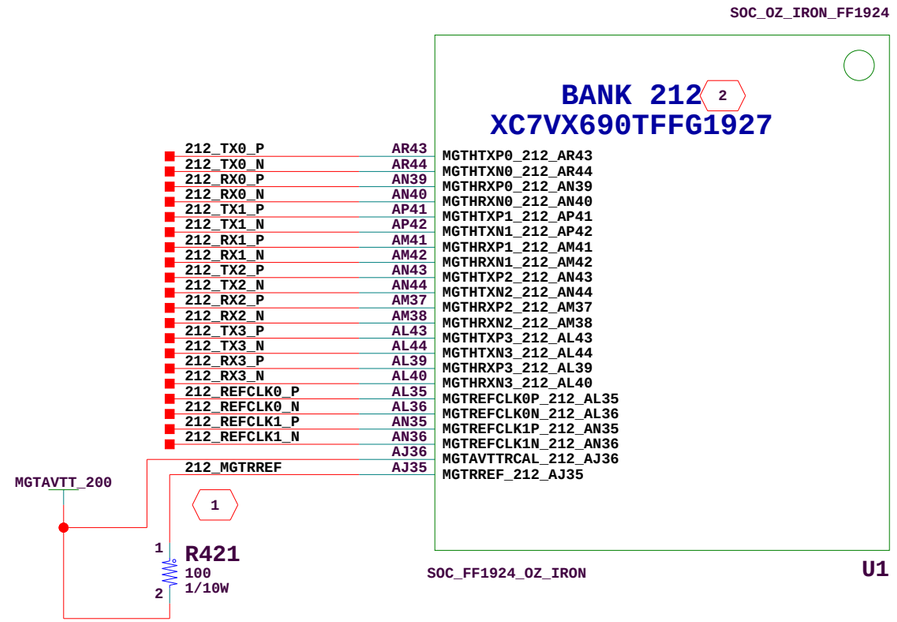
MGT BANK 212





1. TRACE LENGTH FROM RESISTOR PINS TO FPGA PINS MGTRREF AND MGTAVTTRCAL MUST BE OF EQUAL LENGTH AND GEOMETRY.
2. THIS QUAD IS NOT AVAILABLE IN THE X485T AND X415T DEVICES.

XILINX

Title: MGT BANK 212 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
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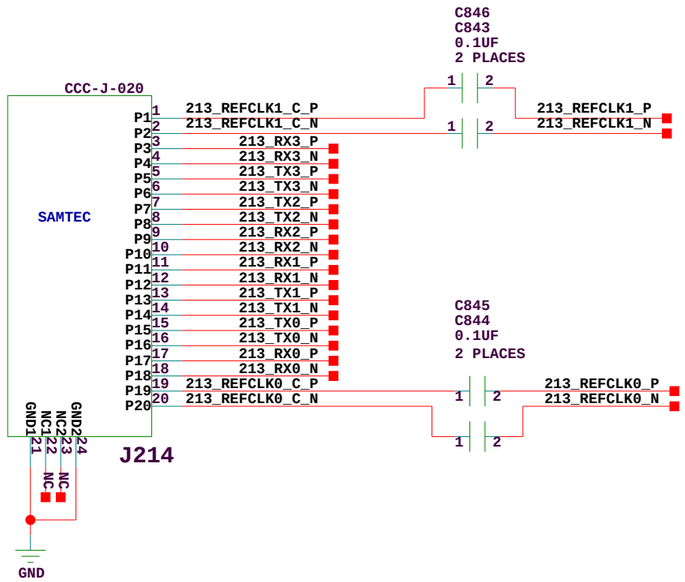
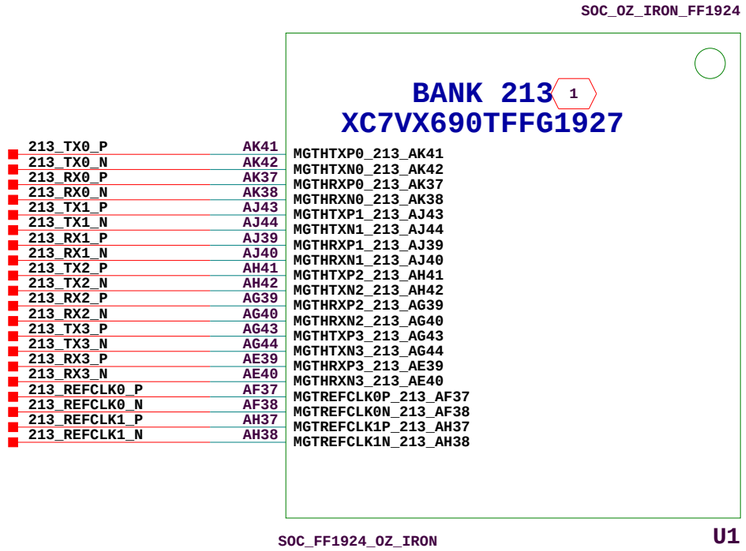
MGT BANK 213





1 THIS QUAD IS NOT AVAILABLE IN THE X415T DEVICE.

XILINX

Title: MGT BANK 213 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
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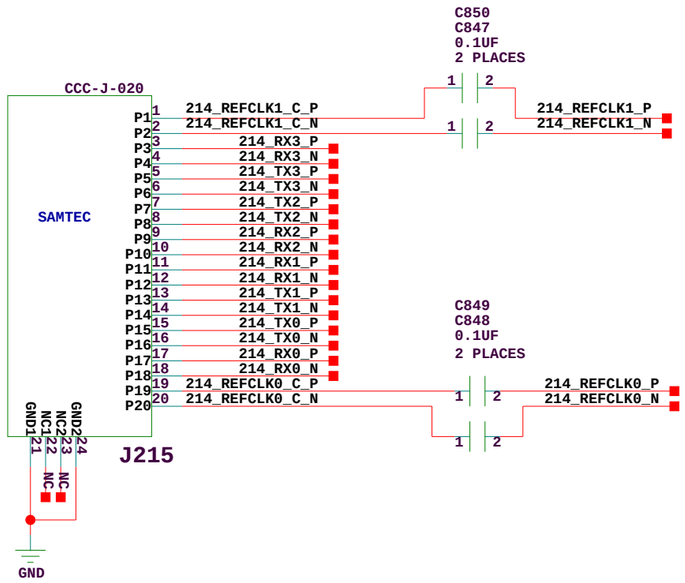
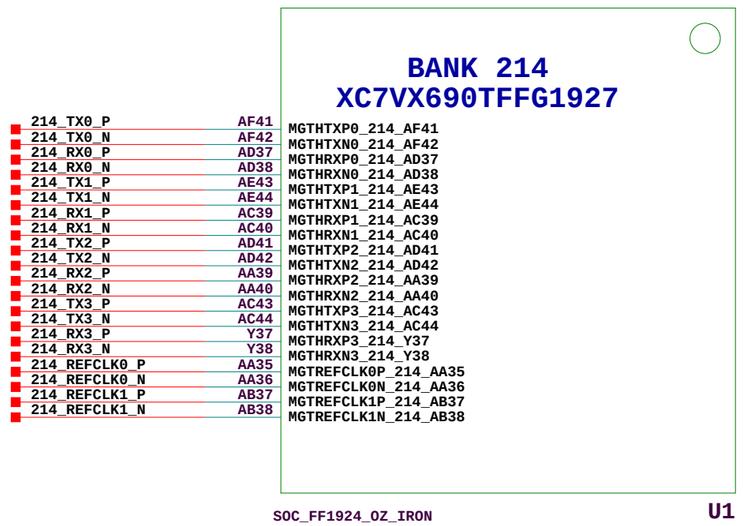
MGT BANK 214



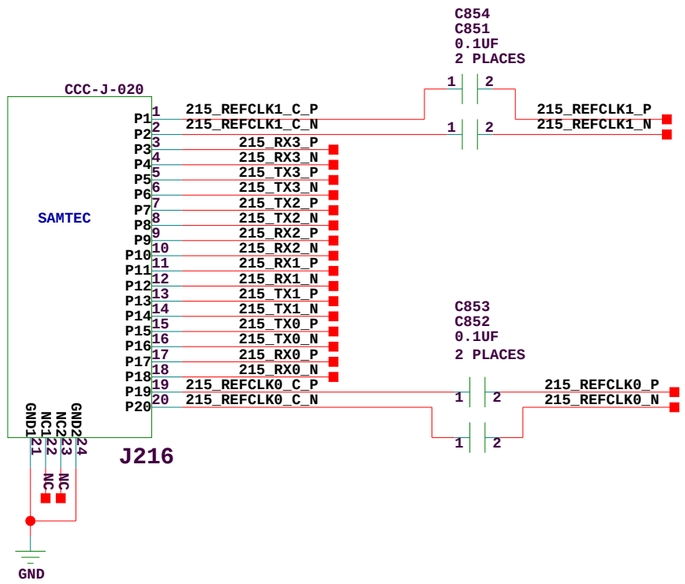
SOC_OZ_IRON_FF1924

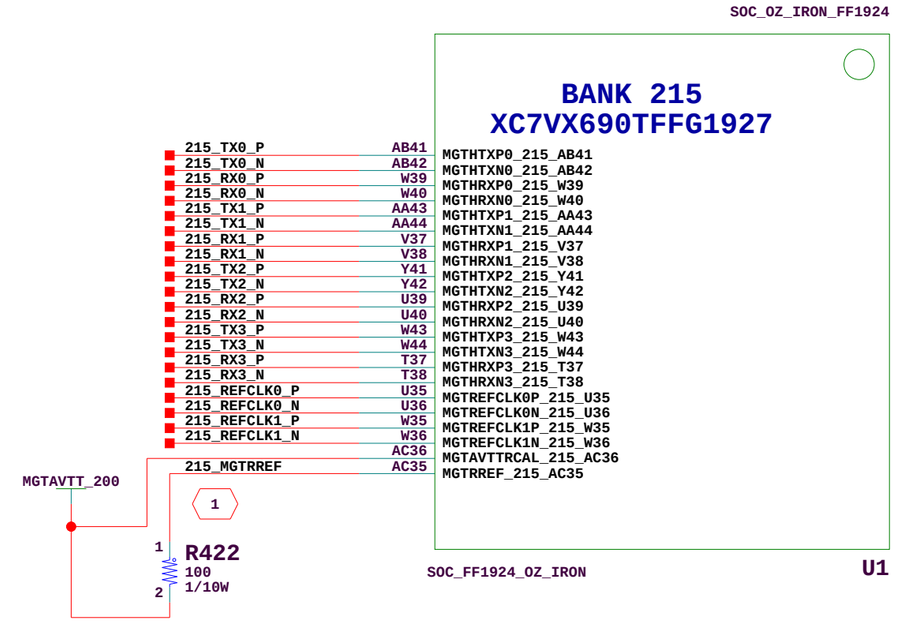


XILINX

Title: MGT BANK 214 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 51 of 90		Drawn By RN	

MGT BANK 215





1 TRACE LENGTH FROM RESISTOR PINS TO FPGA PINS MGTRREF AND MGTAVTTRCAL MUST BE OF EQUAL LENGTH AND GEOMETRY.

XILINX

Title: MGT BANK 215 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
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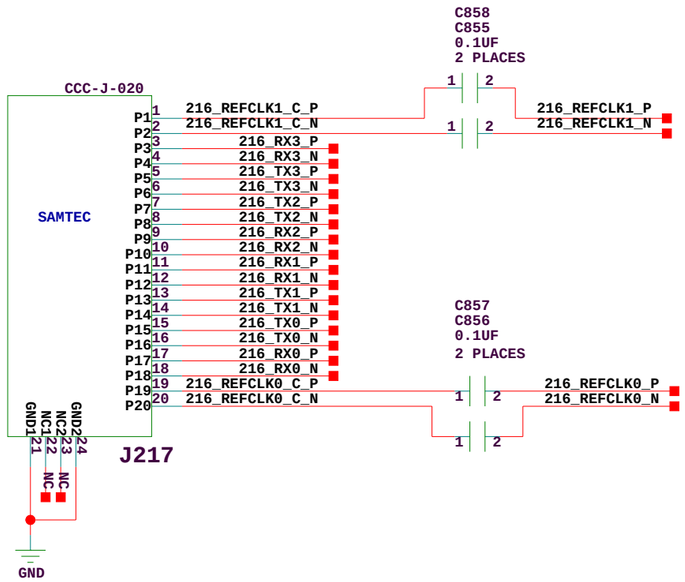
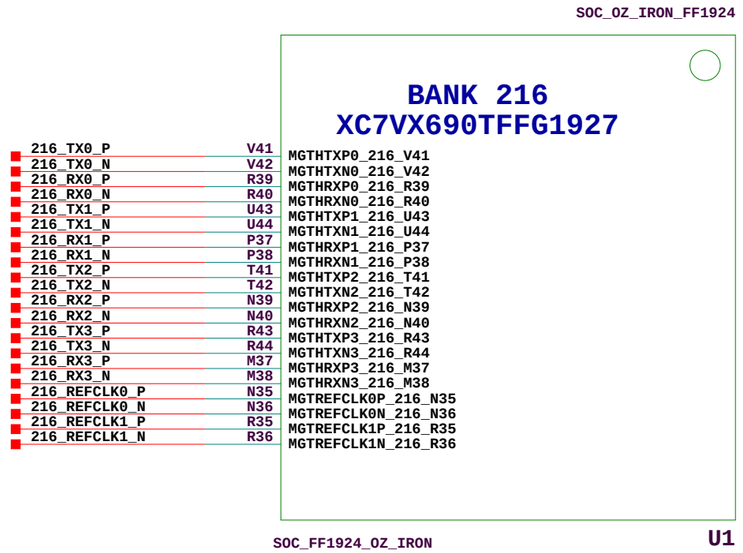
MGT BANK 216





XILINX

Title: MGT BANK 216 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
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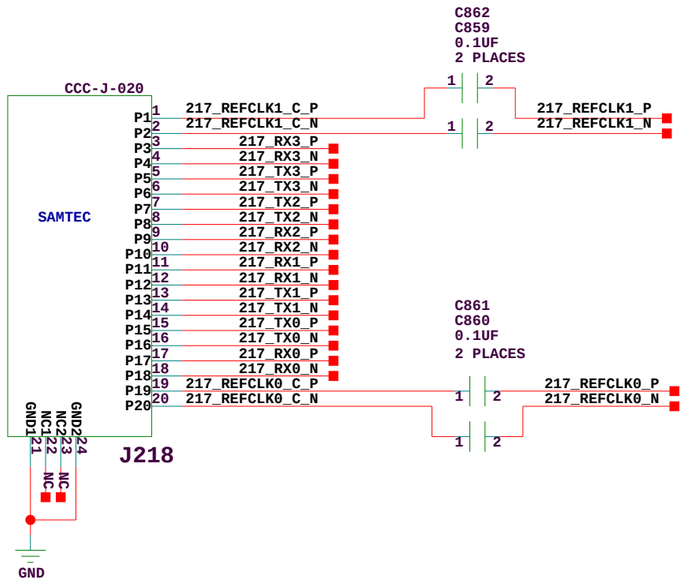
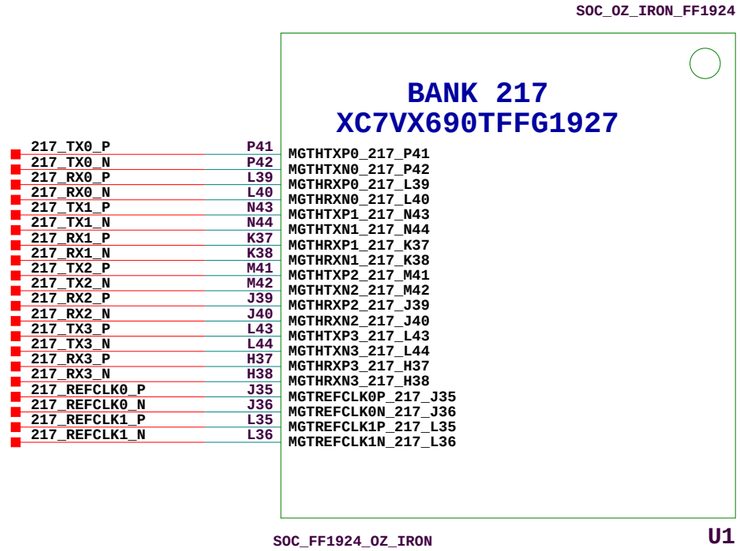
MGT BANK 217





XILINX

Title: MGT BANK 217 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
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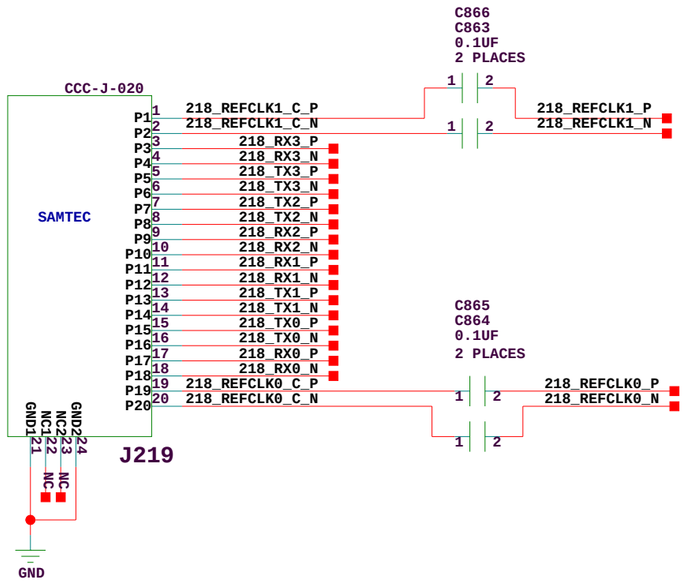
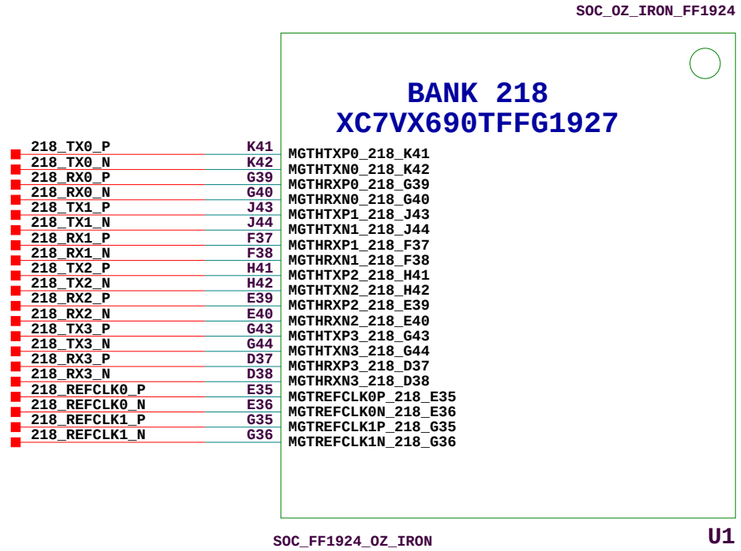
MGT BANK 218





XILINX

Title: MGT BANK 218 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
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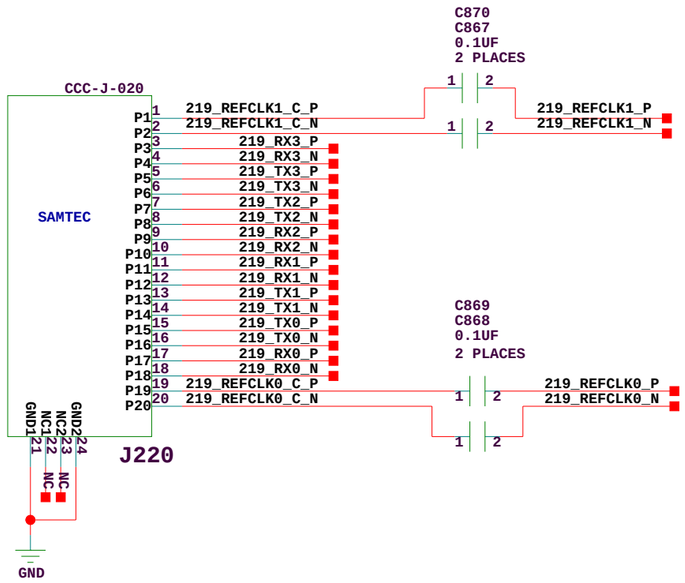
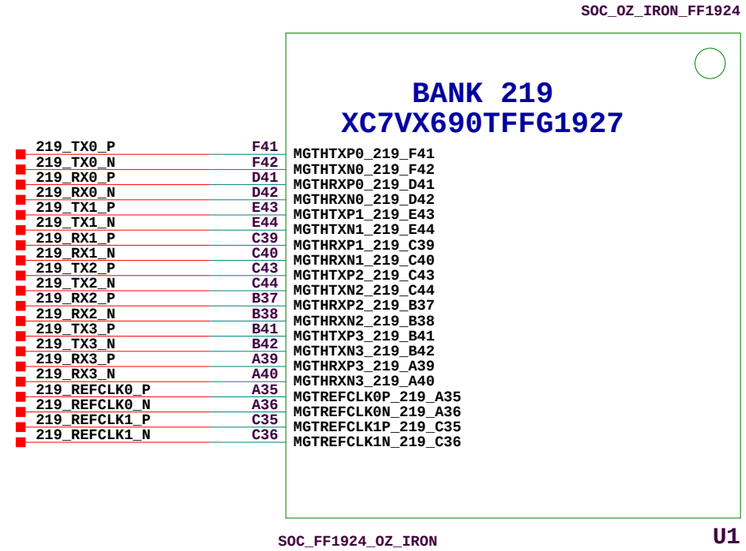
MGT BANK 219





XILINX

Title: MGT BANK 219 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
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MGT POWER, MGTAVCC DECOUPLING

XILINX

Title: MGT POWER / DECOUPLING SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
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MGT POWER, MGTAVTT DECOUPLING

SOC_OZ_IRON_FF1924

BANK MGTAVTT_G9
XC7VX690TFFG1927

MGTAVTT_G9_BC3	BC3
MGTAVTT_G9_BB5	BB5
MGTAVTT_G9_AY5	AY5
MGTAVTT_G9_AW3	AW3
MGTAVTT_G9_AV5	AV5
MGTAVTT_G9_AT5	AT5
MGTAVTT_G9_AR3	AR3
MGTAVTT_G9_AP5	AP5
MGTAVTT_G9_AM5	AM5
MGTAVTT_G9_AL3	AL3

MGTAVTT_100

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTAVTT_G10
XC7VX690TFFG1927

MGTAVTT_G10_Y5	Y5
MGTAVTT_G10_W3	W3
MGTAVTT_G10_V5	V5
MGTAVTT_G10_T5	T5
MGTAVTT_G10_R3	R3
MGTAVTT_G10_AJ3	AJ3
MGTAVTT_G10_AH5	AH5
MGTAVTT_G10_AG3	AG3
MGTAVTT_G10_AF5	AF5
MGTAVTT_G10_AD5	AD5
MGTAVTT_G10_AC3	AC3
MGTAVTT_G10_AB5	AB5

MGTAVTT_100

Y5 → MGTAVTT_100_SPY_P

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTAVTT_G11
XC7VX690TFFG1927

MGTAVTT_G11_P5	P5
MGTAVTT_G11_M5	M5
MGTAVTT_G11_L3	L3
MGTAVTT_G11_K5	K5
MGTAVTT_G11_H5	H5
MGTAVTT_G11_G3	G3
MGTAVTT_G11_F5	F5
MGTAVTT_G11_D5	D5
MGTAVTT_G11_C3	C3
MGTAVTT_G11_B5	B5

MGTAVTT_100

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTAVTT_G19
XC7VX690TFFG1927

MGTAVTT_G19_BC42	BC42
MGTAVTT_G19_BB40	BB40
MGTAVTT_G19_AY40	AY40
MGTAVTT_G19_AW42	AW42
MGTAVTT_G19_AV40	AV40
MGTAVTT_G19_AT40	AT40
MGTAVTT_G19_AR42	AR42
MGTAVTT_G19_AP40	AP40
MGTAVTT_G19_AM40	AM40
MGTAVTT_G19_AL42	AL42

MGTAVTT_200

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTAVTT_G20
XC7VX690TFFG1927

MGTAVTT_G20_Y40	Y40
MGTAVTT_G20_W42	W42
MGTAVTT_G20_V40	V40
MGTAVTT_G20_T40	T40
MGTAVTT_G20_R42	R42
MGTAVTT_G20_AJ42	AJ42
MGTAVTT_G20_AH40	AH40
MGTAVTT_G20_AG42	AG42
MGTAVTT_G20_AF40	AF40
MGTAVTT_G20_AD40	AD40
MGTAVTT_G20_AC42	AC42
MGTAVTT_G20_AB40	AB40

MGTAVTT_200

Y40 → MGTAVTT_200_SPY_P

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTAVTT_G21
XC7VX690TFFG1927

MGTAVTT_G21_P40	P40
MGTAVTT_G21_M40	M40
MGTAVTT_G21_L42	L42
MGTAVTT_G21_K40	K40
MGTAVTT_G21_H40	H40
MGTAVTT_G21_G42	G42
MGTAVTT_G21_F40	F40
MGTAVTT_G21_D40	D40
MGTAVTT_G21_C42	C42
MGTAVTT_G21_B40	B40

MGTAVTT_200

U1 SOC_FF1924_OZ_IRON

MGTAVTT_100

1	C192 4.7UF 10V	2	1	C193 4.7UF 10V	2
			1	C973 4.7UF 10V	2

GND

MGTAVTT_200

1	C974 4.7UF 10V	2	1	C975 4.7UF 10V	2
			1	C976 4.7UF 10V	2

GND

XILINX

Title: MGT POWER / DECOUPLING
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-12-2013_11:36	Ver: 1.0
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MGT POWER, MGTAVCCAUX DECOUPLING

SOC_OZ_IRON_FF1924

BANK MGTVCCAUX_G9
XC7VX690TFFG1927

MGTVCCAUX_G9_AM10 — AM10 — MGTVCCAUX_100

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTVCCAUX_G19
XC7VX690TFFG1927

MGTVCCAUX_G19_AM35 — AM35 — MGTVCCAUX_200

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTVCCAUX_G10
XC7VX690TFFG1927

MGTVCCAUX_G10_V10 — V10
MGTVCCAUX_G10_T10 — T10
MGTVCCAUX_100

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTVCCAUX_G20
XC7VX690TFFG1927

MGTVCCAUX_G20_V35 — V35
MGTVCCAUX_G20_T35 — T35
MGTVCCAUX_200

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTVCCAUX_G11
XC7VX690TFFG1927

MGTVCCAUX_G11_P10 — P10 — MGTVCCAUX_100

U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK MGTVCCAUX_G21
XC7VX690TFFG1927

MGTVCCAUX_G21_P35 — P35 — MGTVCCAUX_200

U1 SOC_FF1924_OZ_IRON

MGTVCCAUX_100

C194 1 2 4.7UF 10V
C195 1 2 4.7UF 10V
C983 1 2 4.7UF 10V

GND

MGTVCCAUX_200

C984 1 2 4.7UF 10V
C985 1 2 4.7UF 10V
C986 1 2 4.7UF 10V

GND

XILINX

Title: MGT POWER / DECOUPLING SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
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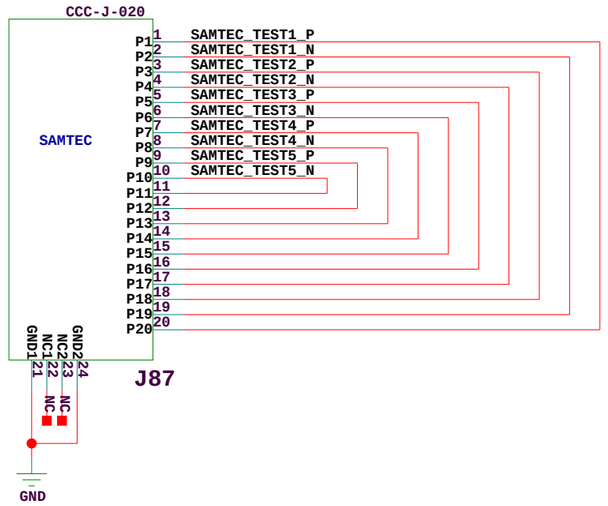
BULLSEYE TEST CHANNELS 1



1 USE "FIGURE 8" PATTERN TO MATCH P AND N PAIRS. SEE LAYOUT GUIDELINES FOR DETAILS.

XILINX

Title: SAMTEC BULLSEYE TEST CHANNELS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
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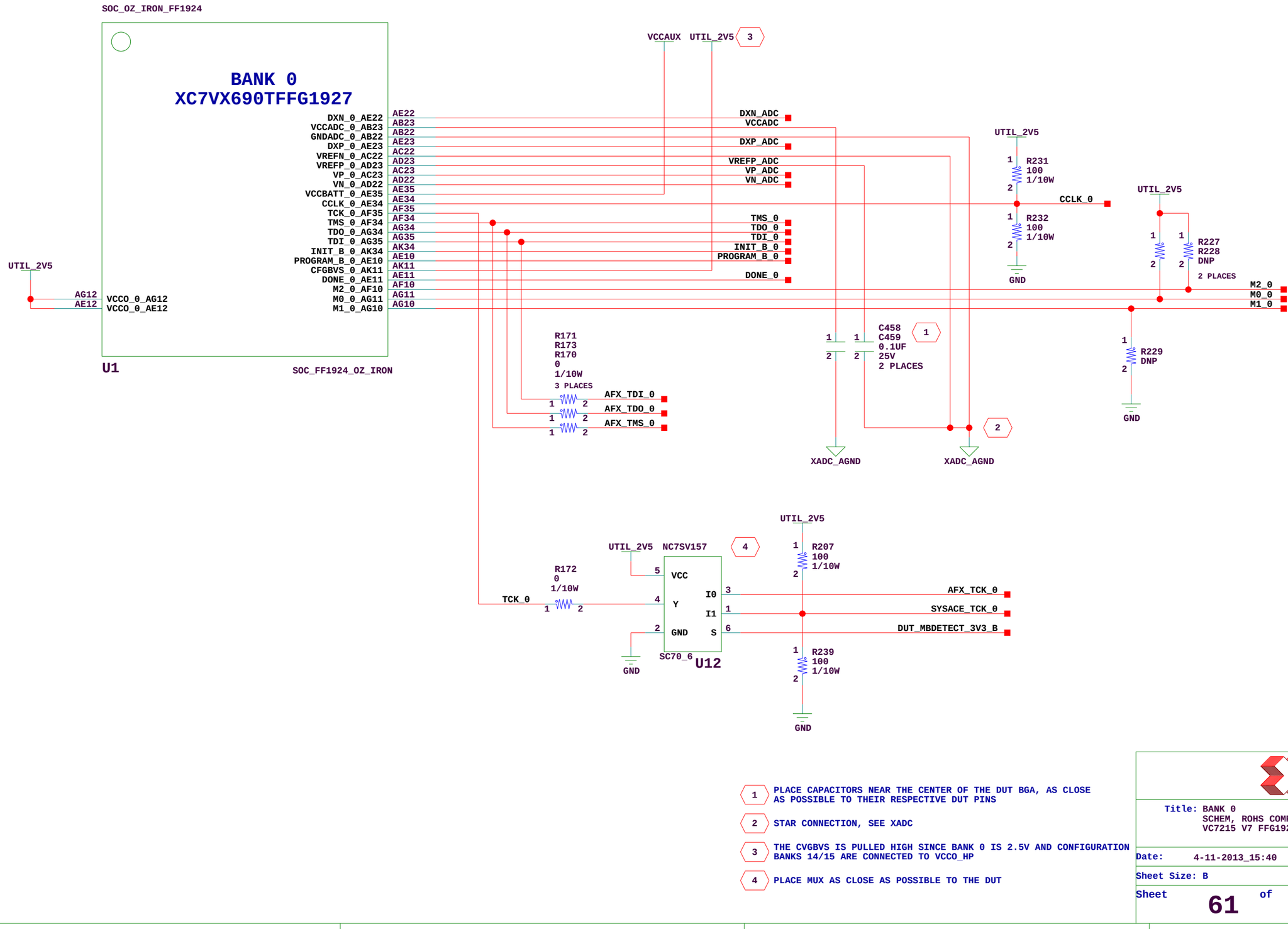

1. PLACE CAPACITORS NEAR THE CENTER OF THE DUT BGA, AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE DUT PINS
2. STAR CONNECTION, SEE XADC
3. THE CVGBVS IS PULLED HIGH SINCE BANK 0 IS 2.5V AND CONFIGURATION BANKS 14/15 ARE CONNECTED TO VCCO_HP
4. PLACE MUX AS CLOSE AS POSSIBLE TO THE DUT

XILINX

Title: BANK 0 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
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SOC_OZ_IRON_FF1924

VCCO_HP

R301
10.0K
1/10W

BANK 14
XC7VX690TFFG1927

	IO_0_VRN_14_AT30	AT30
	IO_L1P_T0_D00_MOSI_14_BC27	BC27
	IO_L1N_T0_D01_DIN_14_BD27	BD27
	IO_L2P_T0_D02_14_BD29	BD29
	IO_L2N_T0_D03_14_BD30	BD30
	IO_L3P_T0_DQS_PUDC_B_14_BB27	BB27
	IO_L3N_T0_DQS_EMCCLK_14_BB28	BB28
	IO_L4P_T0_D04_14_BB30	BB30
	IO_L4N_T0_D05_14_BC30	BC30
	IO_L5P_T0_D06_14_BC28	BC28
	IO_L5N_T0_D07_14_BC29	BC29
	IO_L6P_T0_FCS_B_14_BA29	BA29
	IO_L6N_T0_D08_VREF_14_BA30	BA30
	IO_L7P_T1_D09_14_AW29	AW29
	IO_L7N_T1_D10_14_AY29	AY29
	IO_L8P_T1_D11_14_AW27	AW27
	IO_L8N_T1_D12_14_AY27	AY27
	IO_L9P_T1_DQS_14_AY31	AY31
	IO_L9N_T1_DQS_D13_14_BA31	BA31
	IO_L10P_T1_D14_14_AY28	AY28
	IO_L10N_T1_D15_14_BA28	BA28
	IO_L11P_T1_SRCC_14_AW30	AW30
	IO_L11N_T1_SRCC_14_AW31	AW31
	IO_L12P_T1_MRCC_14_AV27	AV27
	IO_L12N_T1_MRCC_14_AV28	AV28
	IO_L13P_T2_MRCC_14_AU30	AU30
	IO_L13N_T2_MRCC_14_AV30	AV30
	IO_L14P_T2_SRCC_14_AU28	AU28
	IO_L14N_T2_SRCC_14_AV29	AV29
	IO_L15P_T2_DQS_RDWR_B_14_AN27	AN27
	IO_L15N_T2_DQSDOUT_CSOB_14_AP27	AP27
	IO_L16P_T2_CSI_B_14_AT28	AT28
	IO_L16N_T2_A15_D31_14_AT29	AT29
	IO_L17P_T2_A14_D30_14_AP29	AP29
	IO_L17N_T2_A13_D29_14_AP30	AP30
	IO_L18P_T2_A12_D28_14_AR28	AR28
	IO_L18N_T2_A11_D27_14_AR29	AR29
	IO_L19P_T3_A10_D26_14_AN28	AN28
	IO_L19N_T3A09D25_VREF_14_AN29	AN29
	IO_L20P_T3_A08_D24_14_AM30	AM30
	IO_L20N_T3_A07_D23_14_AN30	AN30
	IO_L21P_T3_DQS_14_AK27	AK27
	IO_L21N_T3_DQS_A06_D22_14_AK28	AK28
	IO_L22P_T3_A05_D21_14_AM27	AM27
	IO_L22N_T3_A04_D20_14_AM28	AM28
	IO_L23P_T3_A03_D19_14_AJ29	AJ29
	IO_L23N_T3_A02_D18_14_AK29	AK29
	IO_L24P_T3_A01_D17_14_AL28	AL28
	IO_L24N_T3_A00_D16_14_AL29	AL29
	IO_25_VRP_14_AR27	AR27

FMC2_PRSNT_M2C_L
FMC2_LA19_P
FMC2_LA19_N
FMC2_LA20_P
FMC2_LA20_N
FMC2_LA21_P
FMC2_LA21_N
FMC2_LA22_P
FMC2_LA22_N
FMC2_LA23_P
FMC2_LA23_N
FMC2_LA24_P
FMC2_LA24_N
FMC2_LA25_P
FMC2_LA25_N
FMC2_LA26_P
FMC2_LA26_N
FMC2_LA27_P
FMC2_LA27_N
FMC2_LA28_P
FMC2_LA28_N
FMC2_LA18_CC_P
FMC2_LA18_CC_N
FMC2_LA17_CC_P
FMC2_LA17_CC_N
FMC2_CLK0_M2C_P
FMC2_CLK0_M2C_N
FMC2_CLK1_M2C_P
FMC2_CLK1_M2C_N
FMC2_LA29_P
FMC2_LA29_N
FMC2_LA30_P
FMC2_LA30_N
FMC2_LA31_P
FMC2_LA31_N
FMC2_LA32_P
FMC2_LA32_N
FMC2_LA33_P
FMC2_LA33_N
FMC2_HA07_P
FMC2_HA07_N
FMC2_HA08_P
FMC2_HA08_N
FMC2_HA09_P
FMC2_HA09_N
FMC2_HA10_P
FMC2_HA10_N
FMC2_HA11_P
FMC2_HA11_N
IO_25_VRP_14

DEDICATED PINS
DEDICATED PINS

VCCO_HP

AL27	VCCO_14_AL27
AP28	VCCO_14_AP28
AU29	VCCO_14_AU29
AY30	VCCO_14_AY30
BA27	VCCO_14_BA27
BD28	VCCO_14_BD28

U1

SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK 15
XC7VX690TFFG1927

	IO_0_VRN_15_AR24	AR24
	IO_L1P_T0_AD0P_15_BD25	BD25
	IO_L1N_T0_AD0N_15_BD26	BD26
	IO_L2P_T0_AD8P_15_BB23	BB23
	IO_L2N_T0_AD8N_15_BC23	BC23
	IO_L3P_T0_DQS_AD1P_15_BB25	BB25
	IO_L3N_T0_DQS_AD1N_15_BC25	BC25
	IO_L4P_T0_15_BC24	BC24
	IO_L4N_T0_15_BD24	BD24
	IO_L5P_T0_AD9P_15_BA26	BA26
	IO_L5N_T0_AD9N_15_BB26	BB26
	IO_L6P_T0_15_BA24	BA24
	IO_L6N_T0_VREF_15_BA25	BA25
	IO_L7P_T1_AD2P_15_AW26	AW26
	IO_L7N_T1_AD2N_15_AY26	AY26
	IO_L8P_T1_AD10P_15_AY23	AY23
	IO_L8N_T1_AD10N_15_BA23	BA23
	IO_L9P_T1_DQS_AD3P_15_AV25	AV25
	IO_L9N_T1_DQS_AD3N_15_AW25	AW25
	IO_L10P_T1_AD11P_15_AW24	AW24
	IO_L10N_T1_AD11N_15_AY24	AY24
	IO_L11P_T1_SRCC_15_AV23	AV23
	IO_L11N_T1_SRCC_15_AV24	AV24
	IO_L12P_T1_MRCC_15_AU25	AU25
	IO_L12N_T1_MRCC_15_AU26	AU26
	IO_L13P_T2_MRCC_15_AT23	AT23
	IO_L13N_T2_MRCC_15_AU23	AU23
	IO_L14P_T2_SRCC_15_AT24	AT24
	IO_L14N_T2_SRCC_15_AT25	AT25
	IO_L15P_T2_DQS_15_AN23	AN23
	IO_L15N_T2_DQS_ADV_B_15_AN24	AN24
	IO_L16P_T2_A28_15_AT26	AT26
	IO_L16N_T2_A27_15_AU27	AU27
	IO_L17P_T2_A26_15_AP24	AP24
	IO_L17N_T2_A25_15_AP25	AP25
	IO_L18P_T2_A24_15_AN25	AN25
	IO_L18N_T2_A23_15_AP26	AP26
	IO_L19P_T3_A22_15_AL23	AL23
	IO_L19N_T3_A21_VREF_15_AM23	AM23
	IO_L20P_T3_A20_15_AM25	AM25
	IO_L20N_T3_A19_15_AM26	AM26
	IO_L21P_T3_DQS_15_AK23	AK23
	IO_L21N_T3_DQS_A18_15_AK24	AK24
	IO_L22P_T3_A17_15_AK26	AK26
	IO_L22N_T3_A16_15_AL26	AL26
	IO_L23P_T3_FOE_B_15_AL24	AL24
	IO_L23N_T3_FWE_B_15_AL25	AL25
	IO_L24P_T3_RS1_15_AJ25	AJ25
	IO_L24N_T3_RS0_15_AJ26	AJ26
	IO_25_VRP_15_AR26	AR26

IO_0_VRN_15
FMC2_LA02_P
FMC2_LA02_N
FMC2_LA03_P
FMC2_LA03_N
FMC2_LA04_P
FMC2_LA04_N
FMC2_LA05_P
FMC2_LA05_N
FMC2_LA06_P
FMC2_LA06_N
FMC2_LA07_P
FMC2_LA07_N
FMC2_LA08_P
FMC2_LA08_N
FMC2_LA09_P
FMC2_LA09_N
FMC2_LA10_P
FMC2_LA10_N
FMC2_LA11_P
FMC2_LA11_N
FMC2_LA01_CC_P
FMC2_LA01_CC_N
FMC2_LA00_CC_P
FMC2_LA00_CC_N
FMC2_HA00_CC_P
FMC2_HA00_CC_N
FMC2_HA01_CC_P
FMC2_HA01_CC_N
FMC2_LA12_P
FMC2_LA12_N
FMC2_LA13_P
FMC2_LA13_N
FMC2_LA14_P
FMC2_LA14_N
FMC2_LA15_P
FMC2_LA15_N
FMC2_LA16_P
FMC2_LA16_N
FMC2_HA02_P
FMC2_HA02_N
FMC2_HA03_P
FMC2_HA03_N
FMC2_HA04_P
FMC2_HA04_N
FMC2_HA05_P
FMC2_HA05_N
FMC2_HA06_P
FMC2_HA06_N
IO_25_VRP_15

DEDICATED PINS
DEDICATED PINS

VCCO_HP

AJ23	VCCO_15_AJ23
AM24	VCCO_15_AM24
AR25	VCCO_15_AR25
AV26	VCCO_15_AV26
AW23	VCCO_15_AW23
BB24	VCCO_15_BB24

U1

SOC_FF1924_OZ_IRON

VCCO_HP

R289
100
1/10W

IO_0_VRN_15

IO_25_VRP_15

R288
100
1/10W

GND

XILINX

Title: I/O BANKS 14, 15
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-11-2013_15:40
Ver: 1.0
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SOC_OZ_IRON_FF1924

BANK 16
XC7VX690TFFG1927

IO_0_VRN_16_AU35	AU35	IO_0_VRN_16
IO_L1P_T0_16_AK33	AK33	FMC2_HB01_P
IO_L1N_T0_16_AL33	AL33	FMC2_HB01_N
IO_L2P_T0_16_AJ30	AJ30	FMC2_HB02_P
IO_L2N_T0_16_AJ31	AJ31	FMC2_HB02_N
IO_L3P_T0_DQS_16_AK31	AK31	FMC2_HB03_P
IO_L3N_T0_DQS_16_AL31	AL31	FMC2_HB03_N
IO_L4P_T0_16_AJ32	AJ32	FMC2_HB04_P
IO_L4N_T0_16_AK32	AK32	FMC2_HB04_N
IO_L5P_T0_16_AL30	AL30	FMC2_HB05_P
IO_L5N_T0_16_AM31	AM31	FMC2_HB05_N
IO_L6P_T0_16_AM32	AM32	FMC2_HB07_P
IO_L6N_T0_VREF_16_AM33	AM33	FMC2_HB07_N
IO_L7P_T1_16_AN32	AN32	FMC2_HB08_P
IO_L7N_T1_16_AN33	AN33	FMC2_HB08_N
IO_L8P_T1_16_AR33	AR33	FMC2_HB09_P
IO_L8N_T1_16_AT33	AT33	FMC2_HB09_N
IO_L9P_T1_DQS_16_AP31	AP31	FMC2_HB10_P
IO_L9N_T1_DQS_16_AP32	AP32	FMC2_HB10_N
IO_L10P_T1_16_AR31	AR31	FMC2_HB11_P
IO_L10N_T1_16_AR32	AR32	FMC2_HB11_N
IO_L11P_T1_SRCC_16_AU31	AU31	FMC2_HB06_CC_P
IO_L11N_T1_SRCC_16_AU32	AU32	FMC2_HB06_CC_N
IO_L12P_T1_MRCC_16_AU33	AU33	FMC2_HB00_CC_P
IO_L12N_T1_MRCC_16_AV33	AV33	FMC2_HB00_CC_N
IO_L13P_T2_MRCC_16_AV32	AV32	FMC2_CLK2_BIDIR_P
IO_L13N_T2_MRCC_16_AW32	AW32	FMC2_CLK2_BIDIR_N
IO_L14P_T2_SRCC_16_AV34	AV34	FMC2_CLK3_BIDIR_P
IO_L14N_T2_SRCC_16_AV35	AV35	FMC2_CLK3_BIDIR_N
IO_L15P_T2_DQS_16_AW34	AW34	FMC2_HB12_P
IO_L15N_T2_DQS_16_AW35	AW35	FMC2_HB12_N
IO_L16P_T2_16_AY33	AY33	FMC2_HB13_P
IO_L16N_T2_16_AY34	AY34	FMC2_HB13_N
IO_L17P_T2_16_BA34	BA34	FMC2_HB14_P
IO_L17N_T2_16_BA35	BA35	FMC2_HB14_N
IO_L18P_T2_16_AY32	AY32	FMC2_HB15_P
IO_L18N_T2_16_BA33	BA33	FMC2_HB15_N
IO_L19P_T3_16_BB31	BB31	FMC2_HB16_P
IO_L19N_T3_VREF_16_BB32	BB32	FMC2_HB16_N
IO_L20P_T3_16_BB35	BB35	FMC2_HA12_P
IO_L20N_T3_16_BC35	BC35	FMC2_HA12_N
IO_L21P_T3_DQS_16_BC32	BC32	FMC2_HA13_P
IO_L21N_T3_DQS_16_BC33	BC33	FMC2_HA13_N
IO_L22P_T3_16_BB33	BB33	FMC2_HA14_P
IO_L22N_T3_16_BC34	BC34	FMC2_HA14_N
IO_L23P_T3_16_BD31	BD31	FMC2_HA15_P
IO_L23N_T3_16_BD32	BD32	FMC2_HA15_N
IO_L24P_T3_16_BD34	BD34	FMC2_HA16_P
IO_L24N_T3_16_BD35	BD35	FMC2_HA16_N
IO_25_VRP_16_AT31	AT31	IO_25_VRP_16

VCCO_HP	AK30	VCCO_16_AK30
	AN31	VCCO_16_AN31
	AT32	VCCO_16_AT32
	AW33	VCCO_16_AW33
	BB34	VCCO_16_BB34
	BC31	VCCO_16_BC31

U1

SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK 17
XC7VX690TFFG1927

IO_0_VRN_17_M26	M26	IO_0_VRN_17
IO_L1P_T0_17_B23	B23	USB_GPIO_0
IO_L1N_T0_17_A23	A23	USB_GPIO_1
IO_L2P_T0_17_C25	C25	USB_GPIO_2
IO_L2N_T0_17_B25	B25	USB_GPIO_3
IO_L3P_T0_DQS_17_C23	C23	USB_TXD_0
IO_L3N_T0_DQS_17_C24	C24	USB_RXD_I
IO_L4P_T0_17_A24	A24	USB_RTS_0_B
IO_L4N_T0_17_A25	A25	USB_CTS_I_B
IO_L5P_T0_17_D24	D24	MGT_MOD_SPI_SCK
IO_L5N_T0_17_D25	D25	MGT_MOD_SPI_D
IO_L6P_T0_17_E23	E23	MGT_MOD_SPI_Q
IO_L6N_T0_VREF_17_E24	E24	MGT_MOD_100_SPI_CS
IO_L7P_T1_17_G23	G23	MGT_MOD_200_SPI_CS
IO_L7N_T1_17_F23	F23	SA2_SDHOST_CMD
IO_L8P_T1_17_F24	F24	SA2_SDHOST_D0
IO_L8N_T1_17_F25	F25	SA2_SDHOST_D1
IO_L9P_T1_DQS_17_H23	H23	SA2_SDHOST_D3
IO_L9N_T1_DQS_17_H24	H24	SA2_SDHOST_D2
IO_L10P_T1_17_G25	G25	SA2_SDHOST_CLK
IO_L10N_T1_17_G26	G26	IO_L10N_T1_17
IO_L11P_T1_SRCC_17_J24	J24	IO_L11P_T1_SRCC_17
IO_L11N_T1_SRCC_17_H25	H25	IO_L11N_T1_SRCC_17
IO_L12P_T1_MRCC_17_J25	J25	LVDS_OSC_P
IO_L12N_T1_MRCC_17_J26	J26	LVDS_OSC_N
IO_L13P_T2_MRCC_17_K23	K23	CLK_DIFF_1_P
IO_L13N_T2_MRCC_17_K24	K24	CLK_DIFF_1_N
IO_L14P_T2_SRCC_17_L24	L24	IO_L14P_T2_SRCC_17
IO_L14N_T2_SRCC_17_L25	L25	IO_L14N_T2_SRCC_17
IO_L15P_T2_DQS_17_L26	L26	IO_L15P_T2_DQS_17
IO_L15N_T2_DQS_17_K26	K26	IO_L15N_T2_DQS_17
IO_L16P_T2_17_N23	N23	IO_L16P_T2_17
IO_L16N_T2_17_N24	N24	IO_L16N_T2_17
IO_L17P_T2_17_N25	N25	IO_L17P_T2_17
IO_L17N_T2_17_M25	M25	IO_L17N_T2_17
IO_L18P_T2_17_M23	M23	IO_L18P_T2_17
IO_L18N_T2_17_L23	L23	IO_L18N_T2_17
IO_L19P_T3_17_T24	T24	IO_L19P_T3_17
IO_L19N_T3_VREF_17_T25	T25	IO_L19N_T3_VREF_17
IO_L20P_T3_17_P25	P25	IO_L20P_T3_17
IO_L20N_T3_17_P26	P26	IO_L20N_T3_17
IO_L21P_T3_DQS_17_U25	U25	IO_L21P_T3_DQS_17
IO_L21N_T3_DQS_17_U26	U26	IO_L21N_T3_DQS_17
IO_L22P_T3_17_T26	T26	IO_L22P_T3_17
IO_L22N_T3_17_R26	R26	IO_L22N_T3_17
IO_L23P_T3_17_U23	U23	IO_L23P_T3_17
IO_L23N_T3_17_T23	T23	IO_L23N_T3_17
IO_L24P_T3_17_R23	R23	IO_L24P_T3_17
IO_L24N_T3_17_R24	R24	IO_L24N_T3_17
IO_25_VRP_17_P24	P24	IO_25_VRP_17

USB UART BRIDGE

SPI - MGT PWR MODULE

SYSTEMACE-2

SYSTEM CLOCK

USER DIFF SMA CLOCK

VCCO_HP	B24	VCCO_17_B24
	E25	VCCO_17_E25
	H26	VCCO_17_H26
	J23	VCCO_17_J23
	M24	VCCO_17_M24
	R25	VCCO_17_R25

U1

SOC_FF1924_OZ_IRON

VCCO_HP

R375 100 1/10W

IO_0_VRN_16

IO_25_VRP_16

R374 100 1/10W

GND

LVDS_OSC_P

1

R46 100 1/10W

LVDS_OSC_N

VCCO_HP

R326 100 1/10W

IO_0_VRN_17

IO_25_VRP_17

R325 100 1/10W

GND

NOTES:

1 LVDS TERMINATION RESISTOR: LOCATE CLOSET TO PINS ON FPGA.

XILINX

Title: I/O BANKS 16, 17
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-11-2013_15:40	Ver: 1.0
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SOC_OZ_IRON_FF1924

BANK 18
XC7VX690TFFG1927

IO_0_VRN_18_L30	L30	IO_0_VRN_18
IO_L1P_T0_18_C30	C30	FMC3_HB01_P
IO_L1N_T0_18_B30	B30	FMC3_HB01_N
IO_L2P_T0_18_B33	B33	FMC3_HB02_P
IO_L2N_T0_18_A33	A33	FMC3_HB02_N
IO_L3P_T0_DQS_18_A30	A30	FMC3_HB03_P
IO_L3N_T0_DQS_18_A31	A31	FMC3_HB03_N
IO_L4P_T0_18_C32	C32	CM_LVDS2_P
IO_L4N_T0_18_C33	C33	CM_LVDS2_N
IO_L5P_T0_18_B31	B31	FMC3_HB04_P
IO_L5N_T0_18_B32	B32	FMC3_HB04_N
IO_L6P_T0_18_D30	D30	FMC3_HB05_P
IO_L6N_T0_VREF_18_D31	D31	FMC3_HB05_N
IO_L7P_T1_18_E31	E31	FMC3_HB07_P
IO_L7N_T1_18_D32	D32	FMC3_HB07_N
IO_L8P_T1_18_E32	E32	FMC3_HB08_P
IO_L8N_T1_18_E33	E33	FMC3_HB08_N
IO_L9P_T1_DQS_18_F30	F30	FMC3_HB09_P
IO_L9N_T1_DQS_18_F31	F31	FMC3_HB09_N
IO_L10P_T1_18_G33	G33	FMC3_HB10_P
IO_L10N_T1_18_F33	F33	FMC3_HB10_N
IO_L11P_T1_SRCC_18_G31	G31	FMC3_HB06_CC_P
IO_L11N_T1_SRCC_18_G32	G32	FMC3_HB06_CC_N
IO_L12P_T1_MRCC_18_H30	H30	FMC3_HB00_CC_P
IO_L12N_T1_MRCC_18_G30	G30	FMC3_HB00_CC_N
IO_L13P_T2_MRCC_18_H32	H32	FMC3_CLK2_BIDIR_P
IO_L13N_T2_MRCC_18_H33	H33	FMC3_CLK2_BIDIR_N
IO_L14P_T2_SRCC_18_J30	J30	FMC3_CLK3_BIDIR_P
IO_L14N_T2_SRCC_18_J31	J31	FMC3_CLK3_BIDIR_N
IO_L15P_T2_DQS_18_L31	L31	FMC3_HB11_P
IO_L15N_T2_DQS_18_K31	K31	FMC3_HB11_N
IO_L16P_T2_18_K32	K32	FMC3_HB12_P
IO_L16N_T2_18_J32	J32	FMC3_HB12_N
IO_L17P_T2_18_M31	M31	FMC3_HB13_P
IO_L17N_T2_18_M32	M32	FMC3_HB13_N
IO_L18P_T2_18_L33	L33	FMC3_HB14_P
IO_L18N_T2_18_K33	K33	FMC3_HB14_N
IO_L19P_T3_18_R32	R32	FMC3_HB15_P
IO_L19N_T3_VREF_18_P32	P32	FMC3_HB15_N
IO_L20P_T3_18_N33	N33	FMC3_HA11_P
IO_L20N_T3_18_M33	M33	FMC3_HA11_N
IO_L21P_T3_DQS_18_T31	T31	FMC3_HA12_P
IO_L21N_T3_DQS_18_R31	R31	FMC3_HA12_N
IO_L22P_T3_18_P31	P31	FMC3_HA13_P
IO_L22N_T3_18_N32	N32	FMC3_HA13_N
IO_L23P_T3_18_U32	U32	FMC3_HA14_P
IO_L23N_T3_18_U33	U33	FMC3_HA14_N
IO_L24P_T3_18_T33	T33	CM_LVDS3_P
IO_L24N_T3_18_R33	R33	CM_LVDS3_N
IO_25_VRP_18_U31	U31	IO_25_VRP_18

RECOVERY CLOCK

VCCO_HP

C31	VCCO_18_C31
F32	VCCO_18_F32
J33	VCCO_18_J33
K30	VCCO_18_K30
N31	VCCO_18_N31
T32	VCCO_18_T32

U1

SOC_FF1924_OZ_IRON

VCCO_HP

R330 100 1/10W

IO_0_VRN_18

IO_25_VRP_18

R329 100 1/10W

GND

SOC_OZ_IRON_FF1924

BANK 19
XC7VX690TFFG1927

IO_0_VRN_19_M27	M27	IO_0_VRN_19
IO_L1P_T0_19_A28	A28	DUT_PMB_ALERT
IO_L1N_T0_19_A29	A29	DUT_PMB_CTRL
IO_L2P_T0_19_D29	D29	DUT_PMB_CLK
IO_L2N_T0_19_C29	C29	DUT_PMB_DATA
IO_L3P_T0_DQS_19_C27	C27	IO_L3P_T0_DQS_19
IO_L3N_T0_DQS_19_B27	B27	IO_L3N_T0_DQS_19
IO_L4P_T0_19_C28	C28	IO_L4P_T0_19
IO_L4N_T0_19_B28	B28	IO_L4N_T0_19
IO_L5P_T0_19_B26	B26	IO_L5P_T0_19
IO_L5N_T0_19_A26	A26	USER_SW1
IO_L6P_T0_19_D26	D26	USER_SW2
IO_L6N_T0_VREF_19_D27	D27	USER_SW3
IO_L7P_T1_19_G28	G28	USER_SW4
IO_L7N_T1_19_F28	F28	USER_SW5
IO_L8P_T1_19_F26	F26	USER_SW6
IO_L8N_T1_19_E26	E26	USER_SW7
IO_L9P_T1_DQS_19_F29	F29	USER_SW8
IO_L9N_T1_DQS_19_E29	E29	IO_L9N_T1_DQS_19
IO_L10P_T1_19_E27	E27	IO_L10P_T1_19
IO_L10N_T1_19_E28	E28	IO_L10N_T1_19
IO_L11P_T1_SRCC_19_H27	H27	IO_L11P_T1_SRCC_19
IO_L11N_T1_SRCC_19_G27	G27	IO_L11N_T1_SRCC_19
IO_L12P_T1_MRCC_19_H28	H28	IO_L12P_T1_MRCC_19
IO_L12N_T1_MRCC_19_H29	H29	IO_L12N_T1_MRCC_19
IO_L13P_T2_MRCC_19_K27	K27	IO_L13P_T2_MRCC_19
IO_L13N_T2_MRCC_19_J27	J27	IO_L13N_T2_MRCC_19
IO_L14P_T2_SRCC_19_K28	K28	DUT_I2C_SCL
IO_L14N_T2_SRCC_19_J29	J29	DUT_I2C_SDA
IO_L15P_T2_DQS_19_N30	N30	IO_L15P_T2_DQS_19
IO_L15N_T2_DQS_19_M30	M30	IO_L15N_T2_DQS_19
IO_L16P_T2_19_L28	L28	IO_L16P_T2_19
IO_L16N_T2_19_K29	K29	IO_L16N_T2_19
IO_L17P_T2_19_N28	N28	IO_L17P_T2_19
IO_L17N_T2_19_N29	N29	IO_L17N_T2_19
IO_L18P_T2_19_M28	M28	IO_L18P_T2_19
IO_L18N_T2_19_L29	L29	IO_L18N_T2_19
IO_L19P_T3_19_P29	P29	USER_PB1
IO_L19N_T3_VREF_19_P30	P30	USER_PB2
IO_L20P_T3_19_T28	T28	APP_LED1
IO_L20N_T3_19_T29	T29	APP_LED2
IO_L21P_T3_DQS_19_R28	R28	APP_LED3
IO_L21N_T3_DQS_19_R29	R29	APP_LED4
IO_L22P_T3_19_U30	U30	APP_LED5
IO_L22N_T3_19_T30	T30	APP_LED6
IO_L23P_T3_19_R27	R27	APP_LED7
IO_L23N_T3_19_P27	P27	APP_LED8
IO_L24P_T3_19_U27	U27	IO_L24P_T3_19
IO_L24N_T3_19_U28	U28	IO_L24N_T3_19
IO_25_VRP_19_N27	N27	IO_25_VRP_19

PMBUS (DUT MASTER)

I2C (DUT MASTER)

USER IO (PUSH BUTTONS)

USER IO (LEDS)

USER IO (SWITCHES)

VCCO_HP

A27	VCCO_19_A27
D28	VCCO_19_D28
G29	VCCO_19_G29
L27	VCCO_19_L27
P28	VCCO_19_P28
U29	VCCO_19_U29

U1

SOC_FF1924_OZ_IRON

VCCO_HP

R328 100 1/10W

IO_0_VRN_19

IO_25_VRP_19

R327 100 1/10W

GND

XILINX

Title: I/O BANKS 18, 19
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-11-2013_15:40

Ver: 1.0

Sheet Size: B

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SOC_OZ_IRON_FF1924

BANK 34
XC7VX690TFFG1927

IO_0_VRN_34_AP15	AP15	FMC1_PRSNT_M2C_L
IO_L1P_T0_34_BA18	BA18	FMC1_LA19_P
IO_L1N_T0_34_BB18	BB18	FMC1_LA19_N
IO_L2P_T0_34_BC19	BC19	FMC1_LA20_P
IO_L2N_T0_34_BC18	BC18	FMC1_LA20_N
IO_L3P_T0_DQS_34_BB17	BB17	FMC1_LA21_P
IO_L3N_T0_DQS_34_BC17	BC17	FMC1_LA21_N
IO_L4P_T0_34_BD17	BD17	FMC1_LA22_P
IO_L4N_T0_34_BD16	BD16	FMC1_LA22_N
IO_L5P_T0_34_BC15	BC15	FMC1_LA23_P
IO_L5N_T0_34_BD15	BD15	FMC1_LA23_N
IO_L6P_T0_34_BB16	BB16	FMC1_LA24_P
IO_L6N_T0_VREF_34_BB15	BB15	FMC1_LA24_N
IO_L7P_T1_34_AW17	AW17	FMC1_LA25_P
IO_L7N_T1_34_AY16	AY16	FMC1_LA25_N
IO_L8P_T1_34_AY18	AY18	FMC1_LA26_P
IO_L8N_T1_34_AY17	AY17	FMC1_LA26_N
IO_L9P_T1_DQS_34_AW16	AW16	FMC1_LA27_P
IO_L9N_T1_DQS_34_AW15	AW15	FMC1_LA27_N
IO_L10P_T1_34_BA16	BA16	FMC1_LA28_P
IO_L10N_T1_34_BA15	BA15	FMC1_LA28_N
IO_L11P_T1_SRCC_34_AV18	AV18	FMC1_LA18_CC_P
IO_L11N_T1_SRCC_34_AV17	AV17	FMC1_LA18_CC_N
IO_L12P_T1_MRCC_34_AU15	AU15	FMC1_LA17_CC_P
IO_L12N_T1_MRCC_34_AV15	AV15	FMC1_LA17_CC_N
IO_L13P_T2_MRCC_34_AT18	AT18	FMC1_CLK0_M2C_P
IO_L13N_T2_MRCC_34_AU18	AU18	FMC1_CLK0_M2C_N
IO_L14P_T2_SRCC_34_AU17	AU17	FMC1_CLK1_M2C_P
IO_L14N_T2_SRCC_34_AU16	AU16	FMC1_CLK1_M2C_N
IO_L15P_T2_DQS_34_AP16	AP16	FMC1_LA29_P
IO_L15N_T2_DQS_34_AR16	AR16	FMC1_LA29_N
IO_L16P_T2_34_AR18	AR18	FMC1_LA30_P
IO_L16N_T2_34_AR17	AR17	FMC1_LA30_N
IO_L17P_T2_34_AT16	AT16	FMC1_LA31_P
IO_L17N_T2_34_AT15	AT15	FMC1_LA31_N
IO_L18P_T2_34_AN17	AN17	FMC1_LA32_P
IO_L18N_T2_34_AP17	AP17	FMC1_LA32_N
IO_L19P_T3_34_AM18	AM18	FMC1_LA33_P
IO_L19N_T3_VREF_34_AN18	AN18	FMC1_LA33_N
IO_L20P_T3_34_AM15	AM15	FMC1_HA07_P
IO_L20N_T3_34_AN15	AN15	FMC1_HA07_N
IO_L21P_T3_DQS_34_AK18	AK18	FMC1_HA08_P
IO_L21N_T3_DQS_34_AL18	AL18	FMC1_HA08_N
IO_L22P_T3_34_AM17	AM17	FMC1_HA09_P
IO_L22N_T3_34_AM16	AM16	FMC1_HA09_N
IO_L23P_T3_34_AJ16	AJ16	FMC1_HA10_P
IO_L23N_T3_34_AK16	AK16	FMC1_HA10_N
IO_L24P_T3_34_AL16	AL16	FMC1_HA11_P
IO_L24N_T3_34_AL15	AL15	FMC1_HA11_N
IO_25_VRP_34_AK17	AK17	IO_25_VRP_34

DEDICATED PINS

VCCO_HP

AL17	VCCO_34_AL17
AP18	VCCO_34_AP18
AR15	VCCO_34_AR15
AV16	VCCO_34_AV16
BA17	VCCO_34_BA17
BD18	VCCO_34_BD18

U1

SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924

BANK 35
XC7VX690TFFG1927

IO_0_VRN_35_AR23	AR23	IO_0_VRN_35
IO_L1P_T0_35_BB22	BB22	FMC1_HB01_P
IO_L1N_T0_35_BB21	BB21	FMC1_HB01_N
IO_L2P_T0_AD4P_35_BC22	BC22	FMC1_HB02_P
IO_L2N_T0_AD4N_35_BD22	BD22	FMC1_HB02_N
IO_L3P_T0_DQS_AD12P_35_BC20	BC20	FMC1_HB03_P
IO_L3N_T0_DQS_AD12N_35_BD19	BD19	FMC1_HB03_N
IO_L4P_T0_AD5P_35_BD21	BD21	FMC1_HB04_P
IO_L4N_T0_AD5N_35_BD20	BD20	FMC1_HB04_N
IO_L5P_T0_AD13P_35_BA21	BA21	FMC1_HB05_P
IO_L5N_T0_AD13N_35_BB20	BB20	FMC1_HB05_N
IO_L6P_T0_35_BA20	BA20	FMC1_HB07_P
IO_L6N_T0_VREF_35_BA19	BA19	FMC1_HB07_N
IO_L7P_T1_AD6P_35_AW22	AW22	FMC1_HB08_P
IO_L7N_T1_AD6N_35_AY22	AY22	FMC1_HB08_N
IO_L8P_T1_AD14P_35_AV20	AV20	FMC1_HB09_P
IO_L8N_T1_AD14N_35_AW20	AW20	FMC1_HB09_N
IO_L9P_T1_DQS_AD7P_35_AW21	AW21	FMC1_HB10_P
IO_L9N_T1_DQS_AD7N_35_AY21	AY21	FMC1_HB10_N
IO_L10P_T1_AD15P_35_AW19	AW19	FMC1_HB11_P
IO_L10N_T1_AD15N_35_AY19	AY19	FMC1_HB11_N
IO_L11P_T1_SRCC_35_AU22	AU22	FMC1_HB06_CC_P
IO_L11N_T1_SRCC_35_AV22	AV22	FMC1_HB06_CC_N
IO_L12P_T1_MRCC_35_AU20	AU20	FMC1_HB00_CC_P
IO_L12N_T1_MRCC_35_AV19	AV19	FMC1_HB00_CC_N
IO_L13P_T2_MRCC_35_AT21	AT21	FMC1_CLK2_BIDIR_P
IO_L13N_T2_MRCC_35_AU21	AU21	FMC1_CLK2_BIDIR_N
IO_L14P_T2_SRCC_35_AT20	AT20	FMC1_CLK3_BIDIR_P
IO_L14N_T2_SRCC_35_AT19	AT19	FMC1_CLK3_BIDIR_N
IO_L15P_T2_DQS_35_AP21	AP21	FMC1_HB12_P
IO_L15N_T2_DQS_35_AP20	AP20	FMC1_HB12_N
IO_L16P_T2_35_AR22	AR22	FMC1_HB13_P
IO_L16N_T2_35_AR21	AR21	FMC1_HB13_N
IO_L17P_T2_35_AN20	AN20	FMC1_HB14_P
IO_L17N_T2_35_AP19	AP19	FMC1_HB14_N
IO_L18P_T2_35_AN22	AN22	FMC1_HB15_P
IO_L18N_T2_35_AP22	AP22	FMC1_HB15_N
IO_L19P_T3_35_AM22	AM22	FMC1_HB16_P
IO_L19N_T3_VREF_35_AM21	AM21	FMC1_HB16_N
IO_L20P_T3_35_AJ22	AJ22	FMC1_HA12_P
IO_L20N_T3_35_AJ21	AJ21	FMC1_HA12_N
IO_L21P_T3_DQS_35_AM20	AM20	FMC1_HA13_P
IO_L21N_T3_DQS_35_AN19	AN19	FMC1_HA13_N
IO_L22P_T3_35_AK22	AK22	FMC1_HA14_P
IO_L22N_T3_35_AK21	AK21	FMC1_HA14_N
IO_L23P_T3_35_AL21	AL21	FMC1_HA15_P
IO_L23N_T3_35_AL20	AL20	FMC1_HA15_N
IO_L24P_T3_35_AK19	AK19	FMC1_HA16_P
IO_L24N_T3_35_AL19	AL19	FMC1_HA16_N
IO_25_VRP_35_AR19	AR19	IO_25_VRP_35

DEDICATED PINS

DEDICATED PINS

VCCO_HP

AK20	VCCO_35_AK20
AN21	VCCO_35_AN21
AT22	VCCO_35_AT22
AU19	VCCO_35_AU19
AY20	VCCO_35_AY20
BC21	VCCO_35_BC21

U1

SOC_FF1924_OZ_IRON

VCCO_HP

R332 100 1/10W

IO_0_VRN_35

IO_25_VRP_35

R331 100 1/10W

GND

XILINX

Title: I/O BANKS 34, 35
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-11-2013_15:40

Ver: 1.0

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SOC_OZ_IRON_FF1924

BANK 36
XC7VX690TFFG1927

	IO_0_VRN_36_AP12	AP12
	IO_L1P_T0_36_AJ14	AJ14
	IO_L1N_T0_36_AK14	AK14
	IO_L2P_T0_36_AM13	AM13
	IO_L2N_T0_36_AM12	AM12
	IO_L3P_T0_DQS_36_AK13	AK13
	IO_L3N_T0_DQS_36_AK12	AK12
	IO_L4P_T0_36_AN13	AN13
	IO_L4N_T0_36_AN12	AN12
	IO_L5P_T0_36_AL14	AL14
	IO_L5N_T0_36_AL13	AL13
	IO_L6P_T0_36_AN14	AN14
	IO_L6N_T0_VREF_36_AP14	AP14
	IO_L7P_T1_36_AR13	AR13
	IO_L7N_T1_36_AR12	AR12
	IO_L8P_T1_36_AU12	AU12
	IO_L8N_T1_36_AU11	AU11
	IO_L9P_T1_DQS_36_AT14	AT14
	IO_L9N_T1_DQS_36_AT13	AT13
	IO_L10P_T1_36_AU10	AU10
	IO_L10N_T1_36_AV10	AV10
	IO_L11P_T1_SRCC_36_AV12	AV12
	IO_L11N_T1_SRCC_36_AW12	AW12
	IO_L12P_T1_MRCC_36_AU13	AU13
	IO_L12N_T1_MRCC_36_AV13	AV13
	IO_L13P_T2_MRCC_36_AV14	AV14
	IO_L13N_T2_MRCC_36_AW14	AW14
	IO_L14P_T2_SRCC_36_AW11	AW11
	IO_L14N_T2_SRCC_36_AW10	AW10
	IO_L15P_T2_DQS_36_AY13	AY13
	IO_L15N_T2_DQS_36_BA13	BA13
	IO_L16P_T2_36_AY12	AY12
	IO_L16N_T2_36_AY11	AY11
	IO_L17P_T2_36_BA11	BA11
	IO_L17N_T2_36_BA10	BA10
	IO_L18P_T2_36_AY14	AY14
	IO_L18N_T2_36_BA14	BA14
	IO_L19P_T3_36_BB11	BB11
	IO_L19N_T3_VREF_36_BB10	BB10
	IO_L20P_T3_36_BB12	BB12
	IO_L20N_T3_36_BC12	BC12
	IO_L21P_T3_DQS_36_BD12	BD12
	IO_L21N_T3_DQS_36_BD11	BD11
	IO_L22P_T3_36_BB13	BB13
	IO_L22N_T3_36_BC13	BC13
	IO_L23P_T3_36_BC14	BC14
	IO_L23N_T3_36_BD14	BD14
	IO_L24P_T3_36_BC10	BC10
	IO_L24N_T3_36_BD10	BD10
	IO_25_VRP_36_AR14	AR14

VCCO_HP

AJ13	VCCO_36_AJ13
AM14	VCCO_36_AM14
AT12	VCCO_36_AT12
AW13	VCCO_36_AW13
AY10	VCCO_36_AY10
BB14	VCCO_36_BB14
BC11	VCCO_36_BC11

U1 SOC_FF1924_OZ_IRON

VCCO_HP
- R383 100 1/10W — IO_0_VRN_36
- R382 100 1/10W — IO_25_VRP_36 — GND

NOTES:

1 LVDS TERMINATION RESISTOR: LOCATE CLOSET TO PINS ON FPGA.

CM_GCLK_P
- R52 100 1/10W
- CM_GCLK_N

SOC_OZ_IRON_FF1924

BANK 37
XC7VX690TFFG1927

	IO_0_VRN_37_P19	P19
	IO_L1P_T0_37_B21	B21
	IO_L1N_T0_37_A21	A21
	IO_L2P_T0_37_B20	B20
	IO_L2N_T0_37_A20	A20
	IO_L3P_T0_DQS_37_C22	C22
	IO_L3N_T0_DQS_37_B22	B22
	IO_L4P_T0_37_D20	D20
	IO_L4N_T0_37_C20	C20
	IO_L5P_T0_37_D22	D22
	IO_L5N_T0_37_D21	D21
	IO_L6P_T0_37_E22	E22
	IO_L6N_T0_VREF_37_E21	E21
	IO_L7P_T1_37_G21	G21
	IO_L7N_T1_37_F21	F21
	IO_L8P_T1_37_F20	F20
	IO_L8N_T1_37_F19	F19
	IO_L9P_T1_DQS_37_H22	H22
	IO_L9N_T1_DQS_37_G22	G22
	IO_L10P_T1_37_J19	J19
	IO_L10N_T1_37_H19	H19
	IO_L11P_T1_SRCC_37_J21	J21
	IO_L11N_T1_SRCC_37_J20	J20
	IO_L12P_T1_MRCC_37_H20	H20
	IO_L12N_T1_MRCC_37_G20	G20
	IO_L13P_T2_MRCC_37_K22	K22
	IO_L13N_T2_MRCC_37_J22	J22
	IO_L14P_T2_SRCC_37_L21	L21
	IO_L14N_T2_SRCC_37_K21	K21
	IO_L15P_T2_DQS_37_L19	L19
	IO_L15N_T2_DQS_37_K19	K19
	IO_L16P_T2_37_M20	M20
	IO_L16N_T2_37_L20	L20
	IO_L17P_T2_37_N20	N20
	IO_L17N_T2_37_N19	N19
	IO_L18P_T2_37_N22	N22
	IO_L18N_T2_37_M22	M22
	IO_L19P_T3_37_U20	U20
	IO_L19N_T3_VREF_37_T20	T20
	IO_L20P_T3_37_T19	T19
	IO_L20N_T3_37_R19	R19
	IO_L21P_T3_DQS_37_U22	U22
	IO_L21N_T3_DQS_37_U21	U21
	IO_L22P_T3_37_P21	P21
	IO_L22N_T3_37_P20	P20
	IO_L23P_T3_37_R22	R22
	IO_L23N_T3_37_P22	P22
	IO_L24P_T3_37_T21	T21
	IO_L24N_T3_37_R21	R21
	IO_25_VRP_37_M21	M21

IO_0_VRN_37	P19	
CM_CTRL_0	B21	CLOCK MODULE
CM_CTRL_1	A21	
CM_CTRL_2	B20	
CM_CTRL_3	A20	
CM_CTRL_4	C22	
CM_CTRL_5	B22	
CM_CTRL_6	D20	
CM_CTRL_7	C20	
CM_CTRL_8	D22	
CM_CTRL_9	D21	
CM_CTRL_10	E22	
CM_CTRL_11	E21	
CM_CTRL_12	G21	
CM_CTRL_13	F21	
CM_CTRL_14	F20	
CM_CTRL_15	F19	
CM_CTRL_16	H22	
CM_CTRL_17	G22	
CM_CTRL_18	J19	
CM_CTRL_19	H19	
IO_L11P_T1_SRCC_37	J21	
IO_L11N_T1_SRCC_37	J20	
CLK_DIFF_2_P	H20	
CLK_DIFF_2_N	G20	USER DIFF SMA CLOCK
IO_L13P_T2_MRCC_37	K22	
IO_L13N_T2_MRCC_37	J22	
CM_GCLK_P	L21	
CM_GCLK_N	K21	
CM_CTRL_20	L19	
CM_CTRL_21	K19	CLOCK MODULE
CM_CTRL_22	M20	
CM_CTRL_23	L20	
CM_RST	N20	
IO_L17N_T2_37	N19	
IO_L18P_T2_37	N22	
IO_L18N_T2_37	M22	
IO_L19P_T3_37	U20	
IO_L19N_T3_VREF_37	T20	
IO_L20P_T3_37	T19	
IO_L20N_T3_37	R19	
IO_L21P_T3_DQS_37	U22	
IO_L21N_T3_DQS_37	U21	
IO_L22P_T3_37	P21	
IO_L22N_T3_37	P20	
IO_L23P_T3_37	R22	
IO_L23N_T3_37	P22	
IO_L24P_T3_37	T21	
IO_L24N_T3_37	R21	
IO_25_VRP_37	M21	

VCCO_HP

C21	VCCO_37_C21
F22	VCCO_37_F22
G19	VCCO_37_G19
K20	VCCO_37_K20
N21	VCCO_37_N21
T22	VCCO_37_T22
U19	VCCO_37_U19

U1 SOC_FF1924_OZ_IRON

VCCO_HP
- R287 100 1/10W — IO_0_VRN_37
- R286 100 1/10W — IO_25_VRP_37 — GND

XILINX

Title: I/O BANKS 36, 37 SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
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Sheet 66 of 90	Drawn By RN

SOC_OZ_IRON_FF1924

BANK 38
XC7VX690TFFG1927

IO_0_VRN_38_L15	L15	IO_0_VRN_38
IO_L1P_T0_38_C15	C15	FMC3_LA02_P
IO_L1N_T0_38_C14	C14	FMC3_LA02_N
IO_L2P_T0_38_B15	B15	FMC3_LA03_P
IO_L2N_T0_38_A15	A15	FMC3_LA03_N
IO_L3P_T0_DQS_38_B13	B13	FMC3_LA04_P
IO_L3N_T0_DQS_38_B12	B12	FMC3_LA04_N
IO_L4P_T0_38_A14	A14	FMC3_LA05_P
IO_L4N_T0_38_A13	A13	FMC3_LA05_N
IO_L5P_T0_38_C13	C13	FMC3_LA06_P
IO_L5N_T0_38_C12	C12	FMC3_LA06_N
IO_L6P_T0_38_D15	D15	FMC3_LA07_P
IO_L6N_T0_VREF_38_D14	D14	FMC3_LA07_N
IO_L7P_T1_38_E12	E12	FMC3_LA08_P
IO_L7N_T1_38_D12	D12	FMC3_LA08_N
IO_L8P_T1_38_E14	E14	FMC3_LA09_P
IO_L8N_T1_38_E13	E13	FMC3_LA09_N
IO_L9P_T1_DQS_38_G15	G15	FMC3_LA10_P
IO_L9N_T1_DQS_38_F15	F15	FMC3_LA10_N
IO_L10P_T1_38_F14	F14	FMC3_LA11_P
IO_L10N_T1_38_F13	F13	FMC3_LA11_N
IO_L11P_T1_SRCC_38_H13	H13	FMC3_LA01_CC_P
IO_L11N_T1_SRCC_38_G13	G13	FMC3_LA01_CC_N
IO_L12P_T1_MRCC_38_H15	H15	FMC3_LA00_CC_P
IO_L12N_T1_MRCC_38_H14	H14	FMC3_LA00_CC_N
IO_L13P_T2_MRCC_38_J15	J15	FMC3_HA00_CC_P
IO_L13N_T2_MRCC_38_J14	J14	FMC3_HA00_CC_N
IO_L14P_T2_SRCC_38_K14	K14	FMC3_HA01_CC_P
IO_L14N_T2_SRCC_38_K13	K13	FMC3_HA01_CC_N
IO_L15P_T2_DQS_38_H12	H12	FMC3_LA12_P
IO_L15N_T2_DQS_38_G12	G12	FMC3_LA12_N
IO_L16P_T2_38_M13	M13	FMC3_LA13_P
IO_L16N_T2_38_L13	L13	FMC3_LA13_N
IO_L17P_T2_38_M15	M15	FMC3_LA14_P
IO_L17N_T2_38_L14	L14	FMC3_LA14_N
IO_L18P_T2_38_K12	K12	CM_LVDS1_P
IO_L18N_T2_38_J12	J12	CM_LVDS1_N
IO_L19P_T3_38_R14	R14	FMC3_LA15_P
IO_L19N_T3_VREF_38_P14	P14	FMC3_LA15_N
IO_L20P_T3_38_N14	N14	FMC3_LA16_P
IO_L20N_T3_38_N13	N13	FMC3_LA16_N
IO_L21P_T3_DQS_38_T14	T14	FMC3_HA02_P
IO_L21N_T3_DQS_38_R13	R13	FMC3_HA02_N
IO_L22P_T3_38_N12	N12	FMC3_HA03_P
IO_L22N_T3_38_M12	M12	FMC3_HA03_N
IO_L23P_T3_38_U13	U13	FMC3_HA04_P
IO_L23N_T3_38_T13	T13	FMC3_HA04_N
IO_L24P_T3_38_R12	R12	FMC3_HA05_P
IO_L24N_T3_38_P12	P12	FMC3_HA05_N
IO_25_VRP_38_U12	U12	IO_25_VRP_38

RECOVERY CLOCK

VCCO_HP

B14	VCCO_38_B14
E15	VCCO_38_E15
F12	VCCO_38_F12
J13	VCCO_38_J13
M14	VCCO_38_M14
T12	VCCO_38_T12

U1

SOC_FF1924_OZ_IRON

VCCO_HP

R336 100 1/10W

IO_0_VRN_38

IO_25_VRP_38

R335 100 1/10W

GND

SOC_OZ_IRON_FF1924

BANK 39
XC7VX690TFFG1927

IO_0_VRN_39_K18	K18	FMC3_PRSNT_M2C_L
IO_L1P_T0_39_C18	C18	FMC3_LA19_P
IO_L1N_T0_39_B18	B18	FMC3_LA19_N
IO_L2P_T0_39_B16	B16	FMC3_LA20_P
IO_L2N_T0_39_A16	A16	FMC3_LA20_N
IO_L3P_T0_DQS_39_D19	D19	FMC3_LA21_P
IO_L3N_T0_DQS_39_C19	C19	FMC3_LA21_N
IO_L4P_T0_39_C17	C17	FMC3_LA22_P
IO_L4N_T0_39_B17	B17	FMC3_LA22_N
IO_L5P_T0_39_A19	A19	FMC3_LA23_P
IO_L5N_T0_39_A18	A18	FMC3_LA23_N
IO_L6P_T0_39_D17	D17	FMC3_LA24_P
IO_L6N_T0_VREF_39_D16	D16	FMC3_LA24_N
IO_L7P_T1_39_E17	E17	FMC3_LA25_P
IO_L7N_T1_39_E16	E16	FMC3_LA25_N
IO_L8P_T1_39_G18	G18	FMC3_LA26_P
IO_L8N_T1_39_F18	F18	FMC3_LA26_N
IO_L9P_T1_DQS_39_G16	G16	FMC3_LA27_P
IO_L9N_T1_DQS_39_F16	F16	FMC3_LA27_N
IO_L10P_T1_39_E19	E19	FMC3_LA28_P
IO_L10N_T1_39_E18	E18	FMC3_LA28_N
IO_L11P_T1_SRCC_39_J17	J17	FMC3_LA18_CC_P
IO_L11N_T1_SRCC_39_H17	H17	FMC3_LA18_CC_N
IO_L12P_T1_MRCC_39_H18	H18	FMC3_LA17_CC_P
IO_L12N_T1_MRCC_39_G17	G17	FMC3_LA17_CC_N
IO_L13P_T2_MRCC_39_K17	K17	FMC3_CLK0_M2C_P
IO_L13N_T2_MRCC_39_J16	J16	FMC3_CLK0_M2C_N
IO_L14P_T2_SRCC_39_L16	L16	FMC3_CLK1_M2C_P
IO_L14N_T2_SRCC_39_K16	K16	FMC3_CLK1_M2C_N
IO_L15P_T2_DQS_39_P17	P17	FMC3_LA29_P
IO_L15N_T2_DQS_39_N17	N17	FMC3_LA29_N
IO_L16P_T2_39_M18	M18	FMC3_LA30_P
IO_L16N_T2_39_L18	L18	FMC3_LA30_N
IO_L17P_T2_39_P15	P15	FMC3_LA31_P
IO_L17N_T2_39_N15	N15	FMC3_LA31_N
IO_L18P_T2_39_M17	M17	FMC3_LA32_P
IO_L18N_T2_39_M16	M16	FMC3_LA32_N
IO_L19P_T3_39_T16	T16	FMC3_LA33_P
IO_L19N_T3_VREF_39_T15	T15	FMC3_LA33_N
IO_L20P_T3_39_R16	R16	FMC3_HA06_P
IO_L20N_T3_39_P16	P16	FMC3_HA06_N
IO_L21P_T3_DQS_39_U17	U17	FMC3_HA07_P
IO_L21N_T3_DQS_39_U16	U16	FMC3_HA07_N
IO_L22P_T3_39_R18	R18	FMC3_HA08_P
IO_L22N_T3_39_R17	R17	FMC3_HA08_N
IO_L23P_T3_39_U18	U18	FMC3_HA09_P
IO_L23N_T3_39_T18	T18	FMC3_HA09_N
IO_L24P_T3_39_V15	V15	FMC3_HA10_P
IO_L24N_T3_39_U15	U15	FMC3_HA10_N
IO_25_VRP_39_N18	N18	IO_25_VRP_39

VCCO_HP

A17	VCCO_39_A17
D18	VCCO_39_D18
H16	VCCO_39_H16
L17	VCCO_39_L17
P18	VCCO_39_P18
R15	VCCO_39_R15
V16	VCCO_39_V16

U1

SOC_FF1924_OZ_IRON

XILINX

Title: I/O BANKS 38, 39
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

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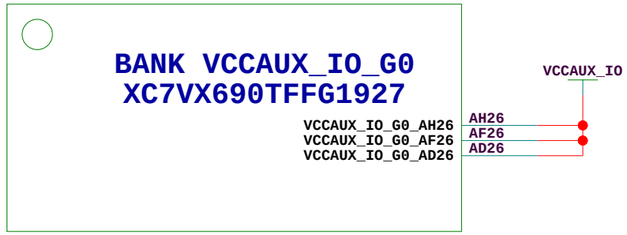
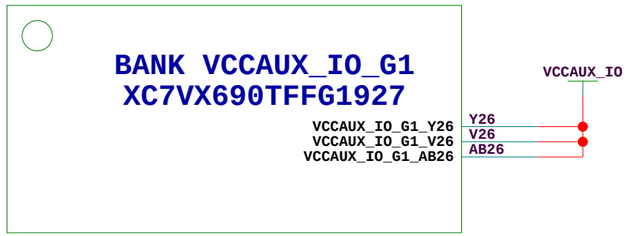
FPGA POWER, VCCAUX / VCCAUX_IO / VCCBRAM

SOC_OZ_IRON_FF1924



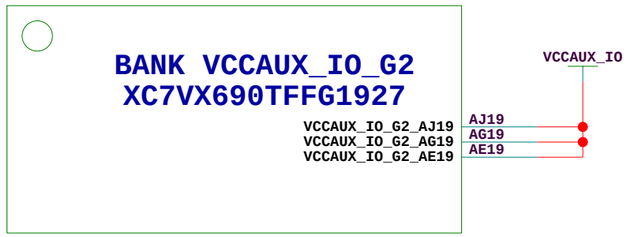
U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924



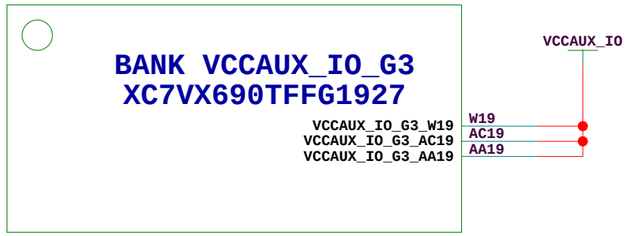
U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924



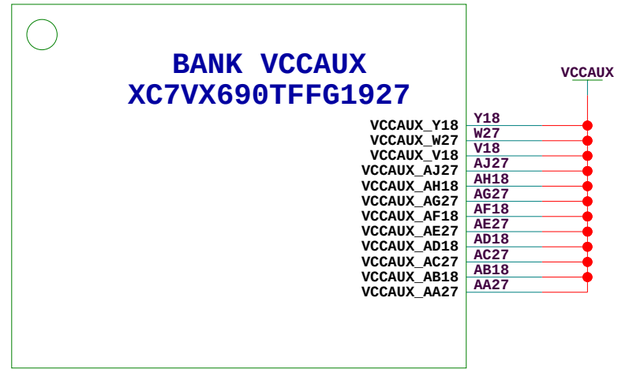
U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924



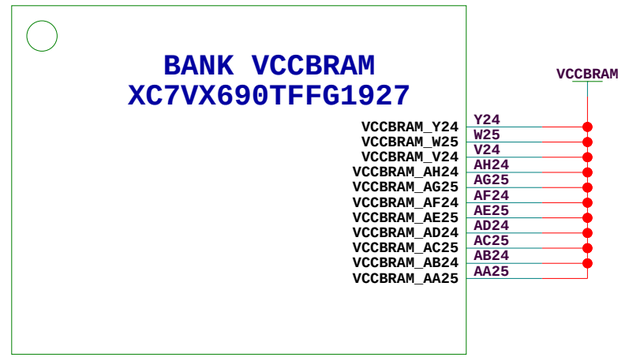
U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924



U1 SOC_FF1924_OZ_IRON

SOC_OZ_IRON_FF1924



U1 SOC_FF1924_OZ_IRON

XILINX

Title: FPGA POWER SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40		Ver: 1.0
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FPGA POWER, VCCINT

SOC_OZ_IRON_FF1924

BANK VCCINT
XC7VX690TFFG1927

VCCINT

VCCINT_Y32	Y32
VCCINT_Y30	Y30
VCCINT_Y28	Y28
VCCINT_Y22	Y22
VCCINT_Y20	Y20
VCCINT_Y16	Y16
VCCINT_Y14	Y14
VCCINT_Y12	Y12
VCCINT_W33	W33
VCCINT_W31	W31
VCCINT_W29	W29
VCCINT_W23	W23
VCCINT_W21	W21
VCCINT_W17	W17
VCCINT_W15	W15
VCCINT_W13	W13
VCCINT_V32	V32
VCCINT_V30	V30
VCCINT_V28	V28
VCCINT_V22	V22
VCCINT_V20	V20
VCCINT_V14	V14
VCCINT_V12	V12
VCCINT_AJ33	AJ33
VCCINT_AJ17	AJ17
VCCINT_AJ15	AJ15
VCCINT_AH32	AH32
VCCINT_AH30	AH30
VCCINT_AH28	AH28
VCCINT_AH22	AH22
VCCINT_AH20	AH20
VCCINT_AH16	AH16
VCCINT_AH14	AH14
VCCINT_AH12	AH12
VCCINT_AG33	AG33
VCCINT_AG31	AG31
VCCINT_AG29	AG29
VCCINT_AG23	AG23
VCCINT_AG21	AG21
VCCINT_AG17	AG17
VCCINT_AG15	AG15
VCCINT_AG13	AG13
VCCINT_AF32	AF32
VCCINT_AF30	AF30
VCCINT_AF28	AF28
VCCINT_AF22	AF22
VCCINT_AF20	AF20
VCCINT_AF16	AF16
VCCINT_AF14	AF14
VCCINT_AF12	AF12
VCCINT_AE33	AE33
VCCINT_AE31	AE31
VCCINT_AE29	AE29
VCCINT_AE21	AE21
VCCINT_AE17	AE17
VCCINT_AE15	AE15
VCCINT_AE13	AE13
VCCINT_AD32	AD32
VCCINT_AD30	AD30
VCCINT_AD28	AD28
VCCINT_AD20	AD20
VCCINT_AD16	AD16
VCCINT_AD14	AD14
VCCINT_AD12	AD12
VCCINT_AC33	AC33
VCCINT_AC31	AC31
VCCINT_AC29	AC29
VCCINT_AC21	AC21
VCCINT_AC17	AC17
VCCINT_AC15	AC15
VCCINT_AC13	AC13
VCCINT_AB32	AB32
VCCINT_AB30	AB30
VCCINT_AB28	AB28
VCCINT_AB20	AB20
VCCINT_AB16	AB16
VCCINT_AB14	AB14
VCCINT_AB12	AB12
VCCINT_AA33	AA33
VCCINT_AA31	AA31
VCCINT_AA29	AA29
VCCINT_AA23	AA23
VCCINT_AA21	AA21
VCCINT_AA17	AA17
VCCINT_AA15	AA15
VCCINT_AA13	AA13

VCCINT_SPY_P

U1

SOC_FF1924_OZ_IRON

XILINX

Title: FPGA POWER
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-11-2013_15:40

Ver: 1.0

Sheet Size: B

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FPGA GROUND

XILINX

Title: FPGA GROUND SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
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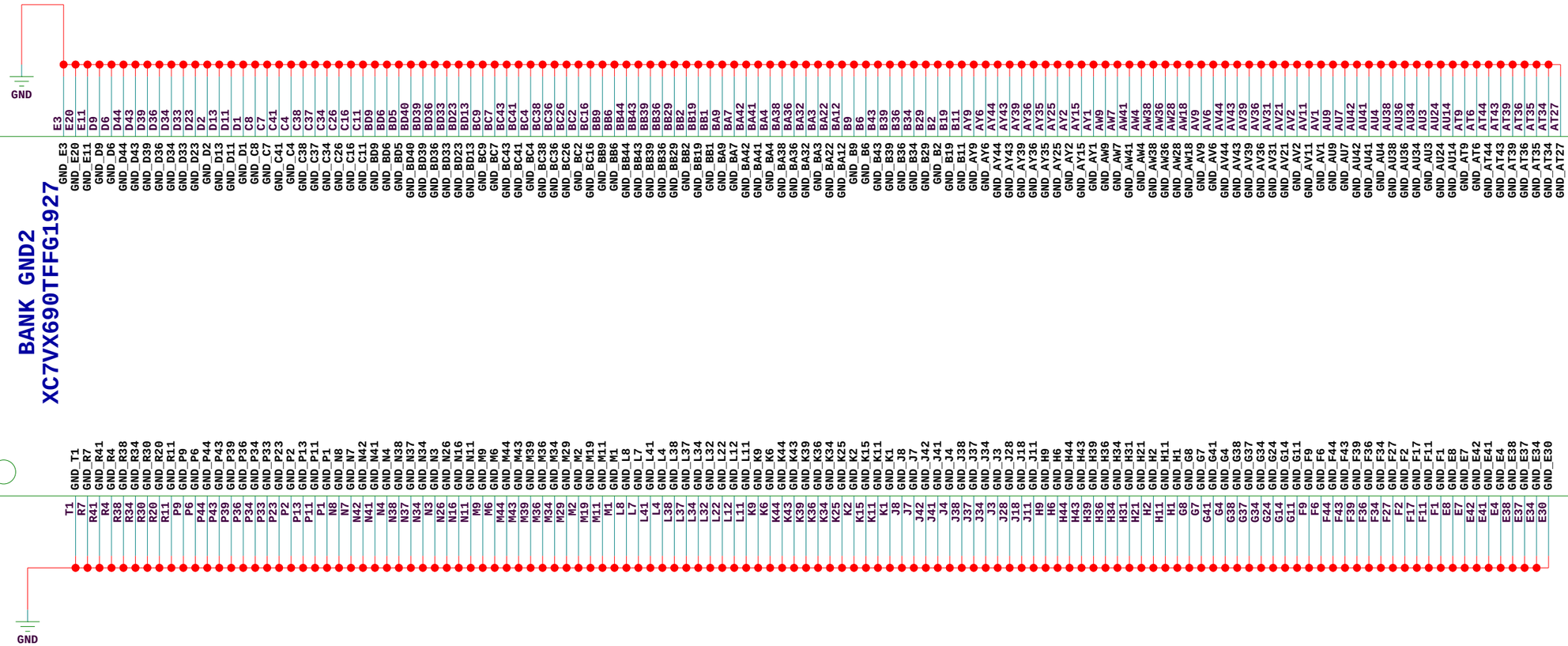
FPGA GROUND



Title: FPGA GROUND SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-12-2013_11:36	Ver: 1.0
Sheet Size: B	Rev: 01
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FPGA GROUND

SOC_OZ_IRON_FF1924

BANK GND3
XC7VX690TFFG1927

GND_Y9	Y9	
GND_Y6	Y6	MGTAVTT_100_SPY_N
GND_Y44	Y44	
GND_Y43	Y43	
GND_Y39	Y39	MGTAVTT_200_SPY_N
GND_Y36	Y36	
GND_Y34	Y34	
GND_Y33	Y33	
GND_Y31	Y31	
GND_Y29	Y29	
GND_Y27	Y27	
GND_Y25	Y25	
GND_Y23	Y23	
GND_Y21	Y21	
GND_Y2	Y2	
GND_Y19	Y19	
GND_Y17	Y17	
GND_Y15	Y15	
GND_Y13	Y13	
GND_Y11	Y11	
GND_Y1	Y1	
GND_W7	W7	
GND_W41	W41	
GND_W4	W4	
GND_W38	W38	
GND_W34	W34	
GND_W32	W32	
GND_W30	W30	
GND_W28	W28	
GND_W26	W26	
GND_W24	W24	
GND_W22	W22	
GND_W20	W20	
GND_W18	W18	
GND_W16	W16	
GND_W14	W14	
GND_W12	W12	
GND_W11	W11	
GND_V9	V9	
GND_V6	V6	
GND_V44	V44	
GND_V43	V43	
GND_V39	V39	
GND_V36	V36	
GND_V34	V34	
GND_V33	V33	
GND_V31	V31	
GND_V29	V29	
GND_V27	V27	
GND_V25	V25	
GND_V23	V23	
GND_V21	V21	
GND_V2	V2	
GND_V19	V19	
GND_V17	V17	
GND_V13	V13	
GND_V11	V11	
GND_V1	V1	
GND_U7	U7	
GND_U42	U42	
GND_U41	U41	
GND_U4	U4	
GND_U38	U38	
GND_U34	U34	
GND_U3	U3	
GND_U24	U24	
GND_U14	U14	
GND_U11	U11	
GND_T9	T9	
GND_T6	T6	
GND_T44	T44	
GND_T43	T43	
GND_T39	T39	
GND_T36	T36	
GND_T34	T34	
GND_T27	T27	
GND_T2	T2	
GND_T17	T17	
GND_T11	T11	

GND

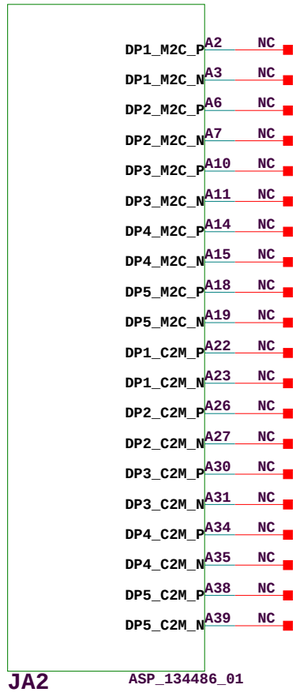
U1

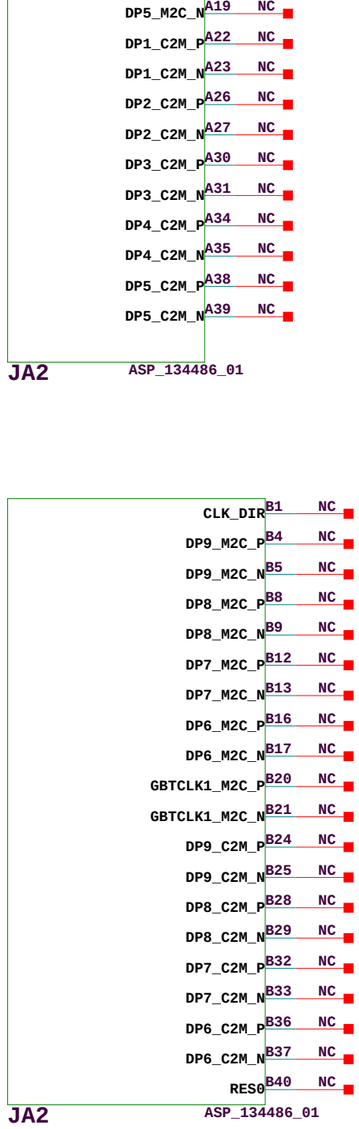
SOC_FF1924_OZ_IRON

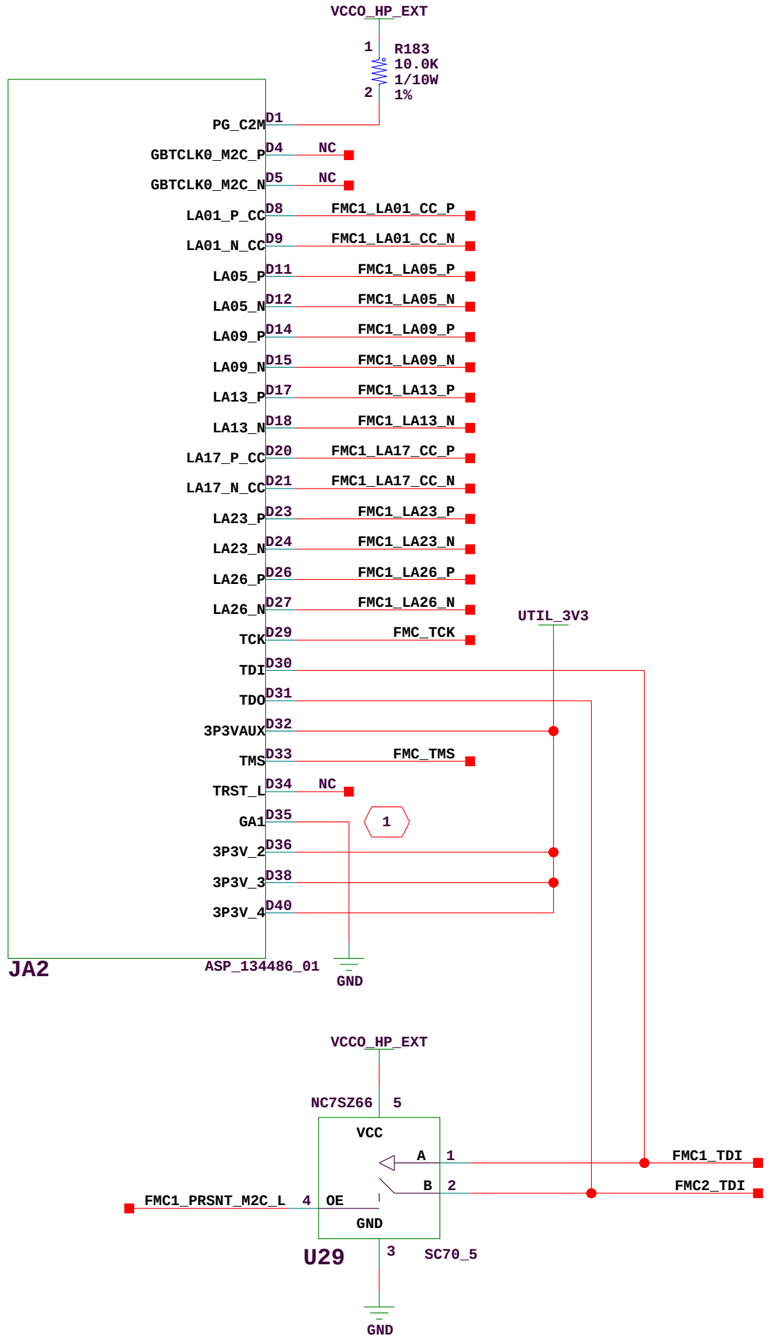
XILINX

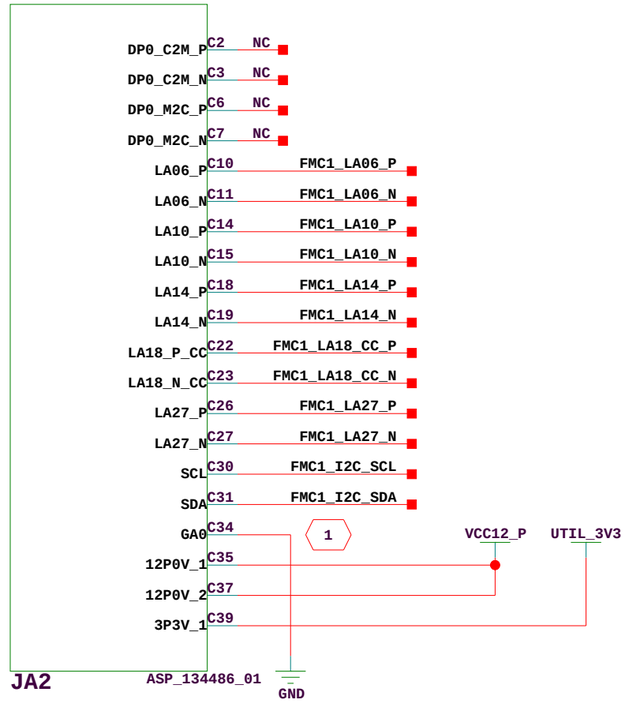
Title: FPGA GROUND SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-12-2013_11:36		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 72 of 90		Drawn By RN	

FMC1 INTERFACE

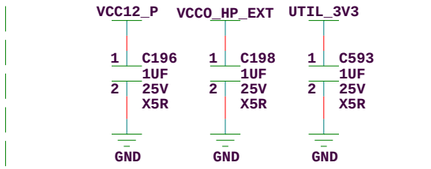








FMC1 DECOUPLING CAPS

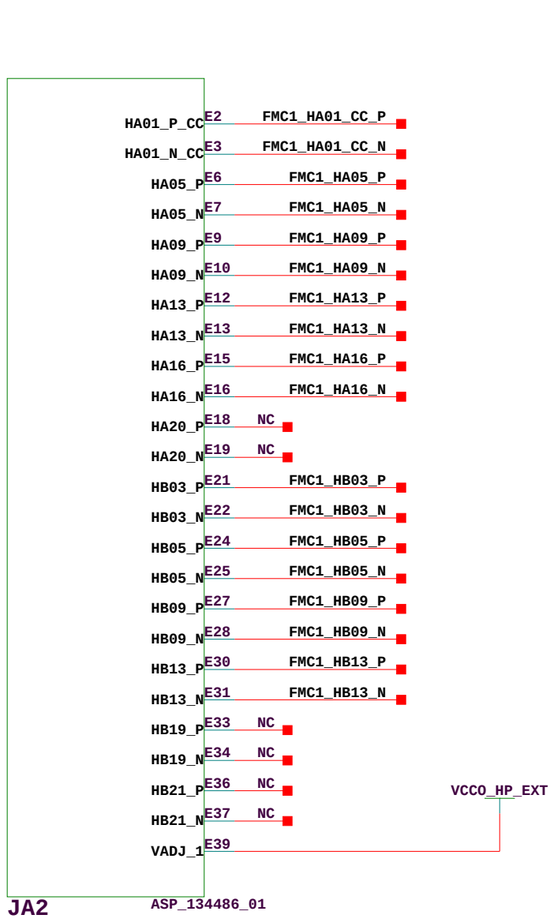


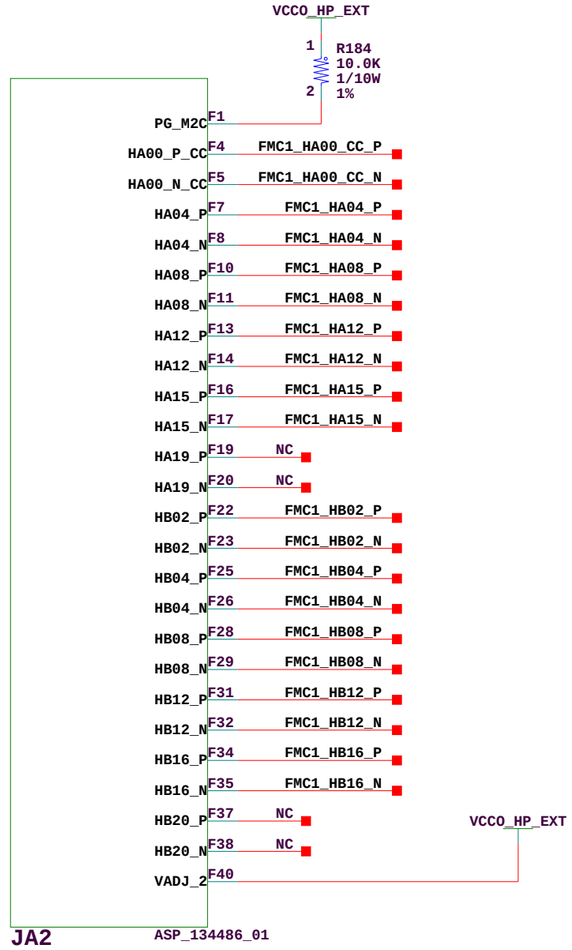
1 FMC GLOBAL ADDRESS BIT GA[0:1]

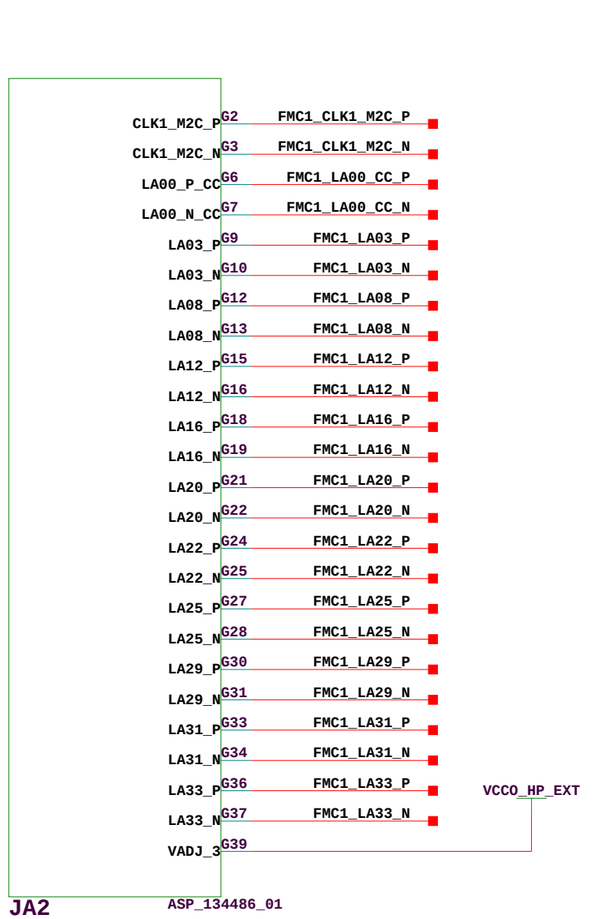
XILINX

Title: FMC1 (ROWS A, B, C, D) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 73 of 90	Drawn By RN

FMC1 INTERFACE



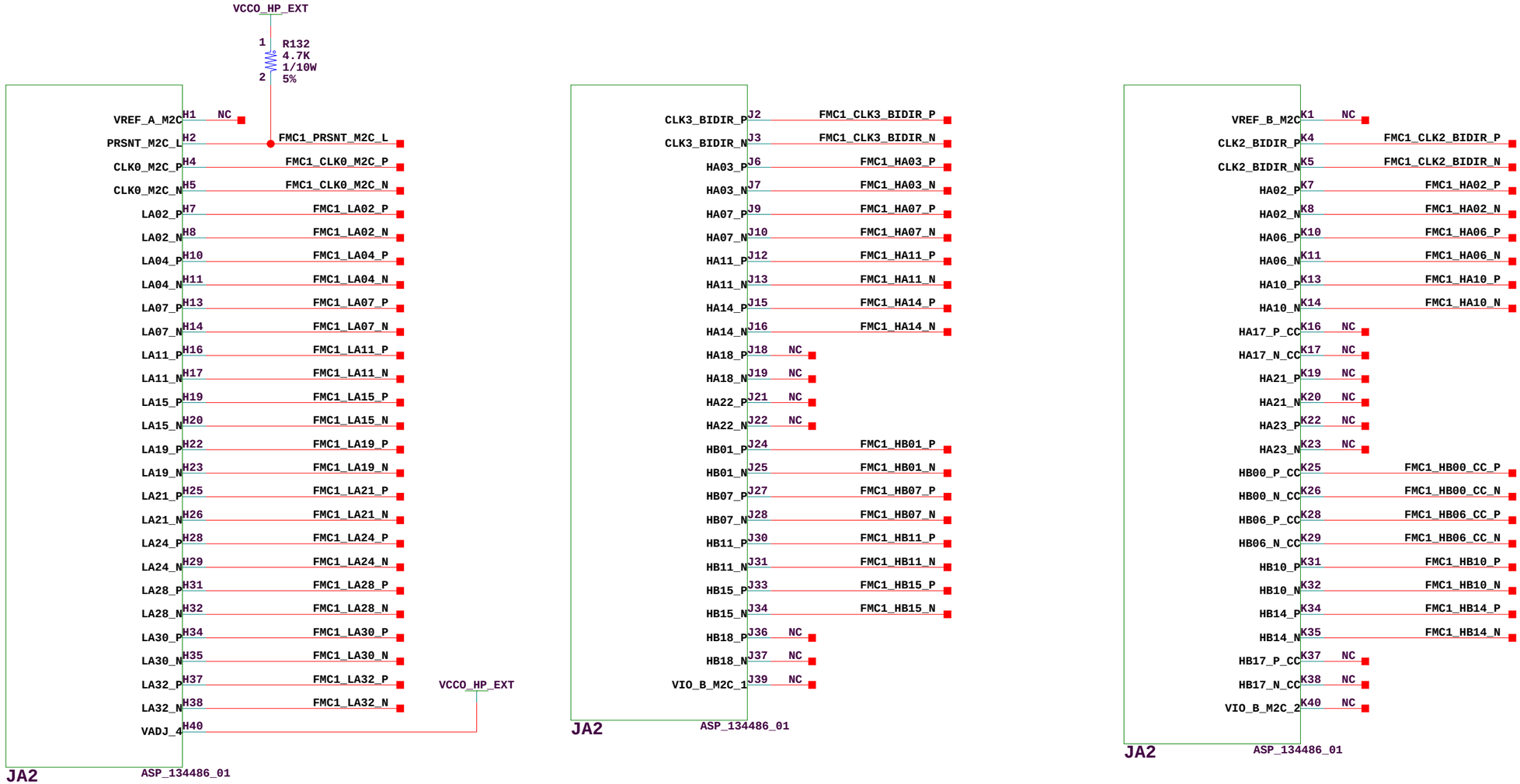




XILINX

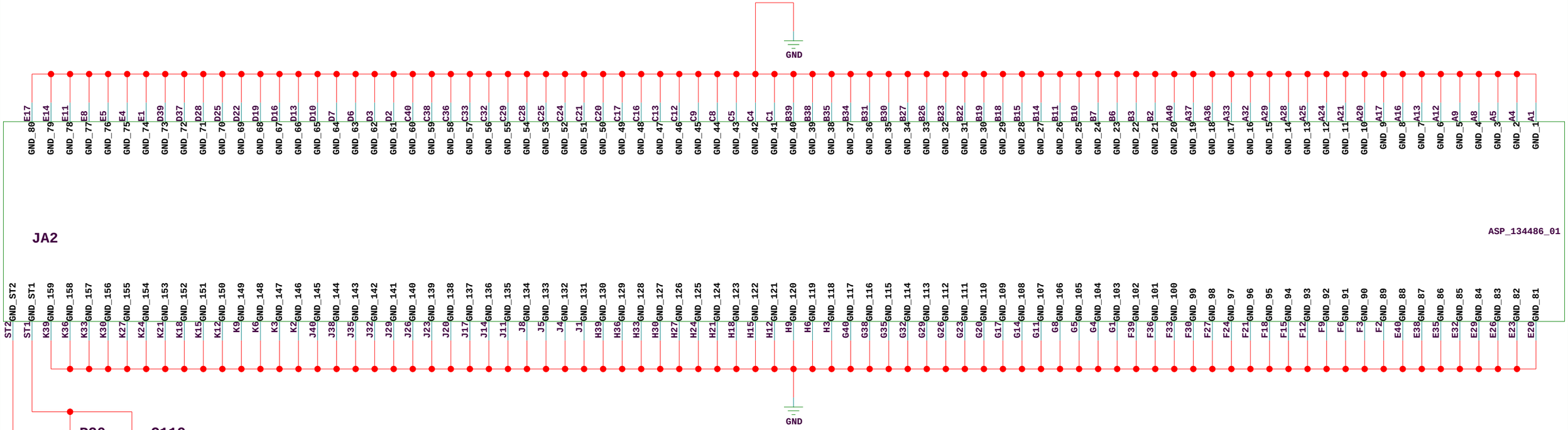
Title: FMC1 (ROWS E, F, G) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 74	of 90	Drawn By RN	

FMC1 INTERFACE



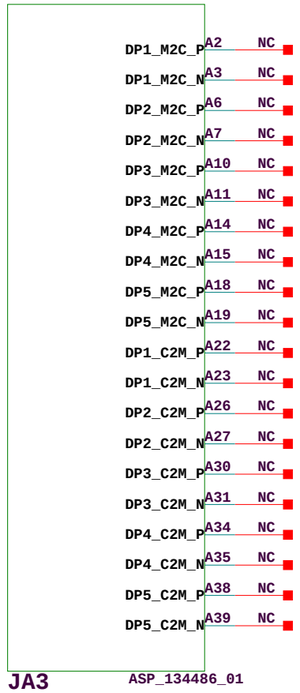
Title:	FMC1 (ROWS H, J, K) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: PCB P/N: SCH P/N: TEST P/N:	0431676 1280597 0381429 TSS0XXX
Date:	4-11-2013_15:40	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	75 of 90	Drawn By	RN

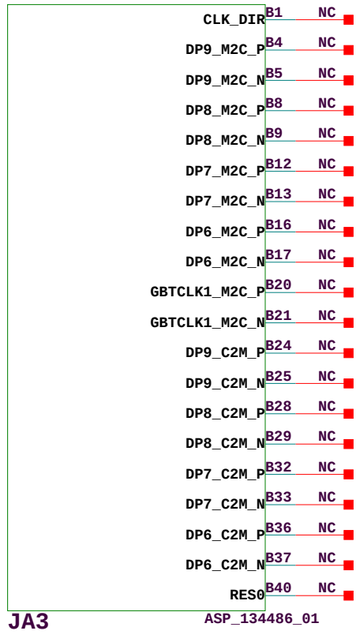
FMC1 INTERFACE

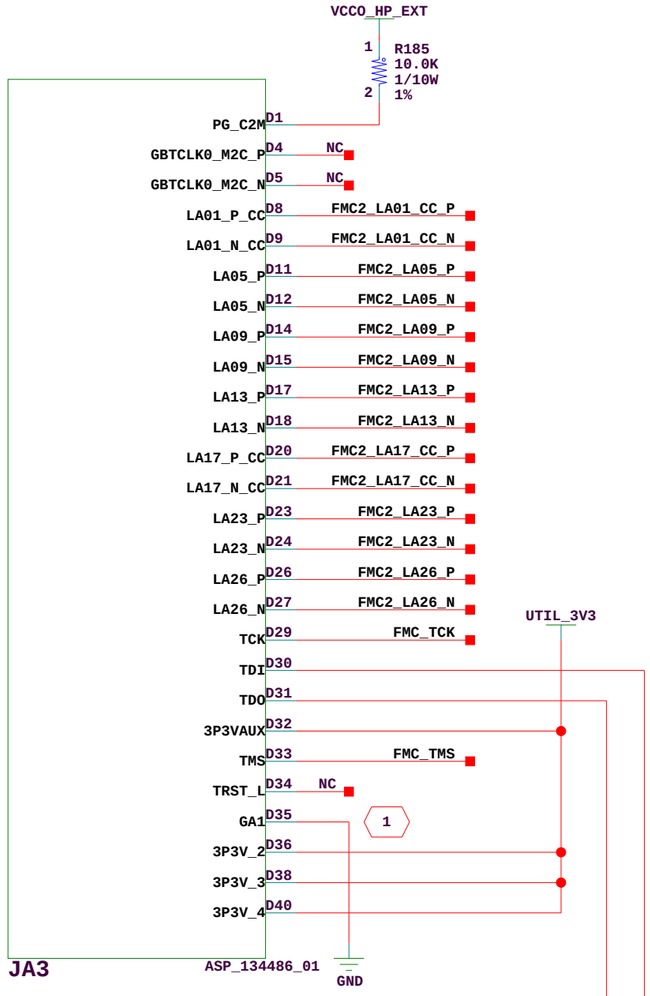


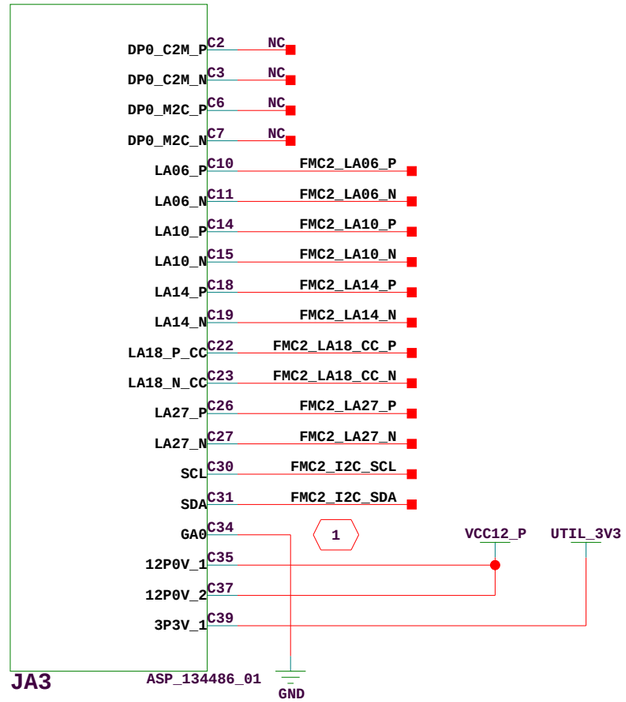
Title: FMC1 (GND) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 76 of 90	Drawn By RN

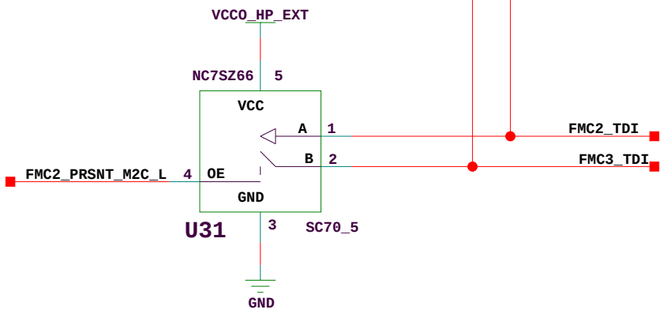
FMC2 INTERFACE

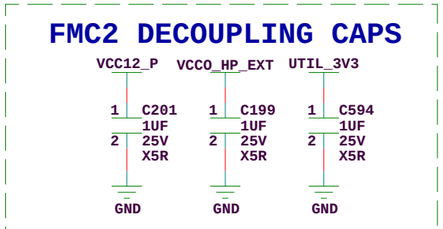












1 FMC GLOBAL ADDRESS BIT GA[0:1]

XILINX

Title: FMC2 (ROWS A, B, C, D) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
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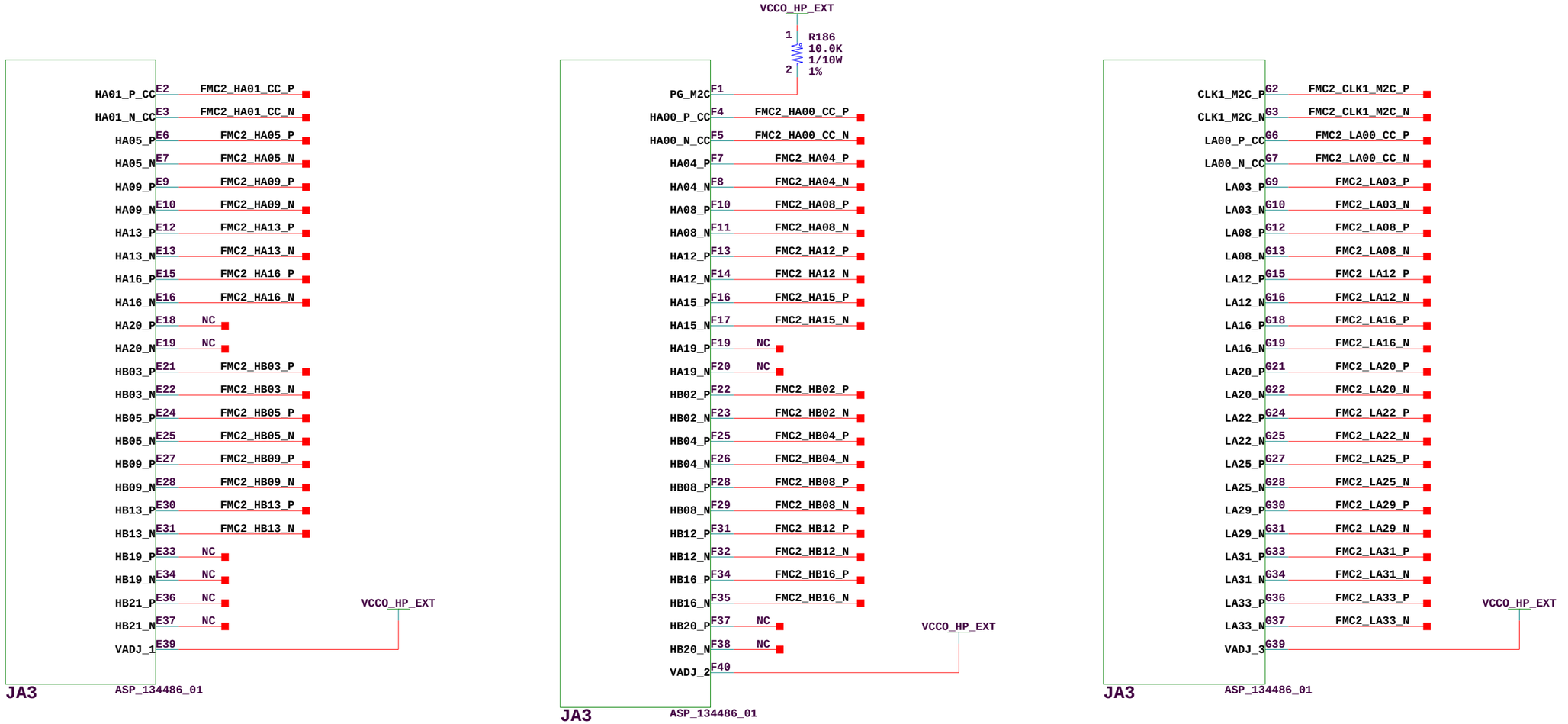
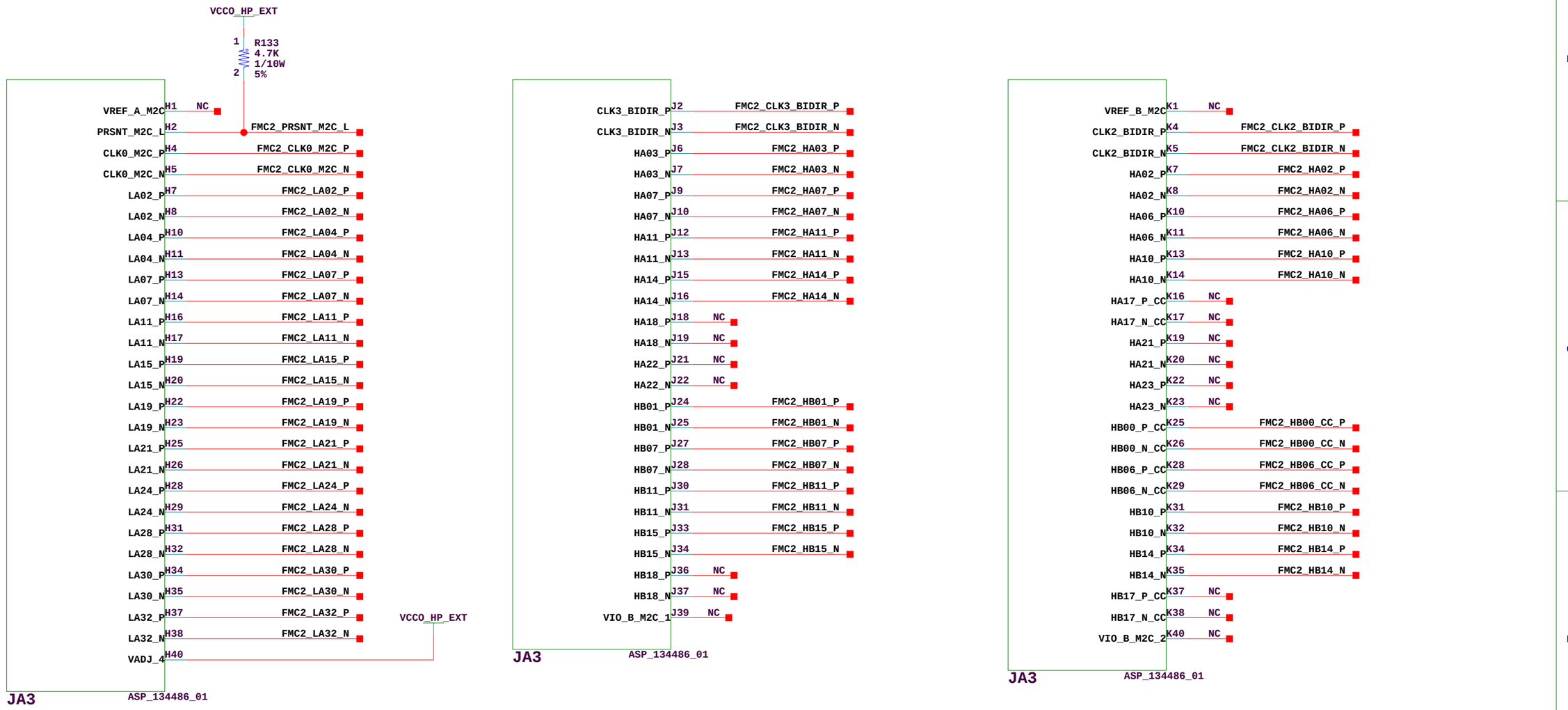
FMC2 INTERFACE



XILINX

Title:	FMC2 (ROWS E, F, G) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N:	0431676
		PCB P/N:	1280597
		SCH P/N:	0381429
		TEST P/N:	TSS0XXX
Date:	4-11-2013_15:40	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	78 of 90	Drawn By	RN

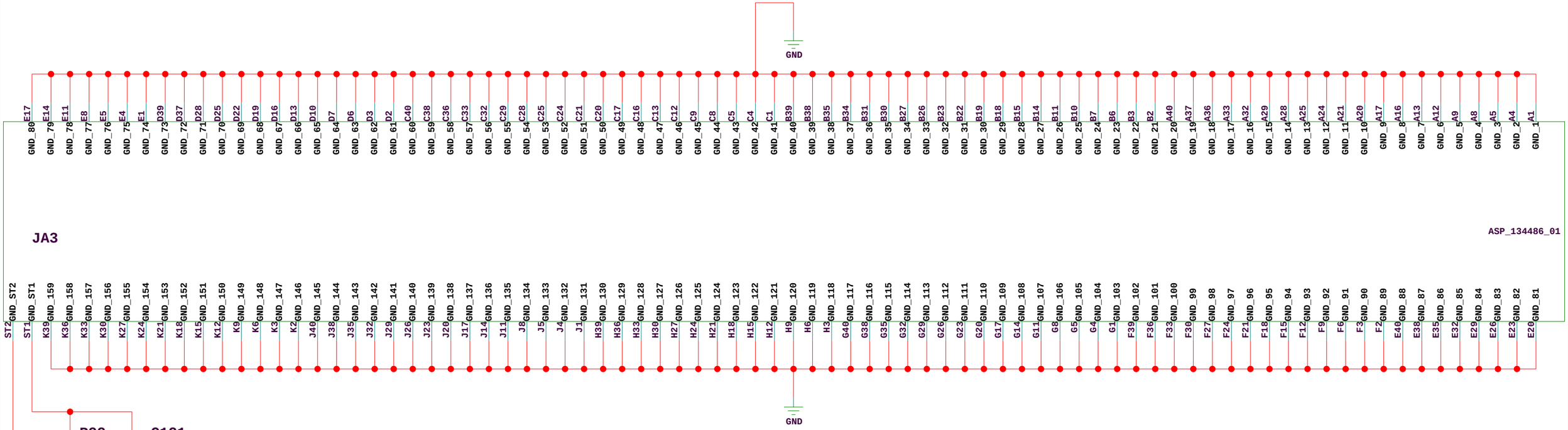
FMC2 INTERFACE



XILINX

Title:	FMC2 (ROWS H, J, K) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: PCB P/N: SCH P/N: TEST P/N:	0431676 1280597 0381429 TSS0XXX
Date:	4-11-2013_15:40	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	79 of 90	Drawn By	RN

FMC2 INTERFACE



XILINX

Title: FMC2 (GND) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0	
Sheet Size: B	Rev: 01	
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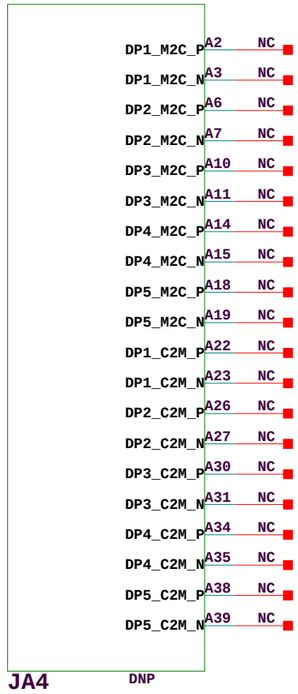
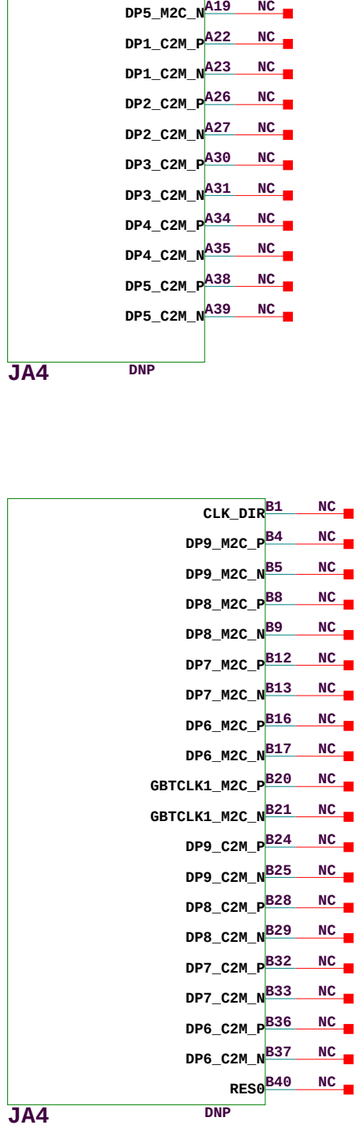
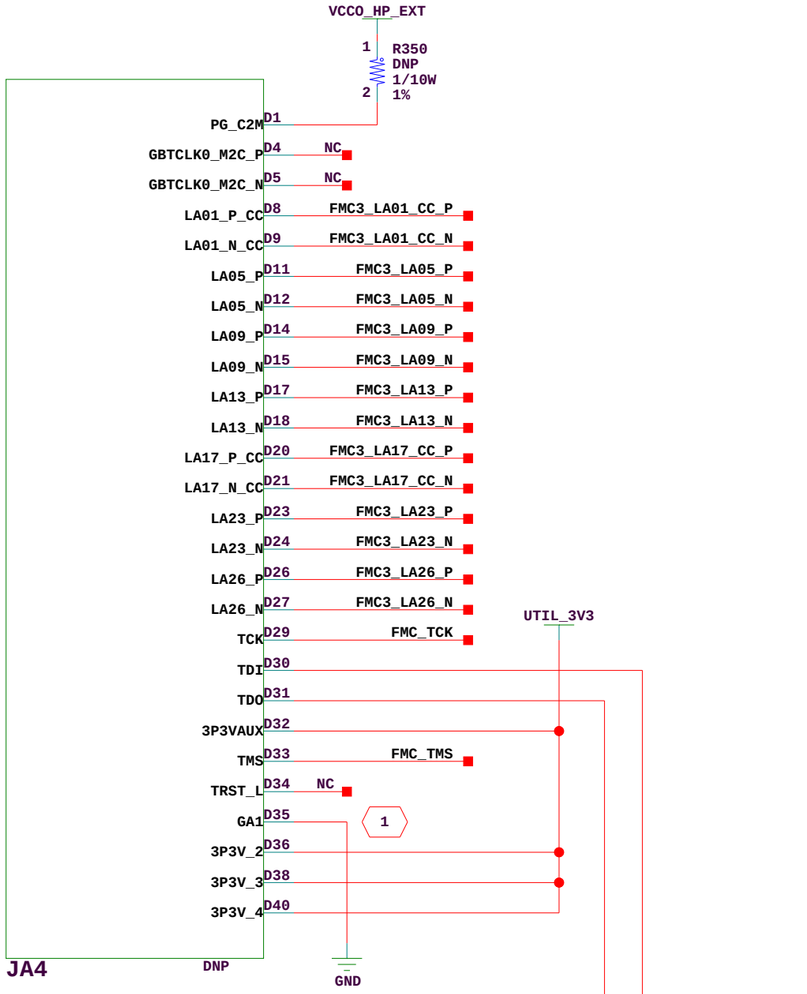
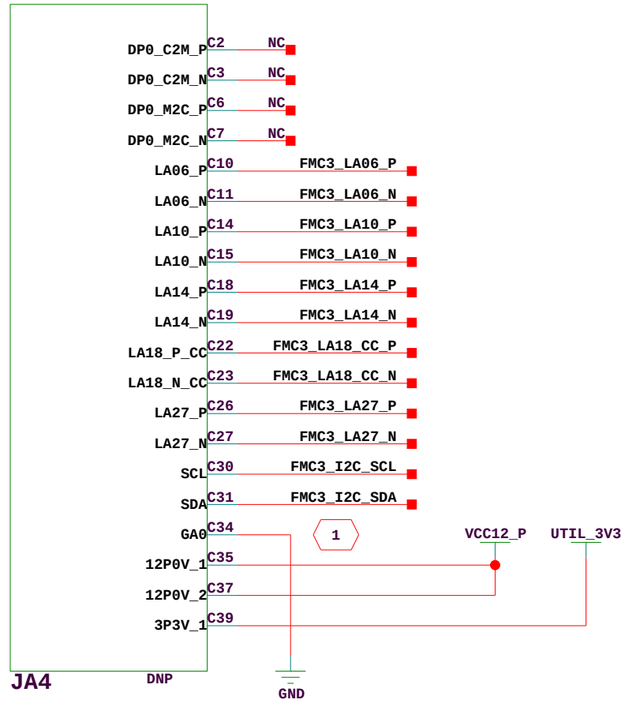
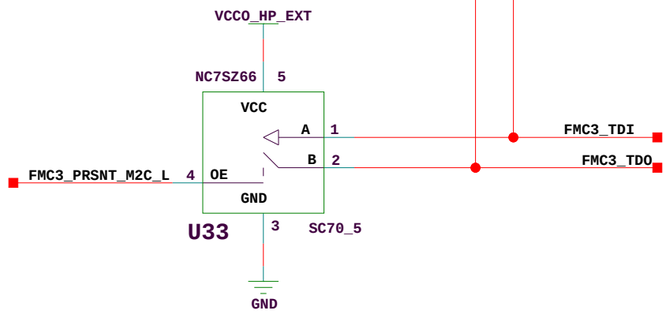
FMC3 INTERFACE



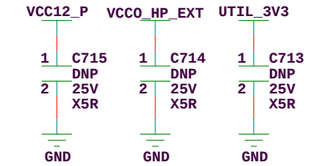








FMC3 DECOUPLING CAPS



1 FMC GLOBAL ADDRESS BIT GA[0:1]

XILINX

Title: FMC3 (ROWS A, B, C, D) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_18:23		Ver: 1.0	
Sheet Size: B		Rev: 01	
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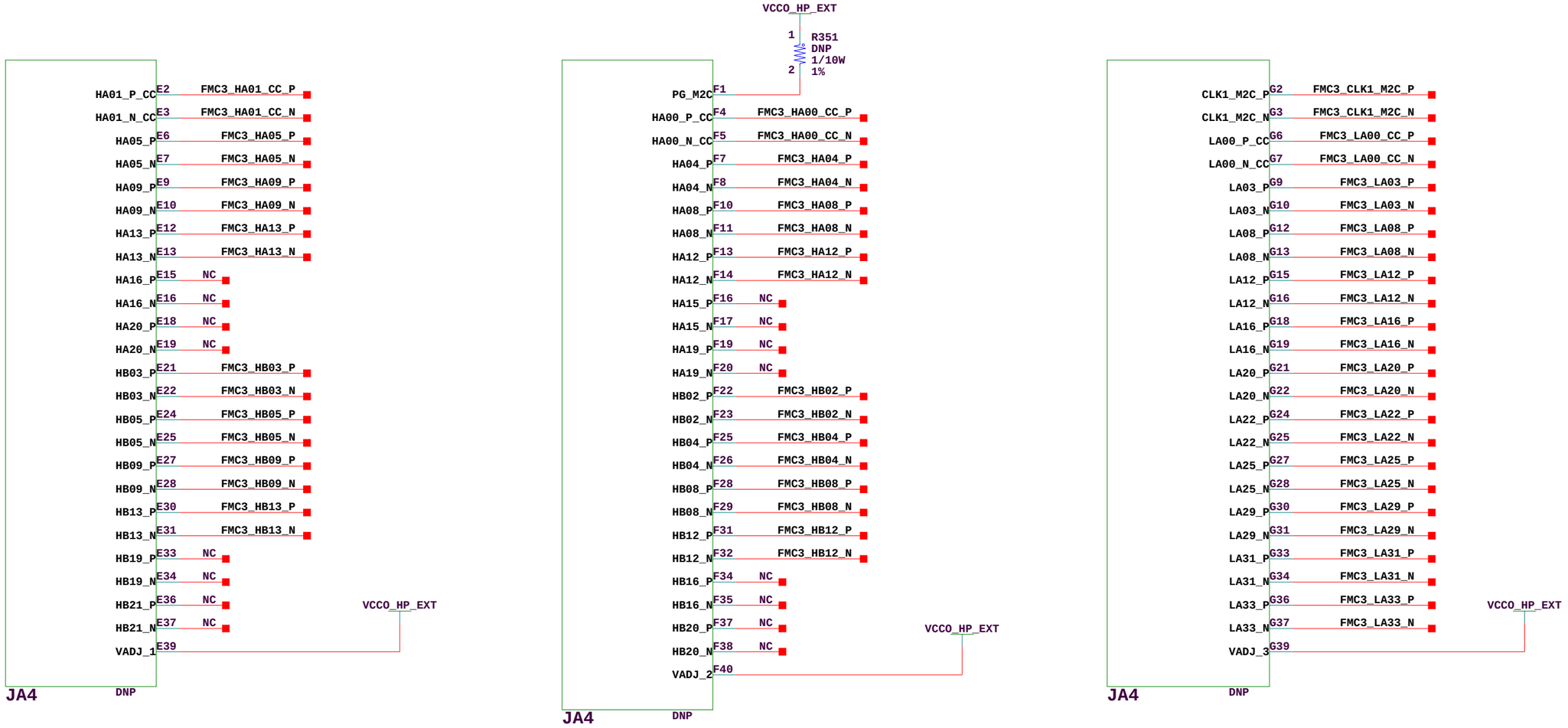
FMC3 INTERFACE



XILINX

Title: FMC3 (ROWS E, F, G) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23		Ver: 1.0
Sheet Size: B		Rev: 01
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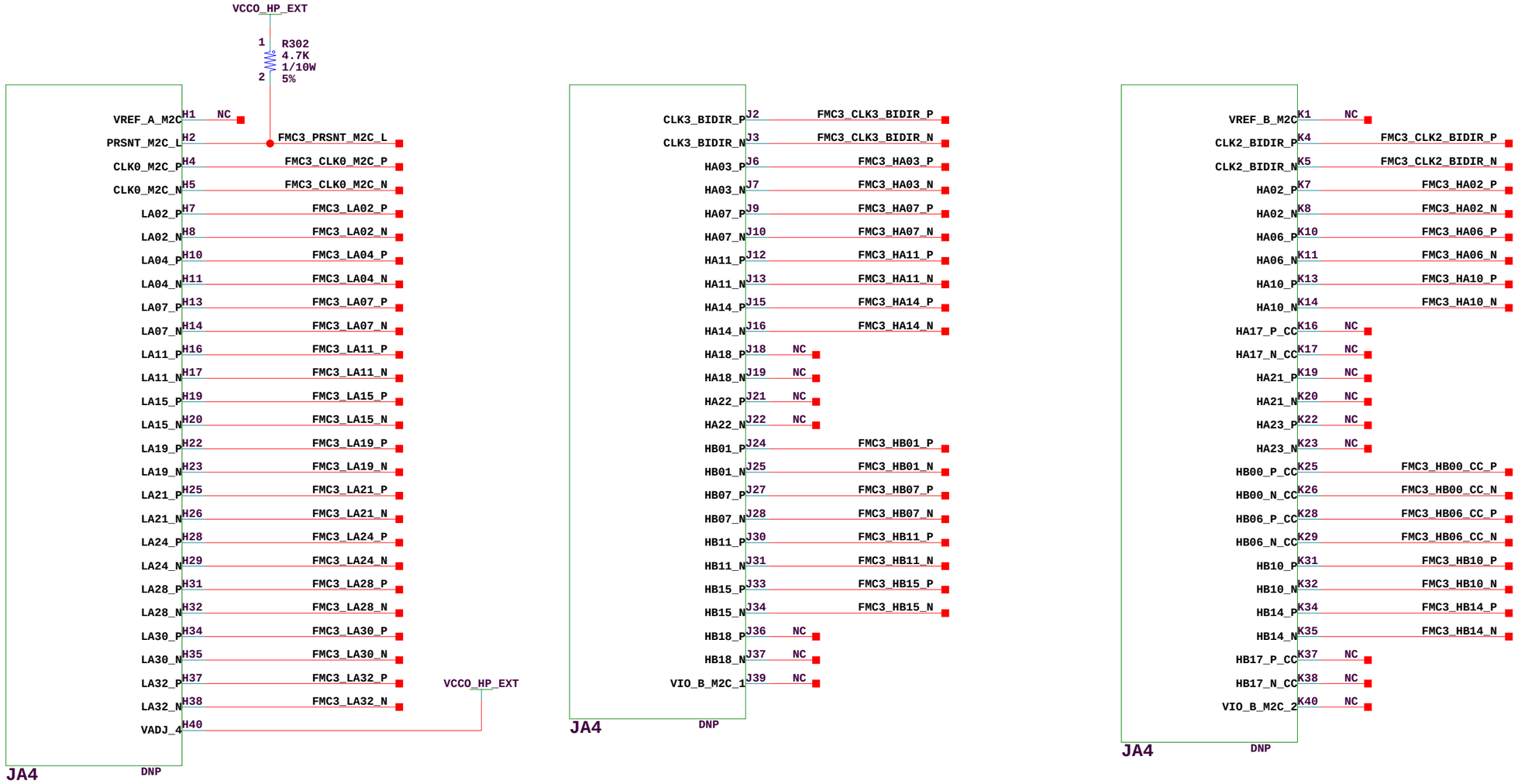
FMC3 INTERFACE



XILINX

Title: FMC3 (ROWS H, J, K) SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_18:23		Ver: 1.0	
Sheet Size: B		Rev: 01	
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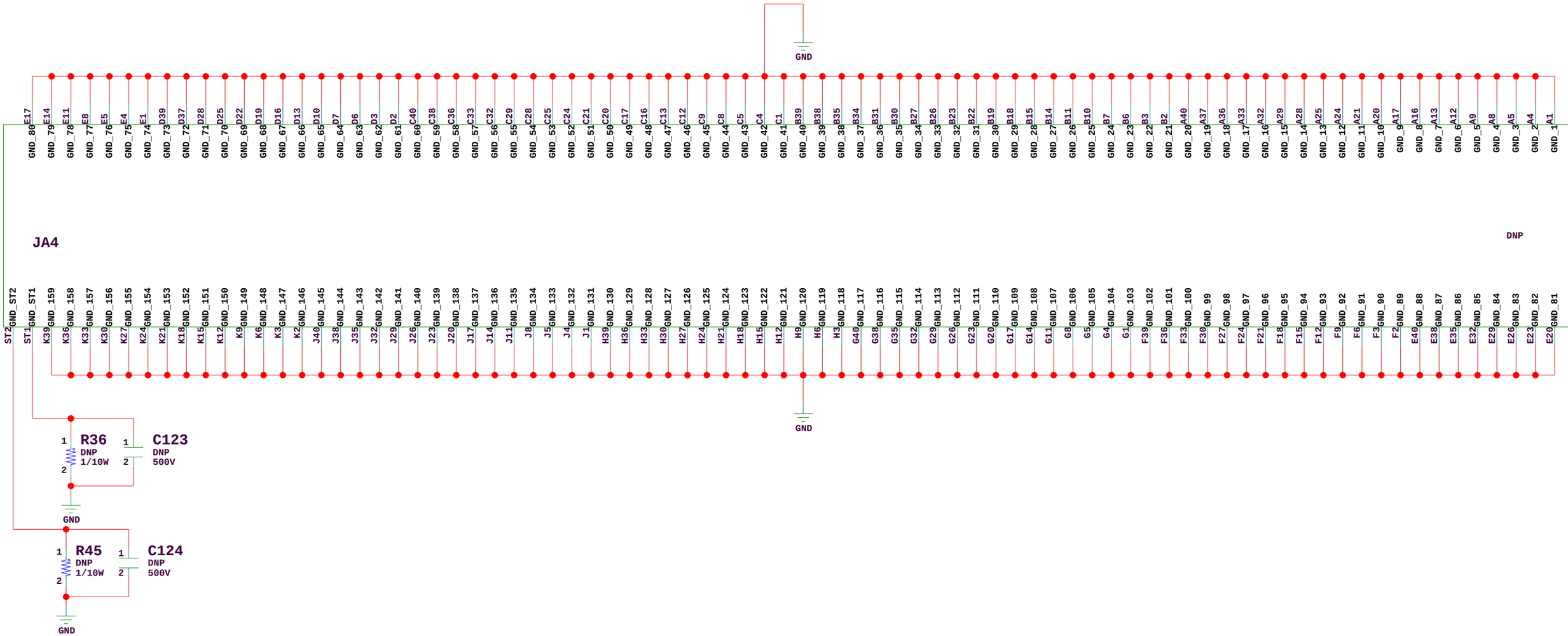
FMC3 INTERFACE



Title: FMC3 GND SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
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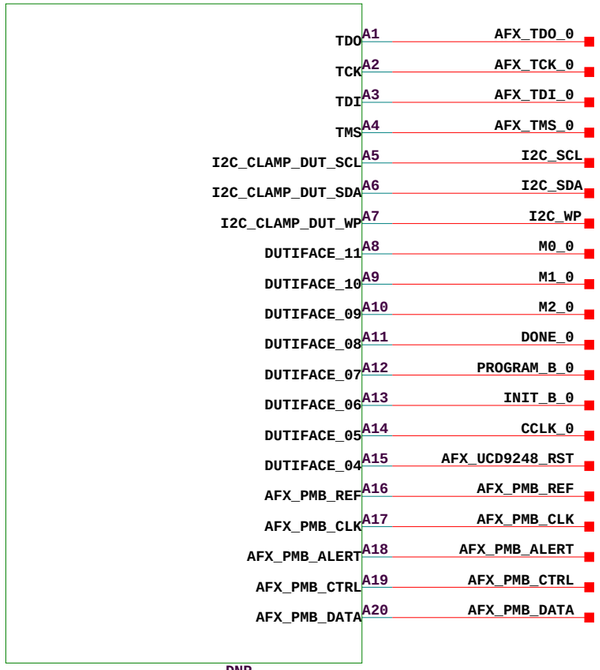
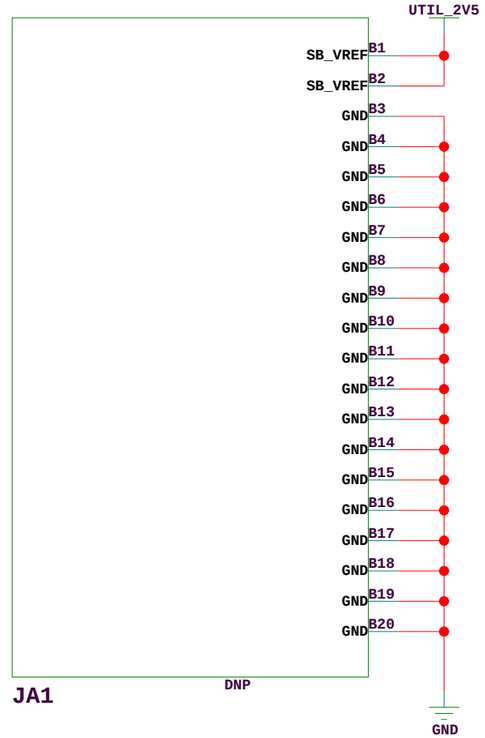
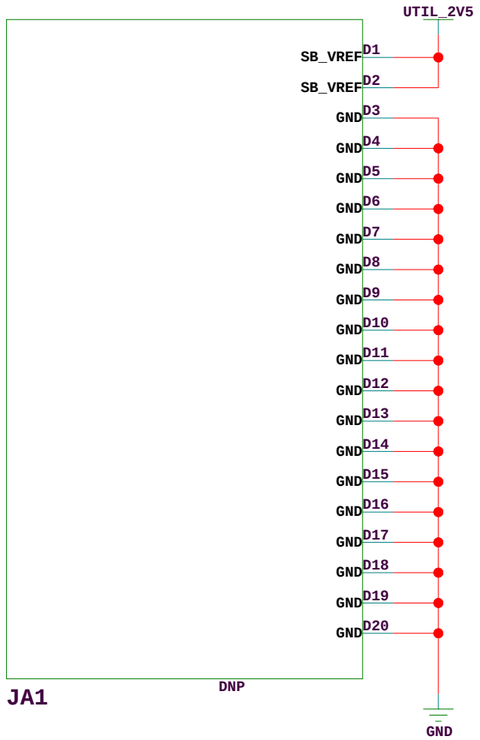
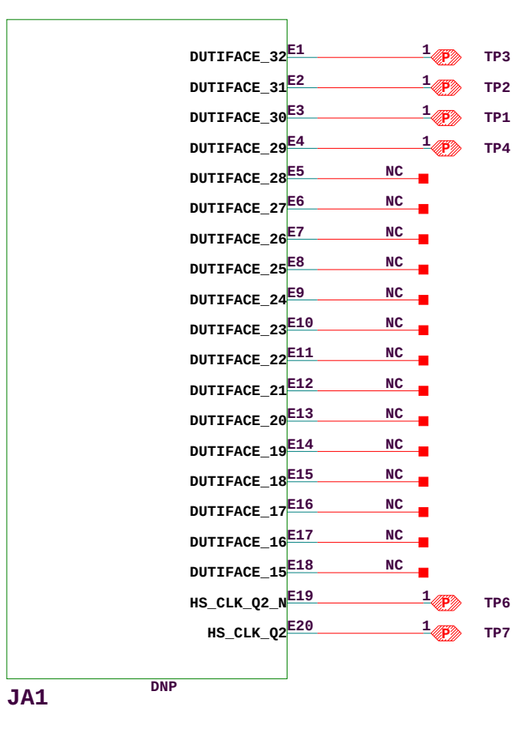
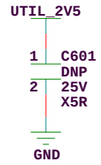
AFX SIDEBAND CONNECTOR











XILINX

Title: AFX CONTROL SIGNALS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
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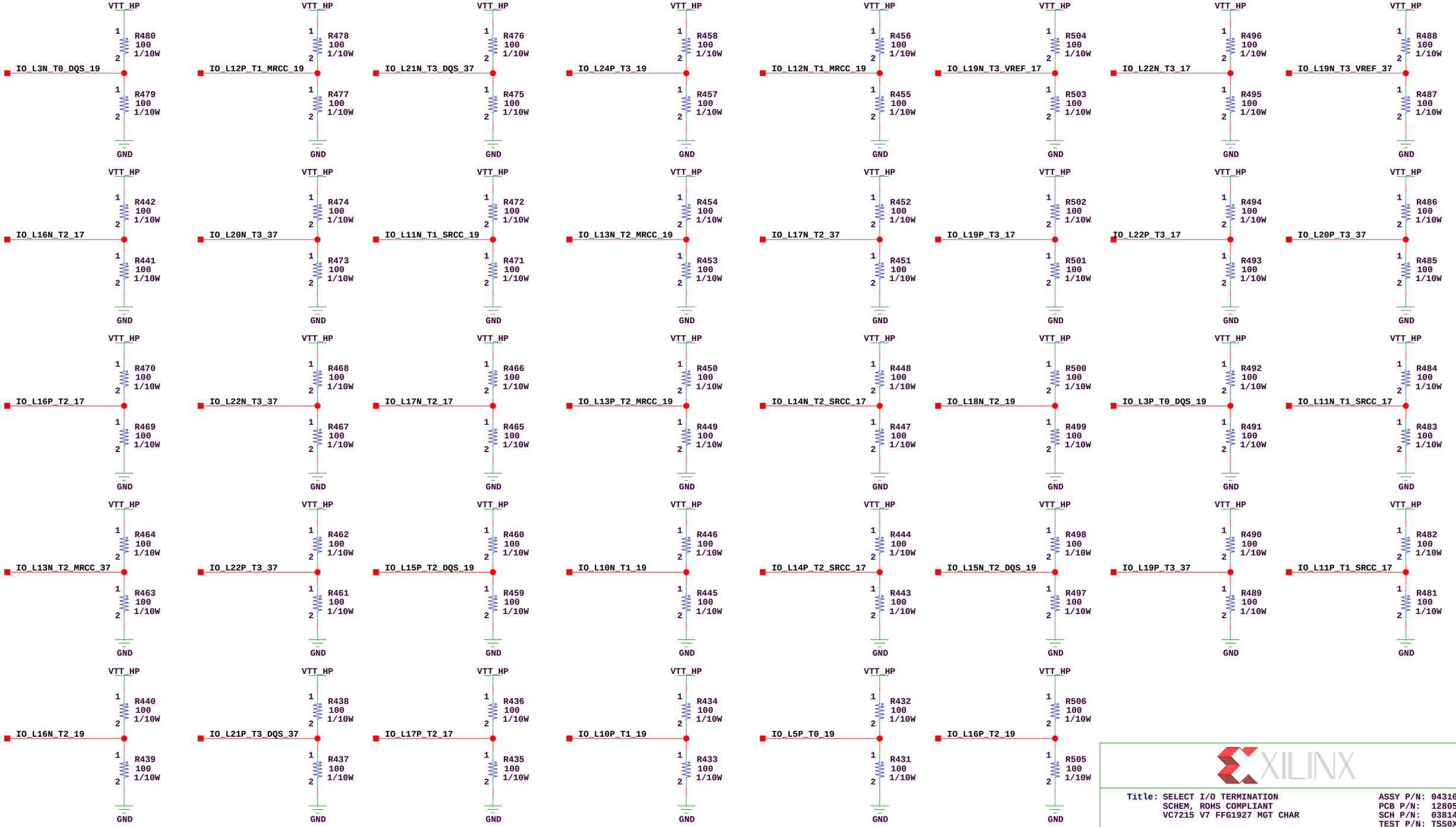
SELECT I/O TERMINATION



XILINX

Title: SELECT I/O TERMINATION SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40	Ver: 1.0
Sheet Size: B	Rev: 01
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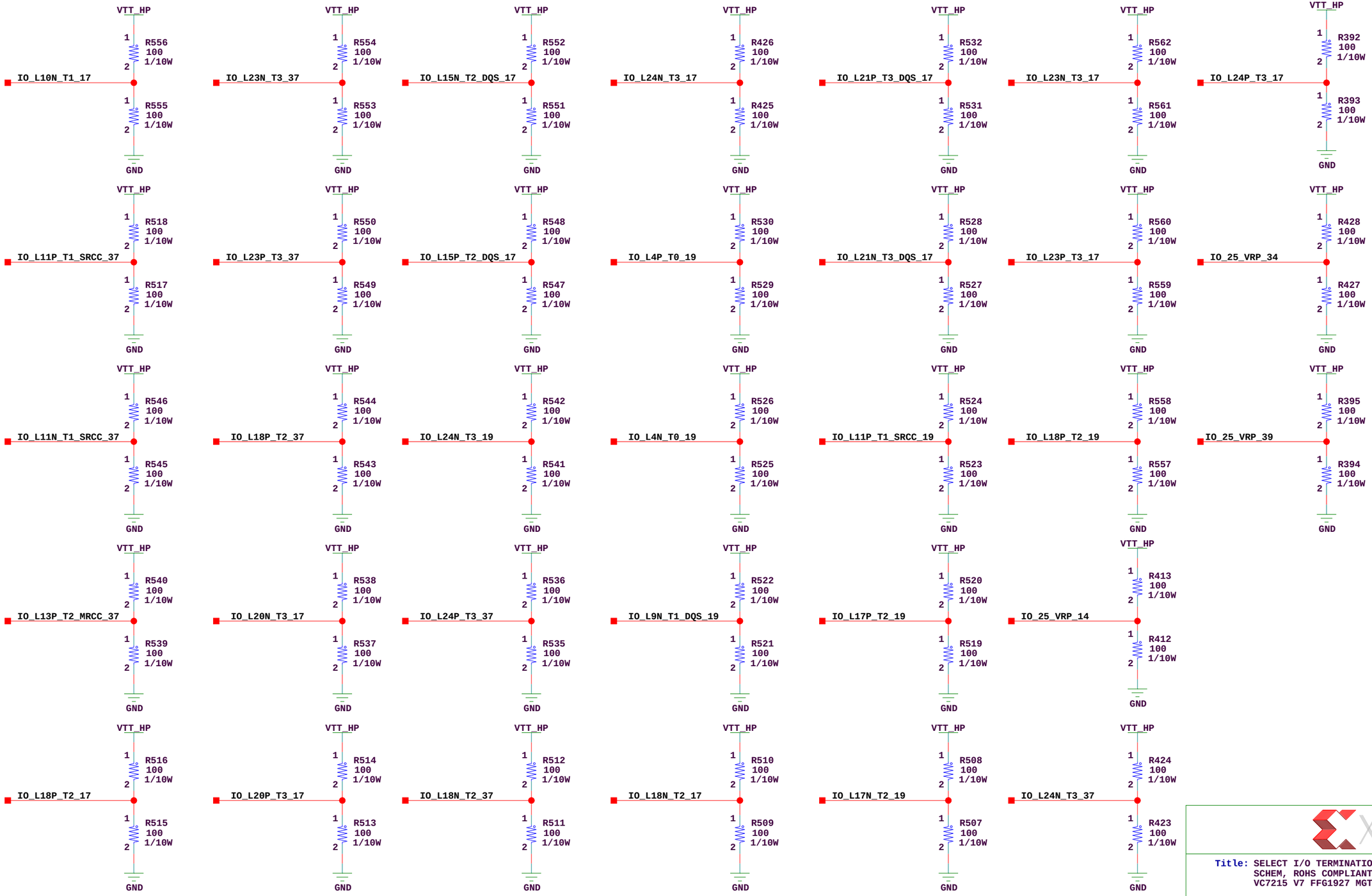
SELECT I/O TERMINATION



XILINX

Title: SELECT I/O TERMINATION SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_15:40		Ver: 1.0
Sheet Size: B		Rev: 01
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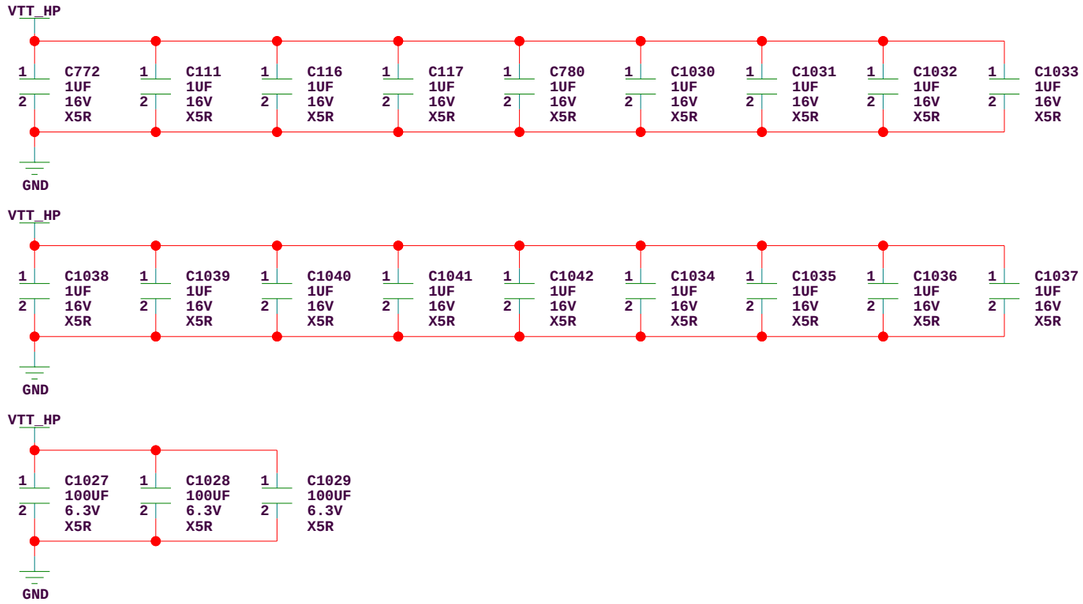
SELECT I/O TERMINATION - DECOUPLING



1 PLACE ONE 1UF CAP FOR EVERY 4 TERMINATED I/O SIGNALS.
PLACE ONE 100UF CAP FOR EVERY 25 TERMINATED I/O SIGNALS.
DISTRIBUTE THE CAPS EVENLY WITH RESPECT TO THE TERMINATION RESISTORS.

XILINX

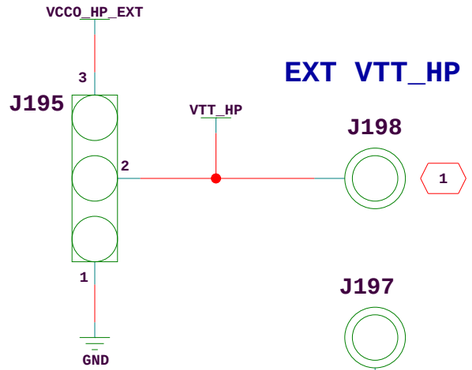
Title: SELECT I/O TERMINATION
SCHEM, ROHS COMPLIANT
VC7215 V7 FFG1927 MGT CHAR

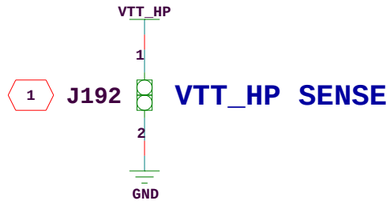
ASSY P/N: 0431676
PCB P/N: 1280597
SCH P/N: 0381429
TEST P/N: TSS0XXX

Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 88 of 90	Drawn By RN

EXT VTT JACKS / MOUNTING HOLES / FIDUCIALS / GND TURRETS

VTT_HP SOURCE, PROBE POINTS

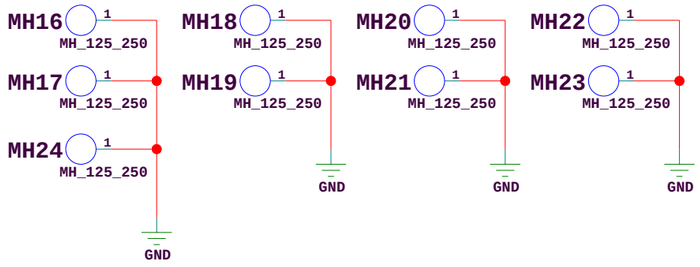




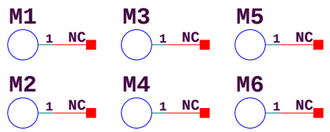
MOUNTING HOLES

SUPERCLOCK-2

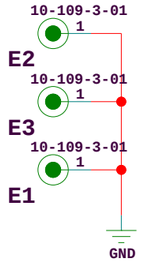
BOARD STANDOFFS



FIDUCIAL HOLES



GROUND TURRETS



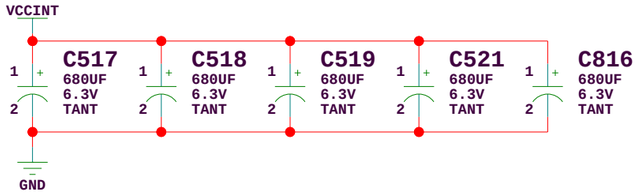
1 PLACE EXT VTT JACK AND VTT SENSE HEADER AT THE OPPOSITE ENDS OF VTT PLANE.

XILINX

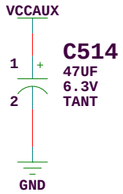
Title: EXT VTT JACK, BOARD MECHANICALS SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR	ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX
Date: 4-11-2013_18:23	Ver: 1.0
Sheet Size: B	Rev: 01
Sheet 89 of 90	Drawn By RN

FPGA DECOUPLING 1

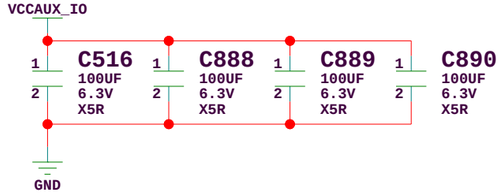
VCCINT



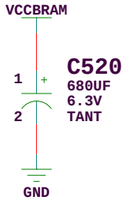
VCCAUX

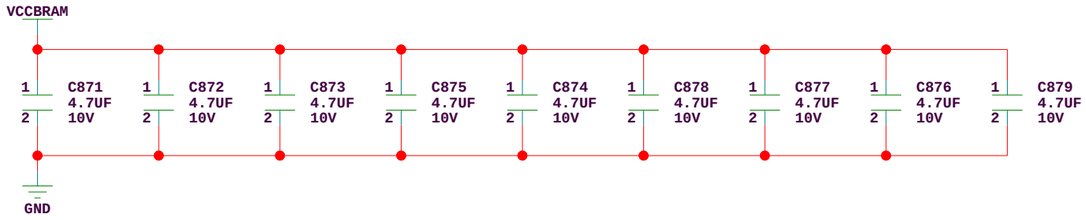


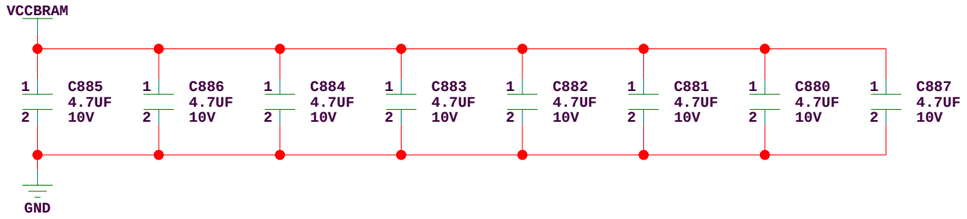
VCCAUX_IO



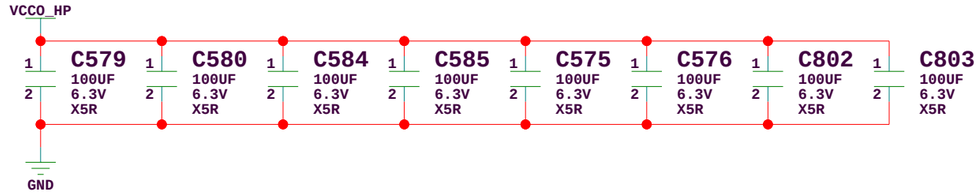
VCCBRAM

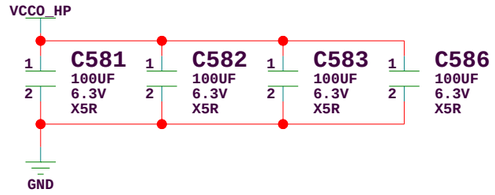






VCCO (12 HP BANKS)





VCCO_0 (BANK 0)

1 MARCH 19, 2012: RECOMMENDED FPGA DECOUPLING NETWORK FOR 7VX690T-FFG1927

XILINX

Title: FPGA DECOUPLING SCHEM, ROHS COMPLIANT VC7215 V7 FFG1927 MGT CHAR		ASSY P/N: 0431676 PCB P/N: 1280597 SCH P/N: 0381429 TEST P/N: TSS0XXX	
Date: 4-11-2013_15:40		Ver: 1.0	
Sheet Size: B		Rev: 01	
Sheet 90	of 90	Drawn By RN	