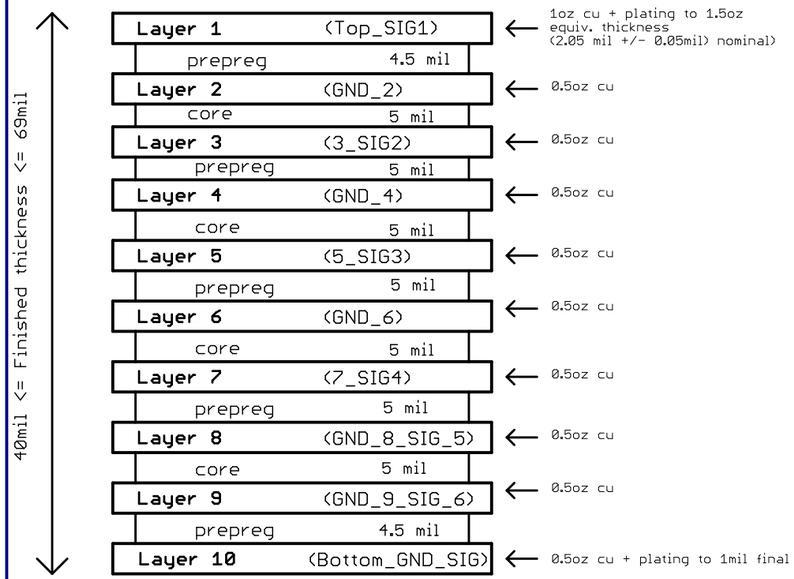
Stack-up, line widths, via specifications and drills

Note: The bottom layer is referred to as "L10" on this sheet. In Eagle, the bottom layer is always Layer 16; please keep this in mind if viewing the board in Eagle.

STACK-UP SPECIFICATIONS FOR REFERENCE



Note 1: All signal layers controlled impedance. Design assumes effective Er. = 3.8, layer thicknesses above, and width and spacing below.

Note 2: Prepreg and core thicknesses are nominal and used for pre-fabrication calculations of impedance specifications. Manufacturer may adjust as needed to meet impedance specifications.

Line width impedance chart for reference

Layer	Single-ended Line width	Differential Line Width	Differential Line Space	Single-ended Impedance	Differential Impedance
L1	5 mil	5mil	7mil	50 Ohms	100 Ohms +5/-10
L3, L5, L7, L8	4 mil	4 mil	8 mil	50 Ohms	100 Ohms +5/-10
L10	5mil	5 mil	7 mil	50 Ohms	100 Ohms +5/-10

DRILL LEGEND

Sym	N°	Mils	MM	Qty	Plated	Tol.
+	1	8.00	0.20	445	YES	+0/-8mil
×	2	10.00	0.25	1338	YES	+0/-10mil
◫	3	11.81	0.30	25	YES	+0/-10mil
◇	4	23.62	0.60	4	YES	+2/-2 mil
⧖	5	25.00	0.64	65	YES	+2/-2 mil
⌖	7	36.00	0.91	3	YES	+2/-2 mil
ϟ	8	47.00	1.19	2	YES	+2/-2 mil
▽	11	125.98	3.20	4	YES	+5/-2 mil
⋈	6	31.50	0.80	4	NOT	+3/-3 mil
⋇	9	50.00	1.27	2	NOT	+3/-3 mil
⋇	10	55.12	1.40	1	NOT	+3/-3 mil

Further fabrication instructions.

1. Substrate nominal dielectric (Er) of ~3.8 (or as needed to meet impedance specifications). E.g.: FR-408, Getek ML200M, Getek ML200C, Getek ML200D N4000-13, N4000-13 EP.
2. Impedance (all signals)
   Differential: 100 Ohms up to 1GHz min.
   Differential nets with names DP*, DP0_*, AUX_SRC_C_*, AUX_RX_AC_CONV_*:
   100 Ohms up to 6GHz min.
   Single-ended: 50 Ohms
   *SEE LINE WIDTH AND IMPEDANCE CHART for detailed normative specifications.
3. Copper: 1 oz cu Lay 1 (top), Lay 10 (bottom)
   1/2 (0.5) oz cu Lay 2-9
   Top and bottom plated to 1.5mil final
   SEE STACK-UP SPECIFICATIONS FOR REFERENCE for normative specifications.
4. Apply solder mask over bare copper (SMBOC) IAW IPC-SM-840 both sides, IPC color green
5. Finish: Gold Immersion (DIG or EING)
6. Silkscreen on both sides with non-conductive epoxy-based ink. Color shall be white/a contrasting color with respect to solder mask color. Distortion of silkscreen is acceptable over traces. Epoxy ink on plated lands is NOT acceptable.
7. Vendor logo/text/date code to be marked on TOP side (L1) near lower-right corner. Total height not to exceed 120mil
8. 100% Electrical test is required for continuity.
9. 100% of signal lines to be tested for specified impedances.
10. Remove all unused pads from internal layers.
11. Soldermask registration within diametrical true position of +/- 2mil (0.002 inches) with applicable hole/pad
12. Vias under JA1 (SEAF) and U202 (SN75DP130SS) to be treated appropriately to assure optimal electrical coupling during assembly. Tenting, plugging, or encroachment may be used depending on the fabricator's established best practices.
13. Vias to be plated to at least 1 (0.5) oz cu.
14. Final PCB thickness to be between 0.048-0.069 inches (48-69 mil);
15. At manufacturer's discretion, sparse (unpopulated) areas in signal layers (3, 5, 7) may be filled with a cross-hatch or other appropriate pattern to assist in inter-layer adhesion, overall flattness, etc. Such fill shall not be connected to any nets and shall maintain no less than 100mil clearance from signals and no less than 25mil clearance from vias connected to net GND.
16. Soldermask under U202 may be altered according to manufacturer's established best practices for QSON-style packages.
17. Fidutials (FID*) are provided to assist in part placement. Layer "Measures" contains measurements for the relative and absolute positions of fidutials and other critical landmarks.
18. This device is not required to meet ROHS requirements and the use of lead-bearing solder is permitted (and desirable).

Further Assembly Instructions

1. Connectors EXT1/EXT2 (QSE-060 connectors) are the only components on on the top side. Suggest gluing and reflowing these first.
Critical part placement and density is on the bottom.
2. Traces DP0_*LANE* will carry signals up to 6GHz and all due care must be taken to ensure impedance matching end-to-end.
3. Post-assembly continuity testing between corresponding pins on EXT1/EXT2 and FMC1 (JA1) is requested.
4. Post-assembly inspection (Xray or otherwise) is requested for all leadless/BGA devices.

Fabrication and Assembly Instructions	
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