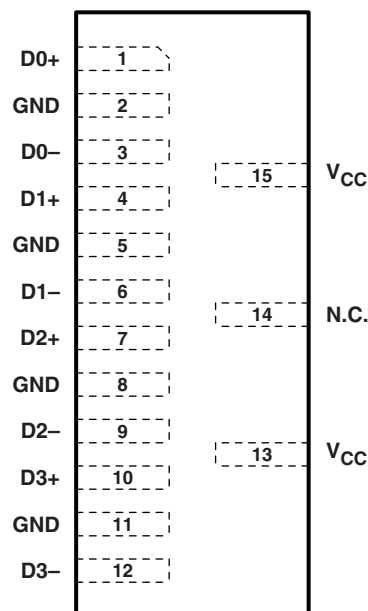


8-CHANNEL DISPLAY/HDMI PORT ESD PROTECTION

FEATURES

- Supports High-Definition Multimedia Interface (HDMI) 1.3 or Display Port Data Rate
- Low 0.8-pF Line Capacitance for Each Data Line
- 0.05-pF Matching Capacitance Between Differential Signal Pair
- Four-Pair Differential Lines to Protect Differential Data and Clock Lines of HDMI and Display Port Interface
- Match With 0.5-mm Pitch Display Port Connector for Seamless Routing and Minimal Line Glitch Due to ESD Clamps
- Flow-Through Single-in-Line Pin Mapping for High-Speed Lines Ensures No Additional Board Layout Burden While Placing ESD Protection Chip Near DP/HDMI Connector
- Supports Data Rates in Excess of 2.7 Gbps
- IEC 61000-4-2 (Level 4) System Level ESD Compliance
- I_{off} Feature
- Commercial Temperature Range: -40°C to 85°C
- 15-Pin 0.5-mm Pitch DSM Package: Length = 6.5 mm, Width = 2.5 mm, and Height = 0.8 mm

DSM PACKAGE
(TOP VIEW)



N.C. – Not internally connected

DESCRIPTION/ORDERING INFORMATION

The TPD8S009 provides an electrostatic discharge (ESD) solution for the display port and high-definition multimedia interface (HDMI) high-speed lines. This device offers eight ESD clamp circuits with flow-through pin mapping that matches the display port or HDMI port connector pin assignments. This device supports HDMI 1.3 or display port data rate (in excess of 3 Gbps).

The Dx+/Dx– ports add only 0.8-pF capacitance to the high-speed differential lines. In addition, the monolithic integrated circuit technology ensures that there is excellent matching between the two signal pairs of the differential line. This is a direct advantage over discrete ESD clamp solutions, where variations between two different ESD clamps may significantly degrade the differential signal quality.

The TPD8S009 complies with IEC61000-4-2 (Level 4) ESD protection. This device is offered in a space-saving SON package with 0.5-mm pitch matching the display port or HDMI connector pitch. The unique pin mapping allows the system designer to select the ESD solution at the last phase of the design without any changes in the board layout or degradation of signal-integrity performance.

The TPD8S009 is characterized for operation over the ambient air temperature range of -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

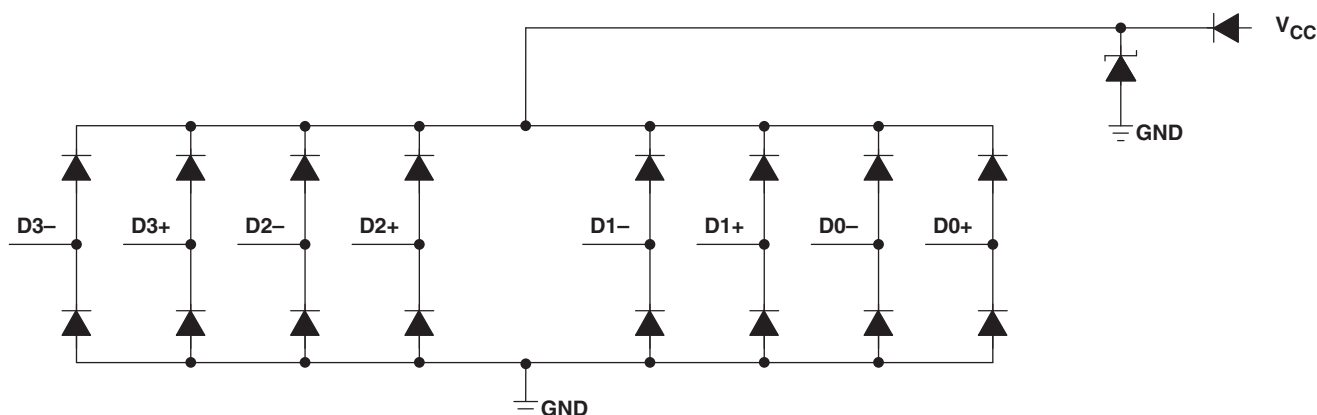
ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SON – DSM	Tape and reel	TPD8S009DSMR	PK009

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
D0+, D0–, D1+, D1–, D2+, D2–, D3+, D3–	1, 3, 4, 6, 7, 9, 10, 12	ESD port	High-speed ESD clamp provides ESD protection to the high-speed display port/HDMI differential data lines.
GND	2, 5, 8, 11	GND	Ground
N.C.	14	No connect	No internal signal connection
V _{CC}	13, 15	Supply	I/O supply

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.3	6	V
V_{IO}	IO signal voltage range	0	V_{CC}	V
T_{stg}	Storage temperature range	–65	125	°C
T_A	Characterized free-air operating temperature range	–40	85	°C
	Lead temperature, 1.6 mm (1/16 in) from case for 10 s		260	°C
	IEC 61000-4-2 Contact Discharge		±8	kV
	IEC 61000-4-2 Air-Gap Discharge		±9	kV
	Peak pulse power ($t_p = 8/20 \mu s$)		25	W
	Peak pulse current ($t_p = 8/20 \mu s$)		2.5	A

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse standoff voltage	Any IO pin to ground			5.5	V
V_{BR}	Breakdown voltage	$I_{IO} = 1 \text{ mA}$ Any IO pin to ground	9			V
I_{IO}	IO port current	$V_{IO} = 3.3 \text{ V}$, $V_{CC} = 5 \text{ V}$ Any IO pin		0.01	0.1	μA
I_{off}	Current from IO port to supply pins	$V_{IO} = 3.3 \text{ V}$, $V_{CC} = 5 \text{ V}$ Any IO pin		0.01	0.1	μA
V_D	Diode forward voltage	$I_{IO} = 8 \text{ mA}$ Lower clamp diode	0.6	0.8	0.95	V
R_{DYN}	Dynamic resistance	$I = 1 \text{ A}$ Any IO pin		1.1		Ω
C_{IO}	IO capacitance	$V_{CC} = 5 \text{ V}$, $V_{IO} = 2.5 \text{ V}$ Any IO pin		0.8		pF
I_{CC}	Operating supply current	$V_{IO} = \text{Open}$, $V_{CC} = 5 \text{ V}$ V_{CC} pin		0.1	1	μA

TYPICAL CHARACTERISTICS

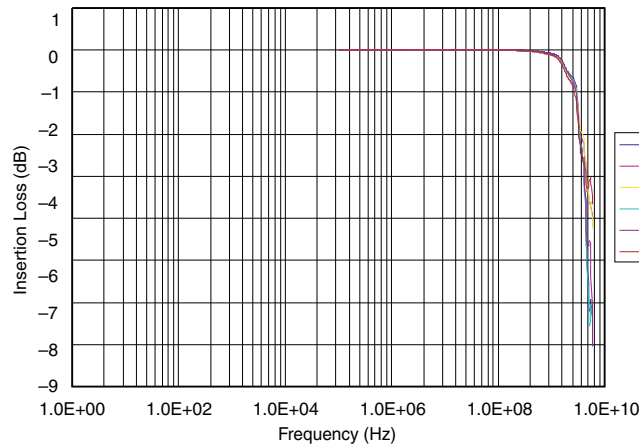


Figure 1. Insertion Loss vs Frequency

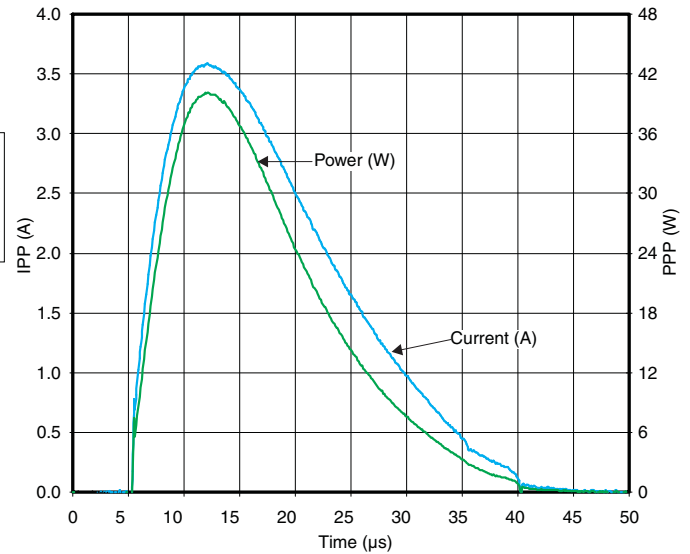


Figure 2. Peak Pulse Waveforms

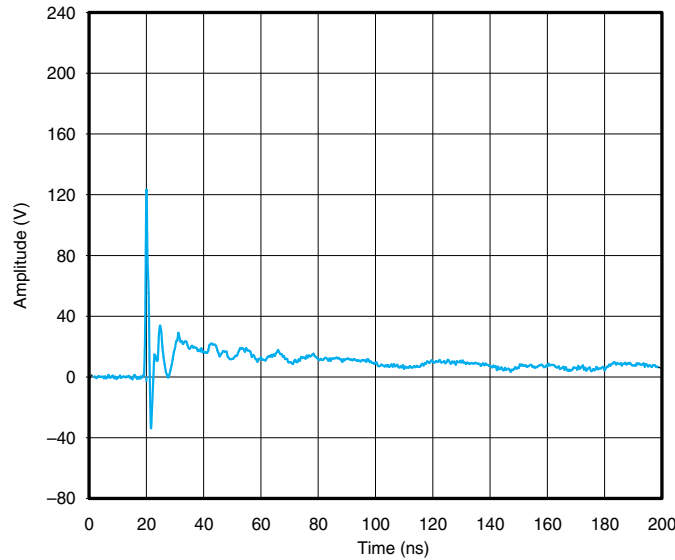


Figure 3. IEC Clamping Waveforms
(8-kV Contact, 20 ns/div)

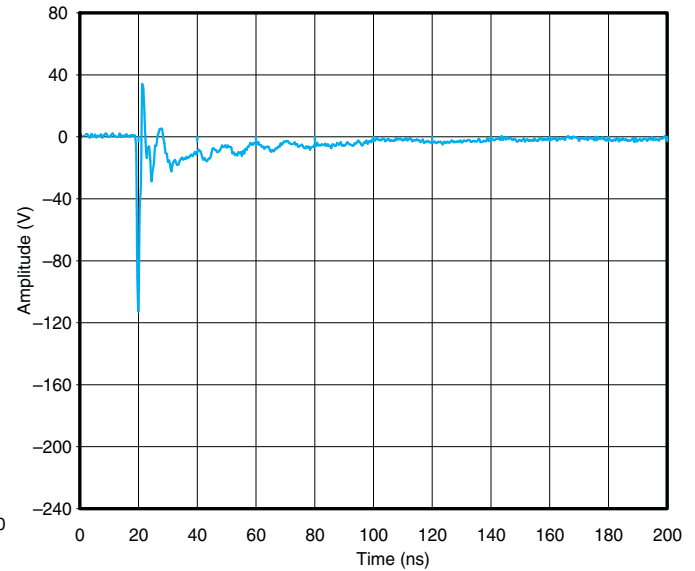


Figure 4. Figure 3. IEC Clamping Waveforms
(-8-kV Contact, 20 ns/div)

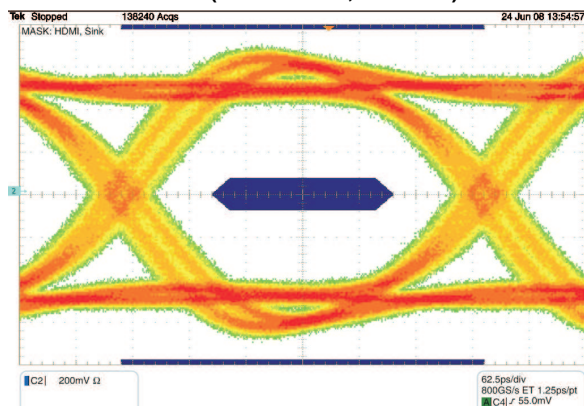


Figure 5. Eye Diagram Without TPD8S009
(2.5 Gbps Data Rate)

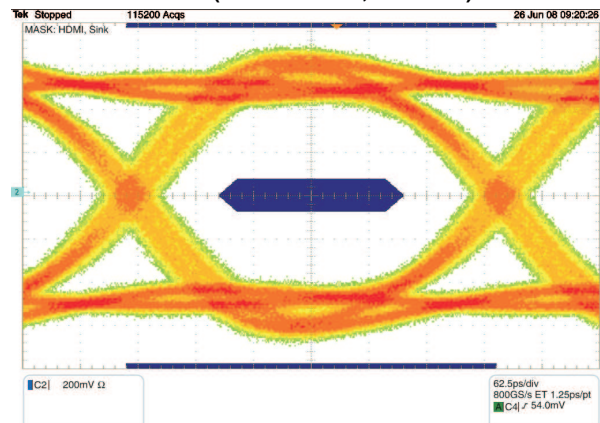


Figure 6. Eye Diagram With TPD8S009
(2.5 Gbps Data Rate)

APPLICATION INFORMATION

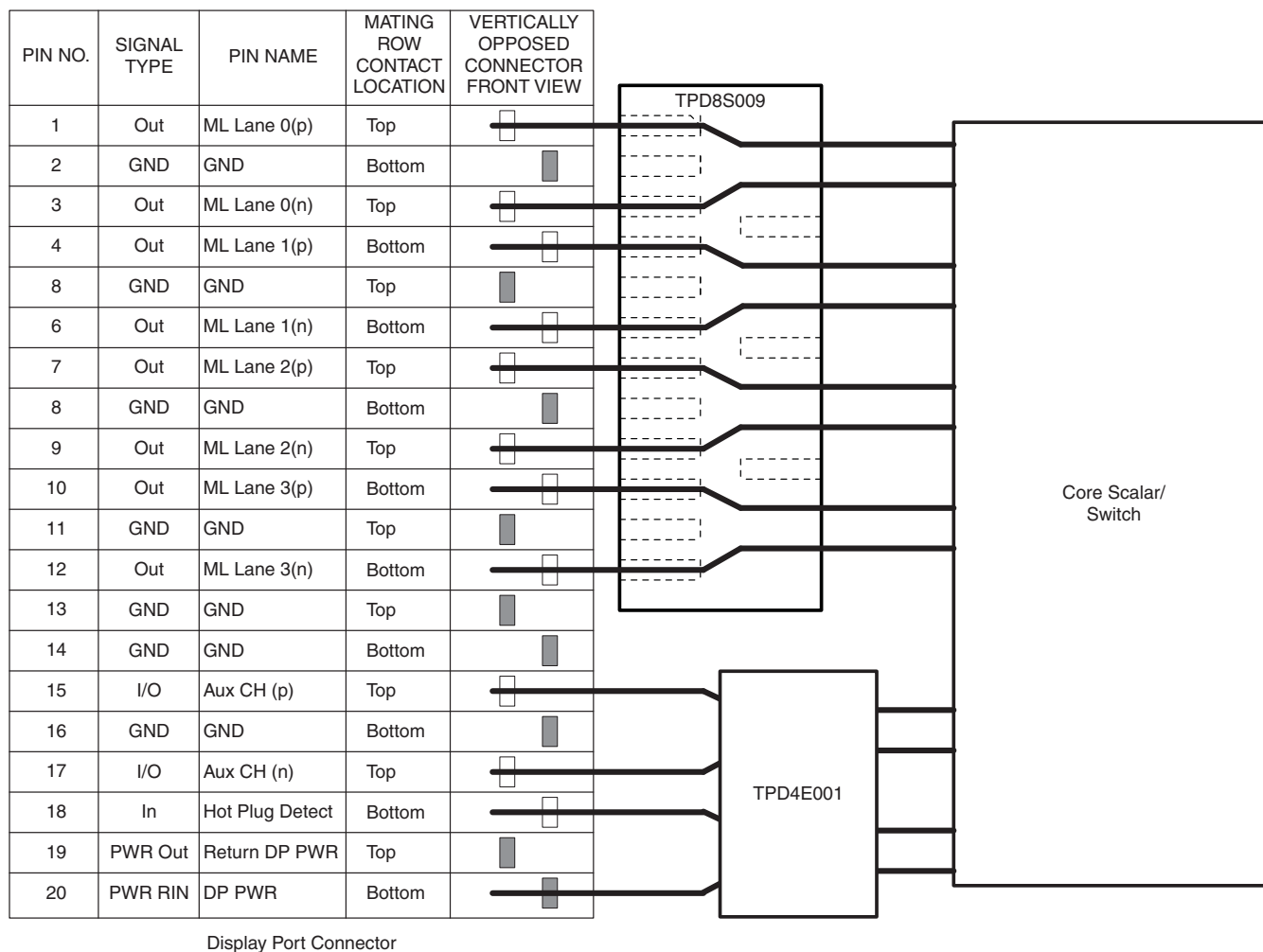


Figure 7. Typical Application

The TPD8S009 can provide system-level ESD protection to the high-speed differential lines of the HDMI or display ports. The flow-through package offers flexibility for board routing with traces up to 15-mm wide. [Figure 7](#) shows the board-layout scheme for the four differential pair lines. The special pin configuration of the TPD8S009 matches the HDMI or display port pin assignments. It allows the differential signal pairs to couple together after they touch the ESD ports (pins 1–3, 4–6, 7–9, and 10–12) of the TPD8S009.

TPD4E001 is recommended for ESD protection of slow-speed control lines.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD8S009DSMR	ACTIVE	SON	DSM	15	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PK009	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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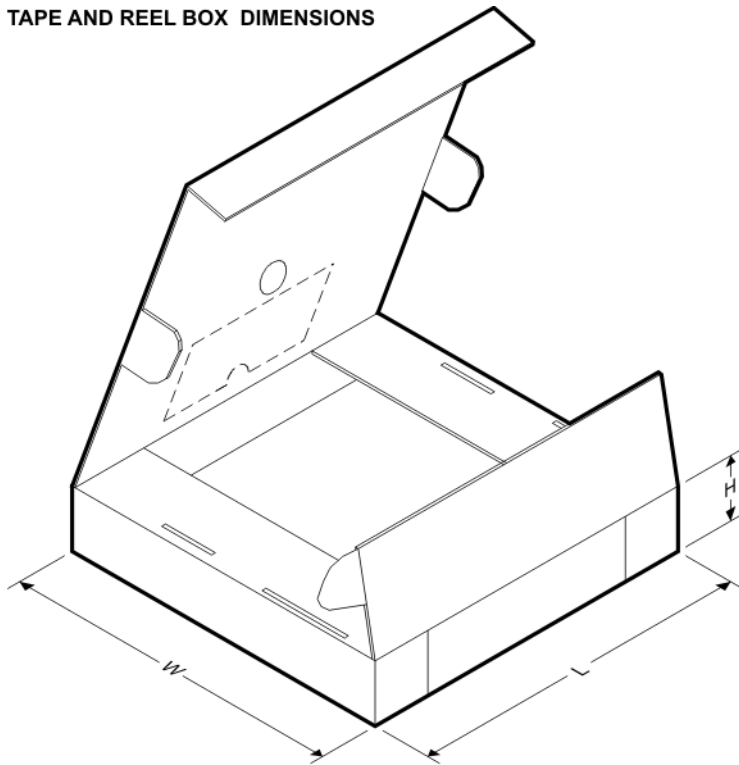
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD8S009DSMR	SON	DSM	15	3000	180.0	12.4	2.75	6.75	0.95	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

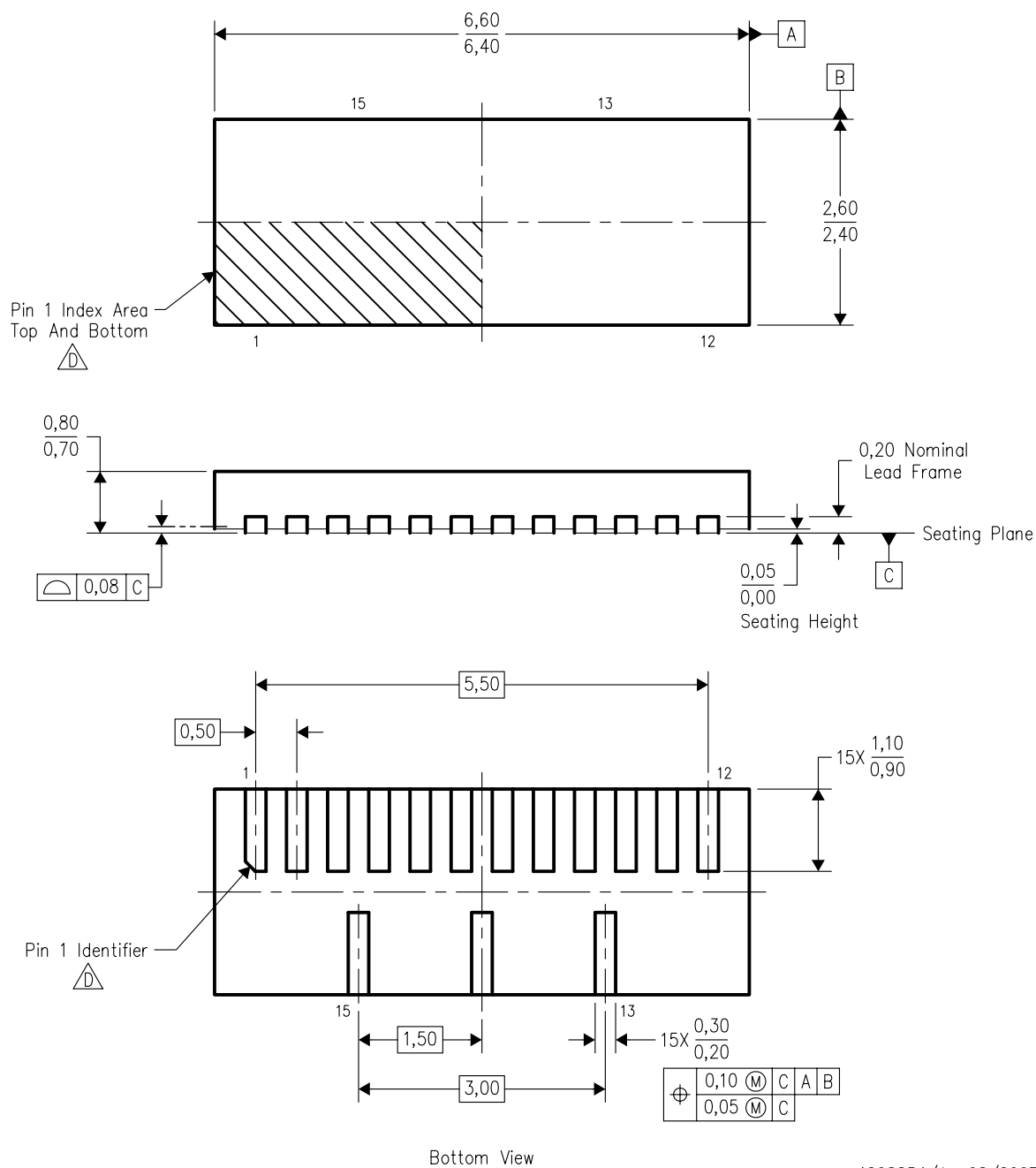


*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD8S009DSMR	SON	DSM	15	3000	203.0	203.0	35.0

DSM (R-PDS0-N15)

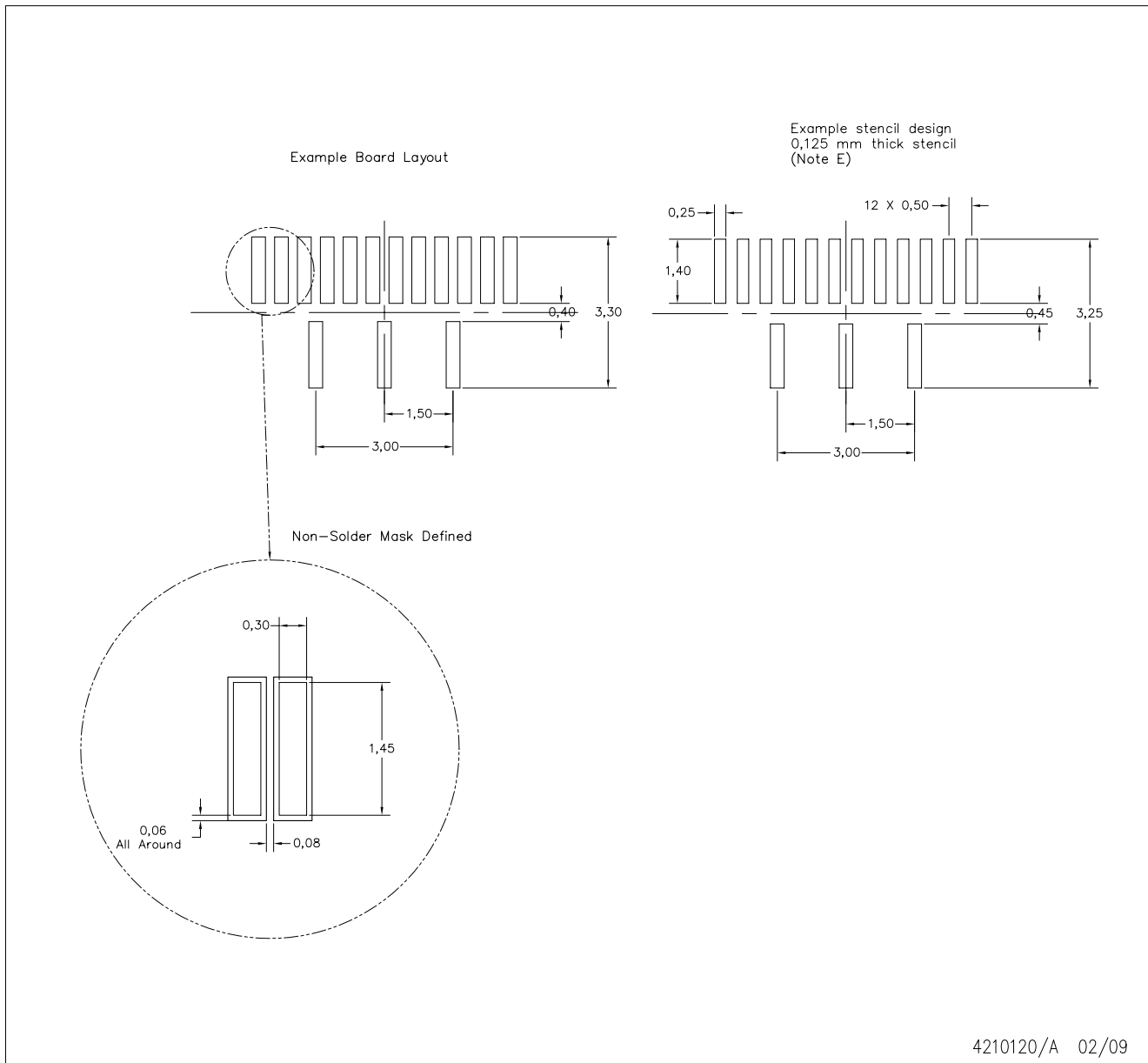
PLASTIC SMALL OUTLINE



4208854/A 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 -  D. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

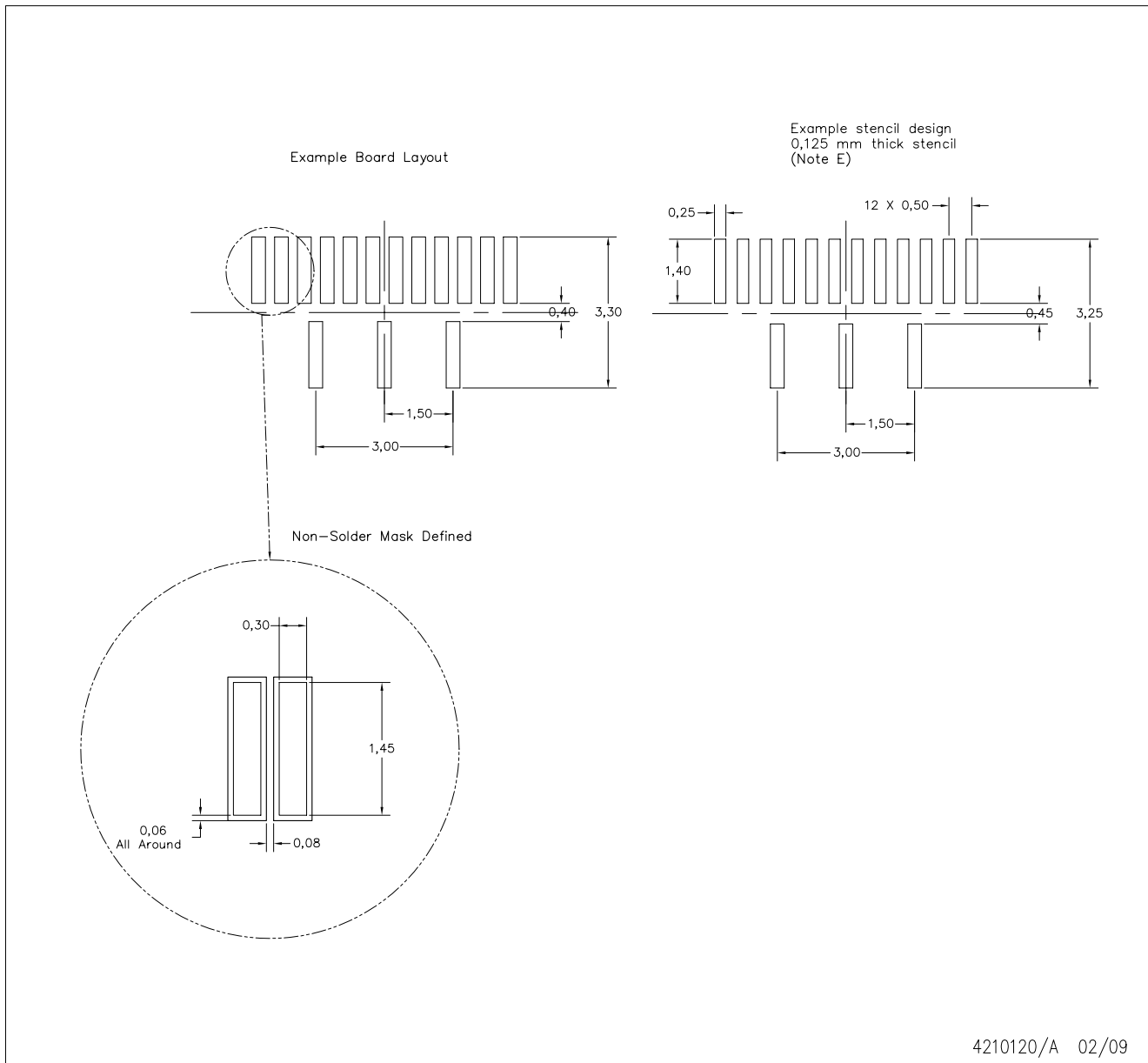
DSM (R-PDSO-N15)



4210120/A 02/09

- NOTES:
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 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DSM (R-PDSO-N15)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
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 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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