August 2009

DLP® Discovery 4100 Debugging Guidelines

IMPORTANT NOTICE

BEFORE USING TECHNICAL INFORMATION, THE USER SHOULD CAREFULLY READ THE FOLLOWING TERMS.

The term "Technical Information" includes reference designs, drawings, specifications, and other information relating to TI DLP® products or applications, contained herein or provided separately in any format or via any medium.

TI is providing Technical Information for the convenience of purchasers of DLP® products ("Users"), and will not accept any responsibility or liability arising from providing the Technical Information or its use. Any use or reliance on Technical Information is strictly the responsibility of the User.

1. **No Warranty.** ***THE TECHNICAL INFORMATION IS PROVIDED "AS IS".*** TI MAKES NO WARRANTIES OR REPRESENTATIONS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING LACK OF VIRUSES, ACCURACY, OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO THE TECHNICAL INFORMATION OR THE USE OF THOSE MATERIALS.

2. **Warranty for Products Not Affected.** The foregoing exclusion and disclaimer of warranty does not affect or diminish any warranty rights with regard to DLP® products. Such rights are governed exclusively by the terms of a written and signed purchase agreement with TI.

3. **Limitations and Exclusion of Damages.** IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF THE TECHNICAL INFORMATION OR THE USE OF THE TECHNICAL INFORMATION.

4. **No Engineering Services.** User is fully responsible for all design decisions and engineering with regard to its products, including decisions relating to application of DLP® products. By providing Technical Information TI does not intend to offer or provide engineering services or advice concerning User's design. If User desires engineering services, then User should rely on its retained employees and consultants and/or procure engineering services from a licensed professional engineer ("LPE").

5. **Compliance with Export Control Laws.** Unless prior authorization is obtained from the U.S. Department of Commerce, User may not export, re-export, or release, directly or indirectly, any Technical Information, or export, directly or indirectly, any direct product of such Technical Information to any destination or country to which the export, re-export or release of the Technical Information or direct product is prohibited by the Export Administration Regulations of the U.S. Department of Commerce ("EAR").

TABLE OF CONTENTS

1. SCOPE OF THIS DOCUMENT 5

2. DEBUGGING GUIDELINES 5

3. TEST POINTS 10

Table of Figures

Figure 1 Data and Command Input to DDC 8
Figure 2 Phased Reset Timing 9

Table of Tables

Table 1 DAD1 Initialization Status 5
Table 2 DAD Output Voltages 6
Table 3 DMD Initialization Status 6
Table 4 DMD Type 6
Table 5 Device Ok 7
Table 6 DAD2 Initialization Status 7
Table 7 DDC Initialization Status 7
Table 8 DDC4100 Test Points 10

1. Scope of this document

This document provides the basic guidelines to debug the DMD Discovery™ 4100 Digital Controller (DDC4100) based systems. It is not a comprehensive list, but is meant to provide a starting point in the debugging process.

2. Debugging Guidelines

Prior to checking the DDC signals, make sure the reference clock to the DDC is running at 50MHz. Check that the *config_done* signal for the FPGA is asserted indicating the FPGA is programmed correctly.

2.1. Initialization

Initialization will automatically start after reset is de-asserted. The initialization process includes the following components in the order presented here:

- Calibration
- DAD1 Initialization
- DMD Initialization
- DAD2 Initialization (if needed)
- Command sequence

2.1.1. Calibration

Calibration is done on each of the data and *dvalid* signals. When calibration is successful, the following signals will go high:

- *cal_a_done_rdq (XGA and 1080p)*
- *cal_b_done_rdq (XGA and 1080p)*
- *cal_c_done_rdq (1080p only)*
- *cal_d_done_rdq (1080p only)*

The training pattern going into the SERDES on the transmit side is different than the pattern on the receive SERDES. On the receive side the value should be “0100”. However, this could translate to “0010” on the transmit side. Please see the Xilinx datasheet for more information. An improper training pattern could cause the part to not perform the commands correctly.

2.1.2. DAD1 Initialization

DAD 1 is initialized for both XGA and 1080p DMDs. The DDC output *DAD_SCP_EN* signal should be asserted indicating that the DDC is ready to communicate to the DAD. One should see toggling on the scp_clk, scp_do (output from DDC) and scpdi (input to DDC) lines. Be sure that the direction of the scp input and output signals are connected correctly.

ECP2_M_TP27	Note
1	DAD 1 initialization in progress
0	DAD 1 initialization complete

Table 1 DAD1 Initialization Status

Check the DAD output voltages listed below to make sure the DAD is set up correctly.

Parameter	Description		Units	DAD Output
VRST_RAIL	Reset Voltage	Min	V	-26.5
		Nom	V	-26
		Max	V	-25.5
VBIAS_RAIL	Bias Voltage	Min	V	22.5
		Max	V	26.5
VOFF_RAIL	Offset Voltage	Min	V	8.25
		Nom	V	8.5
		Max	V	8.75

Table 2 DAD Output Voltages

2.1.3. DMD

The DDC output *DMD_SCP_EN* signal should be asserted indicating that the DDC is ready to communicate to the DMD. One should see toggling on the scp_clk, scp_do (output from DDC) and scpdi (input to DDC) lines. Be sure that the direction of the scp input and output signals are connected correctly.

ECP2_M_TP26	Note
1	DMD initialization in progress
0	DMD initialization complete

Table 3 DMD Initialization Status

Device ID check

The DDC will output a 4-bit bus called *DMD_TYPE(3:0)* which will list the type of DMD attached. Table below shows the possible *DMD_TYPE* output.

DMD_TYPE	DMD
0000	0.95” 1080p Type A
0001	0.7” XGA Type A
0011	0.55” XGA TypeX
1111	DMD not recognized

Table 4 DMD Type

Device_ok check

Only DMDs sold with the Discovery chipset are supported by the DDC4100. The signals *dmd_device_ok_ab* and *dmd_device_ok_cd* will indicate the status of the DMD. These signals may be found on DDC test points ECP2_M_TP11 and ECP2_M_TP12, respectively.

dmd_device_ok_ab	dmd_device_ok_cd	Note
0	0	DMD not initialized or DMD not supported
1	0	Only the a/b side is attached and initialized (could suggest a XGA device)
0	1	Not a valid output
1	1	a/b/c/d are all attached and initialized (1080p device)

Table 5 Device Ok

2.1.4. DAD2 Initialization

The second DAD is only initialized when a 1080p DMD is connected. Follow the same steps in the DAD1 initialization to check the DAD2 initialization.

ECP2_M_TP28	Note
1	DAD 2 initialization in progress
0	DAD 2 initialization complete

Table 6 DAD2 Initialization Status

2.1.5. Command Sequence

The last portion of the initialization process involves a series of commands sent from the DDC to the DMD. This will complete the initialization process.

During this step, check the output of the DAD(s). One should expect to see several reset waveforms indicating the DAD is initialized correctly.

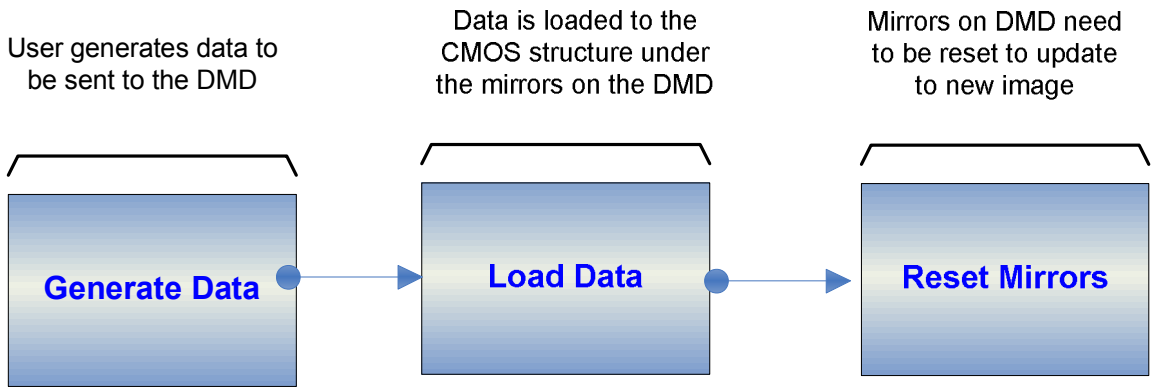
At the end of the initialization sequence, if the initialization is successful, the *comb_init_active* (ECP2_M_TP20) will de-assert (go low) indicating that the initialization process is complete.

ECP2_M_TP20	Note
1	DDC initialization in progress
0	DDC initialization complete

Table 7 DDC Initialization Status

2.2. Image Display

There are 3 steps to displaying an image on the DMD: generate data; load data; and reset mirrors. Each of these steps can cause the image to not display correctly or in some cases not at all. Some checks can be made to debug the image issue.



2.2.1. Generate Data

If there is a problem with the image displayed, one of the first places to check is the data generation. This portion is done outside of the DDC. Please refer to the data sheet (TI DN2510443) for detailed information on how to send the data. Here is a simple diagram of how the data should be sent relative to the clock and command.

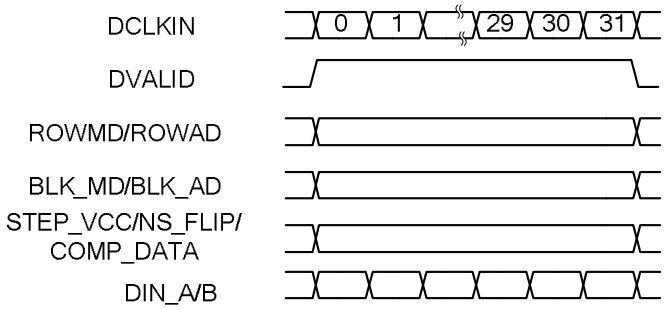


Figure 1 Data and Command Input to DDC

2.2.2. Load Data

After the data and commands are sent to the DDC, the DDC processes the information and passes the processed information to the DMD. If there is no image displayed, first check the output of the DDC and see if there is data coming out. There are 2 signals that will block the data from coming out of the DDC: *device_ok* and *pwr_float*. Check to be sure that

device_ok = '1'
pwr_float = '0'

There is also a float command that can be given that would block the data from coming out of the DDC. Check to see that this command is not inadvertently sent.

The command is set up as follows:

RST2BLKZ	BLK_MD 1	BLK_MD 0	BLK_AD 3	BLK_AD2	BLK_AD1	BLK_AD0	Operation
X	1	1	1	1	X	X	Float blocks 00-15

2.2.3. Reset Data

Reset commands are sent to tell the DMD to load the data to the mirrors. Certain timing requirements need to be met for proper switching of the mirrors. The figure below shows the timing requirements of the global reset. It is required that commands be sent during *RST_ACTIVE* high. If data commands are not being sent then NOP commands should be sent continuously while *RST_ACTIVE* is high to ensure proper resetting of the mirrors.

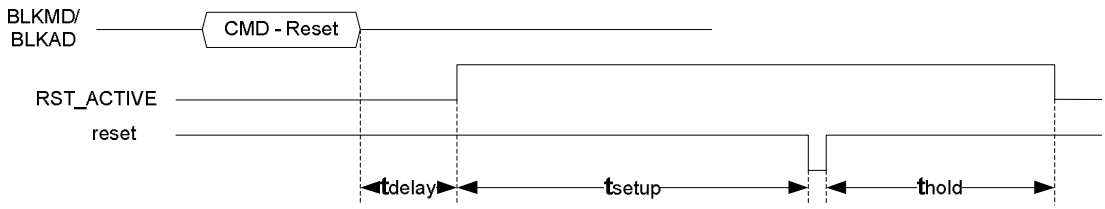


Figure 2 Phased Reset Timing

After the reset command is sent, there is a delay of 12 clocks (t_{delay}) before the *RST_ACTIVE* is asserted. While the *RST_ACTIVE* signal is asserted, new reset commands will be ignored. After the data is loaded to the mirrors, it takes approximately 8us for the mirrors to settle. During this time, the mirrors may not be stable. No commands should be given during this time. This time is included in the *RST_ACTIVE* timing. The t_{setup} and t_{hold} timing parameters are not adjustable. They are automatically insured by the hardware based on the DMD attached.

3. Test Points

The following table shows the current available test points. When designing custom board using the Discovery 4100 chipset, special considerations are needed to gain access to these test points.

Test Point	Signal	Description
3	DCLK_BUF	Buffered data clock
4	CLK_S	System clock
5	DVALID_A(0)	Dvalid A
6	DVALID_B(0)	Dvalid B
7	DVALID_C(0)	Dvalid C
8	DVALID_D(0)	Dvalid D
10	ARSTZ	System reset
11	DMD_DEVICE_OK_AB_SQ	DMD device ok for AB side of DMD
12	DMD_DEVICE_OK_CD_SQ	DMD device ok for CD side of DMD for 1080p
13	CLK_SYSTEM_PLL_LOCKED	System PLL lock signal
14	CLK_REF_PLL_LOCKED	Reference PLL lock signal
15	CLK_SYSTEM_CLOCK	System clock
16	CLK_RELEASE_RESET	Clock reset
17	CLK_SYSPLL_RESET	System PLL reset
18	CLK_REFPLL_RESET	Reference PLL reset
20	INIT_ACTIVE	Indicates when system initialization is in progress
21	CAL_A_DONE	Calibration done for data bus A
22	CAL_B_DONE	Calibration done for data bus B
23	CAL_C_DONE	Calibration done for data bus C
24	CAL_D_DONE	Calibration done for data bus D
26	DMD_INIT_ACTIVE	Indicates when DMD is initializing
27	DAD_INIT_ACTIVE1	Indicates when DAD1 is initializing
28	DAD_INIT_ACTIVE2	Indicates when DAD2 is initializing
29	CALIBRATION_ACTIVE	Indicates when system is in calibration

Table 8 DDC4100 Test Points