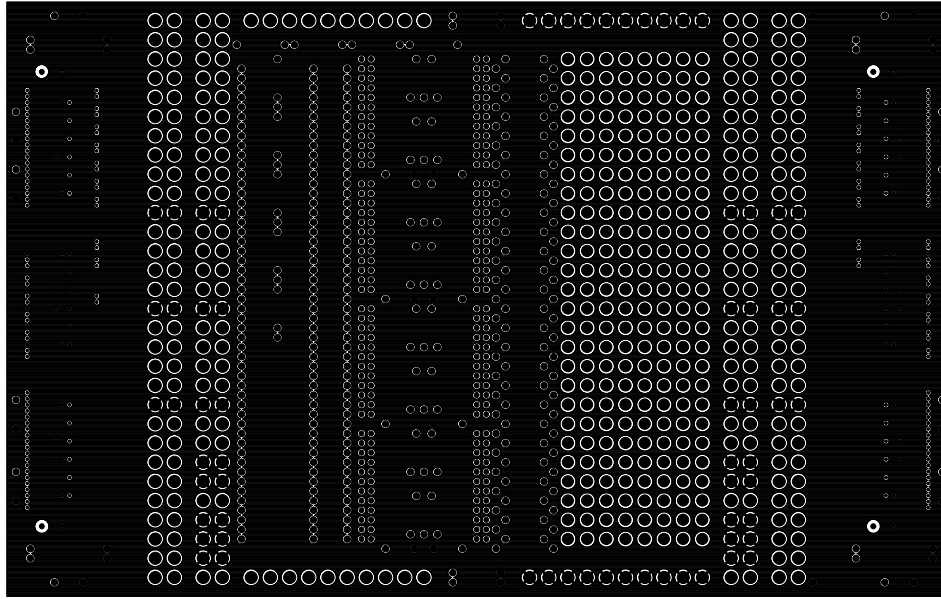
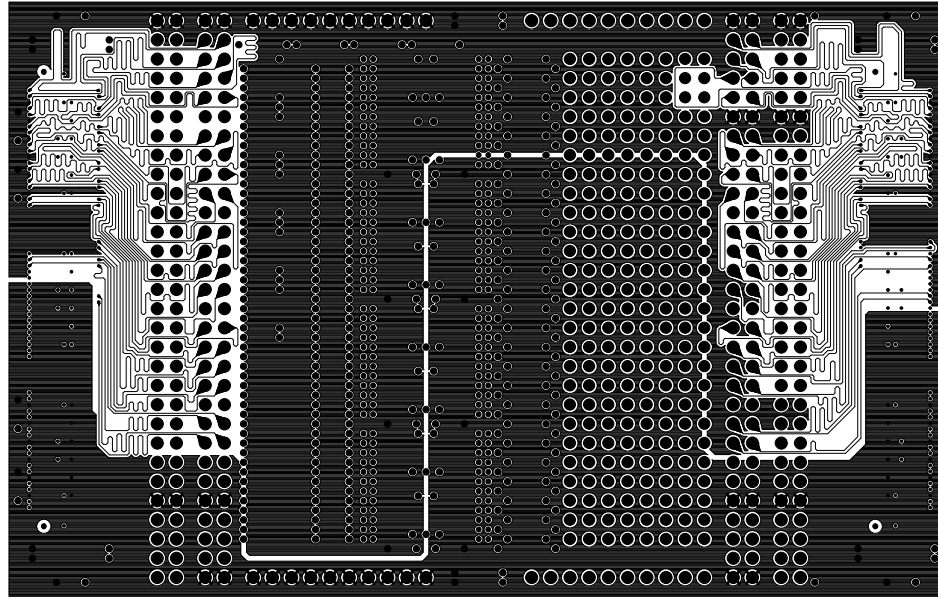


AES	CUSTOMER: AVNET ELECTRONIC MARKETING	DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD	REV: A
	LEVEL: PRIMARY COMPONENT SIDE - LAYER 1	

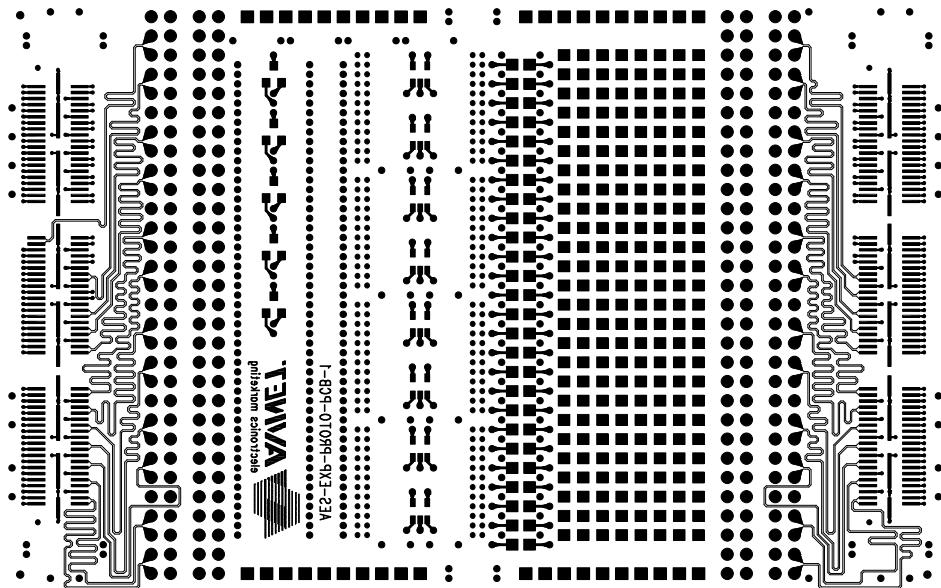


AES	CUSTOMER: AVNET ELECTRONIC MARKETING	DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD	REV: A
	LEVEL: GND PLANE - LAYER 2	

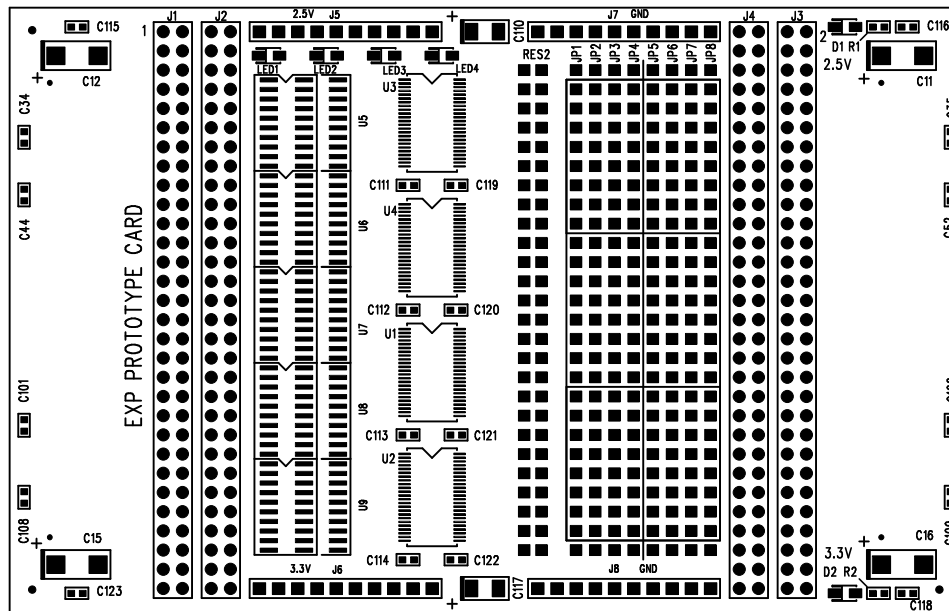




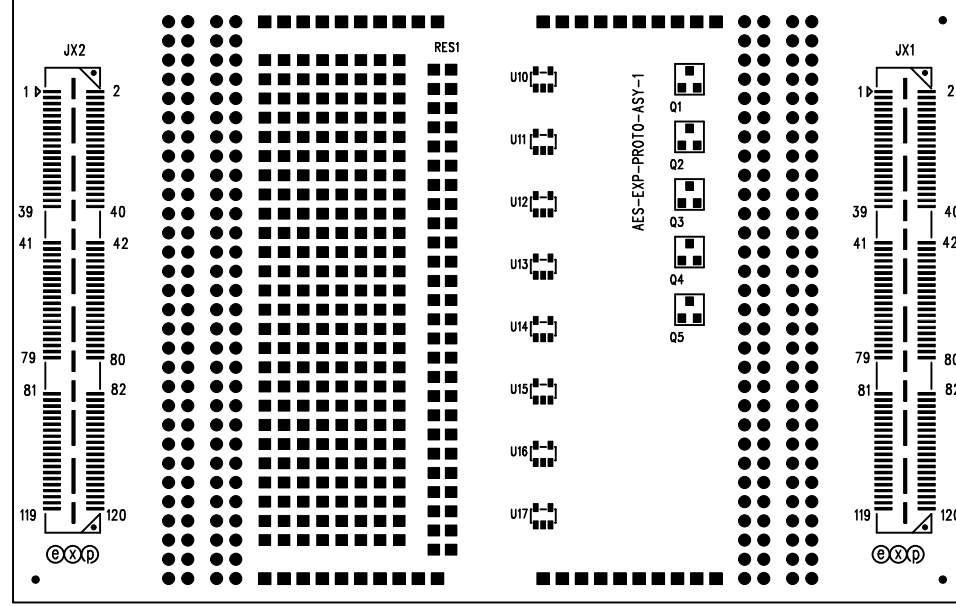
AES	CUSTOMER: AVNET ELECTRONIC MARKETING	DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD	REV: A
	LEVEL: PWR PLANE - LAYER 3	



AES	CUSTOMER: AVNET ELECTRONIC MARKETING		DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD		REV: A
	LEVEL: SECONDARY COMPONENT SIDE - LAYER 4		



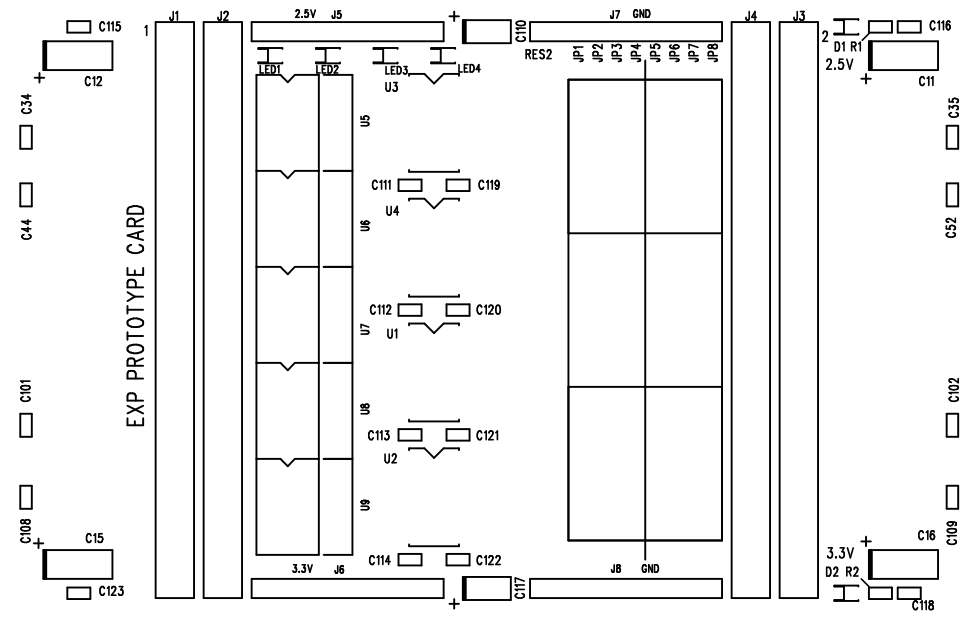
AES	CUSTOMER: AVNET ELECTRONIC MARKETING	DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD	REV: A
	LEVEL: PRIMARY SILKSCREEN	



LEVEL: SECONDARY SILKSCREEN	TITLE: EXP PROTOTYPE CARD	CUSTOMER: AVNET ELECTRONIC MARKETING
REV: A	DATE: SEP-19-08	

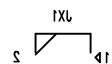
23A





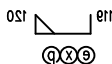
AES	CUSTOMER: AVNET ELECTRONIC MARKETING	DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD	REV: A
	LEVEL: PRIMARY SILKSCREEN	





41  
20  
45

81  
20  
85



1-V2A-01089-9X3-23A

1010

1111

1212

1313

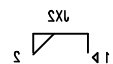
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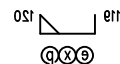
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1234



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81  
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85

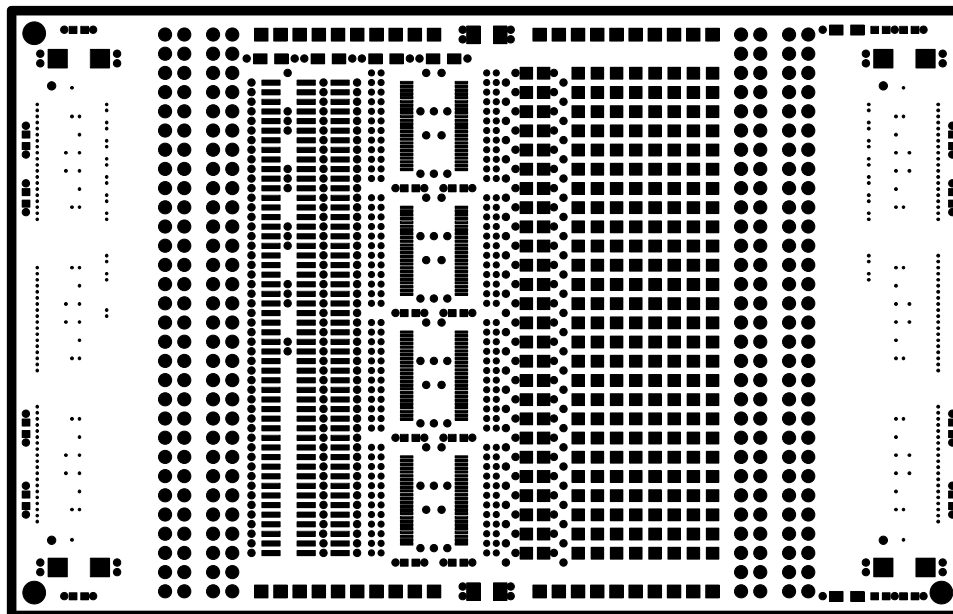


AES

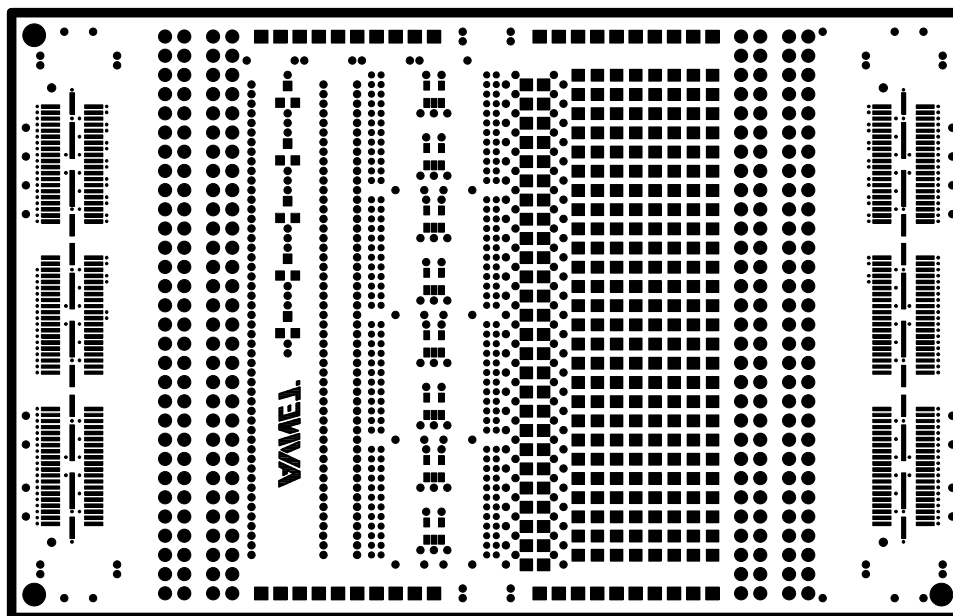
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TITLE: EXP PROTOTYPE CARD    REV: A  
LEVEL: SECONDARY SILKSCREEN



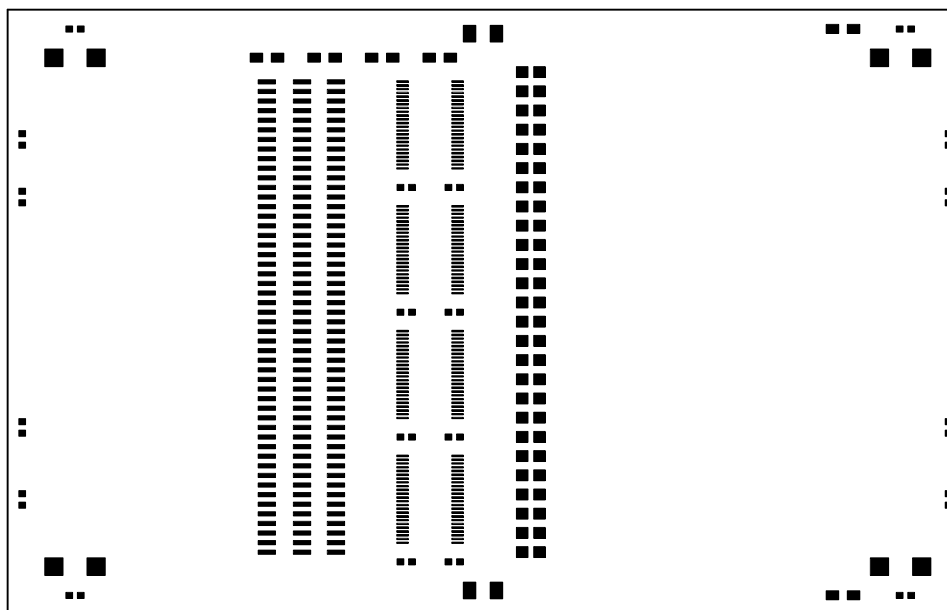




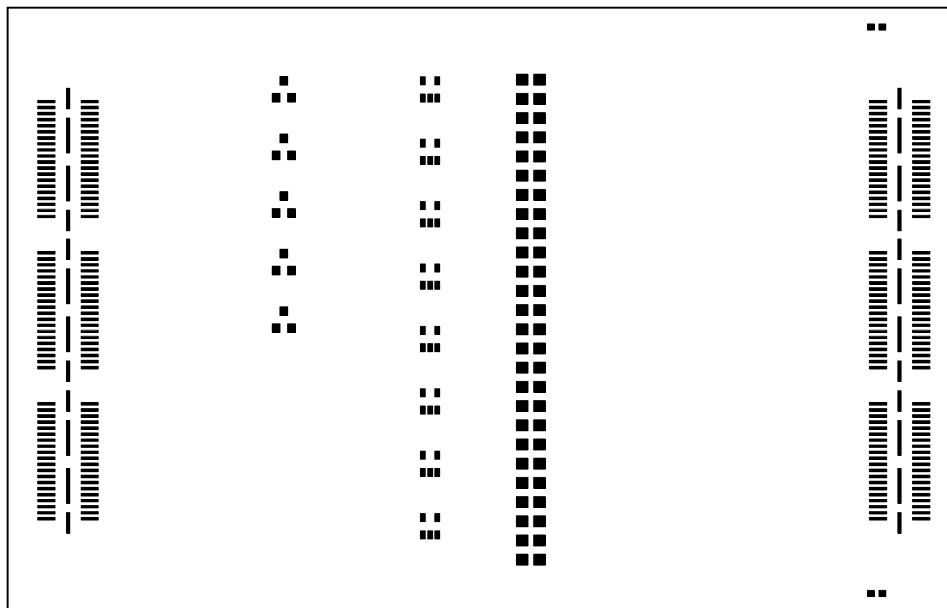
AES	CUSTOMER: AVNET ELECTRONIC MARKETING	DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD	REV: A
	LEVEL: PRIMARY SOLDER MASK	



AES	CUSTOMER: AVNET ELECTRONIC MARKETING	DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD	REV: A
	LEVEL: SECONDARY SOLDER MASK	



AES	CUSTOMER: AVNET ELECTRONIC MARKETING	DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD	REV: A
	LEVEL: PRIMARY SOLDER PASTE	



AES	CUSTOMER: AVNET ELECTRONIC MARKETING	DATE: SEP-19-06
	TITLE: EXP PROTOTYPE CARD	REV: A
	LEVEL: SECONDARY SOLDER PASTE	

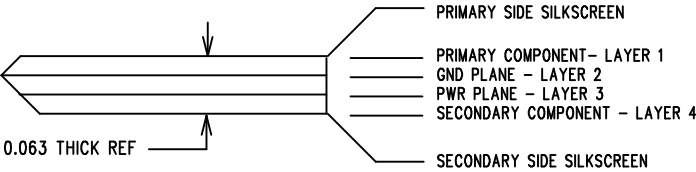


NOTES: UNLESS OTHERWISE SPECIFIED

- 1. BOARD SHALL BE FABRICATED – PERFORMANCE CLASS II AS PER IPC-6011 AND IPC-6012
- 2. VENDOR LOGO, VENDOR P/N, REVISION AND DATE CODE OF MANUFACTURING SHALL BE ETCHED ON THE SOLDER SIDE. THE DATE CODE SHALL BE IN THE FORMAT: "WWYY" WHERE WW=WEEK AND YY=YEAR
- 3. FABRICATE USING FILM "FAB/DRILL IDENT" FOR REFERENCE
- 4. PERMANENTLY MARK BARE BOARD WITH TEST STAMP USING WHITE, NON-CONDUCTIVE, RoHS COMPLIANT INK
- 5. SILKSCREEN BOTH SIDES WITH NON-CONDUCTIVE, RoHS COMPLIANT INK, NOT ALLOWED ON COMPONENT PADS, COMPONENT MOUNTING HOLES, OR VIAS (COLOR = WHITE)
- 6. MATERIAL: PER IPC-4101A/24/26/29/99, COPPER CLAD, HIGH TEMPERATURE FR4 CLASS EPOXY GLASS RATED UL94V-0. MUST BE RoHS COMPLIANT AND SURVIVE A LEAD-FREE ASSEMBLY MAX REFLOW OF 260 DEG C (6 PASSES)
  - Td RATING: > 340 DEG C
  - Z AXIS CTE < 3.5%
  - Tg > 170 DEG C (MIN)
- 7. SOLDER MASK: SMOBC PER IPC-SM-840C, CLASS T, MUST BE RoHS COMPLIANT, TYPE LPI, 0.0002" MIN TO 0.0008" MAX MEASURED OVER COPPER PLATING, MUST CLEAR ALL LANDS AS INDICATED ON GERBER SOLDER MASK LAYERS, (COLOR = RED)
- 8. FINISH: ELECTRO-LESS NICKEL IMMERSION GOLD (ENIG), 2-8 MICRO INCHES GOLD OVER 150-250 MICRO INCHES NICKEL
- 9. SOLDERABILITY TEST: CATEGORY 2 OF J-STD-003
- 10. ALL TEST POINTS SHALL BE FREE OF SOLDERMASK AND SILKSCREEN
- 11. ALL HOLE SIZES ARE AFTER PLATING
- 12. VENDOR MAY USE TEAR DROPS TO IMPROVE ANNULAR RINGS AS LONG AS DRC RULES ARE FOLLOWED
- 13. FINISHED BOARDS SHALL NOT HAVE NICKS, SCRATCHES, VOIDS, EXPOSED COPPER, POOR PLATING OR MISDRILLED HOLES
- 14. TIE-BARS ON THERMAL PADS SHOULD BE 15 MILS MINIMUM WIDTH
- 15. MAKE ALL VIA CONNECTIONS TO POWER AND GROUND PLANES SOLID (IE: THERMALS WITH 25 MIL O.D. OR 45 MIL O.D. SHOULD BE REMOVED FROM INNER PLANE LAYERS)
- 16. VENDOR MAY ADD COPPER THIEVING AS NEEDED TO IMPROVE MANUFACTURABILITY, THIEVING TO BE 0.030" ROUND PADS AT 0.050" SPACING. THIEVING WILL HAVE A MINIMUM OF 0.100" CLEARANCE FROM EXISTING COPPER AND SHOULD NOT BE PLACED UNDER SURFACE MOUNT DEVICES
- 17. ALL UNCONNECTED PADS ON INNER SIGNAL LAYERS MUST BE REMOVED
- 18. ALL FINISHED BOARDS TO BE 100% ELECTRICALLY TESTED
- 19. UNLESS OTHERWISE INDICATED, ALL LINEAR TOLERANCES SHALL BE XX +/- .010 AND XXX +/- .005

ADDITIONAL NOTES:

- 20. FINISHED BOARD THICKNESS = 0.063"(+/- 0.007")



HOLE CHART			
DIA AFTER PLATING	QTY	SYM	PLATE THRU
.010 +.001 -.008	220	+	YES
.014 +.001 -.008	192	×	YES
.020 +/- .003	383	□	YES
.035 +/- .003	208	◇	YES
.040 +/- .003	280	⊠	YES
.040 +/- .003	4	⊞	NO

AES

CUSTOMER: AVNET ELECTRONIC MARKETING

DATE: SEP-19-06

TITLE: EXP PROTOTYPE CARD

REV: A

LEVEL: FAB/DRILL IDENT