DLP® Discovery™ 4100 Chipset Data Sheet

The DLP Discovery 4100 from Texas Instruments offers the highest speed pattern rates in the DLP catalog portfolio with the option for random row addressing. Two offerings currently supported are: 0.7 XGA chipset and 0.95 1080p chipset, which enable binary pattern rates of up to 32 kHz and 23 kHz, respectively. These fast pattern rates set DLP technology apart from other spatial light modulators and offer customers a strategic advantage for equipment needing fast, accurate and programmable light steering capability. The unique capability and value offered by DLP Discovery 4100 chipsets makes them well suited to support a wide variety of industrial, medical, and advanced display applications.

A dedicated chipset provides developers easier access to the DMD as well as high speed, independent micromirror control.

Features

- Allows Input Clock Rates Between 200 Mhz and 400 Mhz
- Provides up to a 64-Bit LVDS Data Bus Interface
- High Speed DDR LVDS DMD Data Bus
- Controls DMD Micromirror Clocking Pulse Timing Power Voltages
- Supports Random Row Addressing

Applications

- Industrial: Direct Imaging Lithography
- Industrial: Laser Marking and Repair Systems
- Industrial: Computer-to-Plate Printers
- Industrial: Rapid Prototyping Machines and 3D Printers
- Industrial: 3D Scanners for Machine Vision and Quality Control
- Medical: Phototherapy Devices
- Medical: Ophthalmology
- Medical: Vascular Imaging
- Medical: Hyperspectral Imaging
- Medical: 3D Scanners for Limb and Skin measurement
- Medical: Confocal Microscopes
- Display: 3D Imaging Microscopes
- Display: Compressive Sensing
- Display: Intelligent and Adaptive Lighting
- Display: Augmented Reality and Information Overlay

1 Purpose

This document provides:

- Descriptions of the DLP Discovery 4100 chipset components.
- Functional and interconnect information for the individual chipset components.
- System-level design guidelines to ensure proper function of the complete DLP Discovery 4100 chipset.

Table 1. Related Documentation

Document	TI Literature Number
DLP7000 0.7 XGA Type-A DMD data sheet	DLPS026
DLP9500 0.95 1080p Type-A DMD data sheet	DLPS025
DLPC410 Digital Controller data sheet	DLPS024
DLPA200 DMD Micromirror Driver data sheet	DLPS015
DLPR410 / DLPR4101 EEPROM data sheet	DLPS027

Device Description

The DLP® Discovery™ 4100 chipset offers developers a convenient way to design a wide variety of industrial, medical, telecom and advanced display applications by delivering maximum flexibility in formatting data, sequencing data, and light patterns.

The DLP® Discovery™ 4100 chipset includes the following four components: DMD Digital Controller (DLPC410), EEPROM (DLPR410 / DLPR4101), DMD Micromirror Driver (DLPA200), and a DMD (DLP7000 or DLP9500).

DLPC410 DMD Digital Controller

- Provides high speed 2XLVDS data and control interface to the user.
- Drives mirror clocking pulse and timing information to the DLPA200.
- Supports random row addressing.

DLPR410 / DLPR4101 EEPROM

- Contains startup configuration information.

DLPA200 DMD Micromirror Driver

- Generates Micromirror Clocking Pulse control (sometimes referred to as a "Reset") of 16 banks of DMD mirrors. (Two required for DLP9500)

DMD: Digital Micromirror Device containing the array of aluminum mirrors that steer light in two digital positions (+12-degrees and -12 degrees).

- DLP9500 DMD: 0.95-inch array diagonal, 1920 x 1080 micromirror array, 1080p display resolution.
- DLP7000 DMD: 0.7-inch array diagonal, 1024 x 768 micromirror array, XGA display resolution

The DLP Discovery 4100 Chipset can have these two configurations:

Table 2. DLP Discovery 4100 Chipset Configurations

0.7 XGA Chipset			0.95 1080p Chipset		
Qty	**TI Part**	**Description**	**Qty**	**TI Part**	**Description**
1	DLP7000	0.7 XGA Type A DMD(digital micromirror device)	1	DLP9500	0.95 1080p Type A DMD(digital micromirror device)
1	DLPC410	DLP Discovery 4100 DMD Controller	1	DLPC410	DLP Discovery 4100 DMD Controller
1	DLPR410 DLPR4101	DLP Discovery 4100 Configuration PROM (1)	1	DLPR410 DLPR4101	DLP Discovery 4100 Configuration PROM (1)
1	DLPA200	DMD Micromirror Driver	2	DLPA200	DMD Micromirror Driver

(1) See DLPS024 "Load 4" section for a description of DLPR4101 enhanced functionality

Reliable function and operation of DLP Discovery 4100 chipsets require the components be used in conjunction with each other. This document describes the proper integration and use of the DLP Discovery 4100 chipset components.

The DLPC410 chipset can be combined with a user programmable Application FPGA (not included) to create high performance systems.

1.1 Discovery 4100 Chipset DMD Features

Table 3. DLPC410 DMD Types Overview

DMD	Array	Patterns/Sec	Data Rate (Gbs)	Mirror Pitch
DLP9500 - 0.95” 1080p	1920 x 1080	23,148	48	10.8 µm
DLP7000 - 0.7”XGA	1024 x 768	32,552	25.6	13.6 µm

Chipset Components

Figure 1 below is a simplified system block diagram showing the use of the DLPC410 with the following components:

- 2XLVDS DMD – Spatial Light Modulator
- DLPA200 – DMD micromirror driver(s) for DMD (Two required for DLP9500 - 0.95" 1080p DMD)
- DLPC410 – Xilinx [XC5VLX30] FPGA configured to provide high-speed DMD data and control, and DLPA200 timing and control
- EEPROM – [XCF16PFSG48C] serial flash PROM contains startup configuration information

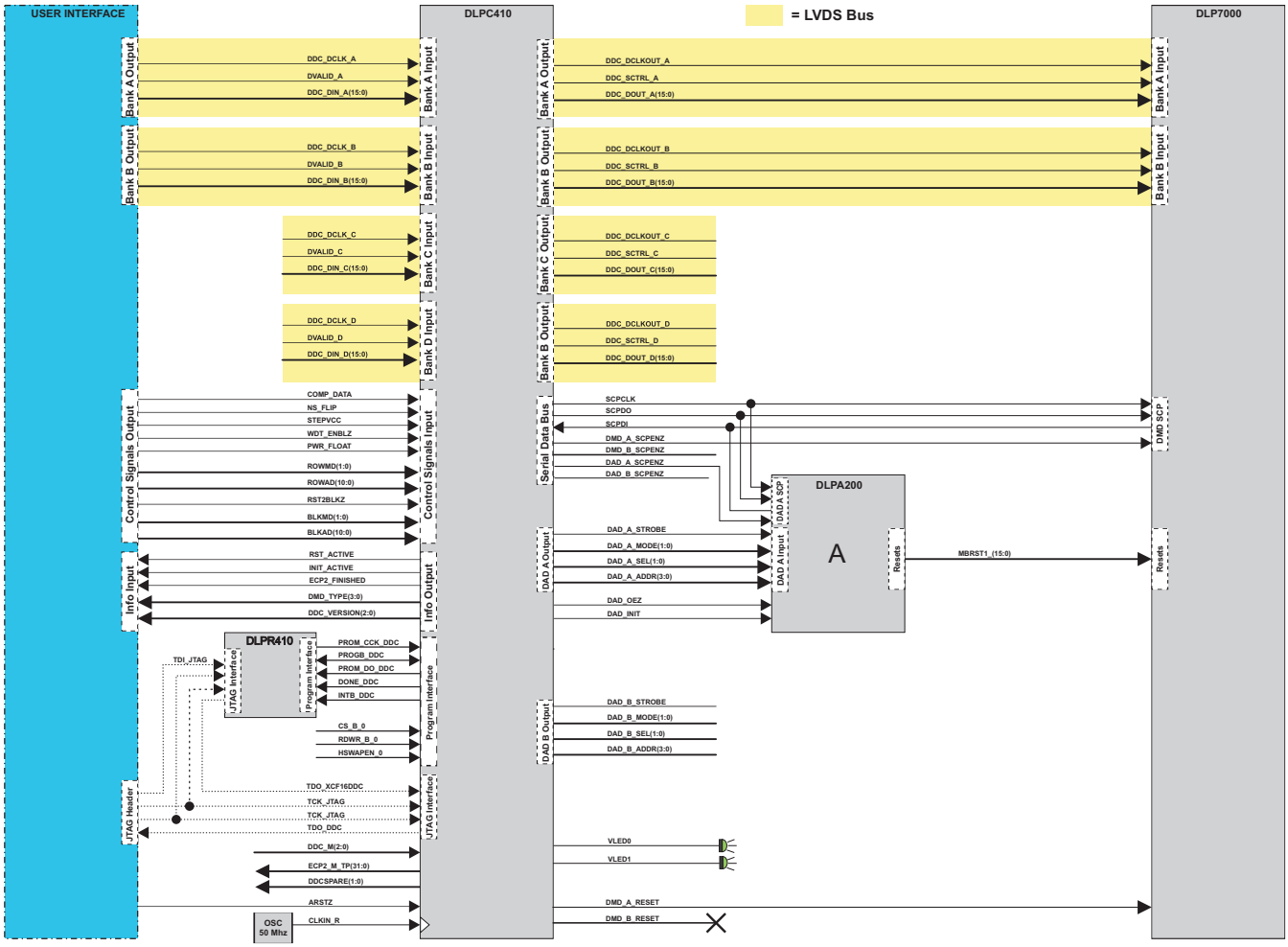

Figure 1. DLPC410 and DLP7000 Chipset Block Diagram

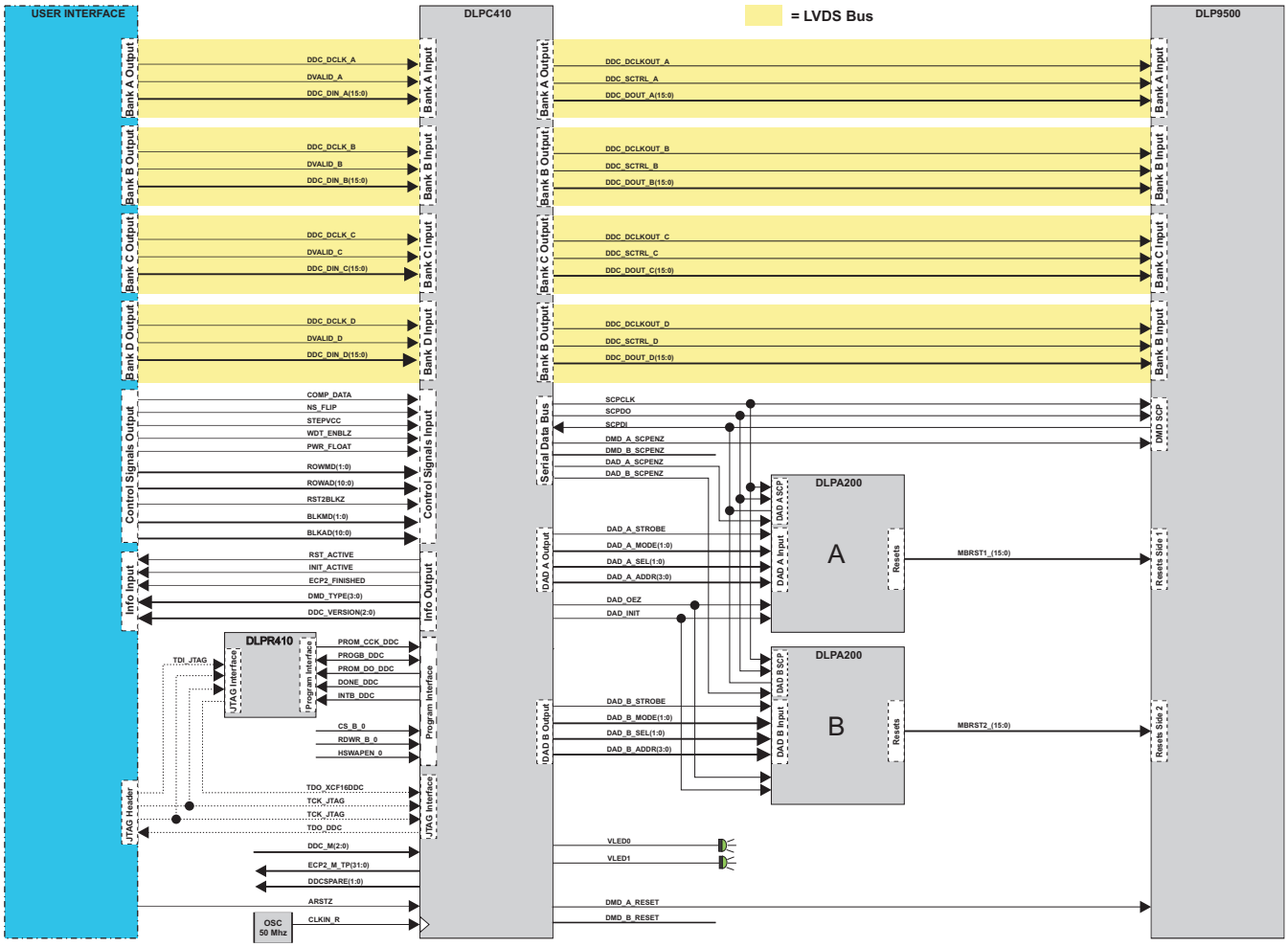

Figure 2. DLPC410 and DLP9500 Chipset Block Diagram

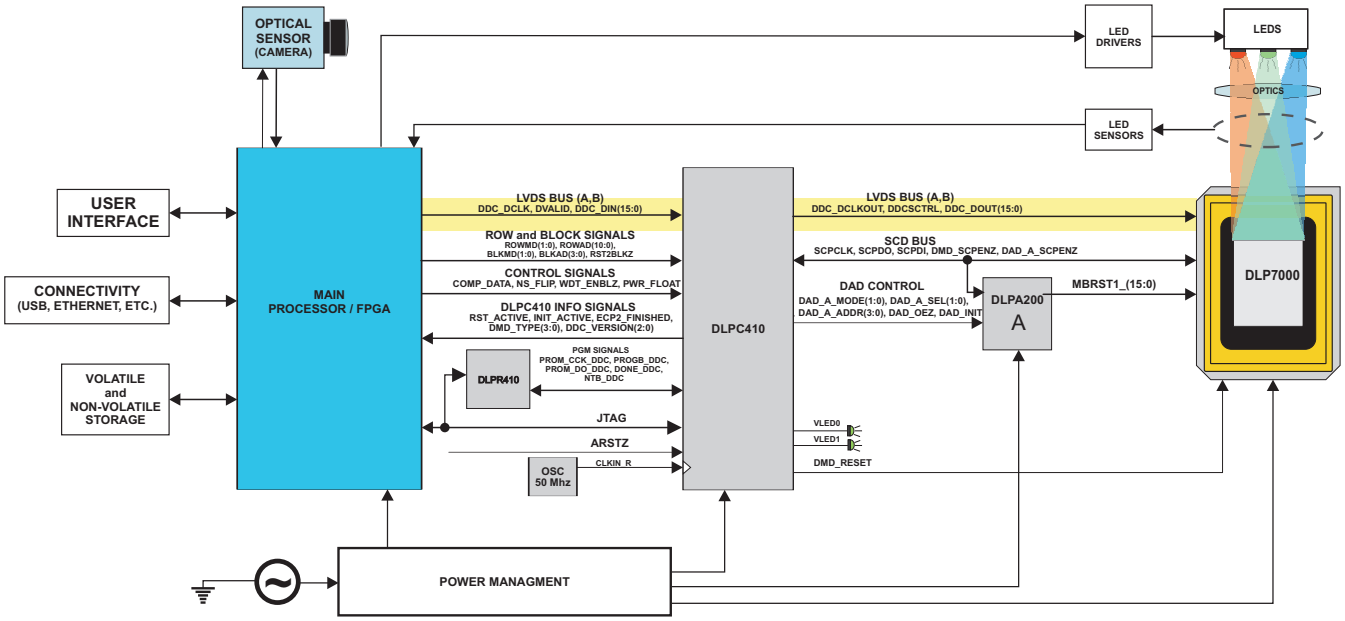

Figure 3. DLPC410 and DLP7000 Embedded Example Block Diagram

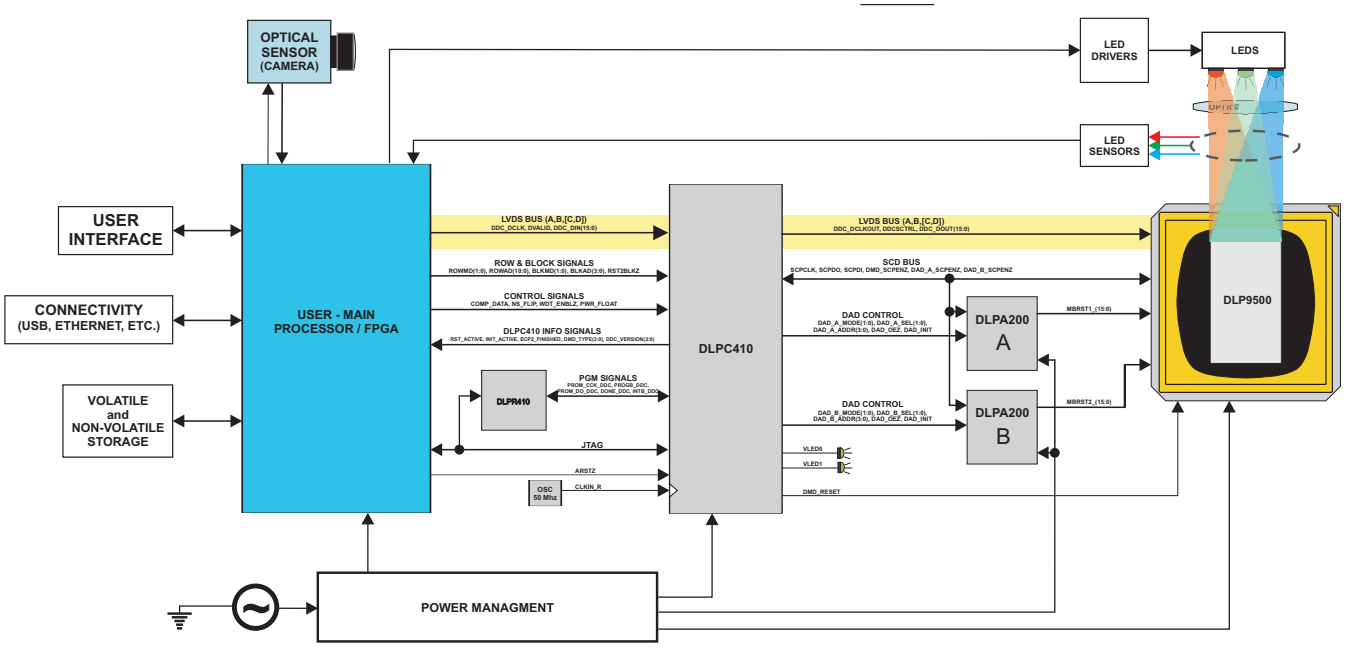

Figure 4. DLPC410 and DLP9500 Embedded Example Block Diagram

1.2 DLPC410 Controller

The DLPC410 chipset includes the DLPC410 controller which provides a high-speed LVDS data and control interface for DMD control. This interface is also connected to a second FPGA used to drive applications (not included in the chipset). The DLPC410 generates DMD and DLPA200 initialization and control signals in response to the inputs on the control interface.

For more information, see the DLPC410 Data Sheet.

1.3 DLPA200 DMD Micromirror Driver(s)

DLPA200 micromirror driver provide the miromirror clocking pulse driver functions for the DMD. One DLPA200 is required for DLP7000 and two for DLP9500.

For more information on the DLPA200, see the DLPA200 data sheet.

1.4 Flash Configuration PROM

The DLPC410 is configured at startup from the serial flash PROM. The contents of this PROM can not be altered. For more information, see the DLPC410 Data Sheet.

1.5 DMD

The DLPC410 supports the 2 x LVDS DMD devices shown in Table 4.

Table 4. DLPC410 DMD Types

TYPE	Number of COLS	Number of ROWS	Global Reset Max FPS	Phased Reset Max FPS	CLKS and ROW	DIN data bus width
DLP9500 - 0.95" 1080p Type A	1920	1080	17636	23148	16	64
DLP7000 - 0.7" XGA Type A	1024	768	22614	32552	16	32

2 DMD Operation

The DLP9500 is used as an example to explain the operation of the DMD. The DLP7000 operates similar to the DLP9500. The DLP9500 is loaded as 15 blocks of 72 rows each. The first 64 bits of pixel data and last 64 bits of pixel data for all rows are not visible. Below is a representation of how the image is loaded by the different Micromirror Clocking Pulse modes. For more detailed information on the operation of the DMD, see the individual DMD reference manual.

There are four Micromirror Clocking Pulse modes that determine which blocks are "reset" when a Micromirror Clocking Pulse command is issued:

- Single block mode
- Dual block mode
- Quad block mode
- Global mode

2.1 Single Block Mode

In single block mode, a single block can be loaded and reset in any order. After a block is loaded, it can be reset to transfer the information to the mechanical state of the mirrors.

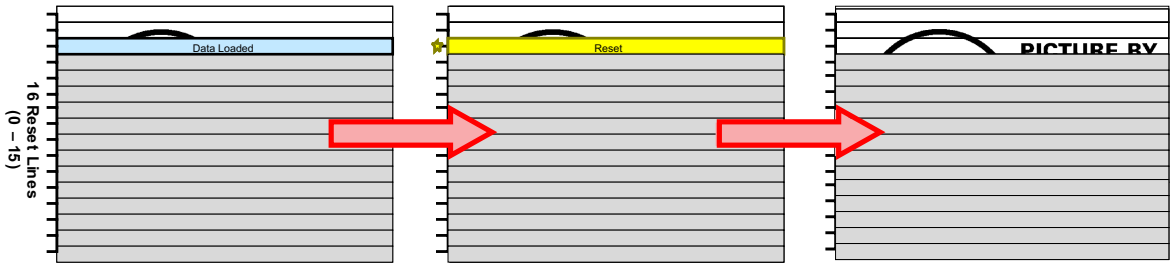

Figure 5. Single Block Mode

2.2 Dual Block Mode

In dual block mode, reset blocks are paired together as follows (0-1), (2-3), (4-5) . . . (14-15). These pairs can be reset in any order. After data is loaded a pair can be reset to transfer the information to the mechanical state of the mirrors.

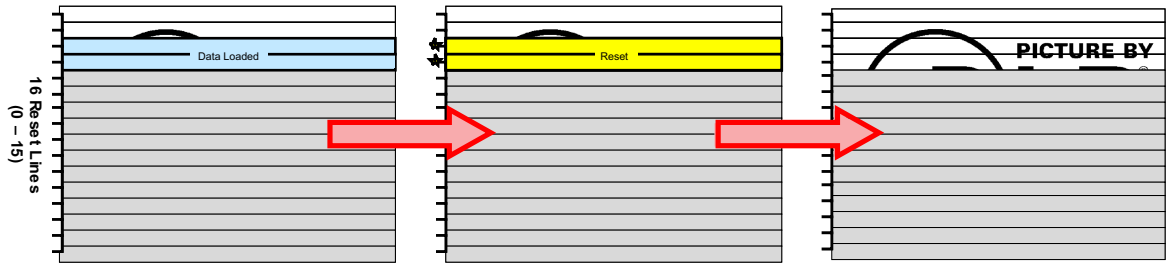

Figure 6. Dual Block Mode

2.3 Quad Block Mode

In quad block mode, reset blocks are grouped together in fours as follows (0-3), (4-7), (8-11) and (12-15). Each quad group can be randomly addressed and reset. After a quad group is loaded, it can be reset to transfer the information to the mechanical state of the mirrors.

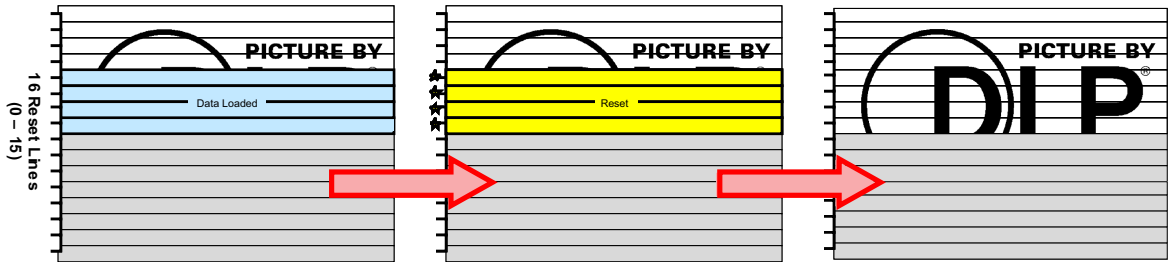

Figure 7. Quad Block Mode

2.4 Global Mode

In global mode, all reset blocks are grouped into a single group and reset together. The entire DMD must be loaded with the desired data before issuing a Global Reset to transfer the information to the mechanical state of the mirrors.

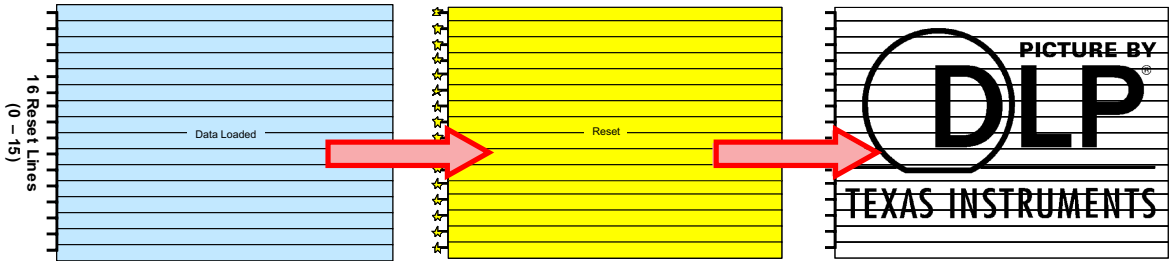

Figure 8. Global Mode

The DMD memory is loaded one row at a time by 2 or 4 semi-independent LVDS buses depending on the specific DMD design. The DLP9500 requires all 4 data buses A, B, C, D while the DLP7000 requires only 2 data buses A, B. Each DDC_DIN bus is comprised of 16 differential pairs of LVDS signals that are input to the DLPC410 as listed in Table 6. Data and control signals are clocked into the DMD on both the rising and falling edges of the DDR data clock DDC_DCLKIN.

The row load length in clocks can be determined by the equation: $\frac{\text{number of pixels per row}}{\text{data bus bit width x 2}}$. There is a two in the denominator because the DMD data bus is dual data rate. This equation yields 15 clocks per row for 1920 x 1080 and a 64 bit bus or 16 clocks per row for 1024 x 768 and a 32 bit bus. However, with the DLP9500 there are 64 bits at the beginning and end of each row that are not displayed. This yields 16 clocks per row for both 1920 x 1080 and 1024 x 768 displays.

Data loading will not cause mirror movement until a Micromirror Clocking Pulse (reset) operation is completed.

Before turning off power to the DMD, the DMD mirrors must be “parked” (or “floated”). Parking (or floating) the DMD mirrors places them in a relatively flat orientation (not tilted in either a +12° or –12° direction). This operation helps to ensure reliable operation over the life of the device. This operation is performed by the DLPC410. For more detailed information, see DLPC410 Data sheet.

3 Discovery 4100 Interfaces

This section will show the interface between the different components included in the chipset.

3.1 User to DLPC410 Interface

3.1.1 DLPC410 IO Description

Table 5 describes the inputs and outputs of the DLPC410 to the user. For more details on these signals, see the DLPC410 data sheet.

Table 5. Input/Output Description

Pin Name	Description	I/O
ARSTZ	Asynchronous active low reset	I
CLKIN_R	Reference clock, 50 MHz	I
DIN_[A,B,C,D](15:0)	LVDS DDR input for data bus A,B,C,D (15:0)	I
DCLKIN[A,B,C,D]	LVDS inputs for data clock (200 - 400 MHz) on bus A, B, C, and D	I
DVALID[A,B,C,D]	LVDS input used to start write sequence for bus A, B, C, and D	I
ROWMD(1:0)	DMD row address and row counter control	I
ROWAD(10:0)	DMD row address pointer	I
BLK_AD(3:0)	DMD mirror block address pointer	I
BLK_MD(1:0)	DMD mirror block reset and clear command modes	I
PWR_FLOAT	Used to float DMD mirrors before complete loss of power	I
DMD_TYPE(3:0)	DMD type in use	O
RST_ACTIVE	Indicates DMD mirror reset in progress	O
INIT_ACTIVE	Initialization in progress.	O
VLED0	System “heartbeat” signal	O
VLED1	Denotes initialization complete	O

3.1.2 Initialization

The *INIT_ACTIVE* (Table 5) signal indicates that the DMD, DAD, and DDC are in an initialization state after power is applied. During this initialization period, the DDC is initializing the DMD and DAD(s) by setting all internal registers to their correct states. When this signal goes low, the system has completed initialization. System initialization takes approximately 220 ms to complete. Data and command write cycles should not be asserted during the initialization.

During initialization the user must send a training pattern to the DLPC410 on all data and DVALID lines to correctly align the data inputs to the data clock. For more information, see the DLPC410 data sheet – Interface Training Pattern.

3.1.3 DMD Device Detection

The DLPC410 automatically detects the DMD type and device ID. DMD_TYPE (Table 5) is an output from the DLPC410 that contains the DMD information. Only DMDs sold with the chipset or kit are recognized by the automatic detection function. All other DMDs does not operate with the DLPC410.

3.1.4 Power Down

To ensure long term reliability of the DMD, a shutdown procedure must be executed. Prior to power removal, assert the PWR_FLOAT (Table 5) signal and allow approximately 300 μs for the procedure to complete. This procedure assures the mirrors are in a flat state. For more details, see the individual DMD data sheet.

3.2 DLPC410 to DMD Interface

3.2.1 DLPC410 to DMD IO Description

Table 6 lists the available controls and status pin names and their corresponding signal type, along with a brief functional description.

Table 6. DLPC410 to DMD I/O Pin Descriptions

Pin Name	Description	I/O
DDC_DOUT_[A,B,C,D](15:0)	LVDS DDR output to DMD data bus A,B,C,D (15:0)	O
DDC_DCLKOUT_[A,B,C,D]	LVDS output to DMD data clock A,B,C,D	O
DDC_SCTRL_[A,B,C,D]	LVDS DDR output to DMD data control A,B,C,D	O

3.2.2 Data Flow

Figure 9 shows the data traffic through the DLPC410. Special considerations are necessary when laying out the DLPC410 to allow best signal flow.

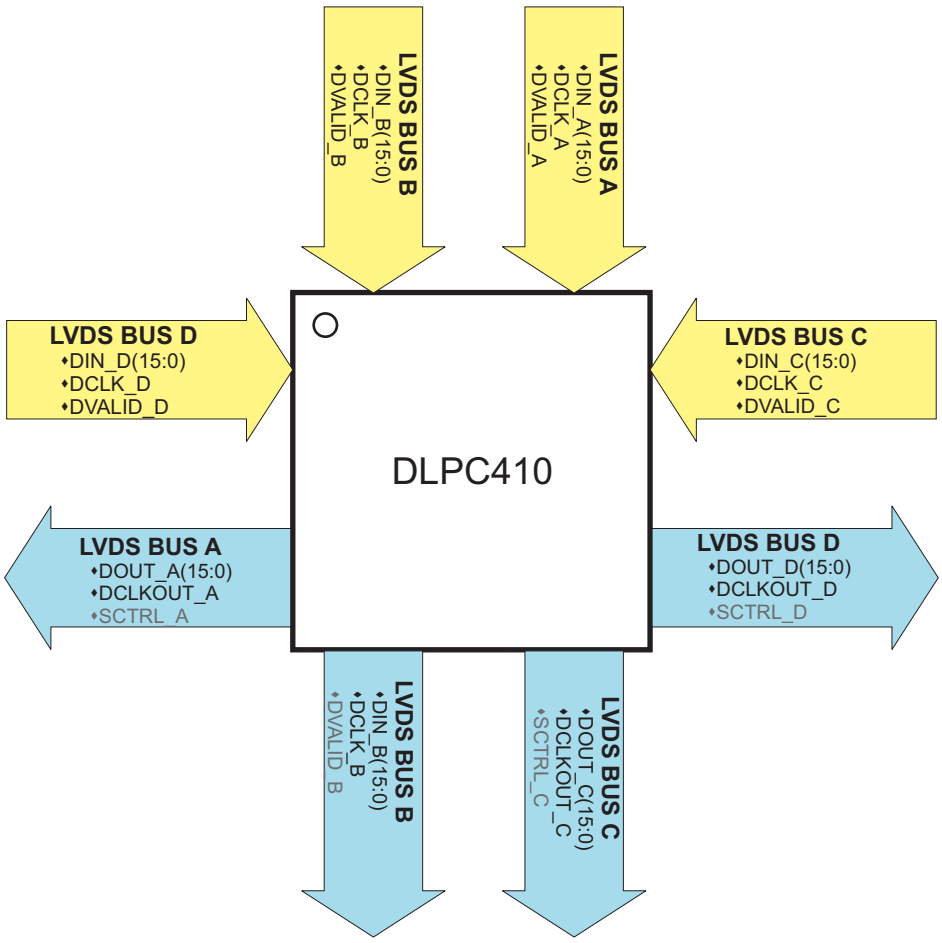

Figure 9. DLPC410 Data Flow

Four LVDS buses transfer the data from the user to the DLPC410. Each bus has its data clock that is input edge aligned with the data (DCLK). Each bus also has its own validation signal that qualifies the data input to the DLPC410 (DVALID).

Output LVDS buses transfer data from the DLPC410 to the DMD. Output buses LVDS C and LVDS D are only used with the DLP9500.

3.3 DLPC410 to DAD Interface

3.3.1 DAD Operation

The DLPA200 DMD Micromirror Driver is a mixed-signal Application Specific Integrated Circuit (ASIC) that combines the necessary high-voltage power supply generation and Micromirror Clocking Pulse functions for a family of DMDs. The DLPA200 is programmable and controllable to meet all current and anticipated DMD requirements.

The DLPA200 operates from a +12 volt power supply input. For more detailed information on the DLPA200, see the DLPA200 data sheet.

3.3.2 DLPC410 to DAD IO Description

The Serial Communications Port (SCP) is a full duplex, synchronous, character-oriented (byte) port that allows exchange of commands from the DLPC410 to the DAD(s). One SCP bus is used for the DLP7000 and a second SCP bus is used with the DLP9500.

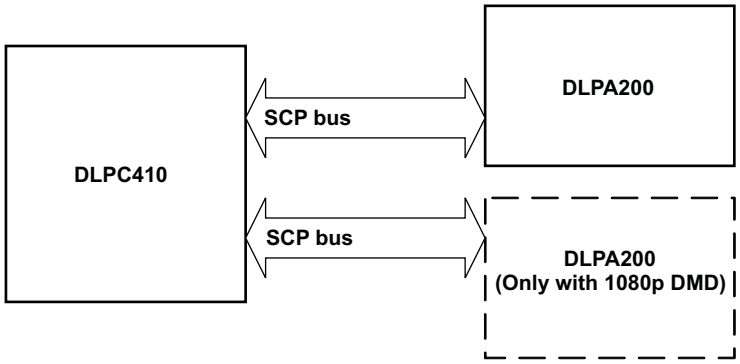

Figure 10. Serial Port System Configuration

There are five signal lines associated with the SCP bus: SCPENZ, SCPCK, SCPDI, SCPDO, and IRQZ .

Table 7 lists the available controls and status pin names and their corresponding signal type, along with a brief functional description.

Table 7. DLPC410 to DAD I/O Pin Descriptions

Pin Name	Description	I/O
DAD_A_SCPENZ	Active low chip select for DLPA200 serial bus	O
DAD_A_STROBE	DLPA200 control signal strobe	O
DAD_A_MODE(1:0)	DLPA200 mode control	O
DAD_A_SEL(1:0)	DLPA200 select control	O
DAD_A_ADDR(3:0)	DLPA200 address control	O
DAD_B_SCPENZ	Active low chip select for DLPA200 serial bus (2)	O
DAD_B_STROBE	DLPA200 control signal strobe (2)	O
DAD_B_MODE(1:0)	DLPA200 mode control	O
DAD_B_SEL(1:0)	DLPA200 select control	O
DAD_B_ADDR(3:0)	DLPA200 address control	O

The DLPA200 provides a variety of output options to the DMD by selecting logic control inputs: MODE[1:0], SEL[1:0] and reset group address A[3:0] (Table 7). The MODE[1:0] input determines whether a single output, two outputs, four outputs, or all outputs, will be selected. Output levels (VBIAS, VOFFSET, or VRESET) are selected by SEL[1:0] pins. Selected outputs are tri-stated on the rising edge of the STROBE signal and latched to the selected voltage level after a break-before-make delay. Outputs will remain latched at the last Micromirror Clocking Pulse waveform level until the next Micromirror Clocking Pulse waveform cycle.

3.4 DAD to DMD Interface

3.4.1 DAD to DMD Interface Overview

The DLPA200 generates three voltages: VBIAS, VRESET, and VOFFSET that are supplied to the DMD MBRST lines in various sequences through the Micromirror Clocking Pulse driver function. VOFFSET is also supplied directly to the DMD as DMDVCC2. A fourth DMD power supply, DMDVCC, is supplied directly to the DMD by regulators.

The function of the Micromirror Clocking Pulse driver is to switch selected outputs in patterns between the three voltage levels (VBIAS, VRESET and VOFFSET) to generate one of several Micromirror Clocking Pulse waveforms. The order of these Micromirror Clocking Pulse waveform events is controlled externally by the logic control inputs and timed by the STROBE signal. DLPC410 automatically detects the DMD type and then uses the DMD type to determine the appropriate Micromirror Clocking Pulse waveform.

A direct Micromirror Clocking Pulse operation causes a mirror to transition directly from one latched state to the next. The address must already be set up on the mirror electrodes when the Micromirror Clocking Pulse is initiated. Where the desired mirror display period does not allow for time to set up the address, a Micromirror Clocking Pulse with release can be performed. This operation allows the mirror to go to a relaxed state regardless of the address while a new address is set up, after which the mirror can be driven to a new latched state.

A mirror in the relaxed state typically reflects light into a system collection aperture and can be thought of as “off” although the light is likely to be more than a mirror latched in the “off” state. System designers should carefully evaluate the impact of relaxed mirror conditions on optical performance.

3.4.1.1 Power-up sequence (handled by the DLPC410)

The sequence of events for DMD system power-up is:

1. Apply logic supply voltages to the DLPA200 and to the DMD according to DMD specifications.
2. Place DLPA200 driver(s) into high impedance states.
3. Turn on DLPA200 bias, offset, or reset supplies according to driver specifications.
4. After all supply voltages are assured to be within the limits specified and with all Micromirror Clocking Pulse operations logically suspended, enable all drivers to either VOFFSET or VBIAS level.
5. Begin Micromirror Clocking Pulse operations.

4 PCB Layout Guidelines

A target impedance of 50Ω for single ended signals and 100Ω between LVDS signals is specified for all signal layers.

4.1 DMD Interface

The digital interface from the DLPC410 to the DMD are LVDS signals that run at clock rates up to 400 MHz. Data is clocked into the DMD on both the rising and falling edge of the clock, so the data rate is 800 MHz. The LVDS signals should have 100 Ω differential impedance. The differential signals should be matched but kept as short as possible. Parallel termination at the LVDS receiver is in the DMD; therefore, on board termination is not necessary. See the DMD data sheet for more details.

4.1.1 Trace Length Matching

The DLPC410 DMD data signals require precise length matching. Differential signals should have impedance of 100Ω (with 5% tolerance). It is important that the propagation delays are matched. The maximum differential pair uncoupled length is 100 mils with a relative propagation delay of ±25 mil between the p and n. Matching all signals exactly will maximize the channel margin. The signal path through all boards, flex cables and internal DMD routing must be considered in this calculation. See the specific DMD data sheet for more information.

4.2 DLPC410 DMD Decoupling

General decoupling capacitors for the DLPC410 DMD should be distributed around the PCB and placed to minimize the distance from IC voltage and ground pads. Each decoupling capacitor (0.1 μF recommended) should have vias directly to the ground and power planes. Via sharing between components (discreet or integrated) is discouraged. The power and ground pads of the DLPC410 DMD should be tied to the voltage and ground planes with their own vias. See the individual DMD data sheet for more details.

4.2.1 Decoupling Capacitors

Decoupling capacitors should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component. It is recommended that the placement of and routing for the decoupling capacitors meet the following guidelines:

- The supply voltage pin of the capacitor should be located close to the device supply voltage pin(s). The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1 inch. Otherwise, the component should be tied to the voltage or ground plane through separate vias.
- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1 inch to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

4.3 VCC and VCC2

The VCC pins of the DMD should be connected directly to the DMD VCC plane. Decoupling for the VCC should be distributed around the DMD and placed to minimize the distance from the voltage and ground pads. Each decoupling capacitor should have vias directly connected to the ground and power planes. The VCC and GND pads of the DMD should be tied to the VCC and ground planes with their own vias.

The VCC2 voltage can be routed to the DMD as a trace. Decoupling capacitors should be placed to minimize the distance from the DMD's VCC2 and ground pads. Using wide etch from the decoupling capacitors to the DMD connection will reduce inductance and improve decoupling performance.

4.4 DMD Layout

See the DMD customer data sheet for package dimensions, timing and pin out information.

4.5 DLPA200

The DLPA200 generates the Micromirror Clocking Pulses for the DMD. The DMD-drive outputs from the DLPA200 (MBRST[15:0] should be routed with minimum trace width of 11 mil and a minimum spacing of 15 mil. The VCC and VCC2 traces from the output capacitors to the DLPA200 should also be routed with a minimum trace width and spacing of 11 mil and 15 mil, respectively. See the DLPA200 customer data sheet for mechanical package and layout information.

5 Power Supply Interface

Four different supply inputs are needed to properly power the chipset. The table below shows these power supplies and their descriptions.

Table 8. DLPC410 Chipset Power Supply

Power Supply	Description
1.0	Provides power to the DLPC410 core
2.5V	Provides power to the DLPC410 I/O
3.3V	Provides power to the EEPROM and the core of the DMD
12V	Provides power to the DLPA200

Revision History

Changes from Original (August 2012) to A Revision **Page**

- Added DLPR4101 to DLPR410 in Related Documentation Table 2
- Added DLPR4101 to DLPR410 in Chipset Configurations Table 2

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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