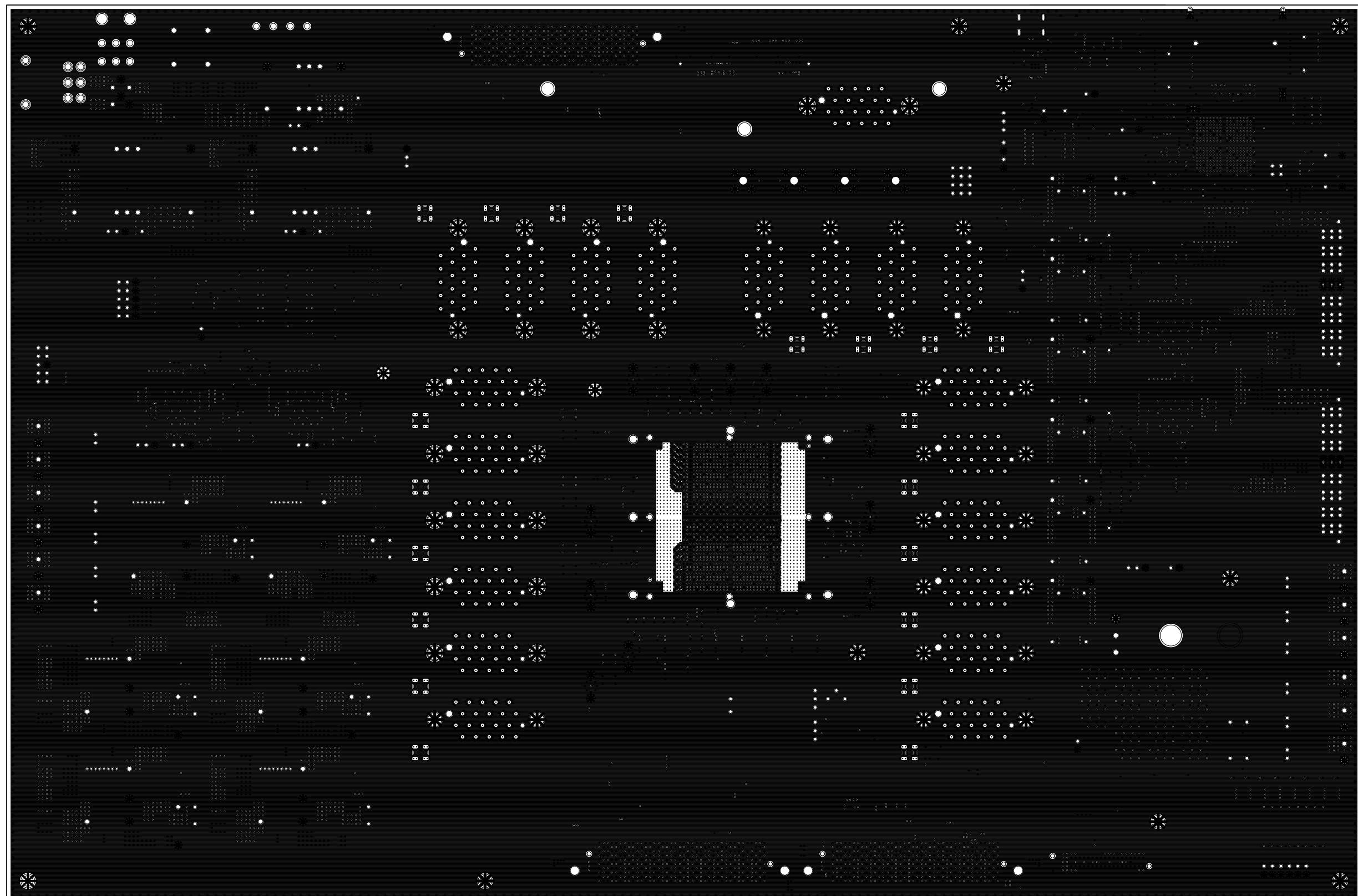
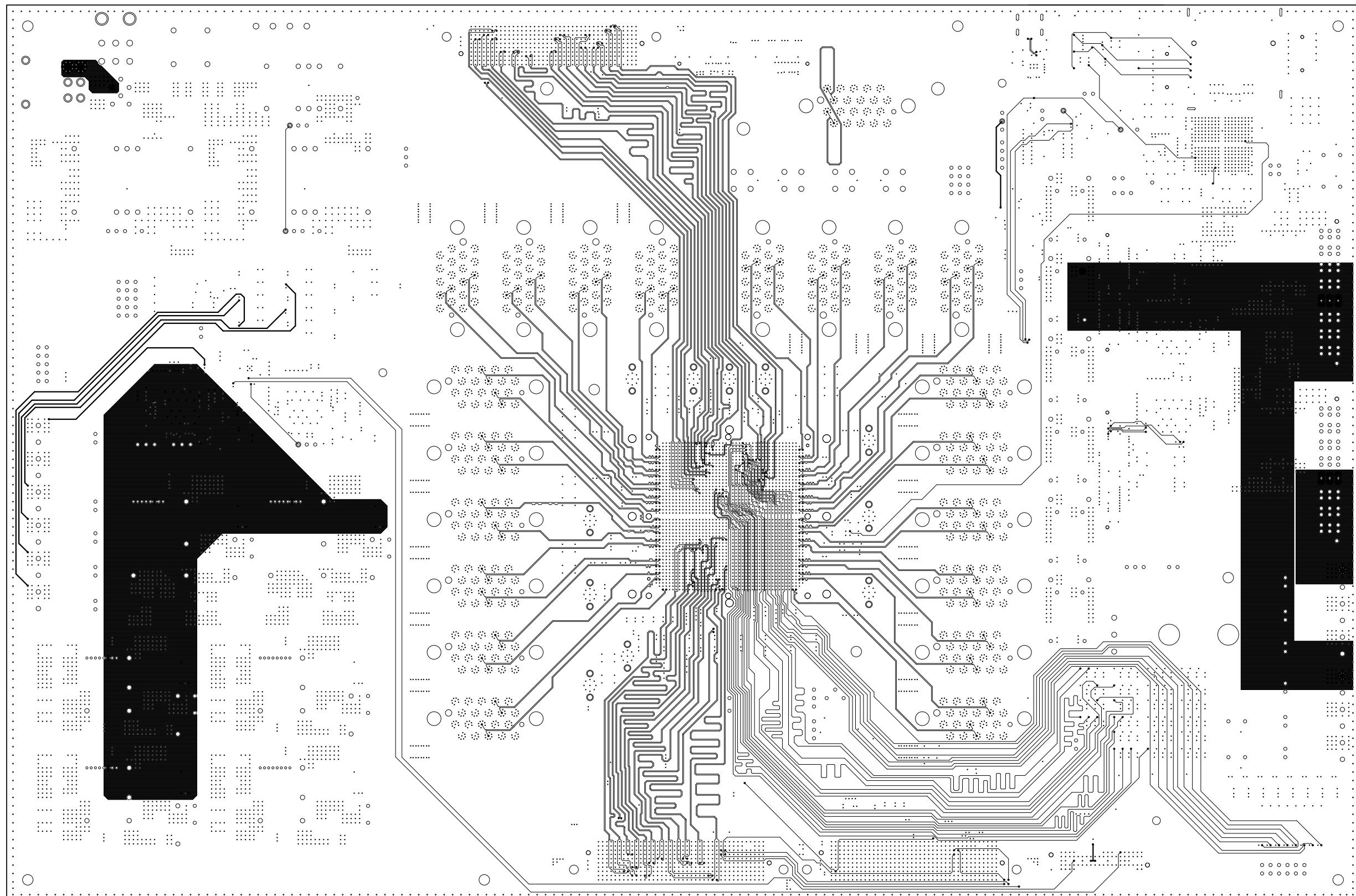


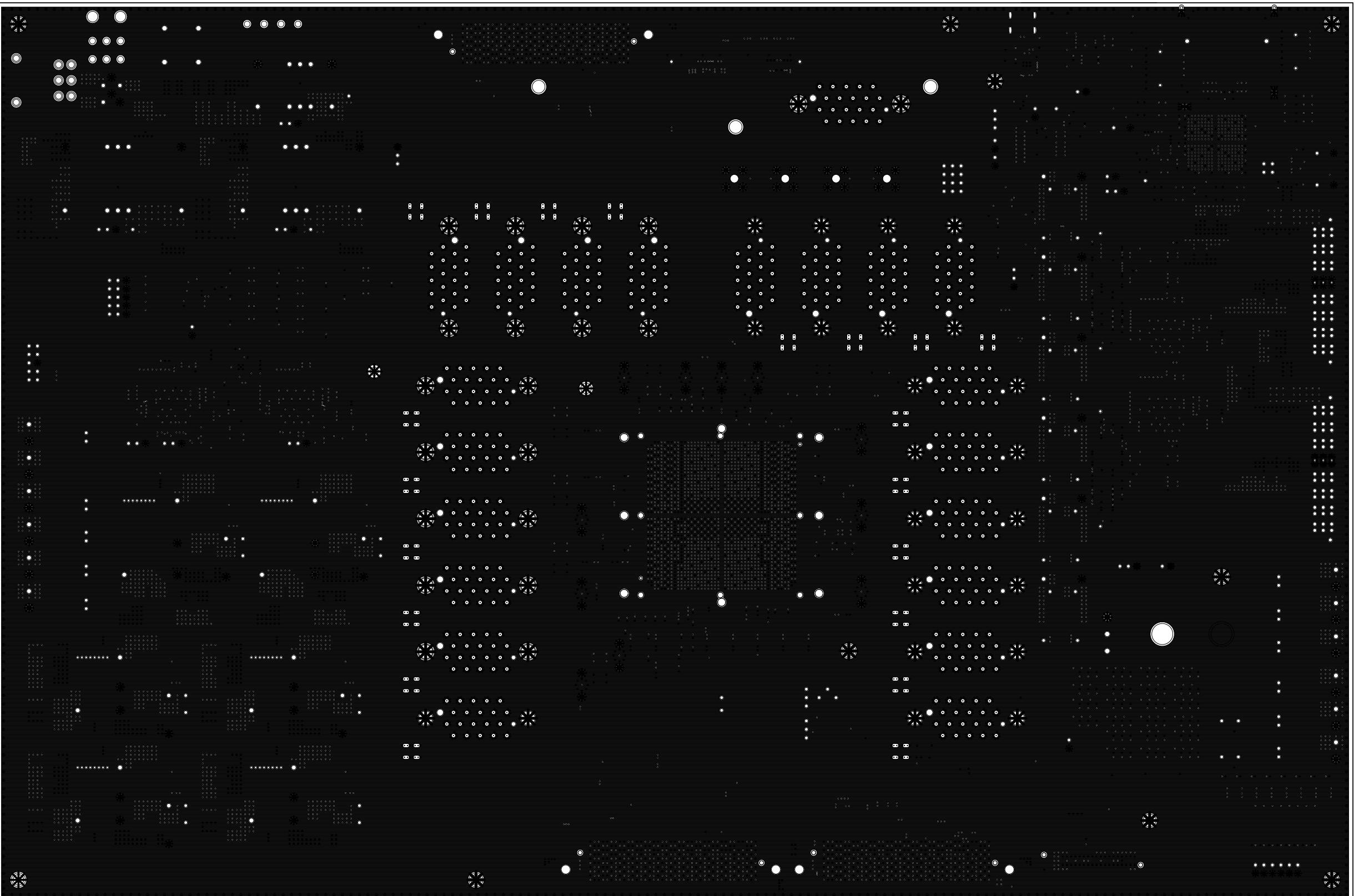
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L1_TOP
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 1 OF 28	XILINX DOC USE ONLY REVISION: 1.0



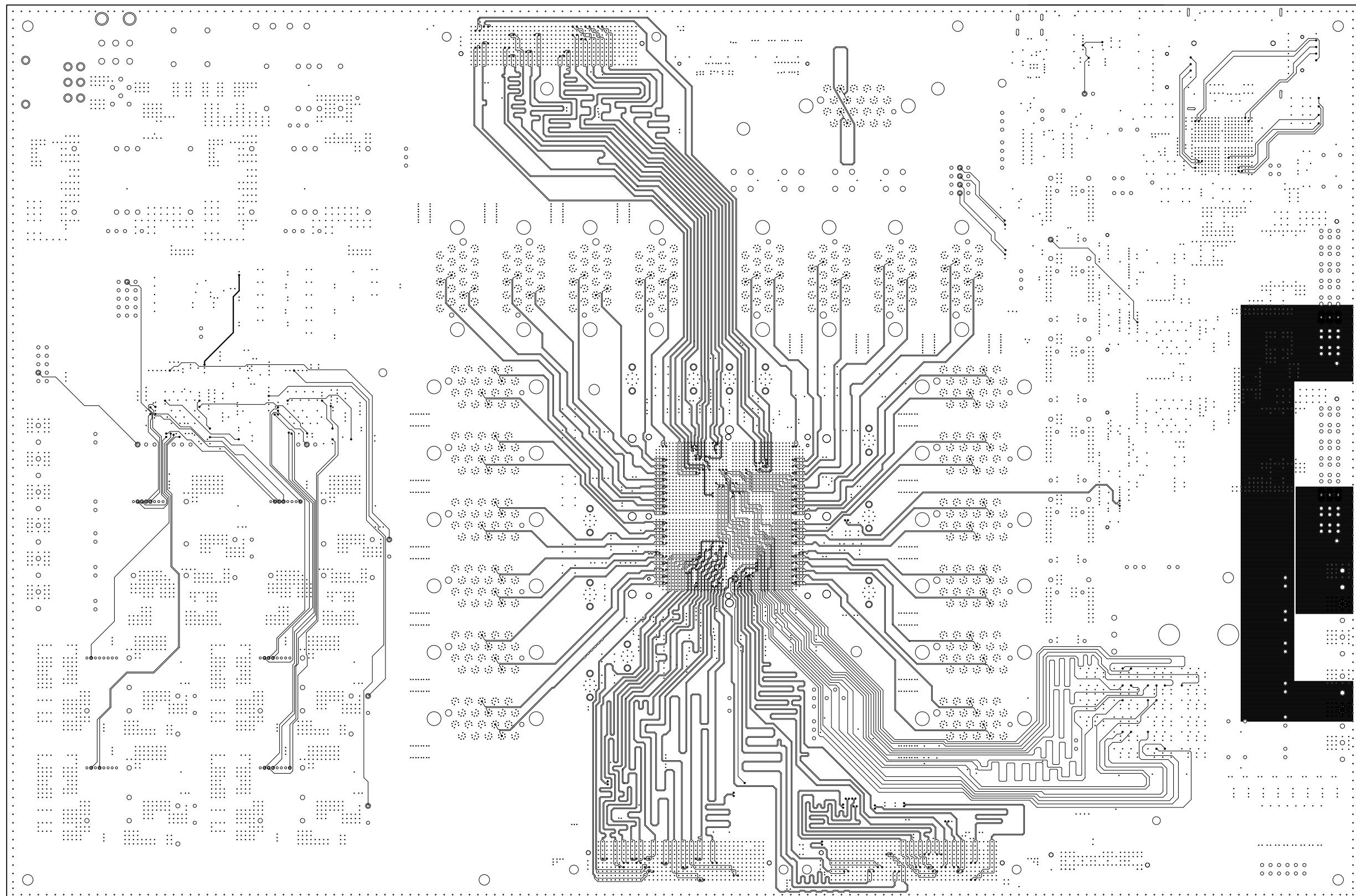
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L2_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 2 OF 28	XILINK DOC USE ONLY REVISION: 1.0



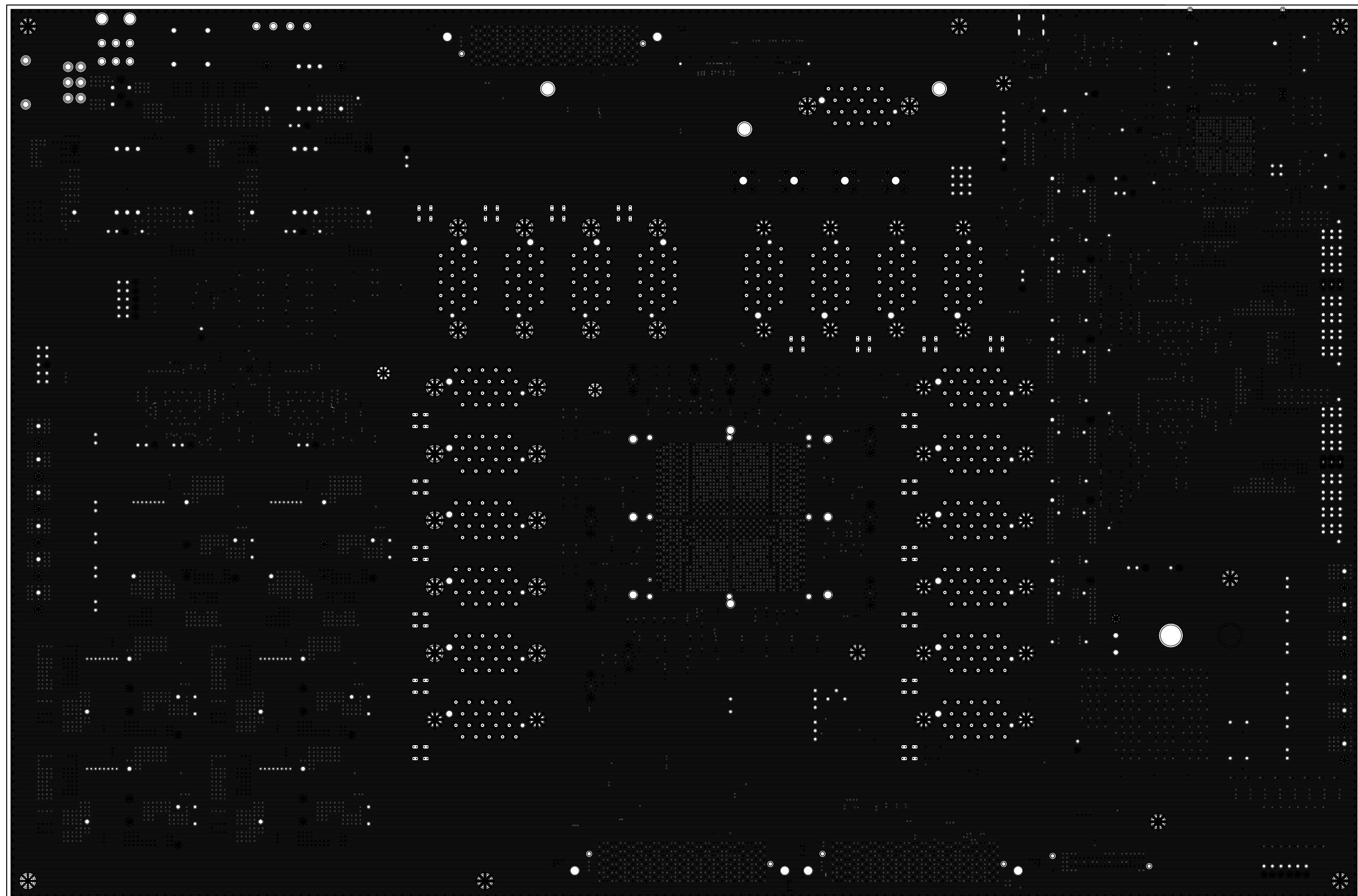
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L3_INNER
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 3 OF 28	XILINK DOC USE ONLY REVISION: 1.0



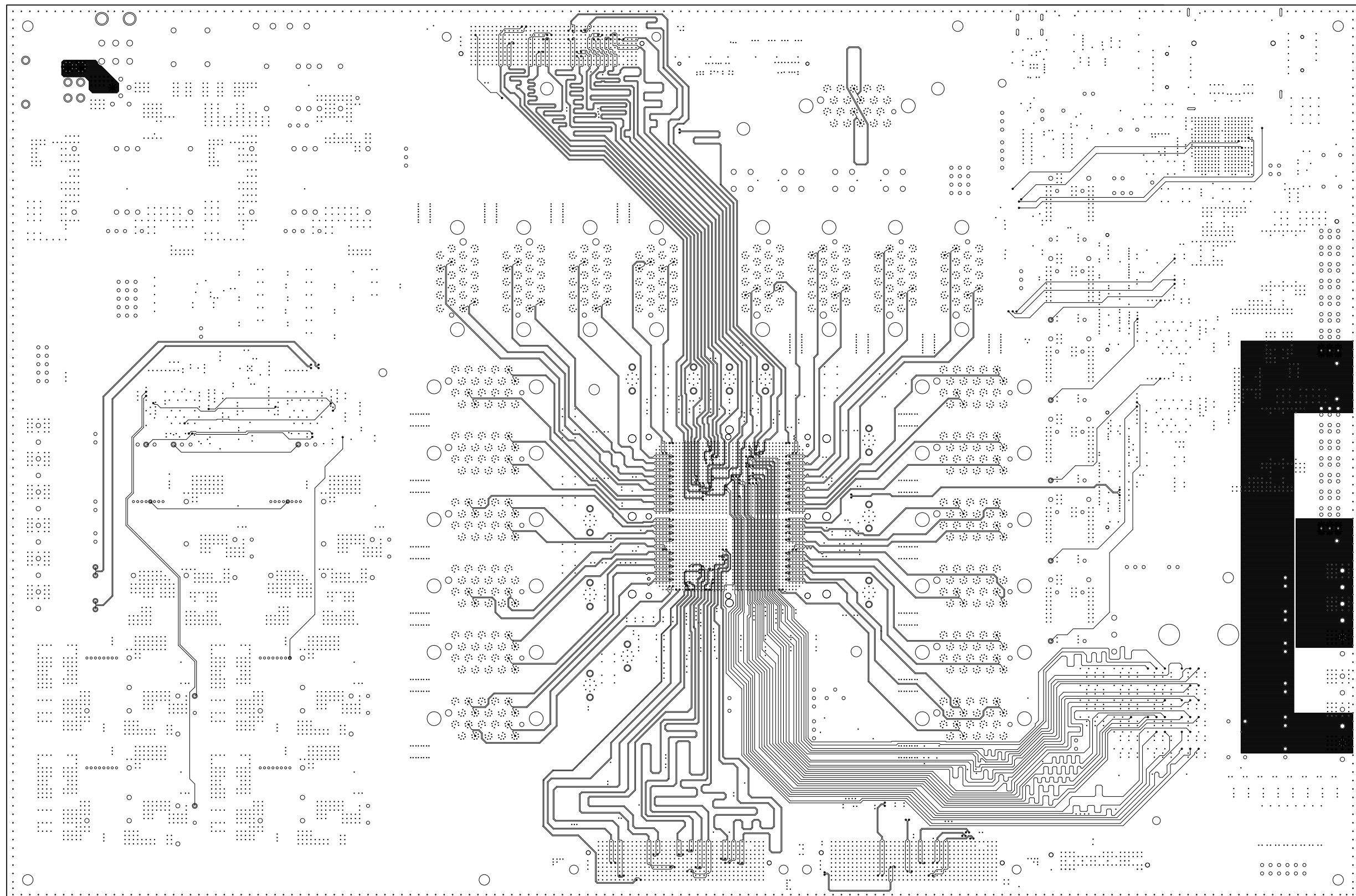
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L4_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 4 OF 28	XILINK DOC USE ONLY REVISION: 1.0



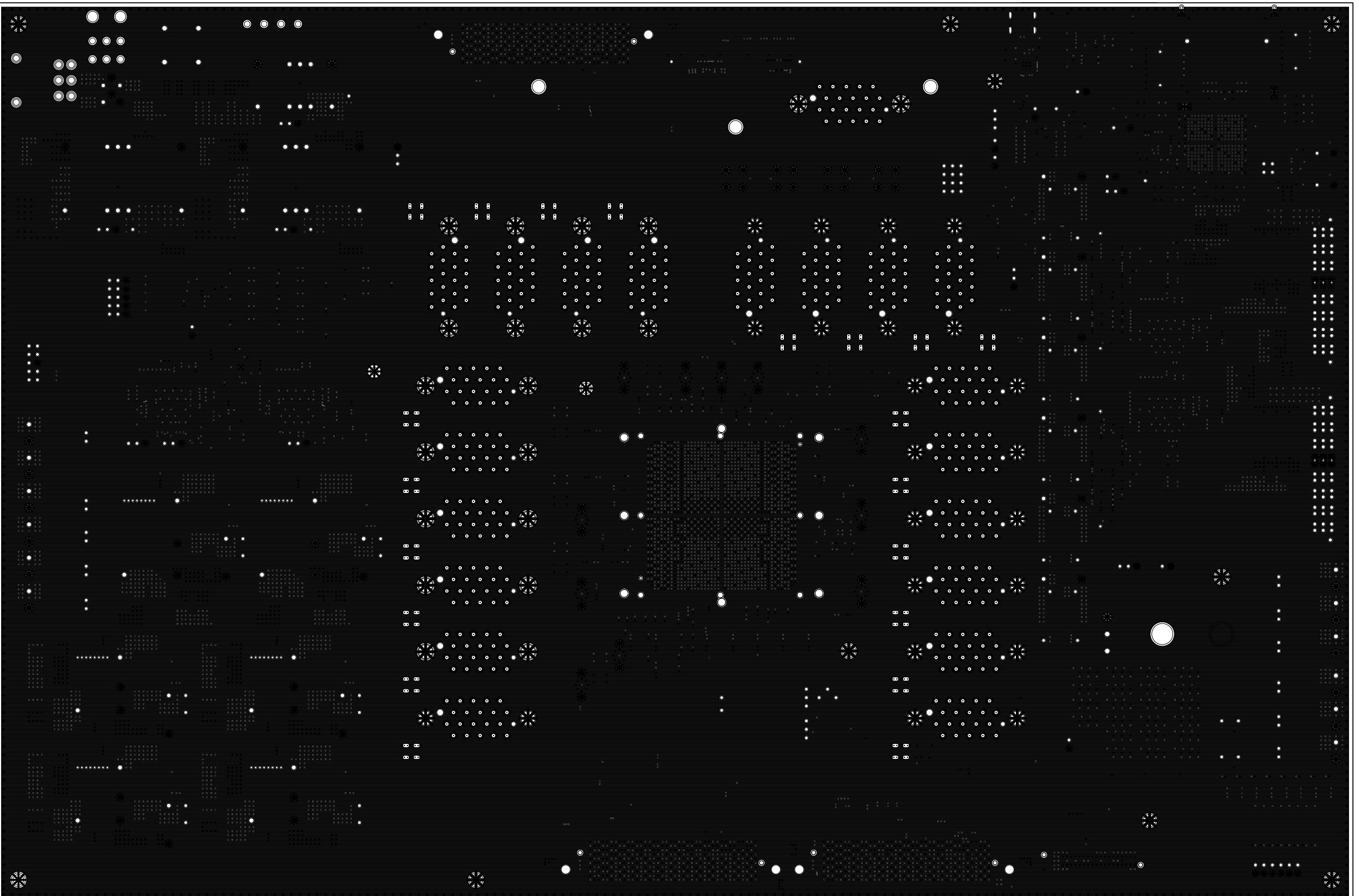
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L5_INNER
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 5 OF 28	XILINK DOC USE ONLY REVISION: 1.0



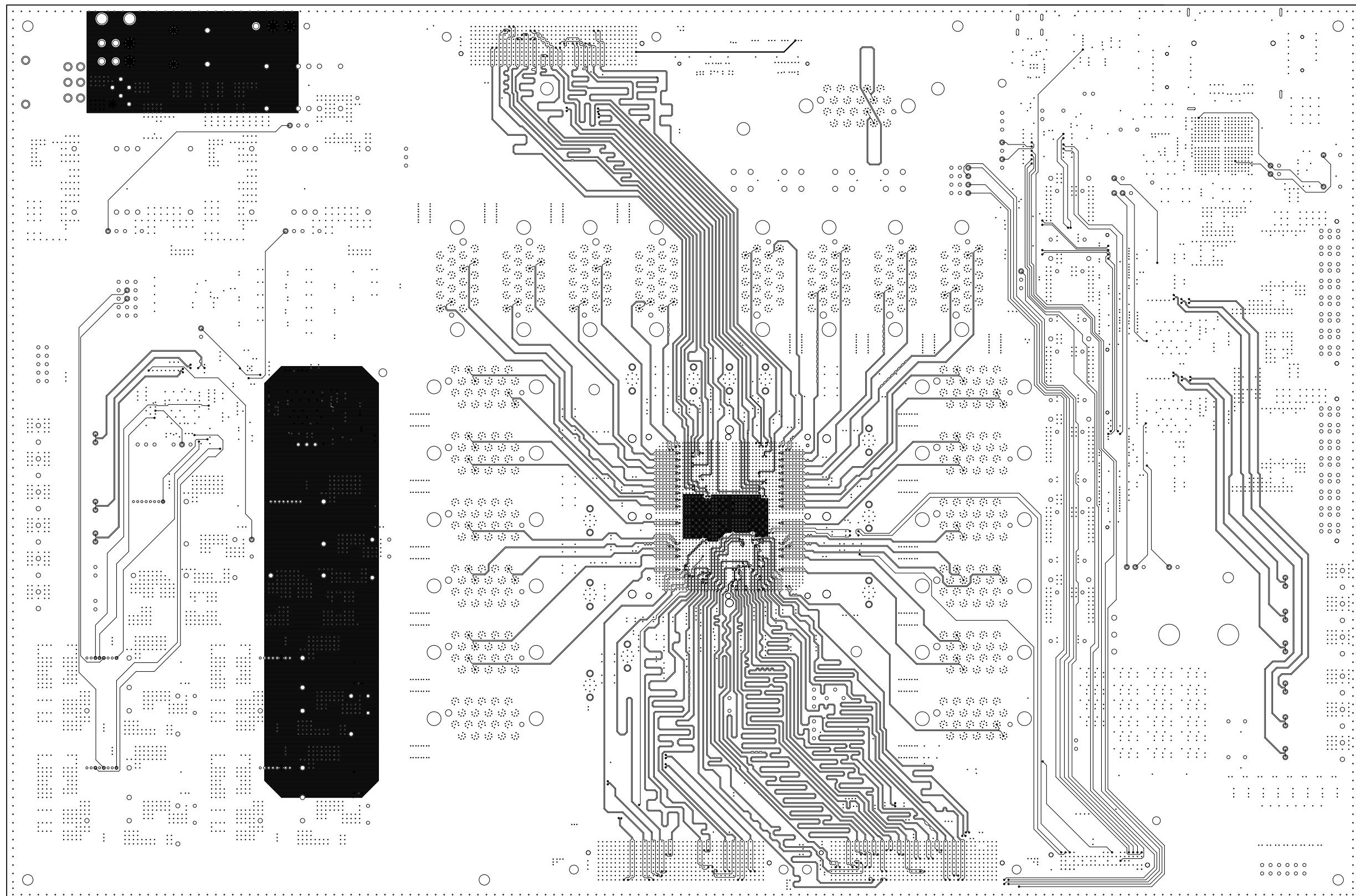
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L6_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 6 OF 28	XILINK DOC USE ONLY REVISION: 1.0



ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L7_INNER
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 7 OF 28	XILINK DOC USE ONLY REVISION: 1.0



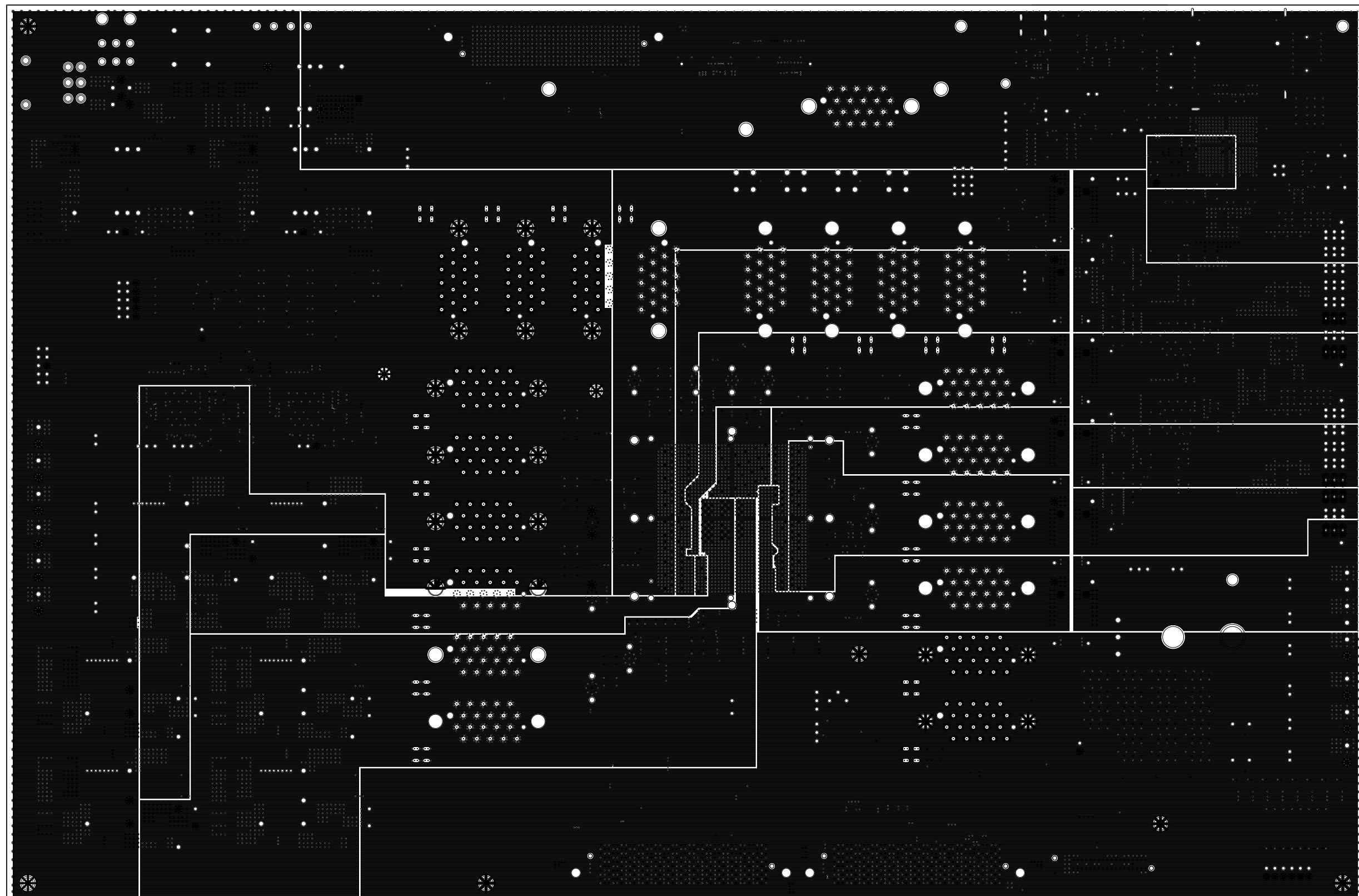
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L8_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 8 OF 28	XILINK DOC USE ONLY REVISION: 1.0



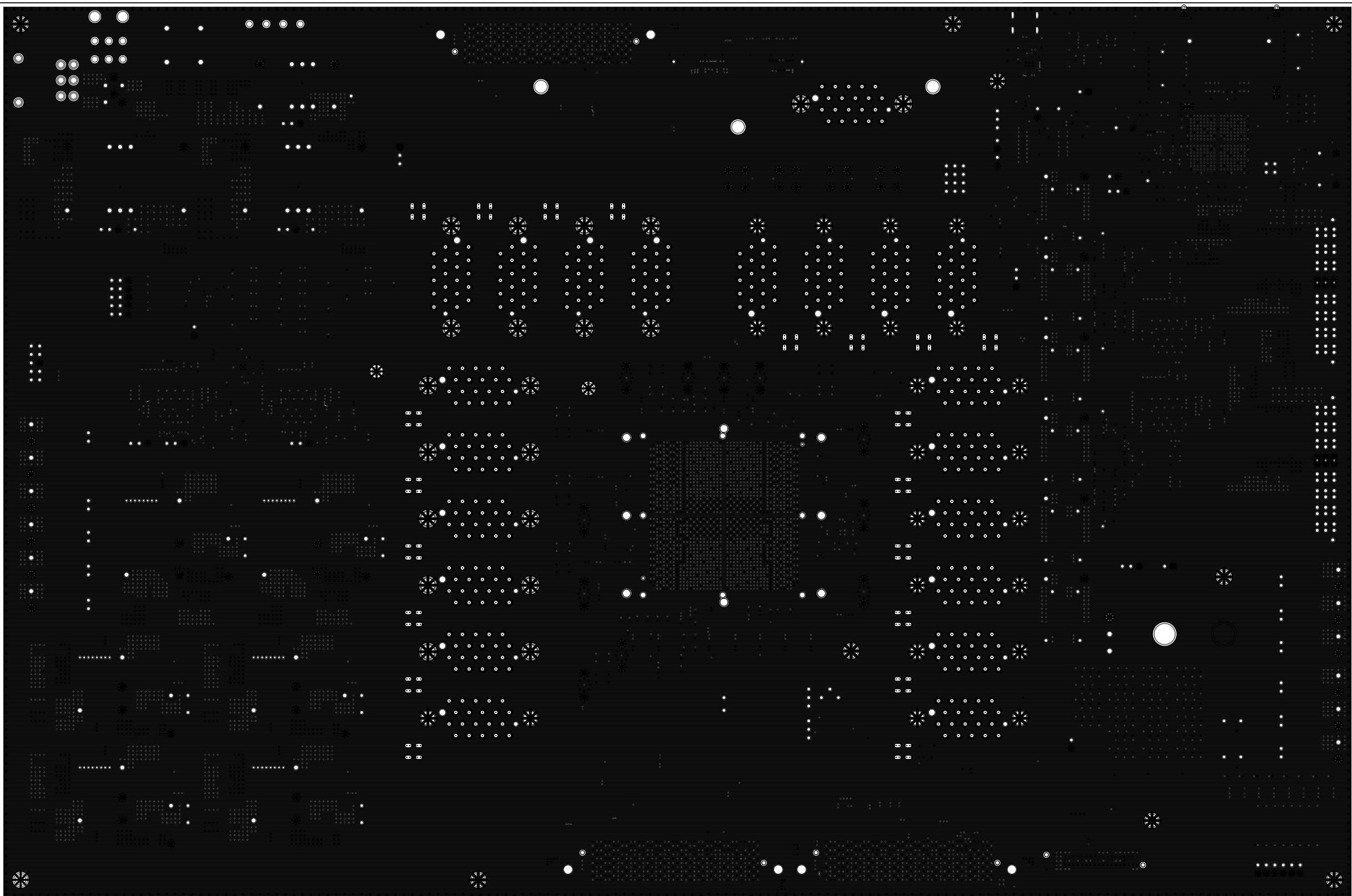
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L9_PWR
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 9 OF 28	XILINX DOC USE ONLY REVISION: 1.0



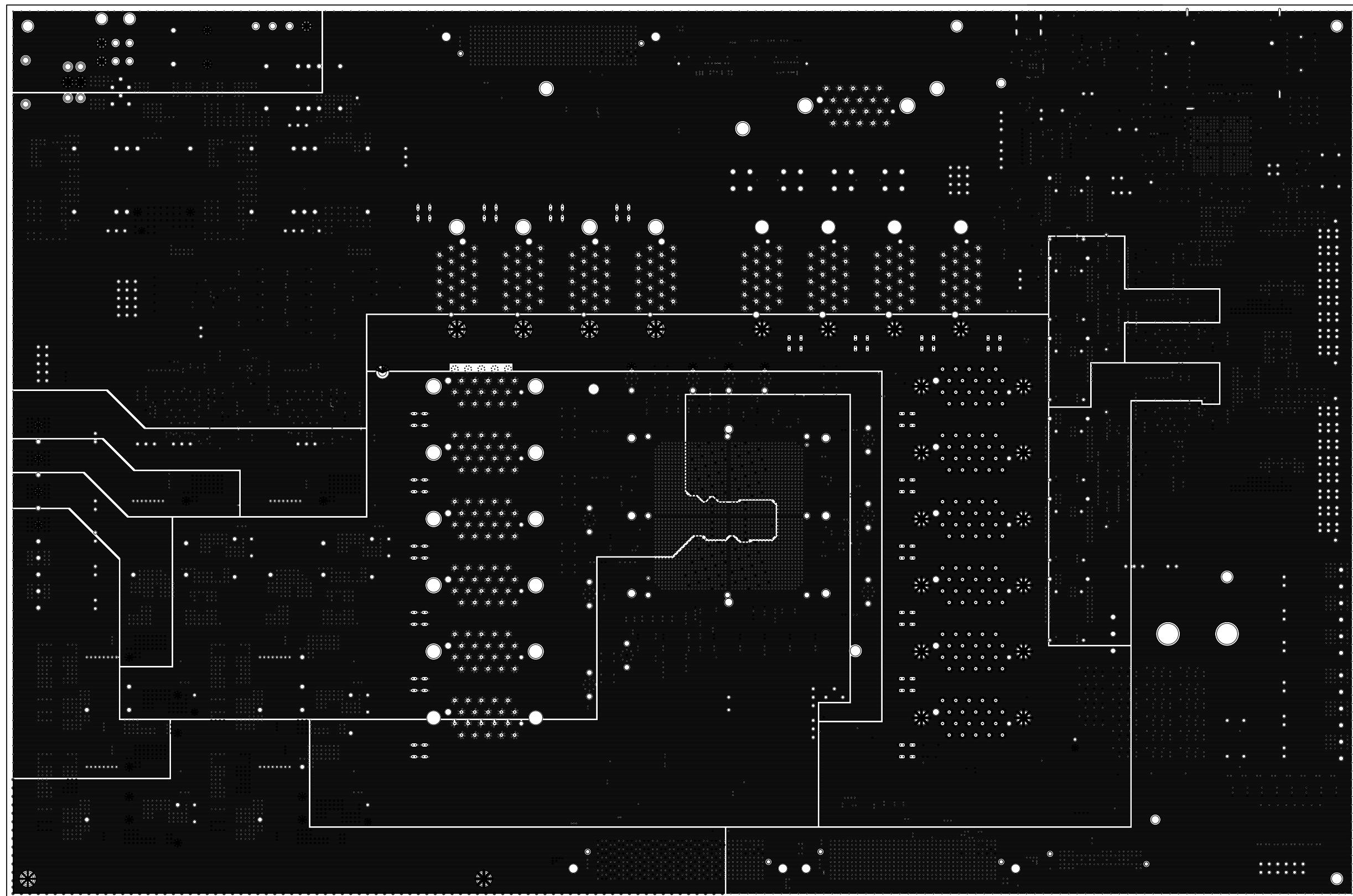
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L10_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 10 OF 28	XILINK DOC USE ONLY REVISION: 1.0



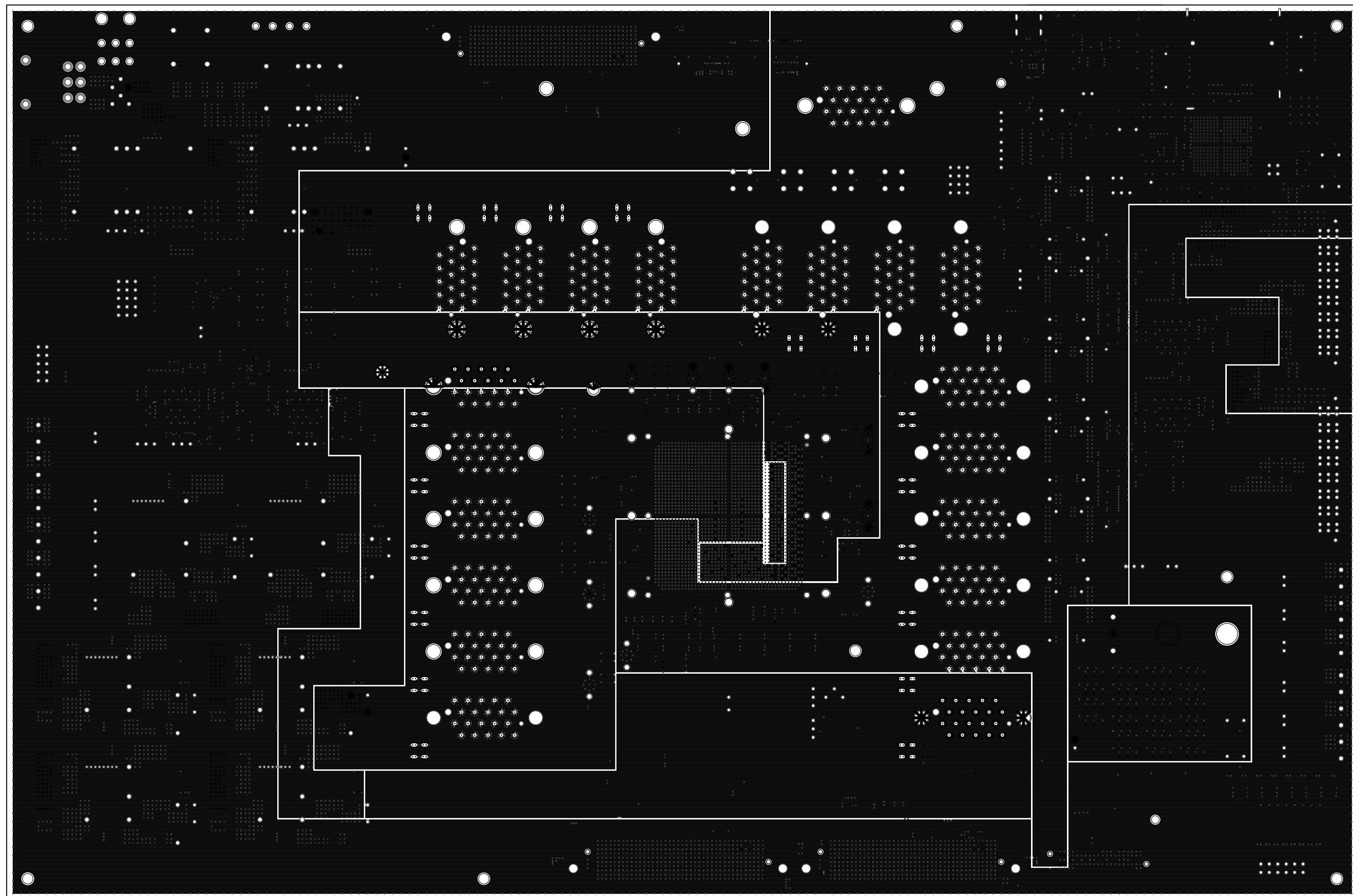
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L11_PWR
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 11 OF 28	XILINK DOC USE ONLY REVISION: 1.0



ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L12_PWR
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 12 OF 28	XILINK DOC USE ONLY REVISION: 1.0



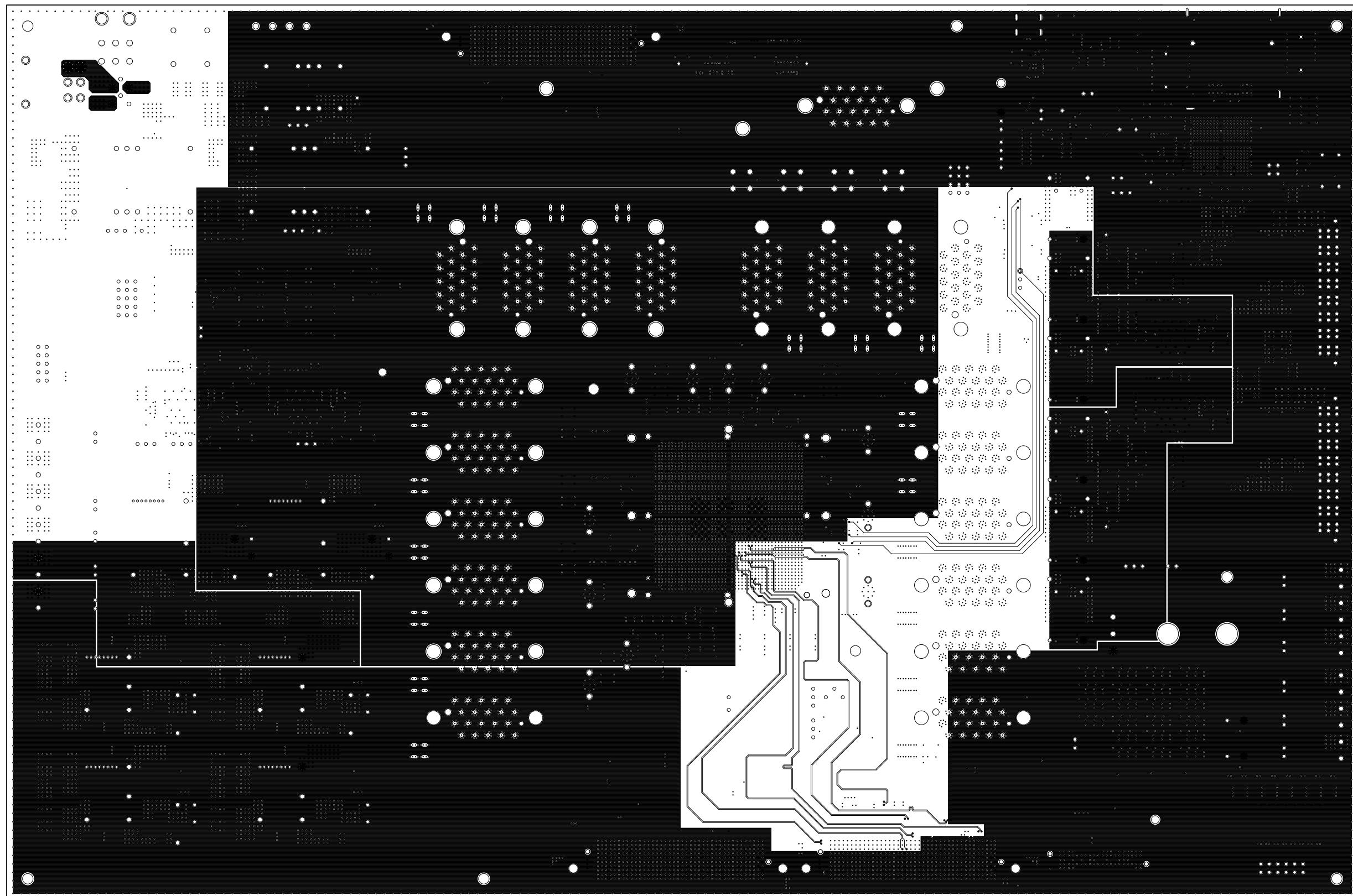
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L13_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 13 OF 28	XILINK DOC USE ONLY REVISION: 1.0



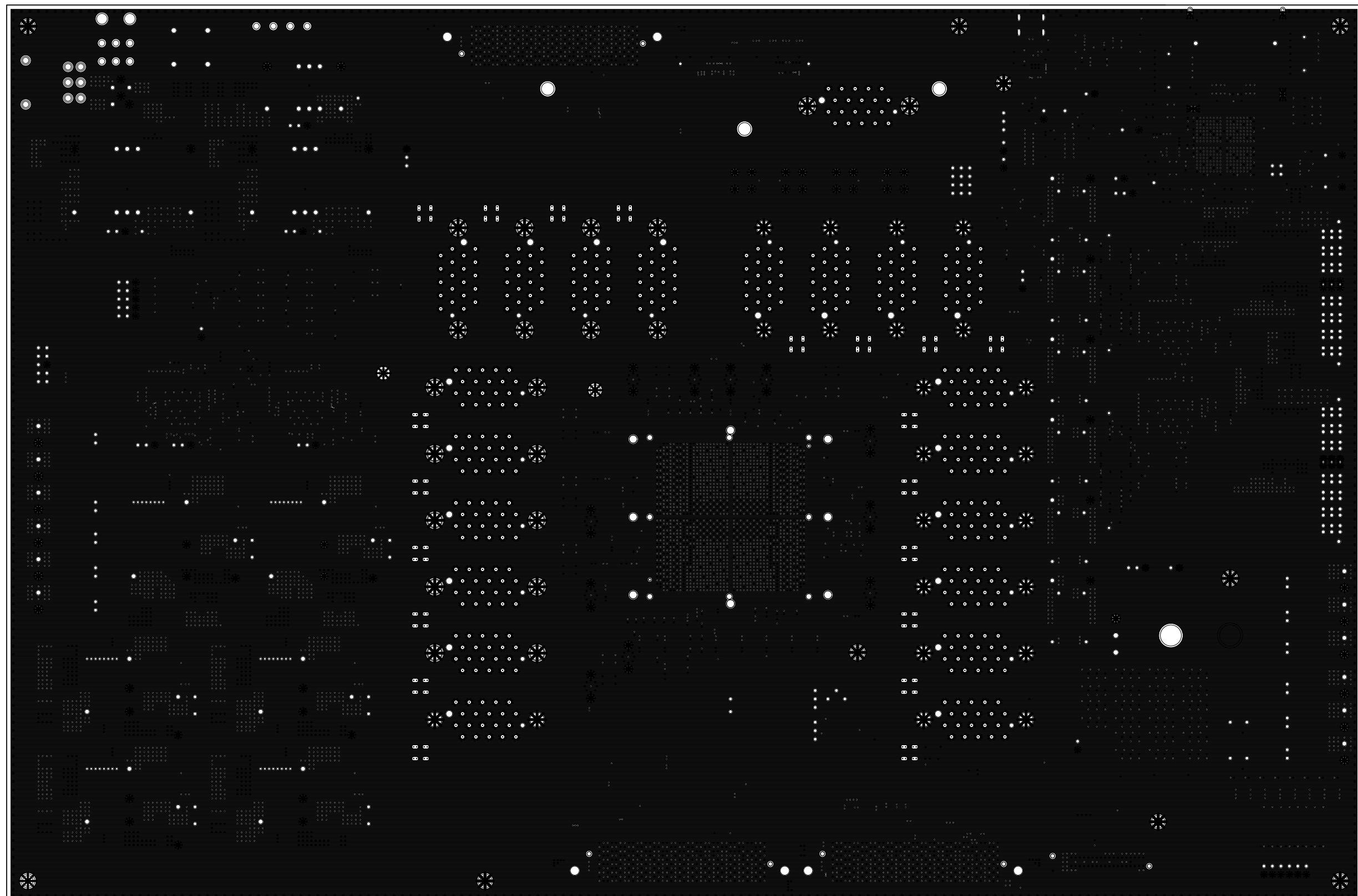
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L14_PWR
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 14 OF 28	XILINK DOC USE ONLY REVISION: 1.0



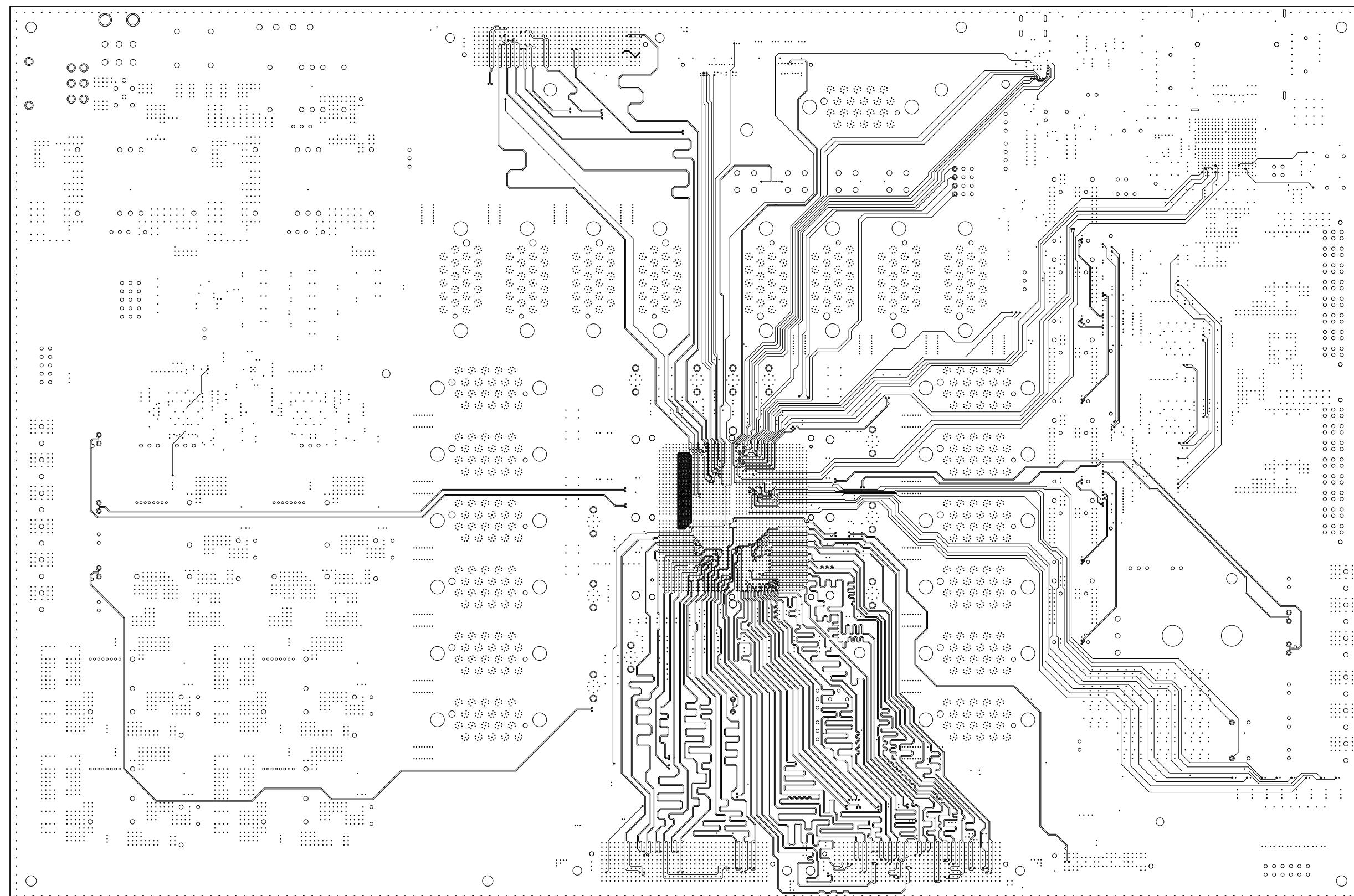
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L15_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 15 OF 28	XILINK DOC USE ONLY REVISION: 1.0



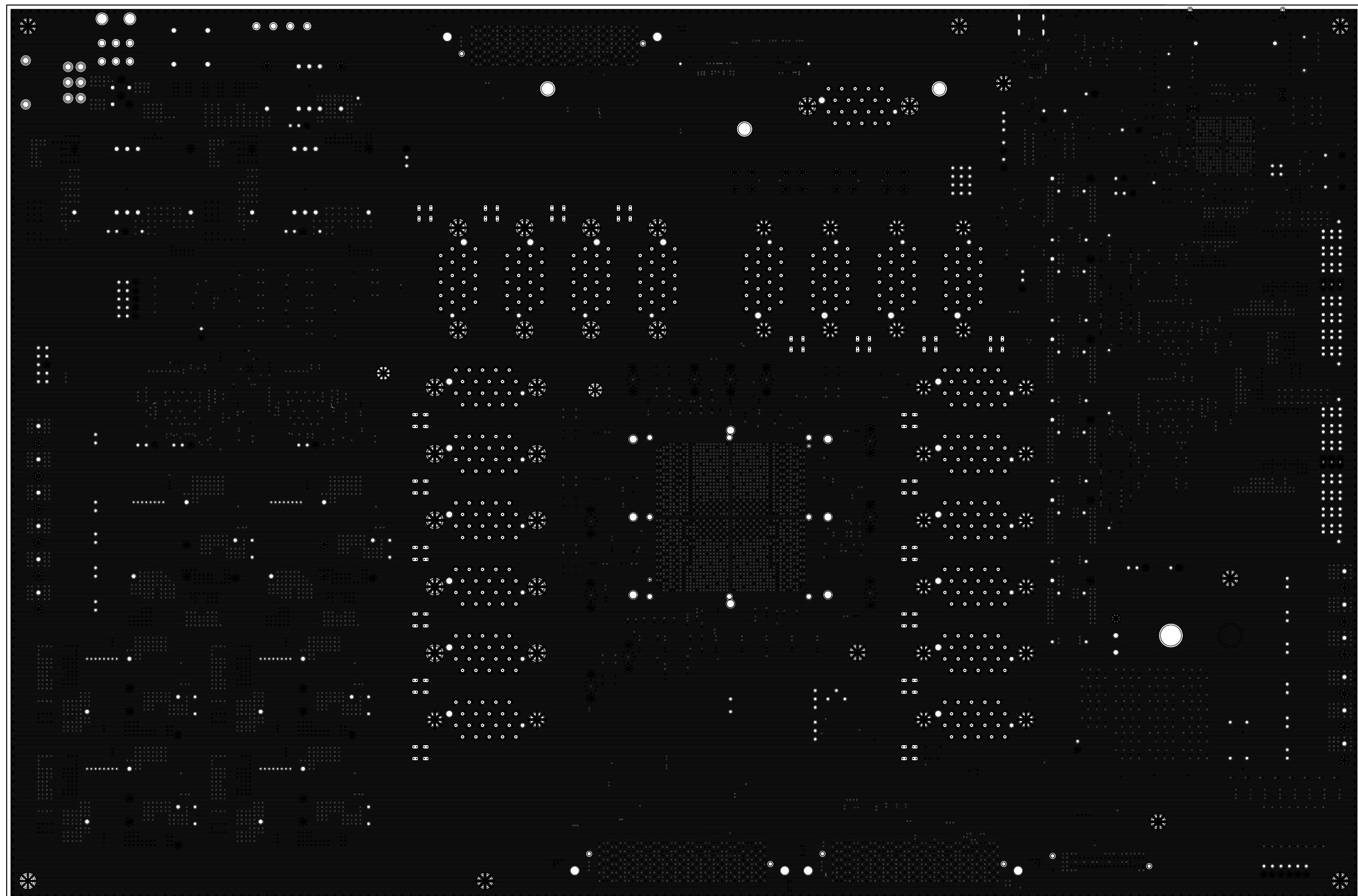
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L16_SIG
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 16 OF 28	XILINK DOC USE ONLY REVISION: 1.0



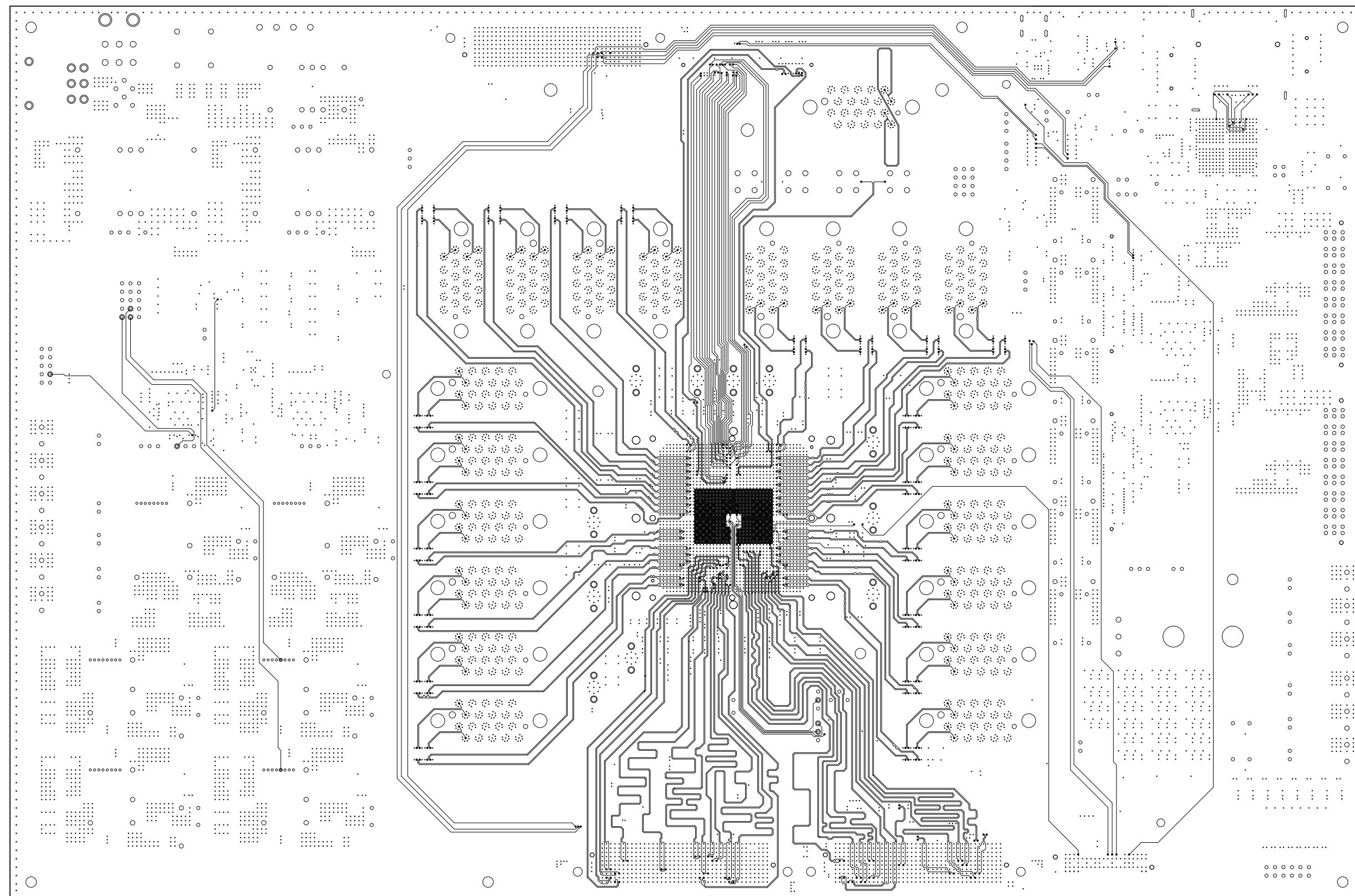
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L17_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 17 OF 28	XILINK DOC USE ONLY REVISION: 1.0



ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L18_INNER
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 18 OF 28	XILINK DOC USE ONLY REVISION: 1.0



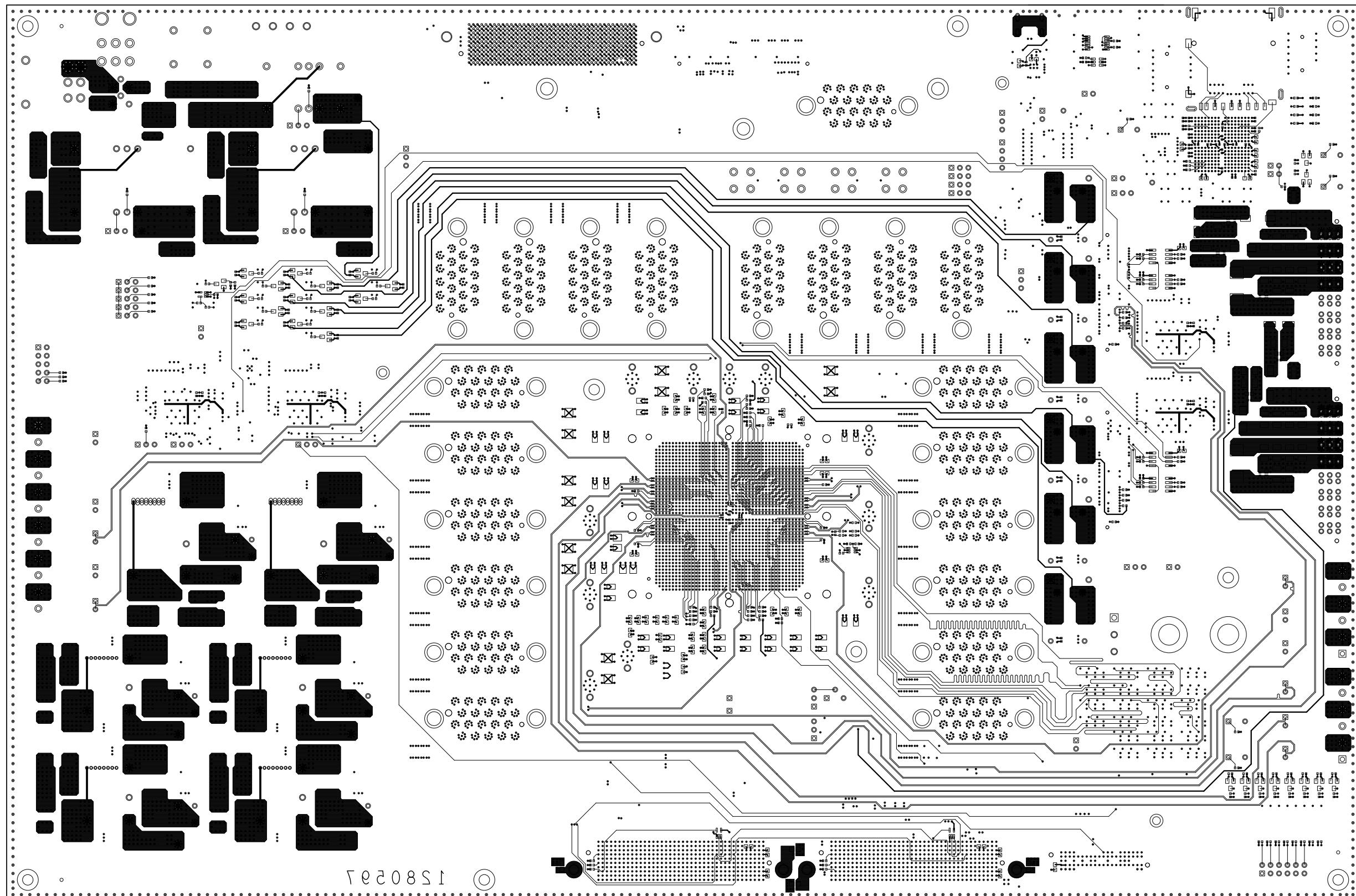
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L19_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 19 OF 28	XILINK DOC USE ONLY REVISION: 1.0



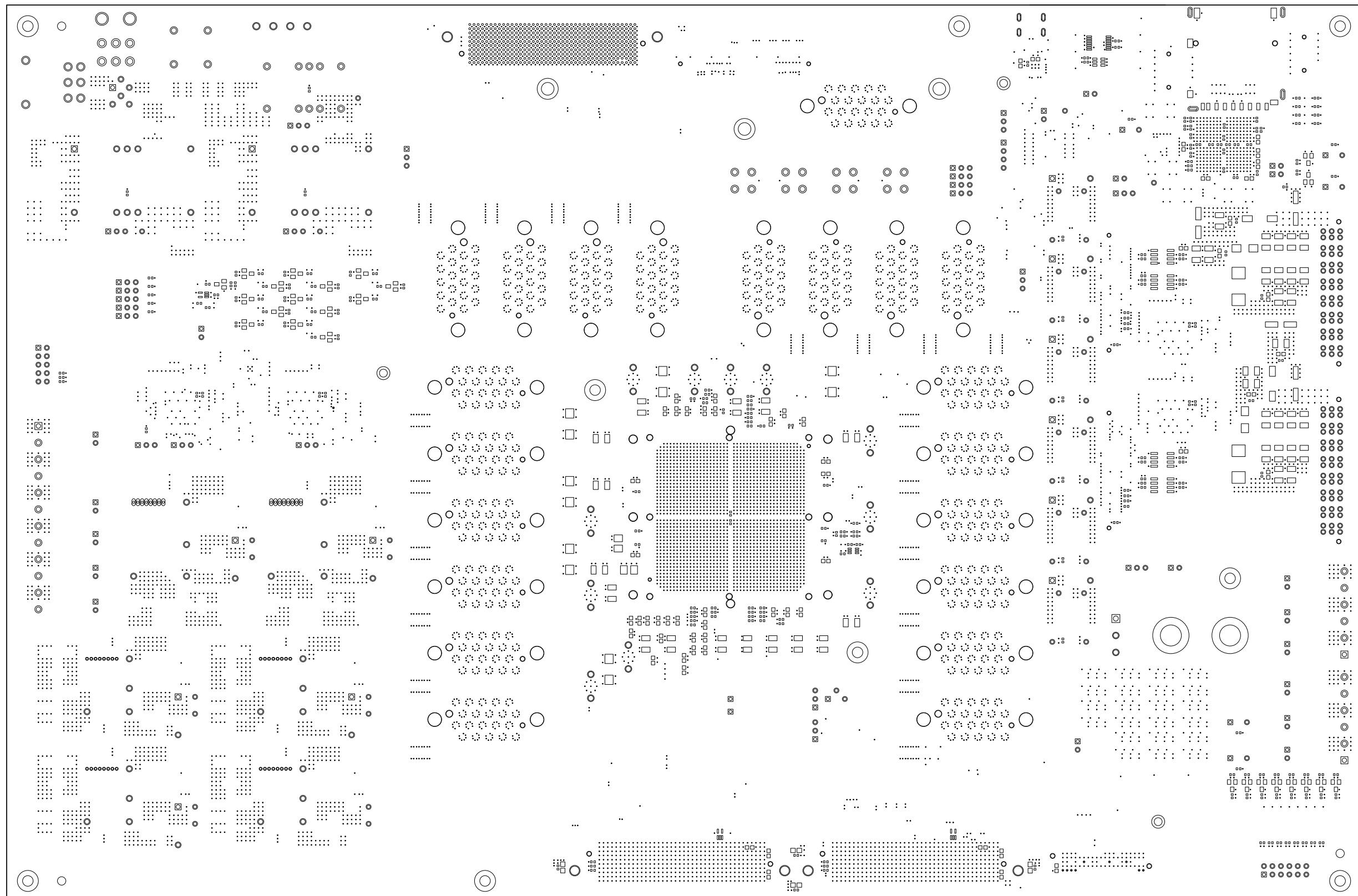
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L20_INNER
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 20 OF 28	XILINK DOC USE ONLY REVISION: 1.0



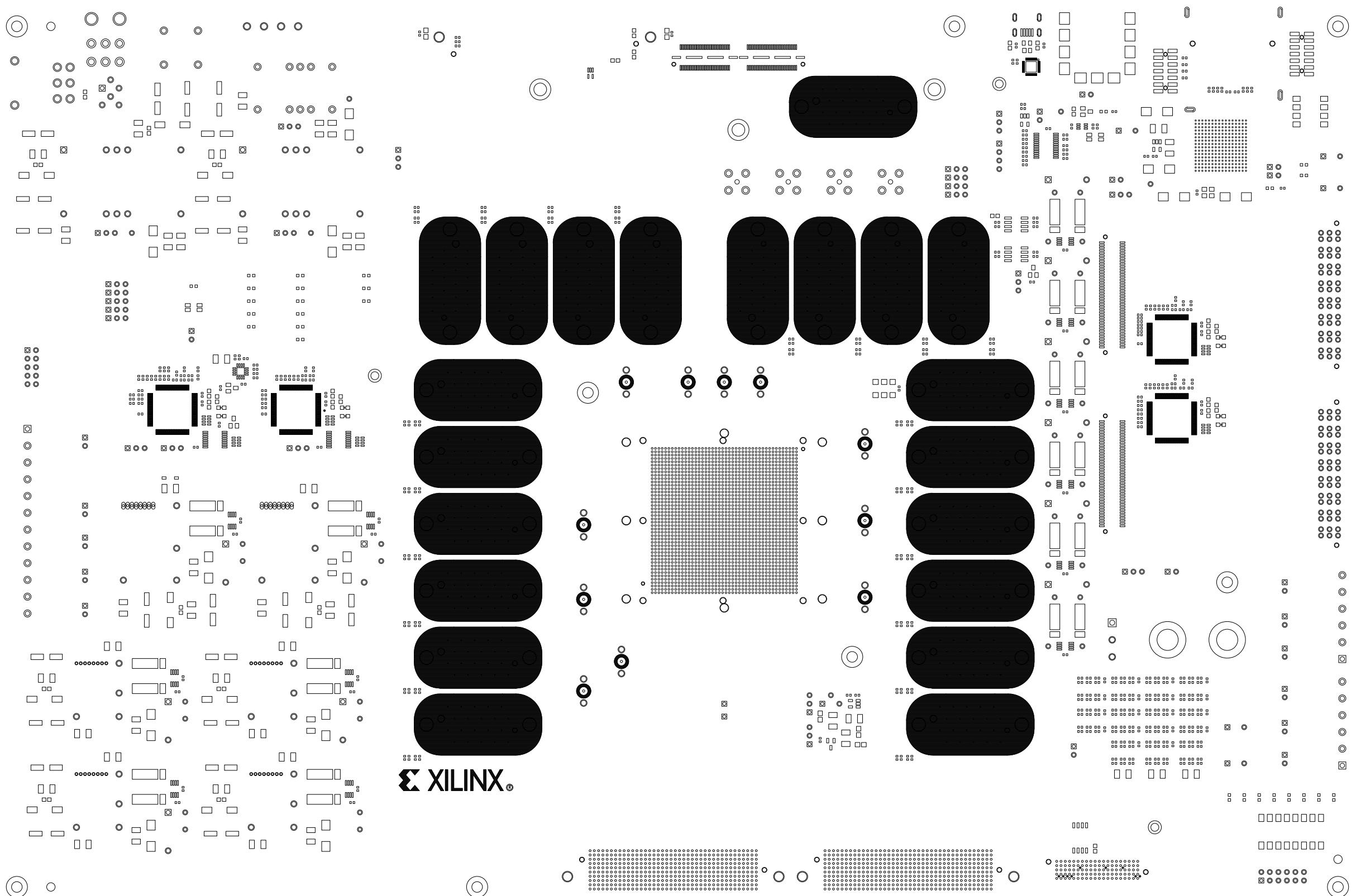
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PCB # 1280597	LAYER: L21_GND
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 21 OF 28	XILINK DOC USE ONLY REVISION: 1.0



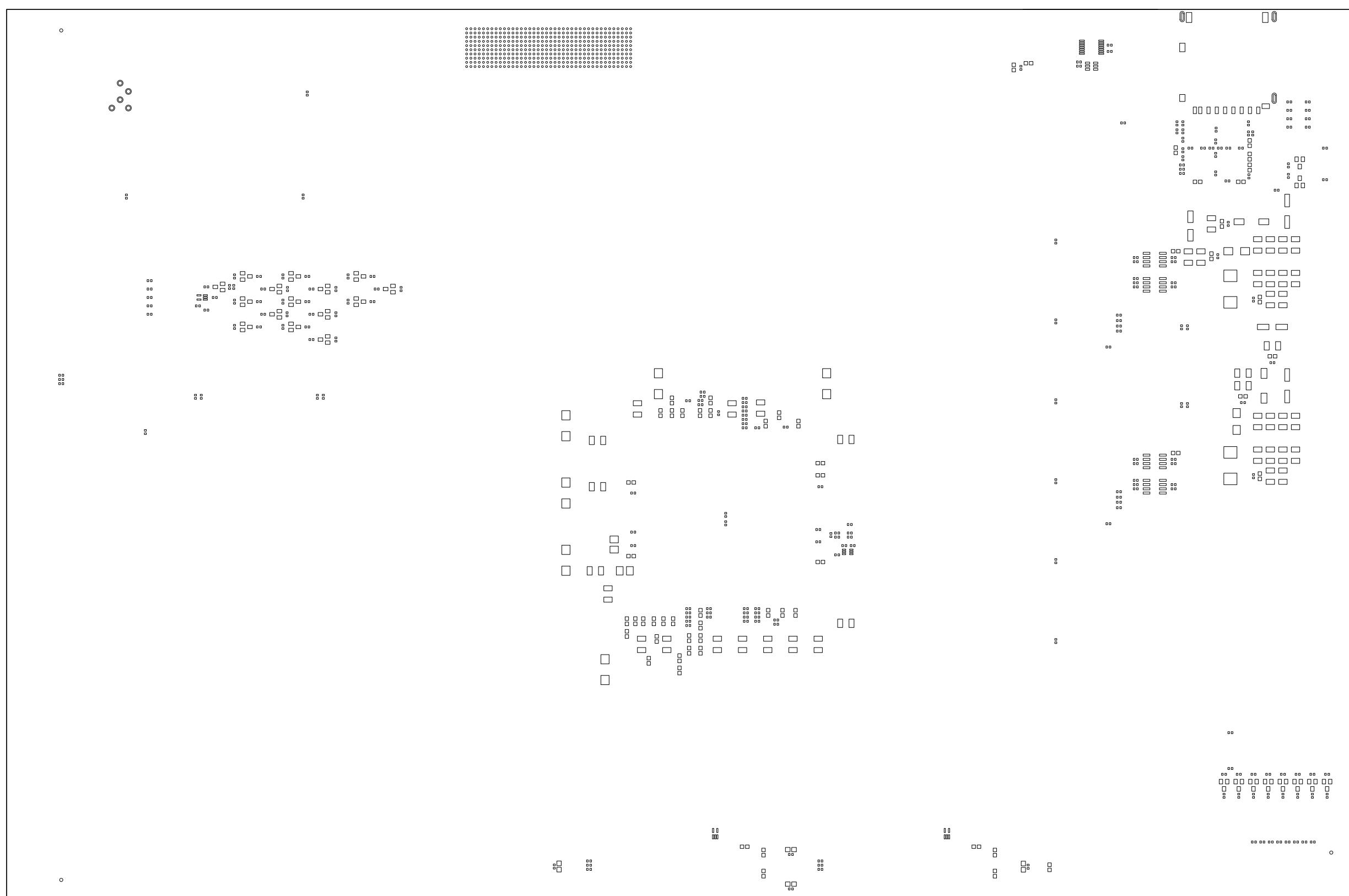
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: L22_BOTTOM
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 22 OF 28	XILINX DOC USE ONLY REVISION: 1.0



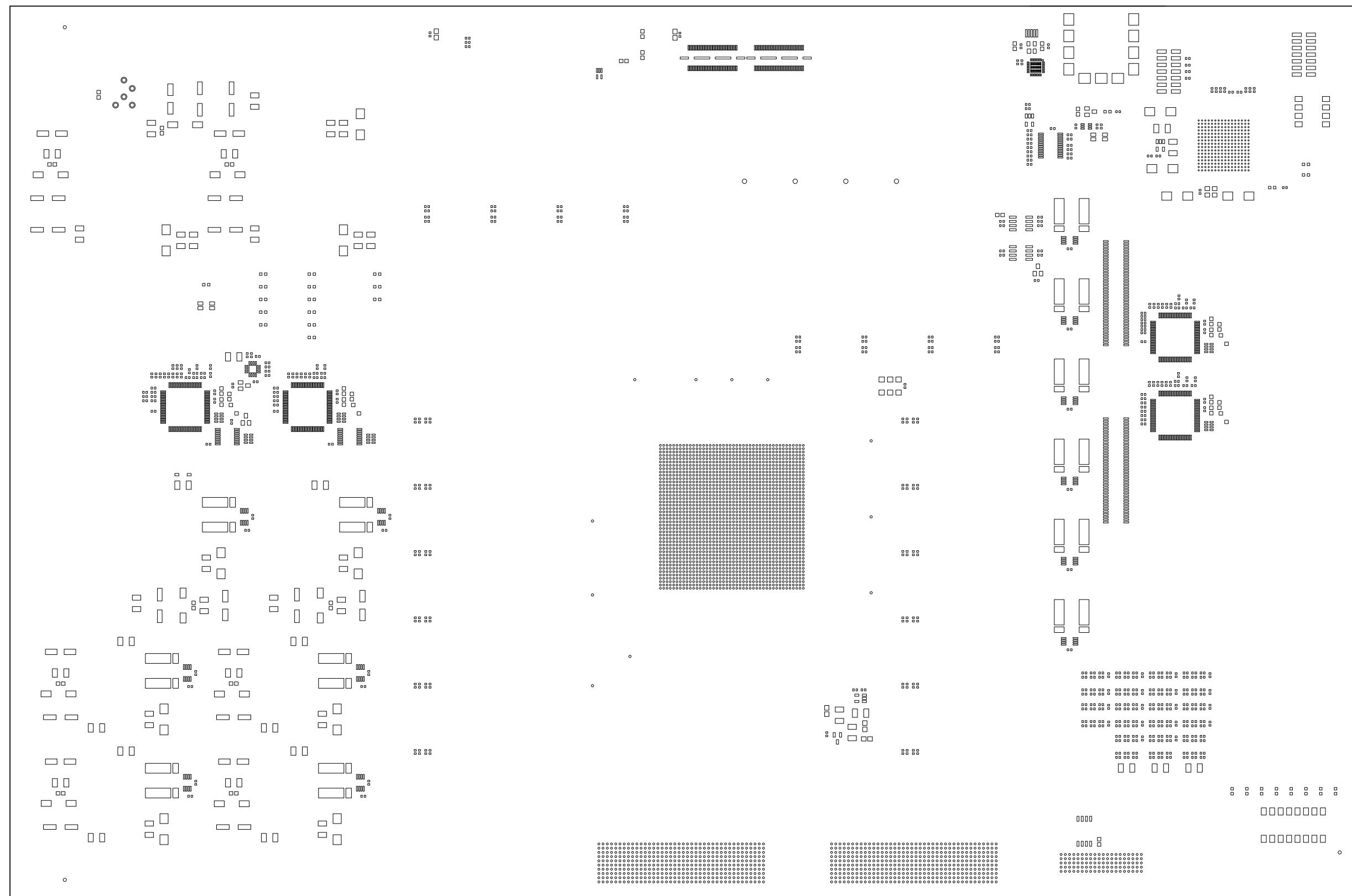
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: MASK_BOTTOM
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 23 OF 28	XILINK DOC USE ONLY REVISION: 1.0



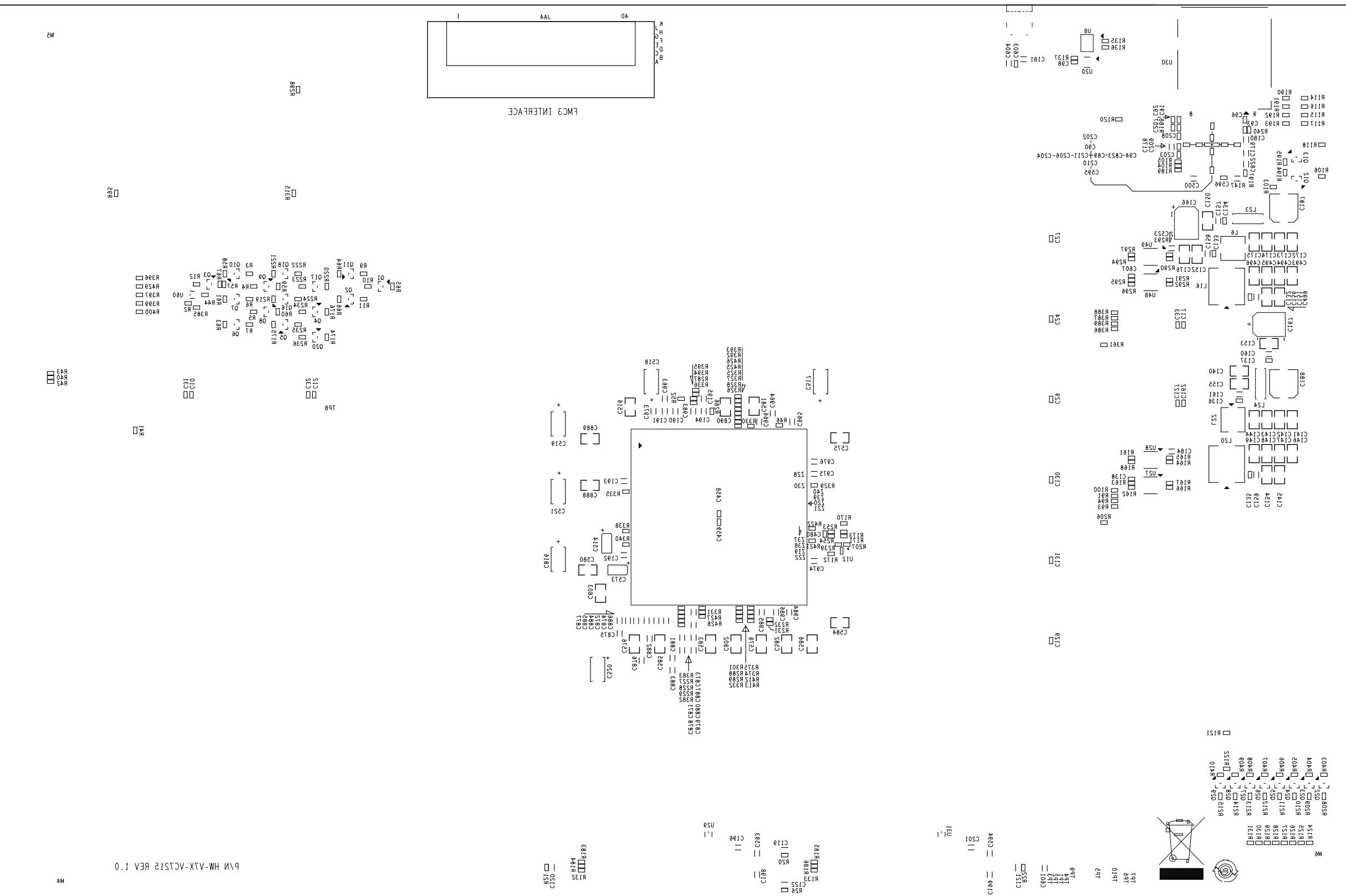
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: MASK_TOP
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 24 OF 28	XILINX DOC USE ONLY REVISION: 1.0



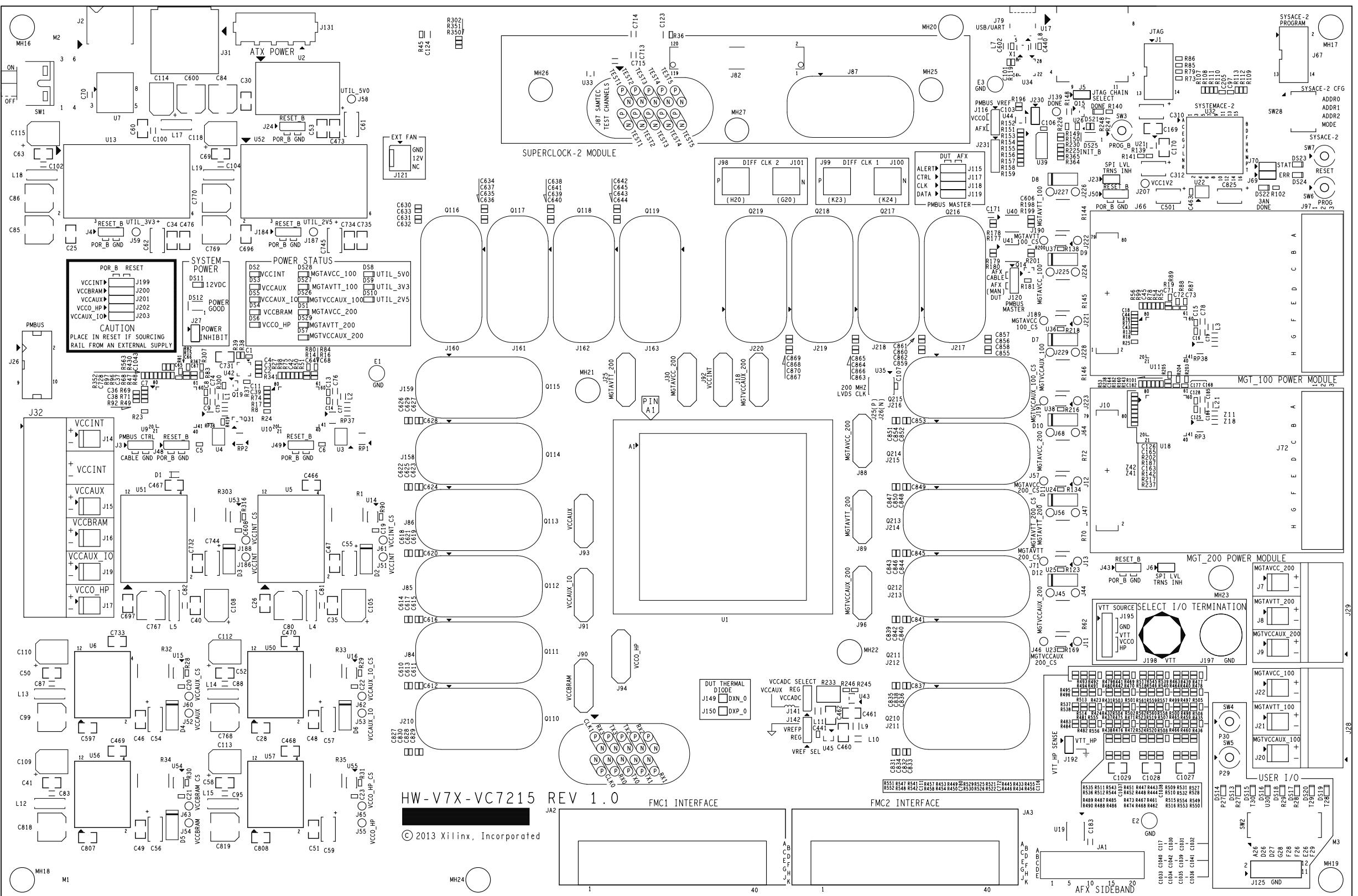
ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: PASTE_BOT
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 25 OF 28	XILINX DOC USE ONLY REVISION: 1.0



ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: PASTE_TOP
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 26 OF 28	XILINK DOC USE ONLY REVISION: 1.0



ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB # 1280597	LAYER: SILK_BOT
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
	XILINX DOC USE ONLY
	REVISION: 1.0
SHEET 27 OF 28	



ARTWORK, ROHS COMPLIANT, HW-V7X-VC7215	
PCB #	1280597
Designed by Xilinx	DATE: 04-16-2013
BOARD designer: MN	PHONE: 408-879-4872
SHEET 28 OF 28	XILINX DOC USE ONLY REVISION: 1.0