Product Preview
TI DN 2509930 Rev A
June 2008

DLP® Discovery™ .55 XGA 2xLVDS 12^{o} Type X DMD

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Table 1. Revision History			
Rev	Date	Section	Summary Of Changes
A	xx/xx/2006	All	Initial Release

Table 2. Product Description		
DMD Part #	Mechanical ICD	Description
*1076N631cW	2507499	0.55 inch diagonal spatial light modulator of aluminum micro-mirrors. Pixel array size is (1024 x 768) in a Square Grid Pixel Arrangement. Low Voltage Differential Signaling (LVDS) data interface, Double Data Rate (DDR). Pixel Architecture is SPD with DarkChip2™.

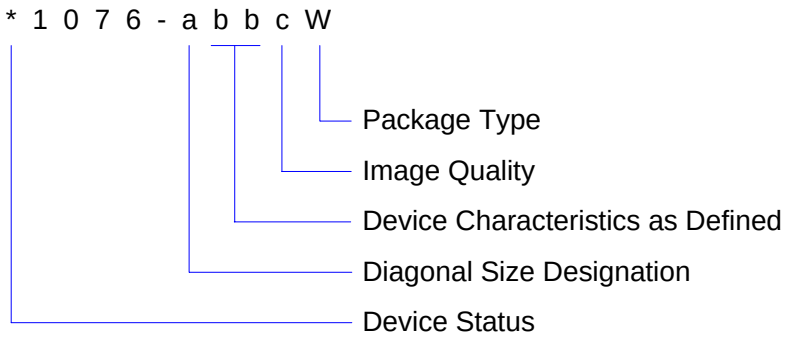

Figure 1. Part Number Description

Device Status:

A lead alpha character of “X” implies the device has been released for restricted sales only.
When no lead alpha character (*) is present, the device has been released for unrestricted sales.

Table 3. Pin Descriptions		
Pin Name	Description	Type
D_AN(15:0) D_AP(15:0)	• LVDS pair for Data Bus A (15:0)	I
D_BN(15:0) D_BP(15:0)	• LVDS pair for Data Bus B (15:0)	I
DCLK_AN DCLK_AP	• LVDS pair for Data Clock A	I
DCLK_BN DCLK_BP	• LVDS pair for Data Clock B	I
SCTRL_AN SCTRL_AP	• LVDS pair for Serial Control (Sync) A	I
SCTRL_BN SCTRL_BP	• LVDS pair for Serial Control (Sync) B	I
MBRST(15:0)	• Non-logic compatible Mirror Bias Reset signals • Connected directly to the array of pixel mirrors • Used to hold or release the mirrors • Bond Pads connect to an internal pull-down resistor	I
MODE_A	• Data Bandwidth Mode Select • Bond Pad connects to an internal pull-down circuit • Refer to for DLP® system board connection information	I
MODE_B	• Data Bandwidth Mode Select • Bond Pad connects to an internal pull-down circuit • Refer to for DLP® system board connection information	I
PWRDNZ	• Active Low Device Reset • Bond Pad connects to an internal pull-down circuit	I
SCPCLK	• Serial Communications Port Clock Input • Bond Pad connects to an internal pull-down circuit	I
SCPDI	• Serial Communications Port Data Input • Synchronous to the rising-edge of SCPCLK • Bond Pad connects to an internal pull-down circuit	I
SCPENZ	• Serial Communications Port Active Low Enable • Synchronous to the rising-edge of SCPCLK • Bond Pad connects to an internal pull-down circuit	I
SCPDO	• Serial Communications Port Output	O
EVCC	• Do Not Connect on the DLP® system board	PWR
VCC (Note)	• Power supply for Low Voltage CMOS logic • Power supply for normal high voltage at mirror address electrodes	PWR
VCCI (Note)	• Power supply for Low Voltage CMOS LVDS interface	PWR
VCC2 (Note)	• Power supply for High Voltage CMOS logic • Power supply for stepped high voltage at mirror address electrodes	PWR
VSS (Note)	• Common return for all power	PWR

Note: VCC2, VCCI, VCC, and VSS power supplies are required for all DMD operating modes.

Table 4. Absolute Maximum Ratings Note 1				
Parameters		Min	Max	Units
LVCMOS Logic Supply voltage: VCC	Note 2	– 0.5	4	VDC
LVCMOS LVDS Interface Supply voltage: VCCI	Note 2	– 0.5	4	VDC
Supply Voltage Delta | VCCI – VCC |	Note 5		0.3	VDC
Mirror Electrode and HVCMOS voltage: VCC2	Note 2	– 0.5	9	VDC
Input voltage: MBRST(15:0)	Note 2	– 28	28	V
Input voltage: other inputs	Note 2 Note 3 Note 4	– 0.5	VCC + 0.3	VDC
Input Differential Voltage: $\|V_{ID}\|$			700	mV
High level output current @ Voh = 2.4v : I_{OH}			– 20	mA
Low level output current @ Vol = 0.4v : I_{OL}			15	mA
Clock Frequency: DCLK_A and DCLK_B			230	MHz
Operating Temperature: • Reference Locations 1 and 2 in Figure 2 • Reference Locations 3 and Array in Figure 2	Note 6 Note 7 Note 8	 10 10	 65 65	 °C °C
Differential Temperature: • Location 1 minus Location 3 in Figure 2 • Location 2 minus Location 3 in Figure 2			 10 10	 °C °C
Storage Temperature (non-operating): • Reference Locations 1, 2, and 3 in Figure 2		 – 40	 80	 °C
Operating Relative Humidity (non-condensing)		0	95	%
Storage Relative Humidity (non-condensing)		0	95	%

Note: VCC2, VCCI, VCC, and VSS (GND) power supplies are required for all DMD operating modes.

Note 1:

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the DMD. This is a stress rating only and functional operation of the DMD at these or any other conditions beyond those indicated in the “Recommended Operating Conditions” section of this product spec is not implied. Exposure to absolute maximum rated conditions for extend periods may affect device reliability.

Note 2:

All voltage values are with respect to GND (VSS)
VCC2, VCCI, VCC, and VSS (GND) power supplies are required for all DMD operating modes.

Note 3:

Excludes Mirror Bias Reset inputs MBRST(15:0)

Note 4:

This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. LVDS differential inputs must not exceed $|V_{ID}|$ = 700mV or damage may result to the internal termination resistors.

Note 5:

To prevent excess current, | V_{CCI} – V_{CC} | should be less than 0.3v

Note 6:

The DMD can be operated between 0° C and 10° C at power-up for a maximum period of 10 minutes without damage.

Note 7:

The Type-X DMD can be used in projectors up to and including 3000 screen lumens. It shall not be used in projectors exceeding 3000 screen lumens.

Note 8:

Active array temperature cannot be measured directly; therefore it must be computed analytically from measurement points on the outside of the Type-X carrier, the carrier thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference frame temperature, thermocouple location 3 (TC3) in Figure 2, is provided by the following equations.

$T_{array} = T_{frame} + (Q_{array} \bullet R_{array\text{-}to\text{-}frame})$

$Q_{array} = (0.00274 \bullet SL) + 2.0$

Where:

T_{array} = computed array temperature (°C)

T_{frame} = measured frame temperature (°C) (TC3 location)

Q_{array} = Total DMD array power (electrical + absorbed) (watts)

$R_{array\text{-}to\text{-}frame}$ = DMD Type-X carrier thermal resistance from array to outside frame (°C/watt)

SL = measured screen lumens

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The nominal electrical power dissipation to use when calculating array temperature is 2.0 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source. The equations shown above are valid for a 1-Chip DMD system with a projection efficiency from the DMD to the screen of 87%. The constants 0.00274 is based on array characteristics. It assumes a spectral efficiency of 300 lumens/watt for the projected light and llumination distribution of 83.7% on the active array, and 16.3% on the array border and window aperture.

Sample Calculation:

Screen lumens = 2000 lumens

T_{frame} = 55.0 C

$Q_{array} = (0.00274 \bullet 2000) + 2.0 = 7.48$ watts

T_{array} = 55.0 °C + (7.48 watts • 0.7 °C/watt) = 60.2 °C

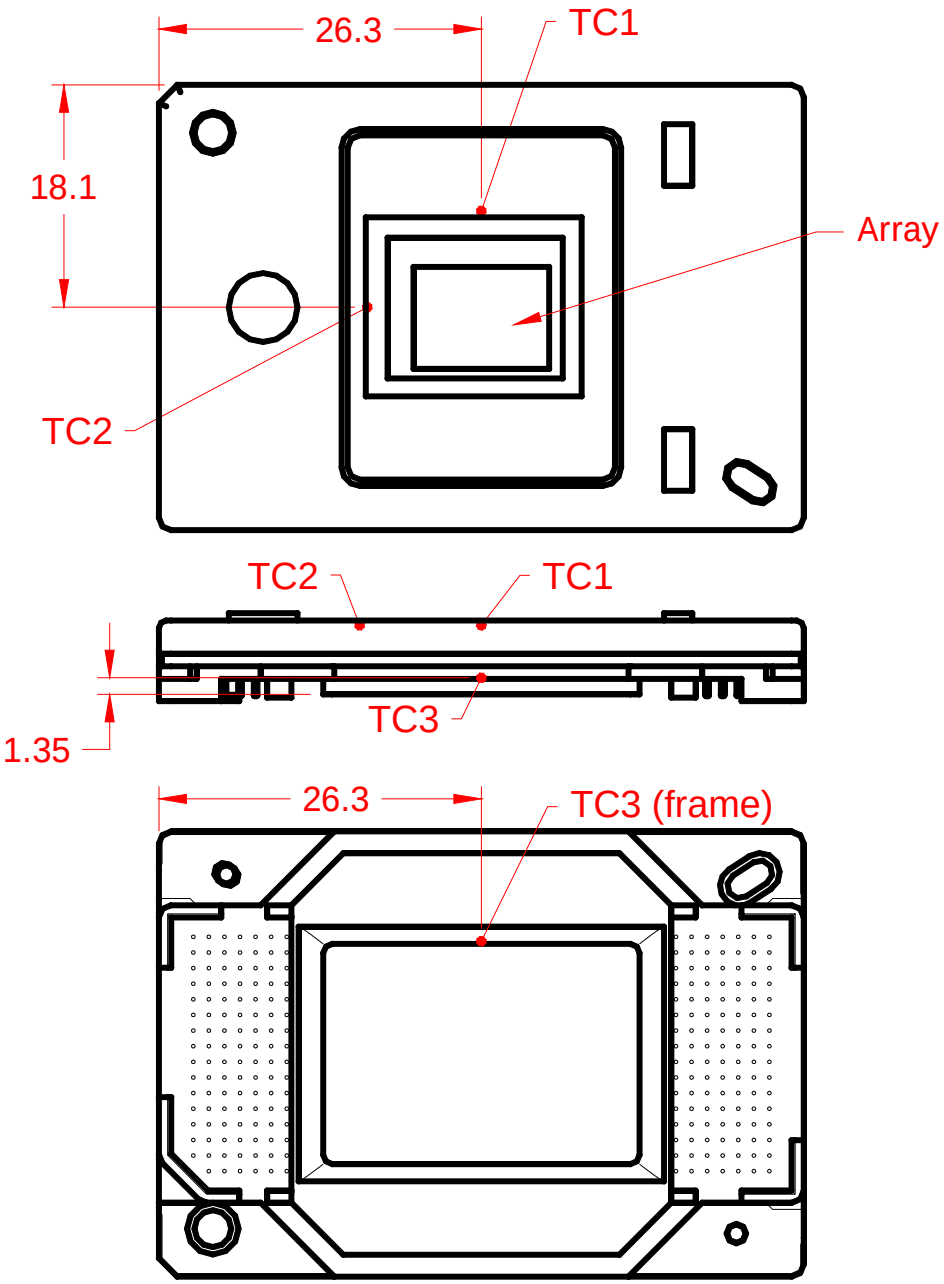

Figure 2. DMD Thermocouple Locations

Table 5. Recommended Operating Conditions						
Parameters			Min	Nom	Max	Units
VCC	LVCMOS Logic Supply voltage	Note 12	3.0	3.3	3.6	V
VCCI	LVCMOS LVDS Interface Supply voltage	Note 12	3.0	3.3	3.6	V
	Supply Voltage Delta | VCCI – VCC |	Note 11		0	0.3	V
VCC2	Mirror Electrode and HVCMOS voltage	Note 12	8.25	8.5	8.75	V
V_{MBRST}	Mirror Bias / Reset voltage	Note 9	– 27		26.5	V
T_C	Operating Case temperature	Note 1	25		45	°C
ILL_{UV}	Illumination , wavelength < 395nm	Note 13			0.68	mW/cm^2
ILL_{IR}	Illumination , wavelength > 800nm	Note 14				mW/cm^2
LVCMOS parameters						
V_{IH}	High level Input voltage	Note 2	1.7	2.5	VCC + 0.3	V
V_{IL}	Low level Input voltage	Note 2	– 0.3		0.7	V
I_{OH}	High level Output current @ Voh = 2.4v				– 20	mA
I_{OL}	Low level Output current @ Vol = 0.4v				15	mA
T_{PWRDNZ}	PWRDNZ pulse width	Note 8	10			ns
SCP parameters		Note 7				
f_{SCPCLK}	SCP Clock frequency	Note 3	50		500	kHz
T_{SCP_SKEW}	Time between valid SCPDI and rising–edge of SCPCLK		– 300		300	ns
T_{SCP_DELAY}	Time between valid SCPDO and rising –edge of SCPCLK	Note 3 Note 5			960	ns
$T_{SCP\_NEG\_ENZ}$	Time between falling–edge of SCPENZ and the first rising –edge of SCPCLK	Note 3 Note 6	30			ns
$T_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)		1			$1/f_{SCPCLK}$
$T_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state)				1.5	ns
T_r , T_f	Rise/Fall Time (20% to 80%)				200	ns
400MHz LVDS parameters		Note 4				
$\|V_{ID}\|$	Input Differential Voltage (absolute value)	Note 10	100	400	600	mV
V_{CM}	Common Mode Voltage	Note 10		1200		mV
V_{LVDS}	LVDS Voltage	Note 10	0		2000	mv
Z_{LINE}	Line Differential Impedance (PWB/trace)		90	100	110	Ω
T_r	Rise Time (20% to 80%)		100		400	ps
T_f	Fall Time (20% to 80%)		100		400	ps
Z_{IN}	Internal Differential Termination Resistance		95		105	Ω
T_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ				10	ns

Note 1:

Operating case temperature limits apply to the Array and Thermocouple location points 1, 2, 3, referenced in Figure 2

Note 2:

Tester Conditions for V_{IH} and V_{IL}:
Frequency = 60MHz. Maximum Rise/Fall Time = 2.5ns @ (20% - 80%)

Note 3:

The SCP clock is a gated clock. Duty cycle shall be 50% +/- 10%.
This parameter is related to the frequency of DCLK_A and DCLK_B, which are assumed to be 400MHz.
f_{DCLK} less than 400 MHz will impact the maximum f_{SCPCLK} range.

Note 4:

For timing parameters, refer to Table 9

Note 5:

This parameter is related to the frequency of DCLK_A and DCLK_B, which are assumed to be 400MHz.
Use $T_{SCP\_DELAY} = (1/f_{DCLK})*(384)$ for f_{DCLK} less than 400 MHz.
f_{DCLK} less than 400 MHz will impact the maximum f_{SCPCLK} range.

Note 6:

This parameter is related to the frequency of DCLK_A and DCLK_B, which are assumed to be 400MHz.
Use $T_{SCP\_NEG\_ENZ} = (1/f_{DCLK})*(12)$ for f_{DCLK} less than 400 MHz.
f_{DCLK} less than 400 MHz will impact the maximum f_{SCPCLK} range.

Note 7:

For all Serial Communications Port (SCP) operations, DCLK_A and DCLK_B are required.

Note 8:

PWRDNZ input pin resets the SCP and disables the LVDS receivers.
PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.

Note 9:

The positive voltage level of this input waveform must be optimized for DMD performance. Each DMD is assigned a bias voltage bin letter, which is marked on the DMD Type-X carrier in the approximate location shown in Figure 3. See the appropriate Hardware and Software ICDs and the electrical reference design schematic for implementation details. The bin letters in Table 6 correspond to the positive voltage levels shown.

Table 6. V_B Bias Voltage Bins

Bin Designation	Min (V)	Max (V)
E	25.5	26.5

Note 10:

See . $V_{LVDS} = V_{CM}$ +/- $|1/2V_{ID}|$, where V_{CM} is bounded by the voltage values of V_{LVDS} and $|V_{ID}|$.

Note 11:

To prevent excess current, | VCCI – VCC | should be less than 0.3v

Note 12:

VCC2, VCCI, VCC, and VSS (GND) power supplies are required for all DMD operating modes.

Note 13:

UV light (<395nm) power density may degrade or reduce DMD performance over time when significant power densities are illuminating the DMD. Consult with TI or TI authorized distributor for applications requiring UV light.

Note 14:

Infrared (IR) Illumination > 800nm has not been well characterized by TI. IR illumination is not known to degrade DMD performance, but has not been characterized or qualified by TI. Therefore, Min and Max ILL_{IR} is not specified.

DMD Marking Locations

The device marking is shown in Figure 3 below. The marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 3. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Example: *1076-631cW GHXXXXX LLLLLLM

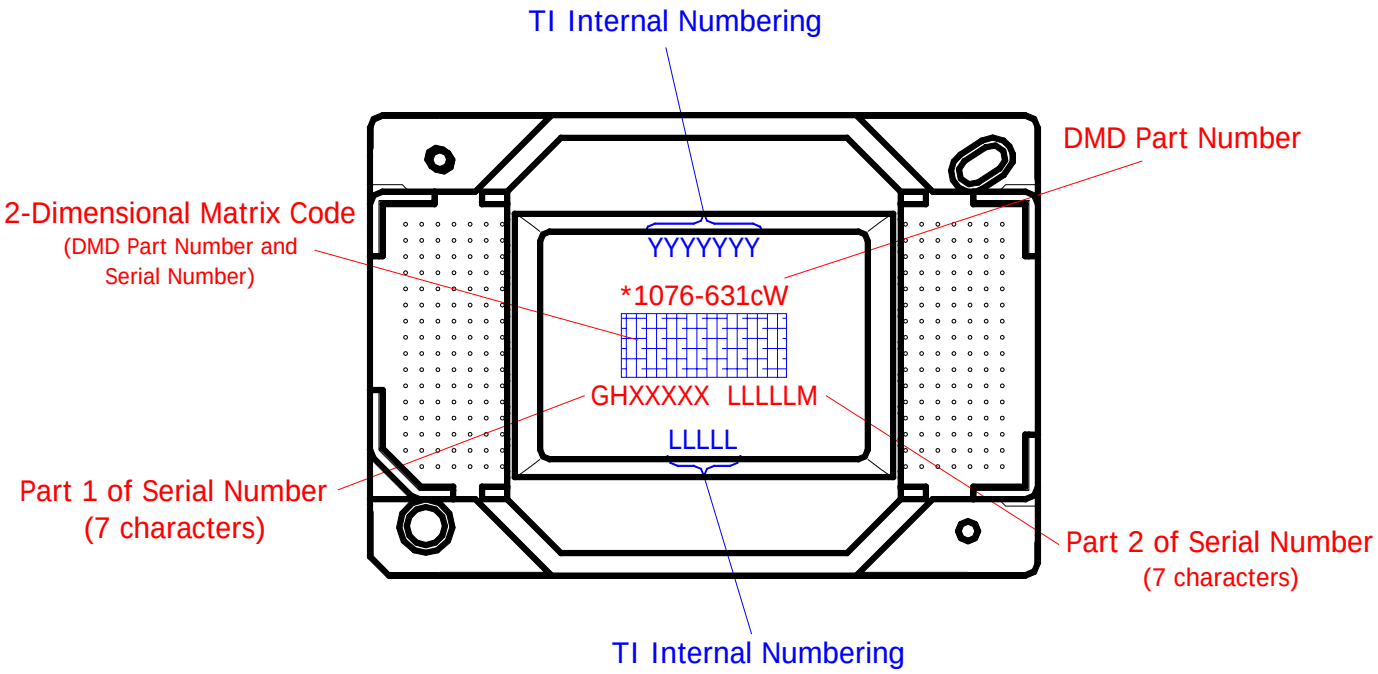

Figure 3. DMD Marking Locations

Table 7. Electrical Characteristics For Recommended Operating Conditions						
Parameters			Test Condition	Min	Max	Units
V_{OH}	High level output voltage		VCC = 3 V I_{OH} = – 20 mA	2.4		V
V_{OL}	Low level output voltage		VCC = 3.6 V I_{OL} = 15 mA		0.4	V
I_{OZ}	Output high impedance current		VCC = 3.6 V		10	uA
I_{IL}	Low level input current		VCC = 3.6 V V_I = 0		– 60	uA
I_{IH}	High level input current	Note 1	VCC = 3.6 V V_I = VCC		200	uA
I_{CC}	ICC current	Note 2	VCC = 3.6 V		750	mA
I_{CCI}	ICCI current	Note 2	VCCI = 3.6 V		450	mA
I_{CC2}	ICC2 current		VCC2 = 8.75 V		25	mA
	Electrical input power				3.4	W

Note 1 :
includes LVCMOS pins only
excludes LVDS pins and MBRST(15:0) pins

Note 2:
To prevent excess current, | VCCI – VCC | should be less than 0.3v

Table 8. Capacitance at Recommended Operating Conditions					
Parameters		Test Condition	Min	Max	Units
C_I	Input Capacitance	f = 1 MHz		10	pf
C_O	Output Capacitance	f = 1 MHz		10	pf
C_{IM}	MBRST(15:0) Input Capacitance	f = 1 MHz (1024 x 768) array all inputs interconnected	160	210	pf

Table 9. LVDS Critical Timing							
Parameter				Min	Typ	Max	Units
T_C	Clock Cycle	DCLK_A	LVDS pair	2.5			ns
T_C	Clock Cycle	DCLK_B	LVDS pair	2.5			ns
T_W	Pulse Width	DCLK_A	LVDS pair	1.19	1.25		ns
T_W	Pulse Width	DCLK_B	LVDS pair	1.19	1.25		ns
T_S	Setup Time	D_A(15:0) before DCLK_A	LVDS pair	0.35			ns
T_S	Setup Time	D_B(15:0) before DCLK_B	LVDS pair	0.35			ns
T_S	Setup Time	SCTRL_A before DCLK_A	LVDS pair	0.35			ns
T_S	Setup Time	SCTRL_B before DCLK_B	LVDS pair	0.35			ns
T_H	Hold Time	D_A(15:0) after DCLK_A	LVDS pair	0.35			ns
T_H	Hold Time	D_B(15:0) after DCLK_B	LVDS pair	0.35			ns
T_H	Hold Time	SCTRL_A after DCLK_A	LVDS pair	0.35			ns
T_H	Hold Time	SCTRL_B after DCLK_B	LVDS pair	0.35			ns
T_{SKEW}	Skew Time	Channel B relative to Channel A	LVDS pair	– 1.25		+ 1.25	ns

Channel A (Bus A):

- DCLK_AN
- DCLK_AP
- SCTRL_AN
- SCTRL_AP
- D_AN(15:0)
- D_AP(15:0)

Channel B (Bus B):

- DCLK_BN
- DCLK_BP
- SCTRL_BN
- SCTRL_BP
- D_BN(15:0)
- D_BP(15:0)

Table 10. Physical Parameters					
Parameter		Min	Nom	Max	Units
Number of Columns			1024		
Number of Rows			768		
Mirror (Pixel) Pitch			10.8		um
Total Width of Active Mirror Array			11.059		mm
Total Height of Active Mirror Array			8.294		mm
Active Array Border	Note 1		POM		
Active Array Border Size			10		mirrors/side

Note 1:

The structure and qualities of the border around the active array includes a band of partially functional mirrors called the “Pond Of Mirrors” (POM). These mirrors are structurally and/or electrically prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”

Table 11. Thermal Parameters					
Parameter		Min	Nom	Max	Unit
Thermal Resistance • Active area to case	Note 1			0.7	°C/W

Note 1:

The DMD is designed to conduct absorbed and dissipated heat to the back of the Type-X carrier where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the carrier within the specified operational temperatures.

The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.

Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

Table 12. Optical Parameters					
Parameter		Min	Nom	Max	Unit
Mirror Tilt – half angle • Variation device to device	Note 1	11	12	13	Degrees
Axis of Rotation with respect to System Datums • Variation device to device	Figure 4	44	45	46	Degrees
Mirror Metal Specular Reflectivity (420nm – 700nm)			89.4		%
DMD Efficiency (420nm – 700nm)	Note 2		68		%
Window Material Designation Type-X			Corning Eagle 2000 or XG		
Window Refractive Index			1.5090		
Minimum Window Transmittance Tmin measured at all angles 0 – 30 AOI (single pass) over the wavelength range (420nm – 680nm)		97			%
Average Window Transmittance Tave measured at all angles 0 – 30 AOI (single pass) over the wavelength range (420nm – 680nm)		99			%
Average Window Transmittance Tave measured at all angles 30 – 45 AOI (single pass) over the wavelength range (420nm – 680nm)		97			%
Window Flatness per 25mm				4	fringes

Note 1: Mirror Tilt

Limits on variability of mirror tilt half angle are critical in the design of the accompanying optical system. Variations in tilt angle within a device may result in apparent non-uniformities, such as line pairing and image mottling, across the projected image. Variations in the average tilt angle between devices may result in colorimetry and system contrast variations. The specified limits represent the tolerances of the tilt angles within a device.

Note 2: DMD Efficiency

The overall DMD efficiency includes window transmittance, active area fill factor, active area mirror specular reflectivity, and diffraction efficiency. It is defined as that percentage of light incident upon the mirror array that is specularly reflected from the mirror array. The measurement is made with all mirrors in the full on-state without electronic duty cycle effects (i.e. measure using 100% duty cycle).

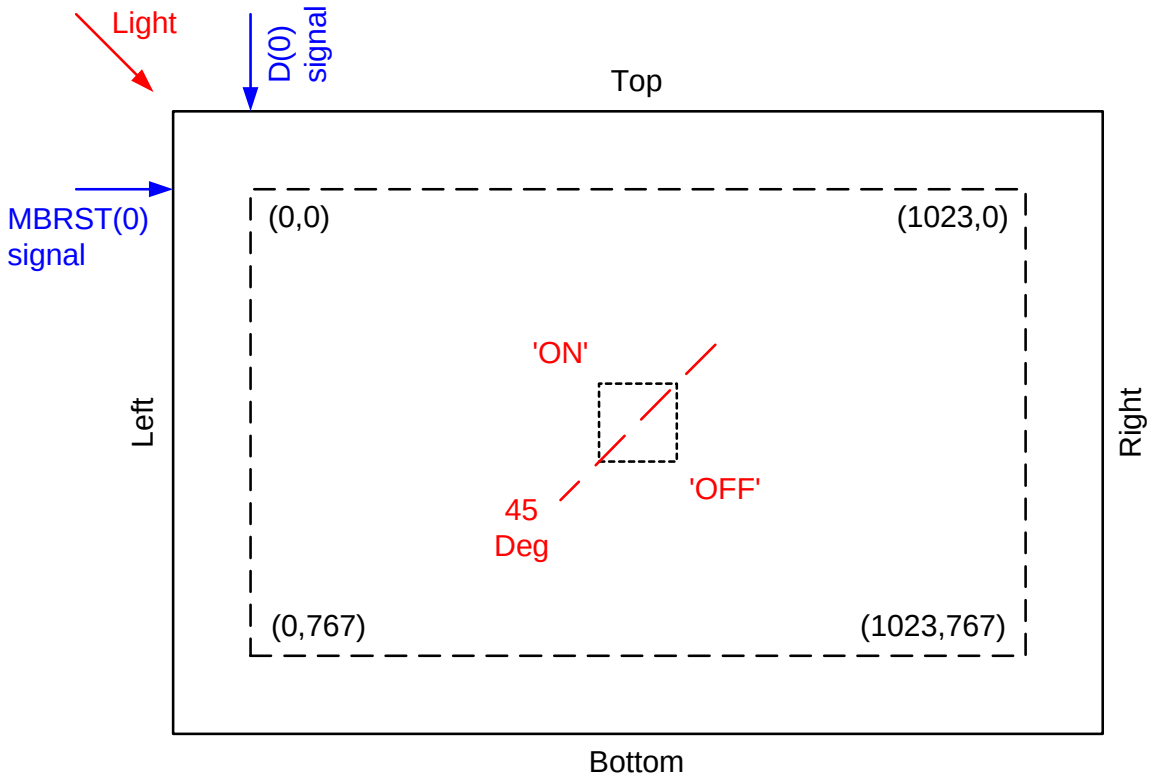

Figure 4. Mirror Tilt Axis Orientation

Table 13. Optical Interface and System Image Quality					
Parameter		Min	Nom	Max	Unit
	Note 1				

Note 1:
Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in a) through c) below:

a) Numerical Aperture and Stray Light Control.
The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

b) Pupil Match.
TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within two degrees of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

c) Illumination Overfill.
The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

TI ASSUMES NO RESPONSIBILITY FOR IMAGE QUALITY ARTIFACTS OR DMD FAILURES CAUSED BY OPTICAL SYSTEM OPERATING CONDITIONS EXCEEDING LIMITS DESCRIBED ABOVE.

Mechanical dimensions and tolerances are shown in the Mechanical ICD drawing referenced in Table 2.

Table 14. System Interface Parameters					
Parameter		Min	Nom	Max	Unit
Maximum Load to be Applied to the • Thermal Interface area • Electrical Interface areas 1 and 2	Figure 5 Each Area			 25 12.5	 lbs lbs

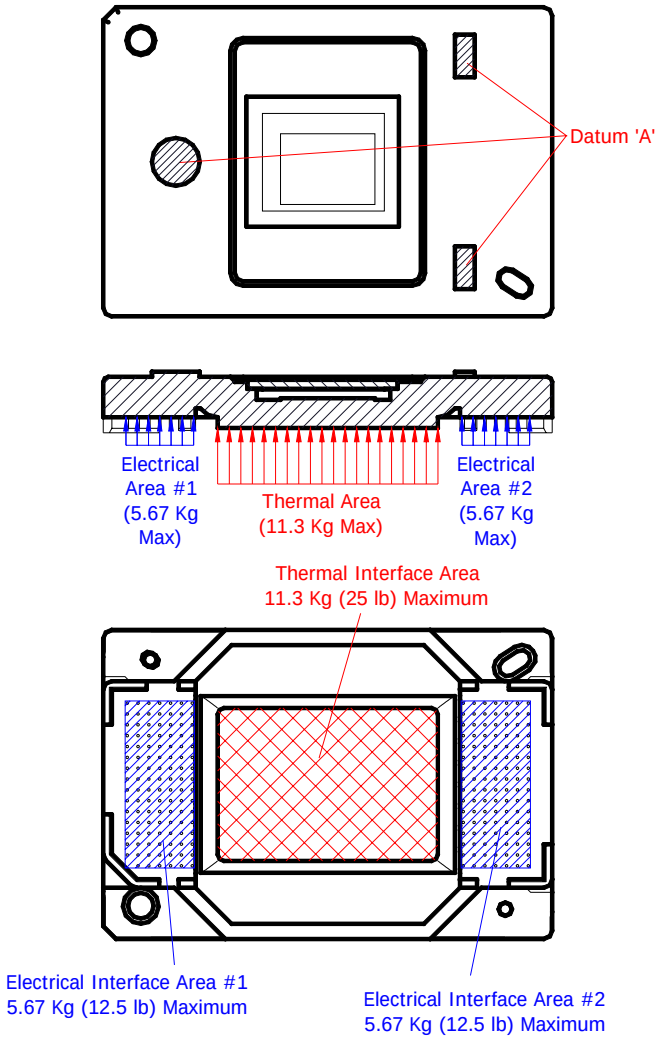

Figure 5. System Interface Loads

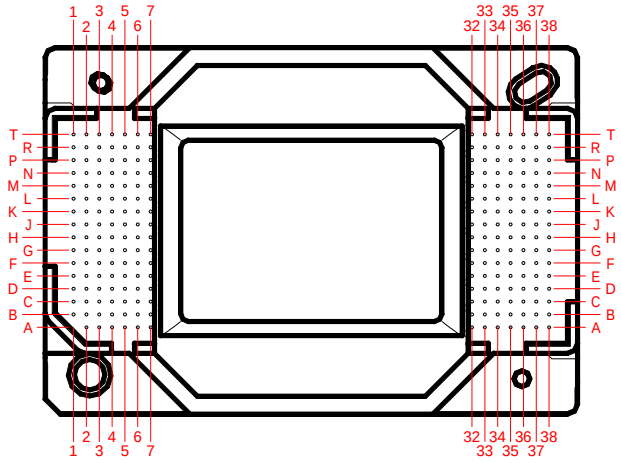

Figure 6. DMD Type-X Carrier Pins - Bottom View

Electrostatic Discharge Immunity

All external signals on the DMD are protected from damage by electrostatic discharge, and are tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).

Table 15. DMD ESD Protection Limits

Type-X Carrier Pin Type	Voltage (maximum)	Units
Input	2000	V
Output	2000	V
Power	2000	V
All MBRST	< 250	V

Notes on Handling

All CMOS devices require proper Electrostatic Discharge (ESD) handling procedures.

Refer to drawing #2506185 DMD Handling Specification, for precautions to protect the DMD from ESD and to protect the DMD's glass and electrical contacts.

Refer to drawing #2504640 DMD Glass Cleaning Procedure, for correct and consistent methods for cleaning the glass of the DMD, in such a way that the anti reflective coatings on the glass surface are not damaged.