REF Schematic for RZW03_RK3568

Main Functions Introduction

1)PMIC: RK809-5+DiscretePower

2)RAM: LPDDR4/4X 1x32Bit------------------Default(8G)

3)ROM: eMMC-------------------------Default(32G)
   Option:SPI Falsh

4)Support:1 x Micro SD Card3.0

5)Support:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1 ----------------Default
   Option:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1   + 1 x 1Lane PCIe2.0(RC Mode)

6)Support:1 x USB2.0 HOST2+ 1 x USB2.0 HOST3 -- ------Default

8)Support:2 x 1Lane PCIe3.0 Connector (RC Mode) ------Default

   Option:1 x 2Lanes PCIe3.0 Connector (RC Mode)
    Option:1 x 2Lanes PCIe3.0 Connector (EP Mode)

9)Support:1 x HDMI2.0 TX

10)Support:1 x LCM MIPI DSI TX0 ----------------------Default

   Option:1 x LCM MIPI DSI TX1
   Option:1 x LCM LVDS TX
   Option:1 x LCM Dual MIPI DSI TX
   Option:1 x LCM eDP TX

11)Support:1 x VGA OUT -------------------------------Default
12)Support:1 x 4Lanes Camera MIPI CSI RX -------------Default
   Option:2 x 2Lanes Camera MIPI CSI RX
   Option:1 x HDMI1.4 RX(HDMI to MIPI CSI)
13)Support:a/b/g/n/ac 2X2 SDIO WIFI5+BT5.0+PCM --------Default
   Option:a/b/g/n/ac 1X1 SDIO WIFI+BT+PCM
   Option:a/b/g/n/ac/ax 2X2 PCIe WIFI6+BT5.0+PCM
14)Support:1 x 10/100/1000 Ethernet(RGMII1_M1) -------Default
   Option:1 x 10/100/1000 Ethernet(RGMII0)
   Option:1 x 10/100/1000 PCIe Ethernet Card
15)Support:1 x Headphone output ----------------------Default
16)Support:1 x ECM MIC + 1 x Speaker out -------------Default
   Option:4 x MEMS MIC + 1 x Speaker out + Loopback or 2 x MEMS MIC + 1 x Speaker out + Loopback
   Option:4 x MEMS MIC + 2 x Speaker out + Loopback
17)Support:1 x IR Receiver ---------------------------Default
18)Support:Array Key(MENU,VOL+,VOL-,ESC),Reset,Power on/off Key
19)Support:3 x UART + 1 x RS485 + 1 x CAN FD(Option)
20)Support:Debug UART and ARM JTAG

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Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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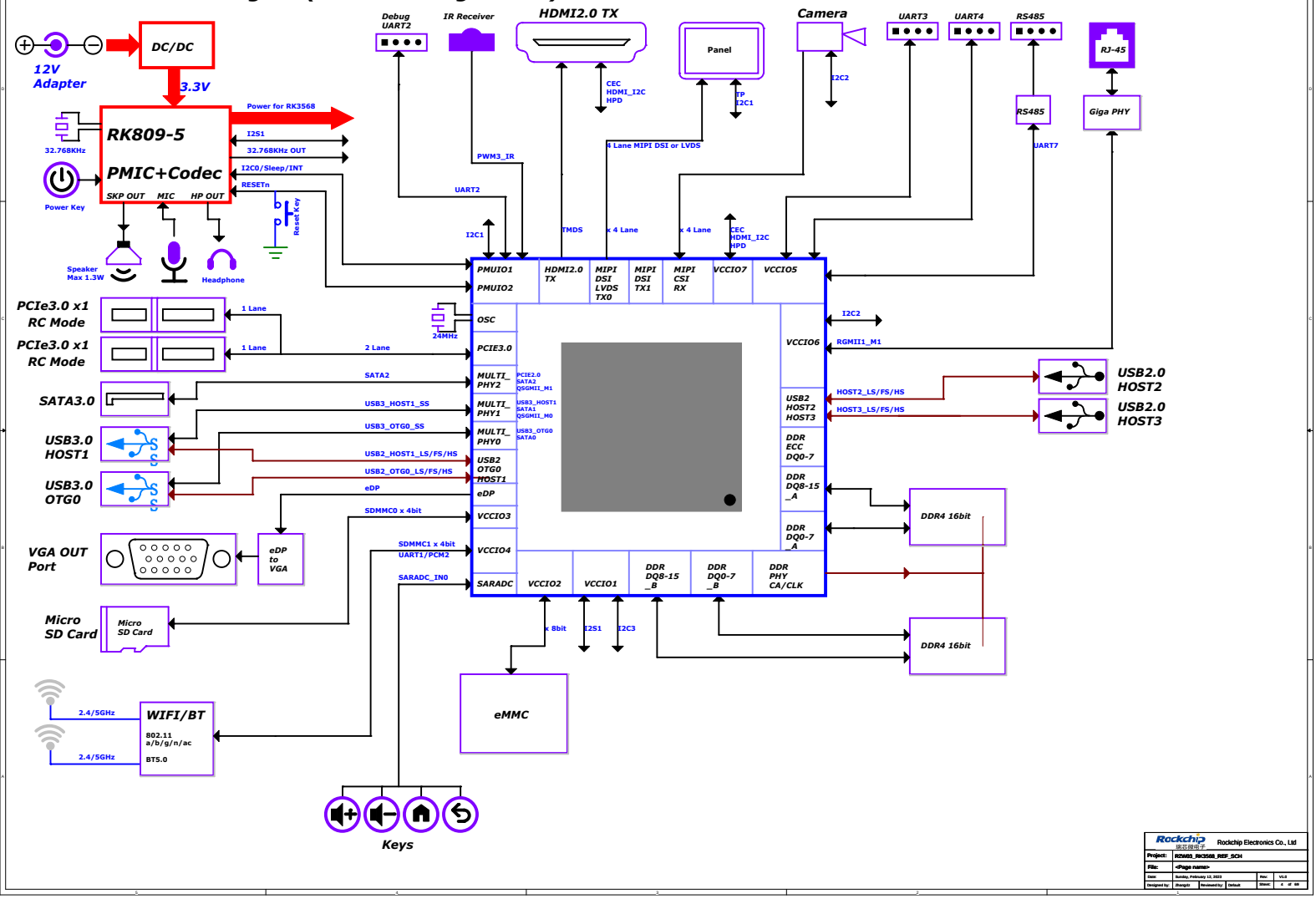
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-02-04	Zhangdz	1:Revision preliminary version	

RK3568 Ref Block Diagram(Default configuration)



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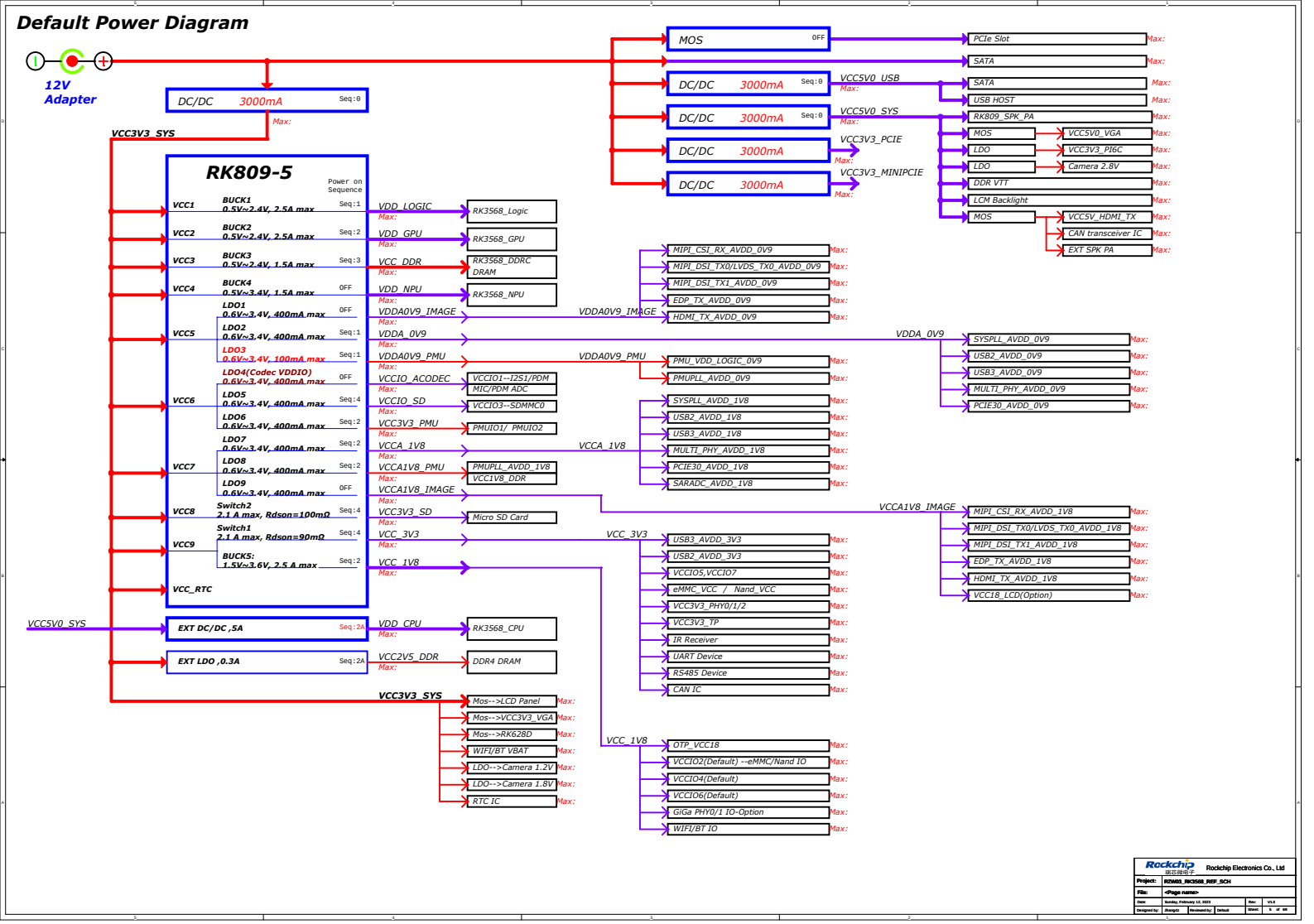
Default Power Diagram



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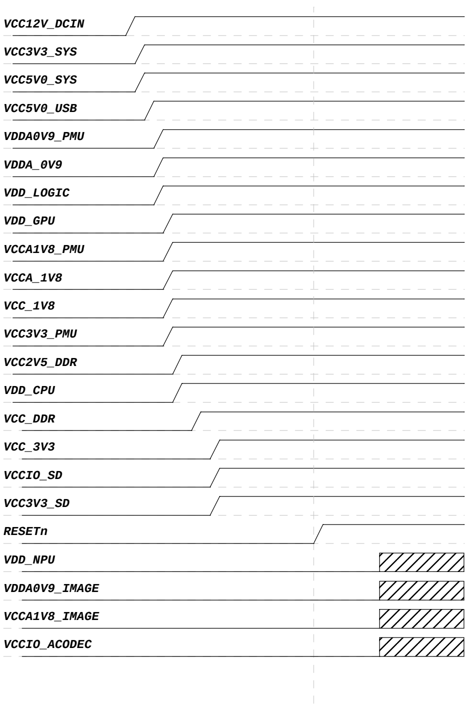
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

Default IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

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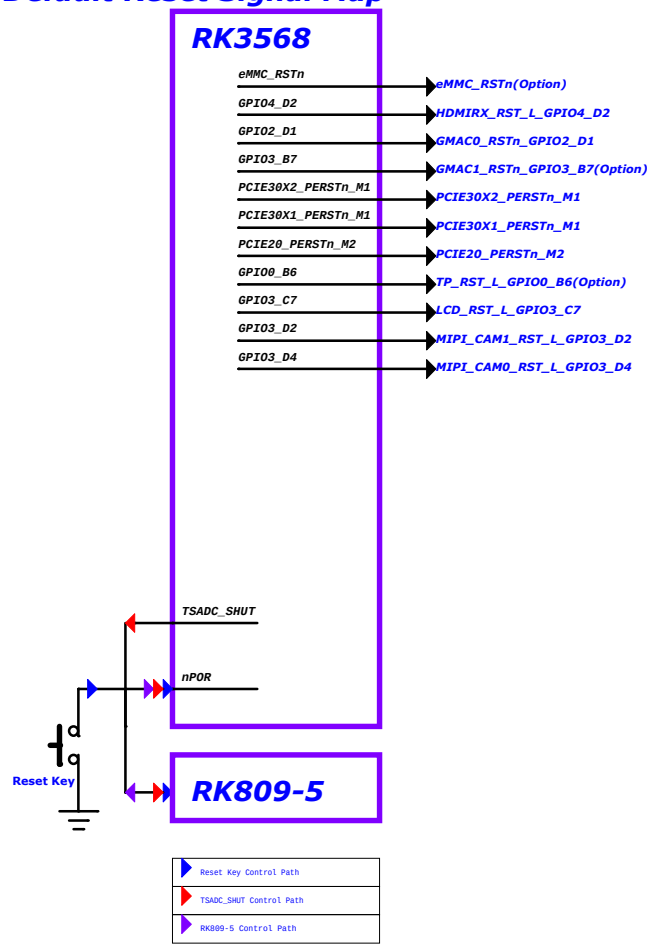
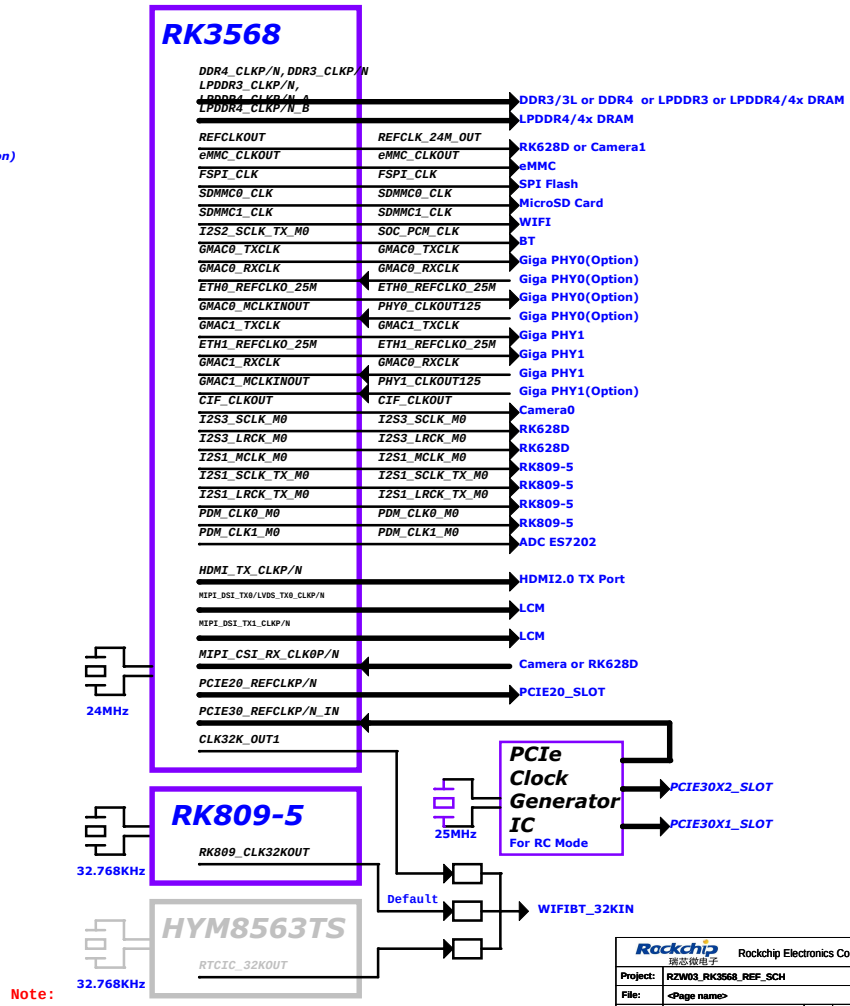
Default Reset Signal Map



Default Clock Map



Note:
The power off hold time scheme is required,
It is recommended to use external RTC IC

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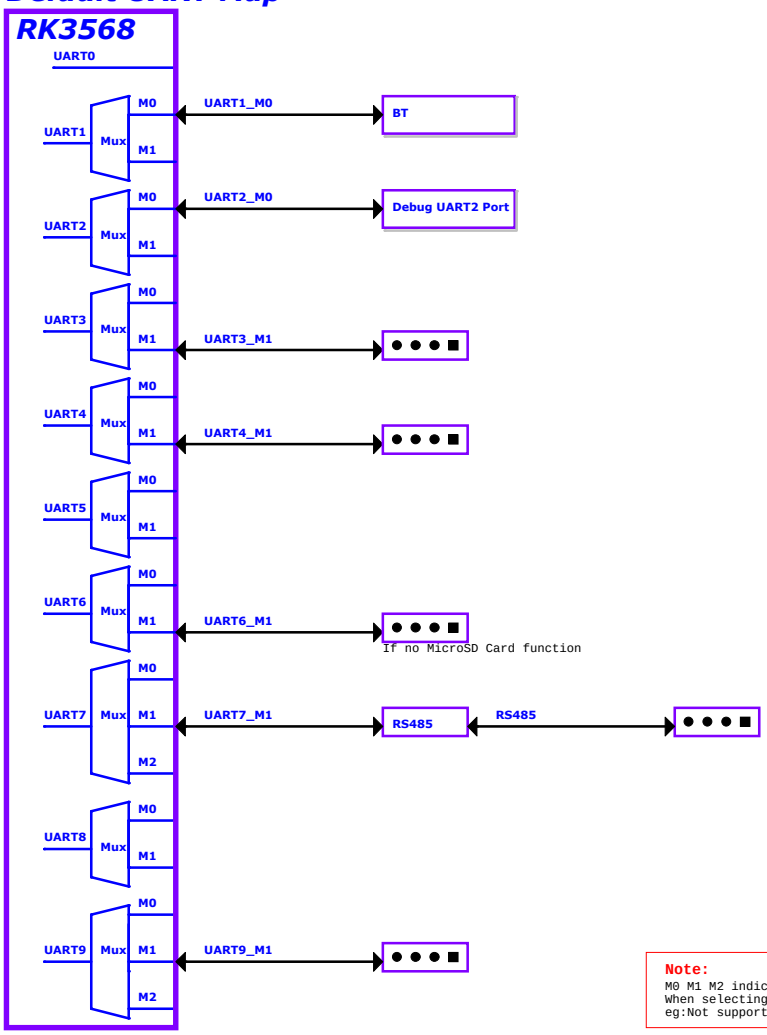
Default UART Map



Note:

M0 M1 M2 indicates that the same function is multiplexed to different IO
When selecting, only M0 or M1 or M2 can be selected
eg:Not supported UART1_TX_M0 and UART1_RX_M1 combination

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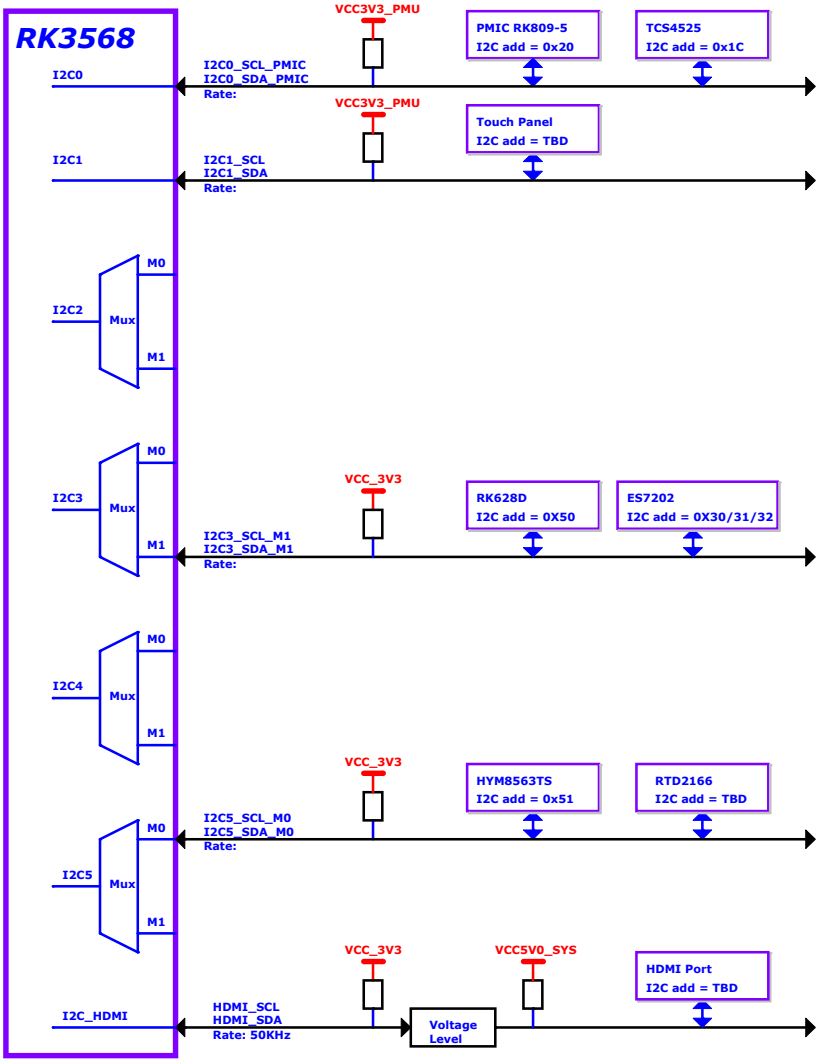
Default I2C Map

Note:
M0 M1 M2 indicates that the same function is multiplexed to different IO. When selecting, only M0 or M1 or M2 can be selected
eg:
Not supported I2C1_SCL_M0 and I2C1_SDA_M1 combination



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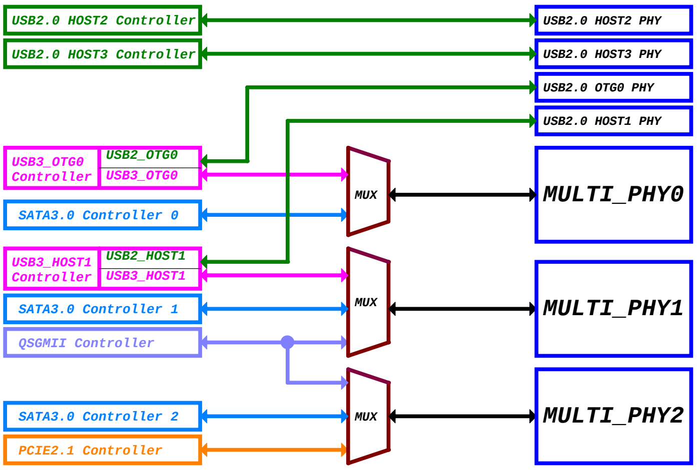
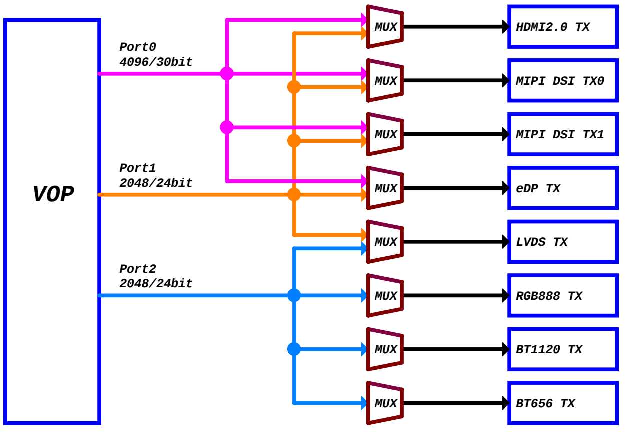
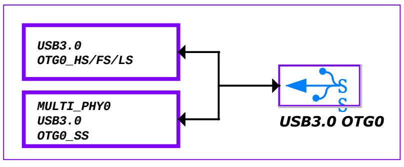
MULTI_PHY0/1/2 Path Map



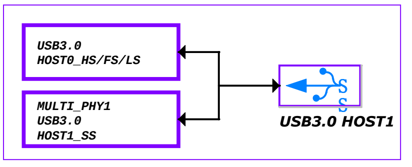
VOP Path Map



USB3.0 OTG0



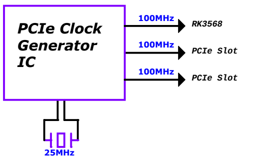
USB3.0 HOST1



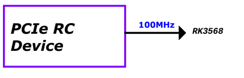
PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIE30_REFCLK (RC/EP:input)	PCIE30_TX0 PCIE30_RX0 PCIE30_TX1 PCIE30_RX1	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIE30_REFCLK (RC:input)	PCIE30_TX0 PCIE30_RX0	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	Only RC
			PCIE30_TX1 PCIE30_RX1	PCIE30X1_CLKREQn PCIE30X1_WAKEn PCIE30X1_PERSTn PCIE30X1_BUTTONRSTn	Only RC

PCIe3.0 REFCLK-RC Mode



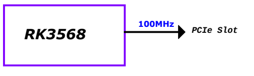
PCIe3.0 REFCLK-EP Mode



PCIe2.1 PHY

MULTI_ PHY2	PCIe2.1 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC

PCIe2.1 REFCLK-RC Mode



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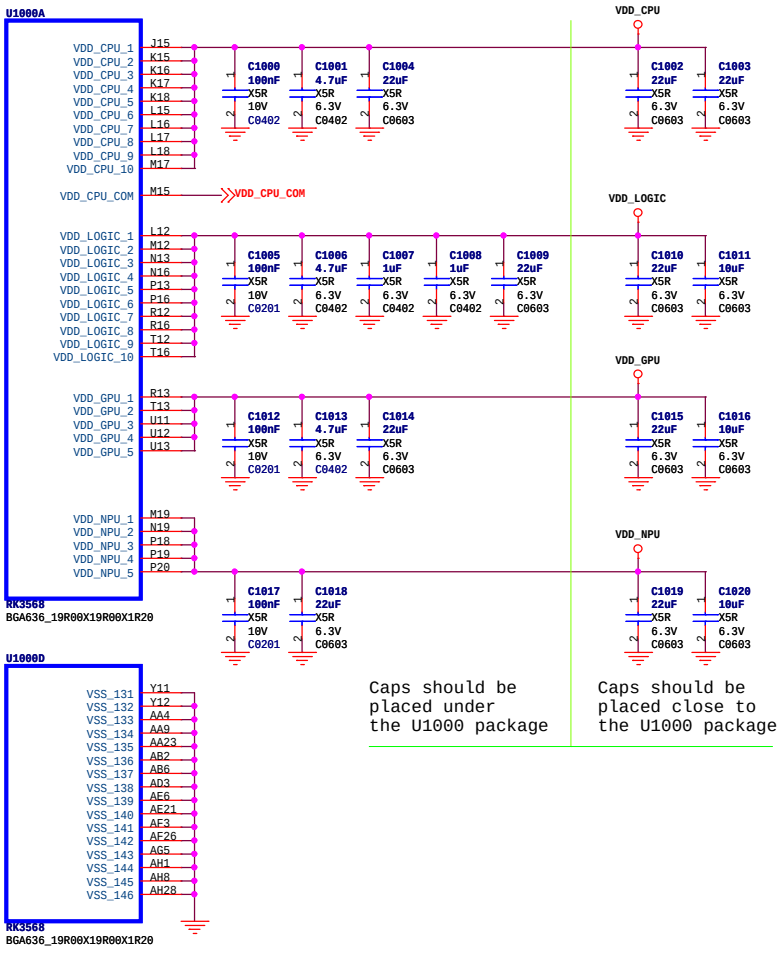
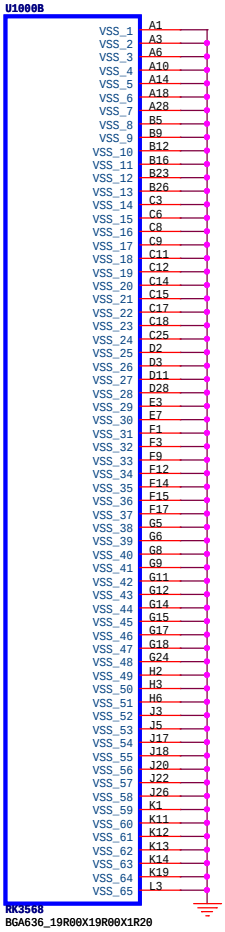
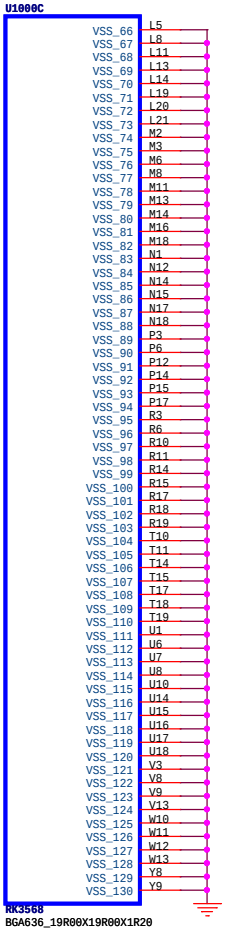
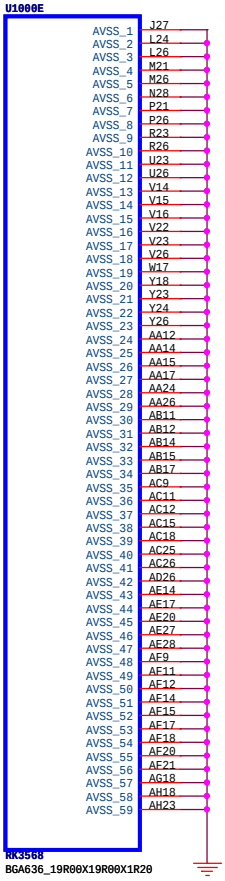
RK3568_ABCDE (Power&Gnd)









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RK3568_F (DDR PHY)

U1000F

DDR4	LPDDR4	DDR3	LPDDR3
DDR_DQ0_A	DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15
DDR_DQ1_A	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14
DDR_DQ2_A	DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ10
DDR_DQ3_A	DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ9
DDR_DQ4_A	DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ13
DDR_DQ5_A	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ12
DDR_DQ6_A	DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ8
DDR_DQ7_A	DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ11
DDR_DM0_A	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1
DDR_DQS0P_A	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P
DDR_DQS0N_A	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N
DDR_DQ8_A	DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25
DDR_DQ9_A	DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24
DDR_DQ10_A	DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ28
DDR_DQ11_A	DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ29
DDR_DQ12_A	DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ26
DDR_DQ13_A	DDR4_DQU4_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ31
DDR_DQ14_A	DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ30
DDR_DQ15_A	DDR4_DQU8_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ27
DDR_DM1_A	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3
DDR_DQS1P_A	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P
DDR_DQS1N_A	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N
DDR_DQ0_B	DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1
DDR_DQ1_B	DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ5
DDR_DQ2_B	DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ6
DDR_DQ3_B	DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4
DDR_DQ4_B	DDR4_DQU8_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ2
DDR_DQ5_B	DDR4_DQU6_B	LPDDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ3
DDR_DQ6_B	DDR4_DQU4_B	LPDDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7
DDR_DQ7_B	DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ0
DDR_DM0_B	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM2	LPDDR3_DM0
DDR_DQS0P_B	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS2P	LPDDR3_DQS0P
DDR_DQS0N_B	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS2N	LPDDR3_DQS0N
DDR_DQ8_B	DDR4_DQL0_B	LPDDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18
DDR_DQ9_B	DDR4_DQL2_B	LPDDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19
DDR_DQ10_B	DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ22
DDR_DQ11_B	DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ23
DDR_DQ12_B	DDR4_DQL7_B	LPDDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ16
DDR_DQ13_B	DDR4_DQL5_B	LPDDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ17
DDR_DQ14_B	DDR4_DQL3_B	LPDDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ20
DDR_DQ15_B	DDR4_DQL1_B	LPDDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ21
DDR_DM1_B	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM3	LPDDR3_DM2
DDR_DQS1P_B	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS3P	LPDDR3_DQS2P
DDR_DQS1N_B	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS3N	LPDDR3_DQS2N
DDR_ECC_DQ0	DDR4_ECC_DQ7	--	DDR3_ECC_DQ0	
DDR_ECC_DQ1	DDR4_ECC_DQ0	--	DDR3_ECC_DQ1	
DDR_ECC_DQ2	DDR4_ECC_DQ2	--	DDR3_ECC_DQ2	
DDR_ECC_DQ3	DDR4_ECC_DQ1	--	DDR3_ECC_DQ3	
DDR_ECC_DQ4	DDR4_ECC_DQ6	--	DDR3_ECC_DQ4	
DDR_ECC_DQ5	DDR4_ECC_DQ4	--	DDR3_ECC_DQ5	
DDR_ECC_DQ6	DDR4_ECC_DQ3	--	DDR3_ECC_DQ6	
DDR_ECC_DQ7	DDR4_ECC_DQ5	--	DDR3_ECC_DQ7	
DDR_ECC_DM	DDR4_ECC_DM	--	DDR3_ECC_DM	
DDR_ECC_DQS_P	DDR4_ECC_DQS_P	--	DDR3_ECC_DQS_P	
DDR_ECC_DQS_N	DDR4_ECC_DQS_N	--	DDR3_ECC_DQS_N	

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BGA636_19R00X19R00X1R20

DDR4	LPDDR4	DDR3	LPDDR3
DDR4_A0	LPDDR4_CLKP_B	DDR3_A9	---	AC9
DDR4_A1	---	DDR3_A2	---	AC1
DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6	AC2
DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---	AC3
DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3	AC4
DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2	AC5
DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1	AC6
DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---	AC7
DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9	AC8
DDR4_A9	LPDDR4_CLKN_B	DDR3_A5	---	AC9
DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---	AC10
DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A0	AC11
DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---	AC12
DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0	AC13
DDR4_A14_WEn	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5	AC14
DDR4_A15_CASn	LPDDR4_A2_A	DDR3_A0	---	AC15
DDR4_A16_RASn	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7	AC16
DDR4_ACTn	LPDDR4_CKE1_B	DDR3_CASn	---	AC17
DDR4_BA0	LPDDR4_A2_B	DDR3_A1	---	AC18
DDR4_BA1	LPDDR4_A4_B	DDR3_A12	LPDDR3_A4	AC19
DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEn	---	AC20
DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	---	AC21
DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE	AC22
DDR4_CLKP	LPDDR4_CLKP_A	DDR3_CLKP	LPDDR3_CLKP	AC23
DDR4_CLKN	LPDDR4_CLKN_A	DDR3_CLKN	LPDDR3_CLKN	AC24
DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0	AC25
DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_ODT1	AC26
DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	LPDDR3_CS1n	AC27
DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS0n	AC28
DDR4_RESETn	LPDDR4_RESETn	DDR3_RESETn	---	AC29

Note: Sequences can not be swap

Note:
Except DDR3, other DQ sequences can not be swap

DDR_RZQ
DDR_VREFOUT

DDR3L =1.35V
DDR3 =1.5V
DDR4 =1.2V
LPDDR3 =1.2V
LPDDR4 =1.1V
LPDDR4x =1.1V

DDRPHY_VDDQ_1
DDRPHY_VDDQ_2
DDRPHY_VDDQ_3
DDRPHY_VDDQ_4
DDRPHY_VDDQ_5
DDRPHY_VDDQ_6
DDRPHY_VDDQ_7
DDRPHY_VDDQ_8

DDR3L =1.35V
DDR3 =1.5V
DDR4 =1.2V
LPDDR3 =1.2V
LPDDR4 =1.1V
LPDDR4x =0.6V

DDRPHY_VDDQL_1
DDRPHY_VDDQL_2
DDRPHY_VDDQL_3
DDRPHY_VDDQL_4
DDRPHY_VDDQL_5
DDRPHY_VDDQL_6

DDR_AVSS

DDR_RZQ — R1101 120R 1% R0201 — R1102 NC R0201 — VCC_DDR

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ pin

LPDDR4/LPDDR4x

VCC_DDR
C1100 100nF X5R 10V C0201
C1101 100nF X5R 10V C0201
C1102 4.7uF X5R 6.3V C0402
C1103 4.7uF X5R 6.3V C0402
C1104 10uF X5R 6.3V C0603

VCC0V6_DDR
C1105 100nF X5R 10V C0201
C1106 100nF X5R 10V C0201
C1107 4.7uF X5R 6.3V C0402
C1108 4.7uF X5R 6.3V C0402
C1109 4.7uF X5R 6.3V C0402

Caps should be placed under the U1000 package

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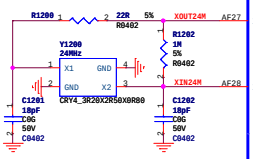
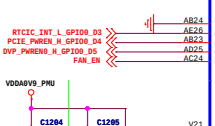
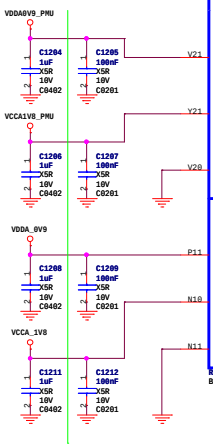
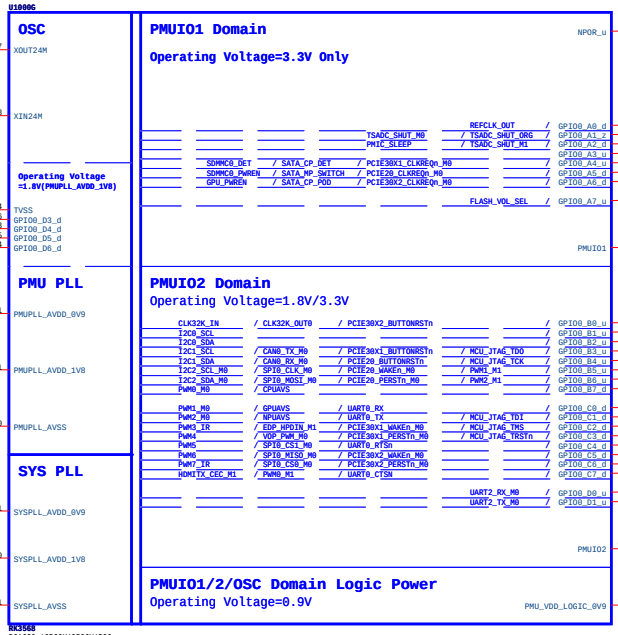
RK3568_G(OSC/PLL/PMUIO1/2)

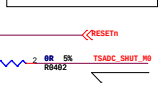
Note:
Adjusted the load capacitance
according to the crystal specification.

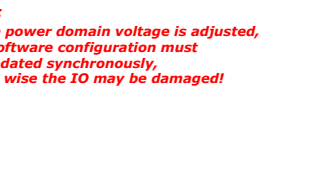


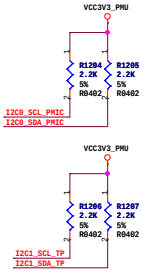












Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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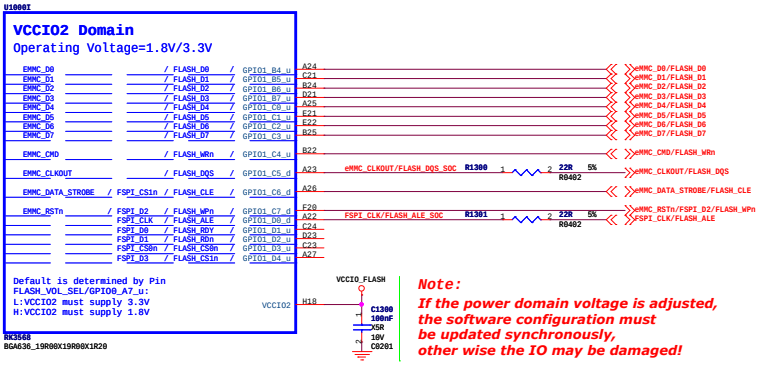
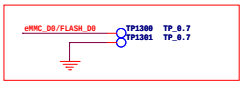
RK3568_I(VCCIO2 Domain)



Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!



Note:
For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

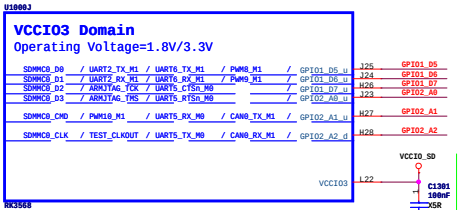
Layout note:
Test point must be placed on the line, and no branch can be added

Note:
For SPI Flash:
If FSPI_CLK=0V at after power on and reset, then system will enter into Maskrom mode.

Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware
When writing mismatched firmware or other conditions result in boot failure, use this test point

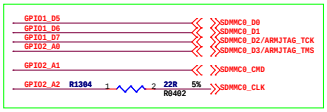
Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)



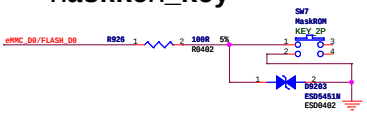
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Default
SDMMC0&JTAG



Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

MaskROM_Key



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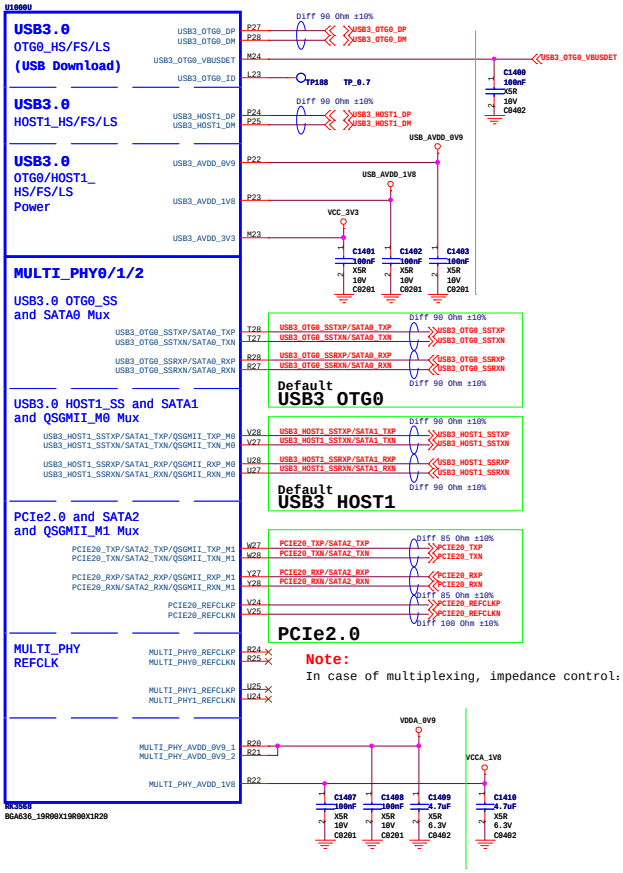
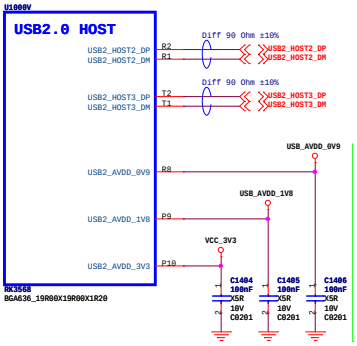
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



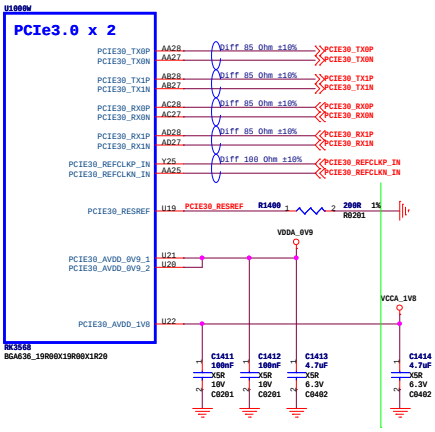
Note:
In case of multiplexing, impedance control: Diff 90 Ohm ±10%

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



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RK3568_K(VCCIO4 Domain)

RGMII0

U1000K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SDMMC1_D0	/ GMAC0_RXD2	/ UART6_RX_M0		/	GPIO2_A3_u
SDMMC1_D1	/ GMAC0_RXD3	/ UART6_TX_M0		/	GPIO2_A4_u
SDMMC1_D2	/ GMAC0_RXCLK	/ UART7_RX_M0		/	GPIO2_A5_u
SDMMC1_D3	/ GMAC0_TXD2	/ UART7_TX_M0		/	GPIO2_A6_u
SDMMC1_CMD	/ GMAC0_TXD3	/ UART9_RX_M0		/	GPIO2_A7_u
SDMMC1_CLK	/ GMAC0_TXCLK	/ UART9_TX_M0		/	GPIO2_B0_d
SDMMC1_PWREN	/ I2C4_SDA_M1	/ UART8_RTSn_M0	/ CAN2_RX_M1	/	GPIO2_B1_d
SDMMC1_DET	/ I2C4_SCL_M1	/ UART8_CTSn_M0	/ CAN2_TX_M1	/	GPIO2_B2_u
	GMAC0_TXD0	/ UART1_RX_M0		/	GPIO2_B3_u
	GMAC0_TXD1	/ UART1_TX_M0		/	GPIO2_B4_u
	GMAC0_TXEN	/ UART1_RTSn_M0	/ SPI1_CLK_M0	/	GPIO2_B5_u
	GMAC0_RXD0	/ UART1_CTSn_M0	/ SPI1_MISO_M0	/	GPIO2_B6_u
I2S2_SCLK_RX_M0	/ GMAC0_RXD1	/ UART6_RTSn_M0	/ SPI1_MOSI_M0	/	GPIO2_B7_d
I2S2_LRCK_RX_M0	/ GMAC0_RXDV_CRS	/ UART6_CTSn_M0	/ SPI1_CS0_M0	/	GPIO2_C0_d
I2S2_MCLK_M0	/ ETH0_REFCLKO_25M	/ UART7_RTSn_M0	/ SPI2_CLK_M0	/	GPIO2_C1_d
I2S2_SCLK_TX_M0	/ GMAC0_MCLKINOUT	/ UART7_CTSn_M0	/ SPI2_MISO_M0	/	GPIO2_C2_d
I2S2_LRCK_TX_M0	/ GMAC0_MDC	/ UART9_RTSn_M0	/ SPI2_MOSI_M0	/	GPIO2_C3_d
I2S2_SDO_M0	/ GMAC0_MDIO	/ UART9_CTSn_M0	/ SPI2_CS0_M0	/	GPIO2_C4_d
I2S2_SDI_M0	/ GMAC0_RXER	/ UART8_TX_M0	/ SPI2_CS1_M0	/	GPIO2_C5_d
CLK32K_OUT1		/ UART8_RX_M0	/ SPI1_CS1_M0	/	GPIO2_C6_d

RK3568
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E27 GPIO2_A3 → GMAC0_RXD2
E28 GPIO2_A4 → GMAC0_RXD3
B28 GPIO2_A5 → GMAC0_RXCLK
C27 GPIO2_A6 — R1500 1 2 22R 5% R0402 — GMAC0_TXD2
C28 GPIO2_A7 — R1501 1 2 22R 5% R0402 — GMAC0_TXD3
D27 GPIO2_B0 — R1503 1 2 22R 5% R0402 — GMAC0_TXCLK
D26 / E25 — TP204 TP_0.7, TP205 TP_0.7
F28 GPIO2_B3 — R1504 1 2 22R 5% R0402 — GMAC0_TXD0
G27 GPIO2_B4 — R1505 1 2 22R 5% R0402 — GMAC0_TXD1
G28 GPIO2_B5 — R1506 1 2 22R 5% R0402 — GMAC0_TXEN
F27 GPIO2_B6 → GMAC0_RXD0
H25 GPIO2_B7 → GMAC0_RXD1
F24 GPIO2_C0 → GMAC0_RXDV_CRS
G23 GPIO2_C1 — R1507 1 2 22R 5% R0402 — ETH0_REFCLKO_25M
F25 GPIO2_C2 → GMAC0_MCLKINOUT
H24 GPIO2_C3 — R1613 1 2 0R 5% R0402 — GMAC0_MDC
H23 GPIO2_C4 → GMAC0_MDIO
F26 GPIO2_C5 → GMAC0_RXER
E26 GPIO2_C6_d — TP202 TP_0.7

VCCIO4
J21 — R1509 1 2 0R 5% R0402 — VCC_1V8
J21 — R1511 1 2 0R 5% DNP R0402 — VCC_3V3
C1508 100nF X5R 10V C0201

Note:
If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

Note:
According to the actual choice of mounted Cannot be mounted at the same time
Default:1.8V
Select the voltage according to the application

GMAC0_TXEN — R1515 4.7K 5% R0402 DNP — GMAC0_RXER — TP203 TP_0.7

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_N(VCCIO7 Domain)

Note:
When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices

U1000N

VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PWM14_M1	/ SPI3_CLK_M1	/ CAN1_RX_M1	/ PCIE30X2_CLKREQn_M2	/ I2S3_MCLK_M1	/ GPIO4_C2_d
PWM15_IR_M1	/ SPI3_MOSI_M1	/ CAN1_TX_M1	/ PCIE30X2_WAKEn_M2	/ I2S3_SCLK_M1	/ GPIO4_C3_d
EDP_HPDIN_M0	/ SPDIF_TX_M2	/ SATA2_ACT_LED	/ PCIE30X2_PERSTn_M2	/ I2S3_LRCK_M1	/ GPIO4_C4_d
PWM12_M1	/ SPI3_MISO_M1	/ SATA1_ACT_LED	/ UART9_TX_M1	/ I2S3_SDO_M1	/ GPIO4_C5_d
PWM13_M1	/ SPI3_CS0_M1	/ SATA0_ACT_LED	/ UART9_RX_M1	/ I2S3_SDI_M1	/ GPIO4_C6_d
HDMITX_SCL	/ I2C5_SCL_M1				/ GPIO4_C7_u
HDMITX_SDA	/ I2C5_SDA_M1				/ GPIO4_D0_u
HDMITX_CEC_M0	/ SPI3_CS1_M1				/ GPIO4_D1_u
					GPIO4_D2_d

RK3568
BGA636_19R00X19R00X1R20

AF8 → PCIE30X2_CLKREQn_M2
AA11 → PCIE30X2_WAKEn_M2
AH7 → PCIE30X2_PERSTn_M2
AD8 → UART9_TX_M1
AE8 → UART9_RX_M1
AG8 → HDMITX_SCL
AG7 → HDMITX_SDA
AH6 → HDMITX_CEC_M0
AB9 → GPIO4_D2_d

VCCIO7 V12 — VCC_3V3 — C1509 100nF X5R 10V C0201

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_O(SARADC/OTP)

U1000O

SARADC

Recovery/

SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY	C1501 1nF X5R 50V C0402
SARADC_VIN1	C26	SARADC_VIN1_HW_ID	C1502 1nF X5R 50V C0402
SARADC_VIN2	D24	SARADC_VIN2_HP_HOOK	C1503 1nF X5R 50V C0402
SARADC_VIN3	E23	SARADC_VIN3_BOM_ID	C1504 1nF X5R 50V C0402
SARADC_VIN4	G21	SARADC_VIN4	C1505 1nF X5R 50V C0402
SARADC_VIN5	F22	SARADC_VIN5	C1506 1nF X5R 50V C0402
SARADC_VIN6	G20	SARADC_VIN6	C1507 1nF X5R 50V C0402
SARADC_VIN7	F21	SARADC_VIN7	C1508 1nF X5R 50V C0402

SARADC_AVDD_1V8 H22 — VCCA_1V8 — C1510 100nF X5R 10V C0201

OTP

OTP_VCC18 H20 — VCC_1V8 — C1511 100nF X5R 10V C0201

RK3568
BGA636_19R00X19R00X1R20

Note:
Must be mounted

VCCA_1V8 — R1512 10K 1% R0402 — SARADC_VIN0_KEY/RECOVERY

SARADC_VIN0_KEY/RECOVERY — TP1501 TP_0.7, TP1502 TP_0.7

Note:
If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

SARADC_VIN0_KEY/RECOVERY
SARADC_VIN1_HW_ID
SARADC_VIN2_HP_HOOK
SARADC_VIN3_BOM_ID
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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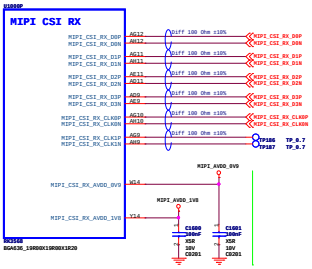
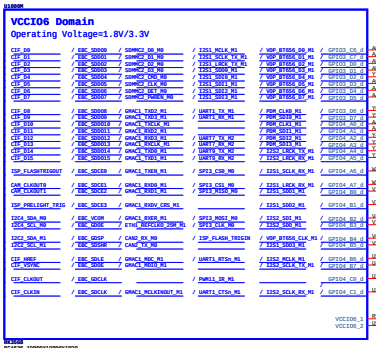
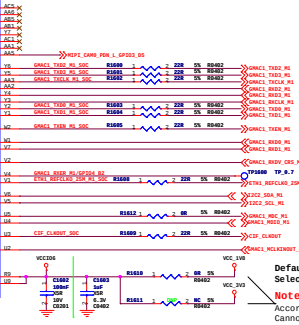
RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)





Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D8-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

Default:1.8V
Select the voltage according to the application

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_RXDV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx_XTALIN			
GMACx_MCLKINOUT	<-------	PHYx_CLKOUT(50M/25M)	GMACx_MCLKINOUT	------->	PHYx_XTALIN/REFCLK
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

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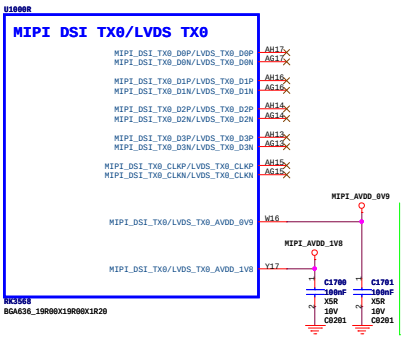
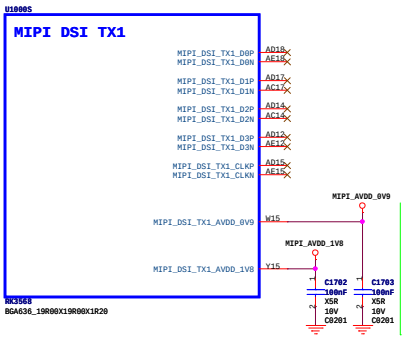
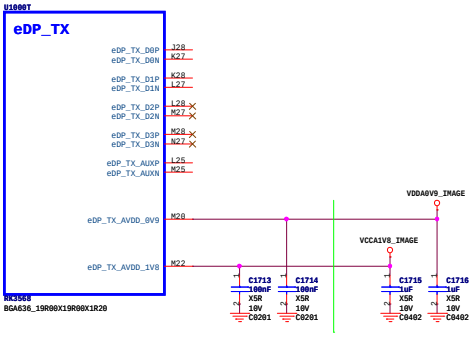
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

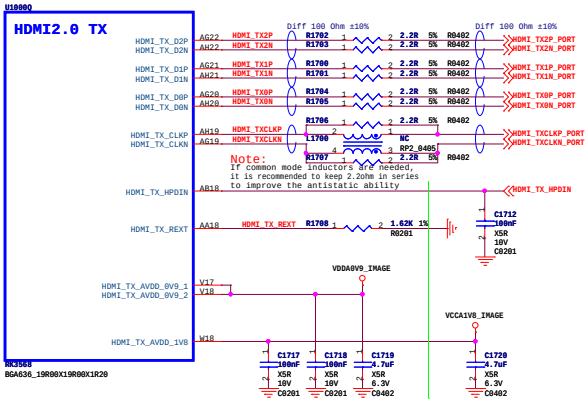


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



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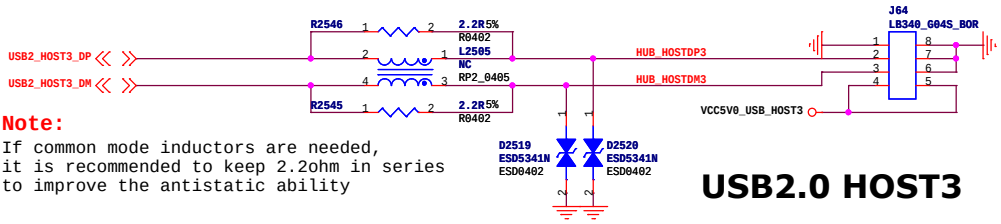
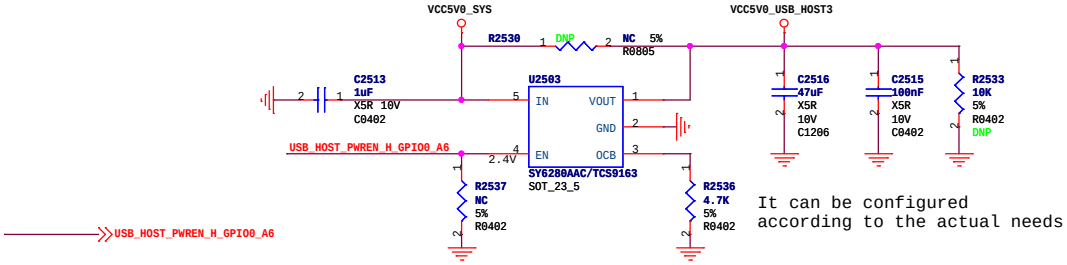


Note:

If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability

USB2.0 HOST3



It can be configured
according to the actual needs

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RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3568
BGA636_19R00X19R00X1R20

AG6	GPIO2_D0_d	PCIE20_CLKREQn_M1
AD7	GPIO2_D1_d	PCIE20_WAKEn_M1
AC8	GPIO2_D2_d	GPIO2_D2_d
AC7	GPIO2_D3_d	GPIO2_D3_d
AF5	GPIO2_D4_d	SPI2_CS1_M1
AF6	GPIO2_D5_d	SPI2_CS0_M1
AD6	GPIO2_D6_d	SPI2_MOSI_M1
AH5	GPIO2_D7_d	SPI2_MISO_M1
AH4	GPIO3_A0_d	SPI2_CLK_M1
AB8	GPIO3_A1_d	GPIO3_A1_d
AE5	GPIO3_A2_d	I2S3_MCLK_M0
AG4	GPIO3_A3_d	I2S3_SCLK_M0
AF4	GPIO3_A4_d	I2S3_LRCK_M0
AH3	GPIO3_A5_d	I2S3_SDO_M0
AG3	GPIO3_A6_d	I2S3_SDI_M0
AH2	GPIO3_A7_d	GMAC1_INT/PMEB_GPIO3_A7
AG2	GPIO3_B0_d	GMAC1_RSTn_GPIO3_B0
AG1	GPIO3_B1_d	UART4_RX_M1
AF2	GPIO3_B2_d	UART4_TX_M1
AF1	GPIO3_B3_d	I2C5_SCL_M0
AE1	GPIO3_B4_d	I2C5_SDA_M0
AE2	GPIO3_B5_d	GPIO3_B5_d
AE3	GPIO3_B6_d	PWM11_IR_M0
AD4	GPIO3_B7	GMAC0_RSTn_GPIO3_B7
AD2	GPIO3_C0_d	GMAC0_INT/PMEB_GPIO3_C0
AD1	GPIO3_C1_d	PCIE20_PERSTn_M1
AA7	GPIO3_C2_d	HP_DET_L_GPIO3_C2
AC4	GPIO3_C3_d	GPIO3_C3_d
AC3	GPIO3_C4_d	UART7_TX_M1
AC2	GPIO3_C5_d	UART7_RX_M1

VCC_3V3

VCCIO5_1 V10
VCCIO5_2 V11

C1800 100nF X5R 10V C0201

VCC_3V3

R1800 10K 5% R0402 — GMAC0_INT/PMEB_GPIO3_C0
R1801 10K 5% R0402 — GMAC1_INT/PMEB_GPIO3_A7

VCC_3V3

R1804 2.2K 5% R0402 — I2C5_SCL_M0
R1805 2.2K 5% R0402 — I2C5_SDA_M0

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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RK3568_H(VCCIO1 Domain)

U1000H

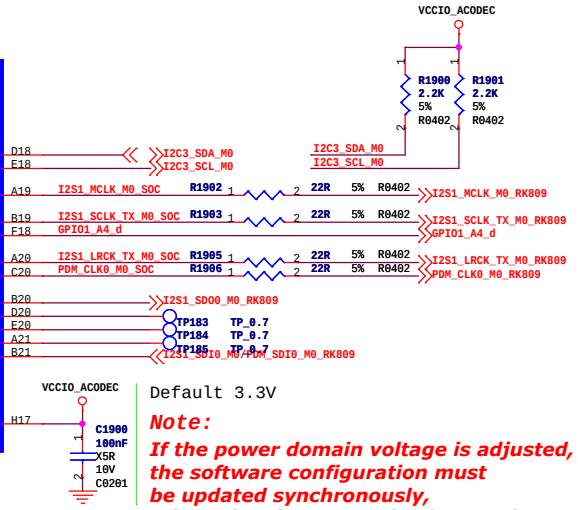
VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0		/ CAN1_RX_M0		/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0		/ CAN1_TX_M0		/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0		/ SCR_CLK	/ PCIE30X1_PERSTn_M2			/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0		/ SCR_IO	/ PCIE30X1_WAKEn_M2		/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0			/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0		/ SCR_RST	/ PCIE30X1_CLKREQn_M2		/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0			/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0		/ SCR_DET		/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0		/ PCIE20_CLKREQn_M2		/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0		/ PCIE20_WAKEn_M2		/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0		/ PCIE20_PERSTn_M2			/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0					/ GPIO1_B3_d

VCCIO1

RK3568
BGA636_19R00X19R00X1R20



Default 3.3V

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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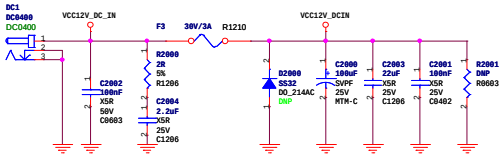
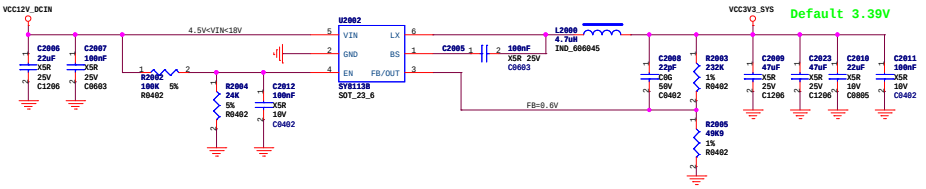
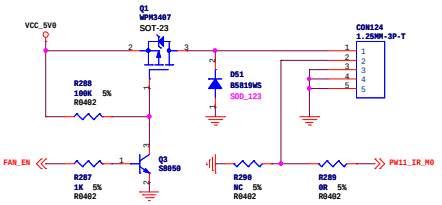
12V/3A DCIN

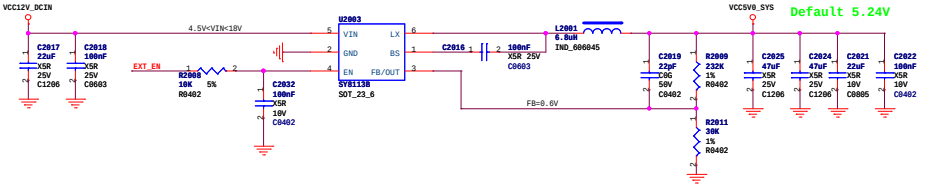


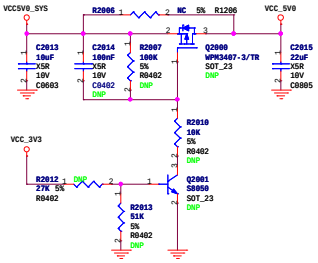
VCC3V3_SYS





VCC5V0_SYS





EXT_EN

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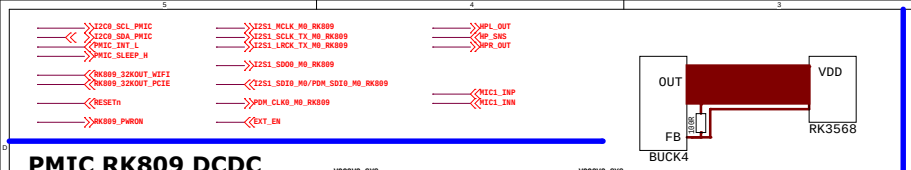
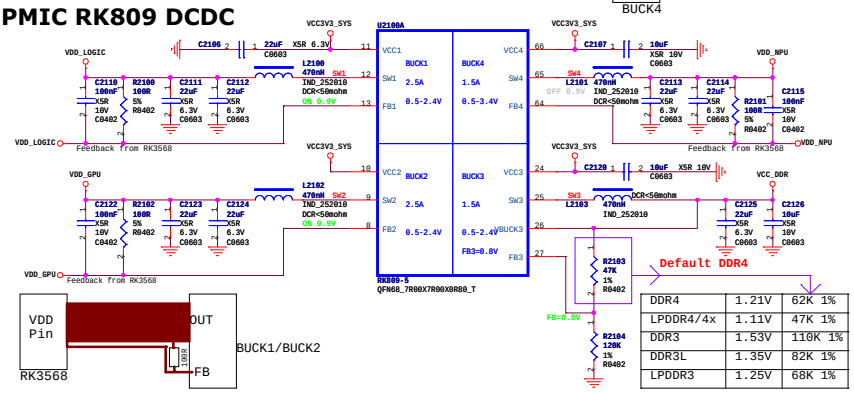
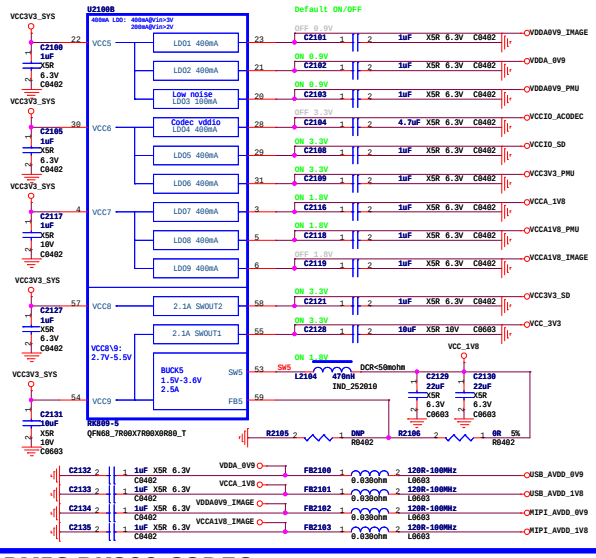


PMIC RK809 DCDC

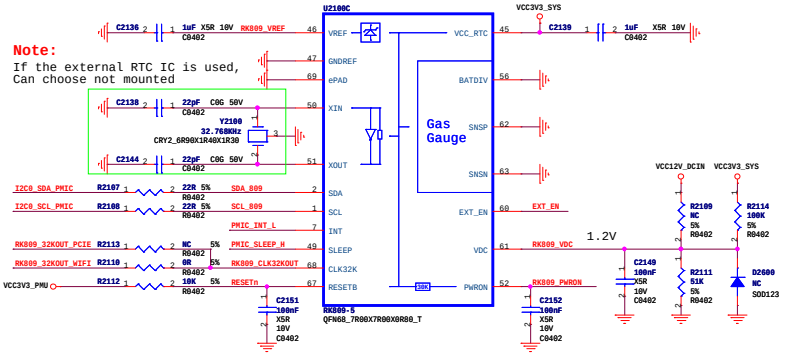


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

PMIC RK809 LDO



PMIC RK809 Managerment



Note:
If the external RTC IC is used,
Can choose not mounted

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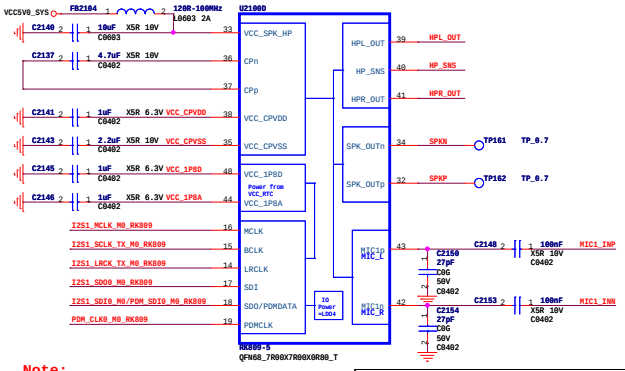
PMIC RK809 CODEC



Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

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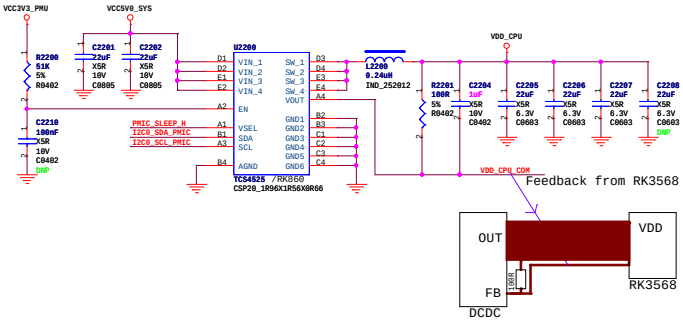
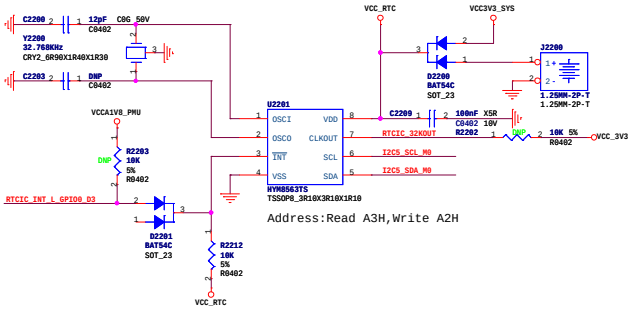
VDD_CPU



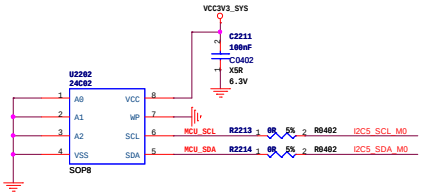
RTC IC --Option

Note:

The power off hold time scheme is required,
It is recommended to use external RTC IC
But, it will not support the timing poweron function



Address:Read A3H,Write A2H



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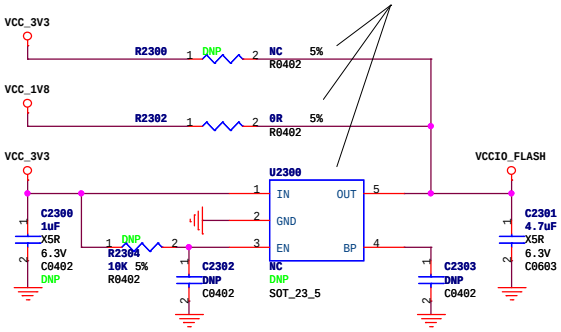
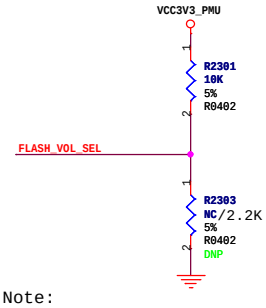
FLASH_VOL_SEL

Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:
According to the actual choice of mounted
Cannot be mounted at the same time





Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

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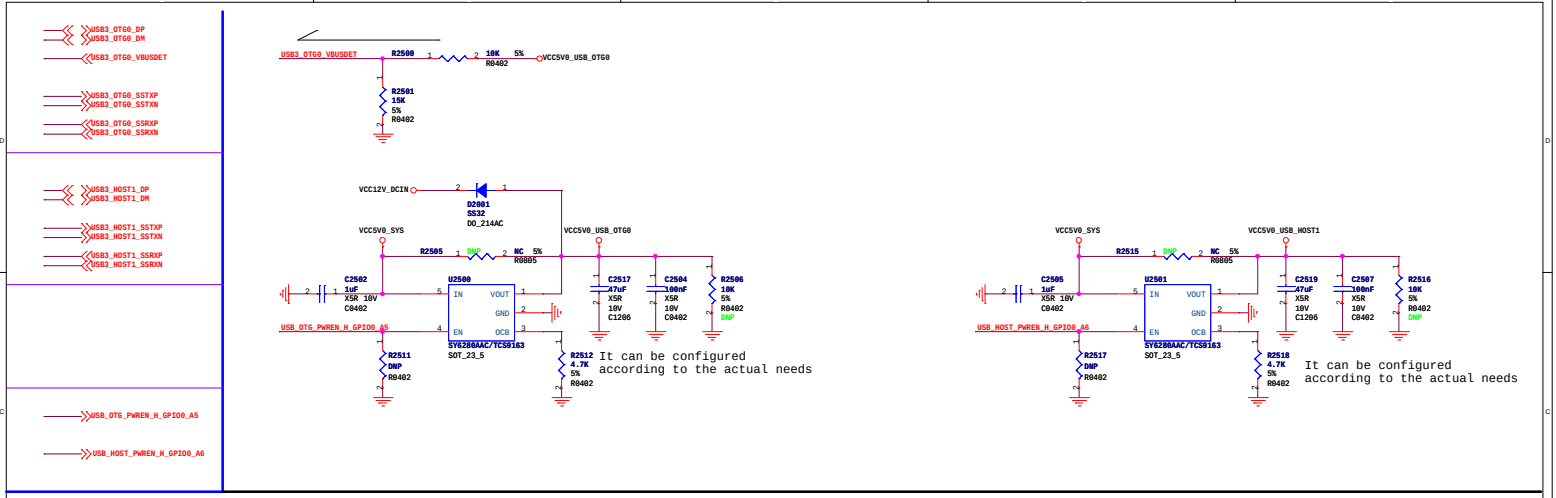
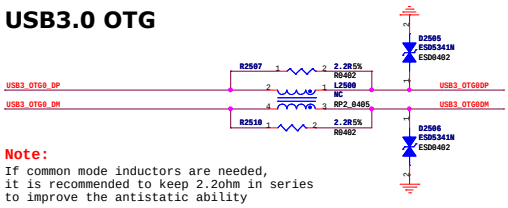
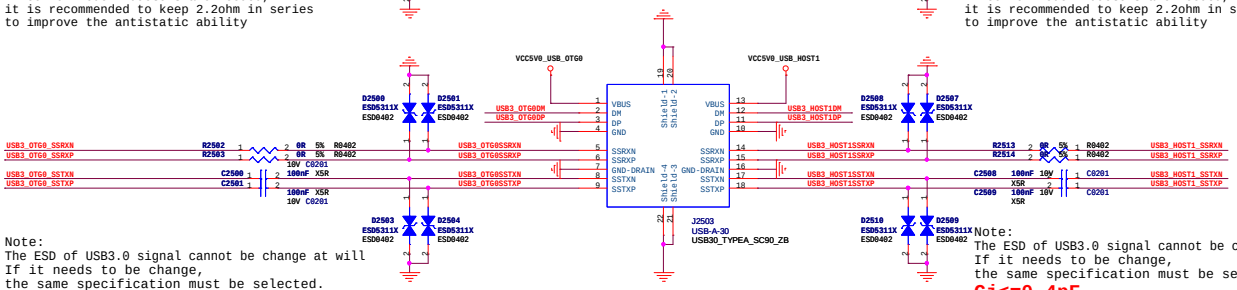


USB3.0 OTG

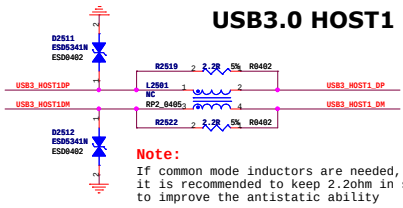


Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability



Note:
The ESD of USB3.0 signal cannot be change at will
If it needs to be change,
the same specification must be selected.
Cj<=0.4pF

USB3.0 HOST1



Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability

Note:
The ESD of USB3.0 signal cannot be change at will
If it needs to be change,
the same specification must be selected.
Cj<=0.4pF

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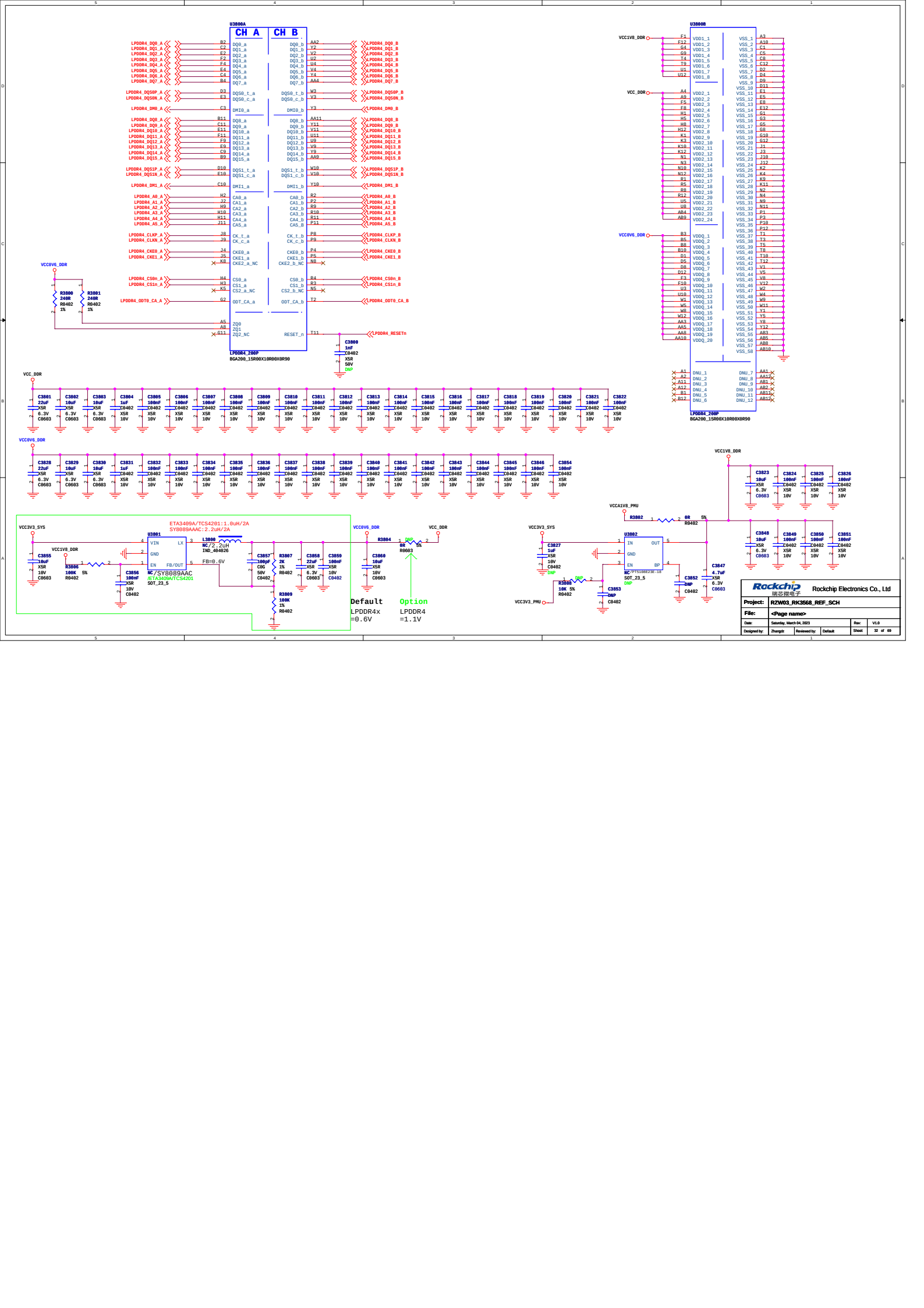
U3800A
CH A
CH B
LPDDR4_DQ0_A
LPDDR4_DQ1_A
LPDDR4_DQ2_A
LPDDR4_DQ3_A
LPDDR4_DQ4_A
LPDDR4_DQ5_A
LPDDR4_DQ6_A
LPDDR4_DQ7_A
LPDDR4_DQS0P_A
LPDDR4_DQS0N_A
LPDDR4_DM0_A
LPDDR4_DQ8_A
LPDDR4_DQ9_A
LPDDR4_DQ10_A
LPDDR4_DQ11_A
LPDDR4_DQ12_A
LPDDR4_DQ13_A
LPDDR4_DQ14_A
LPDDR4_DQ15_A
LPDDR4_DQS1P_A
LPDDR4_DQS1N_A
LPDDR4_DM1_A
LPDDR4_A0_A
LPDDR4_A1_A
LPDDR4_A2_A
LPDDR4_A3_A
LPDDR4_A4_A
LPDDR4_A5_A
LPDDR4_CLKP_A
LPDDR4_CLKN_A
LPDDR4_CKE0_A
LPDDR4_CKE1_A
LPDDR4_CS0n_A
LPDDR4_CS1n_A
LPDDR4_ODT0_CA_A
LPDDR4_DQ0_B
LPDDR4_DQ1_B
LPDDR4_DQ2_B
LPDDR4_DQ3_B
LPDDR4_DQ4_B
LPDDR4_DQ5_B
LPDDR4_DQ6_B
LPDDR4_DQ7_B
LPDDR4_DQS0P_B
LPDDR4_DQS0N_B
LPDDR4_DM0_B
LPDDR4_DQ8_B
LPDDR4_DQ9_B
LPDDR4_DQ10_B
LPDDR4_DQ11_B
LPDDR4_DQ12_B
LPDDR4_DQ13_B
LPDDR4_DQ14_B
LPDDR4_DQ15_B
LPDDR4_DQS1P_B
LPDDR4_DQS1N_B
LPDDR4_DM1_B
LPDDR4_A0_B
LPDDR4_A1_B
LPDDR4_A2_B
LPDDR4_A3_B
LPDDR4_A4_B
LPDDR4_A5_B
LPDDR4_CLKP_B
LPDDR4_CLKN_B
LPDDR4_CKE0_B
LPDDR4_CKE1_B
LPDDR4_CS0n_B
LPDDR4_CS1n_B
LPDDR4_ODT0_CA_B
LPDDR4_RESETn
ZQ0
ZQ1
ZQ2_NC
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC0V6_DDR
R3800 240R R0402 1%
R3801 240R R0402 1%
C3800 1nF C0402 X5R 50V DNP
U3800B
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
VDD1_1
VDD1_2
VDD1_3
VDD1_4
VDD1_5
VDD1_6
VDD1_7
VDD1_8
VDD2_1
VDD2_2
VDD2_3
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VSS_58
DNU_1
DNU_2
DNU_3
DNU_4
DNU_5
DNU_6
DNU_7
DNU_8
DNU_9
DNU_10
DNU_11
DNU_12
LPDDR4_200P
BGA200_15R00X10R00X0R90
C3801 22uF X5R 6.3V C0603
C3802 10uF X5R 6.3V C0603
C3803 10uF X5R 6.3V C0603
C3804 1uF X5R 10V C0402
C3805 100nF X5R 10V C0402
C3806 100nF X5R 10V C0402
C3807 100nF X5R 10V C0402
C3808 100nF X5R 10V C0402
C3809 100nF X5R 10V C0402
C3810 100nF X5R 10V C0402
C3811 100nF X5R 10V C0402
C3812 100nF X5R 10V C0402
C3813 100nF X5R 10V C0402
C3814 100nF X5R 10V C0402
C3815 100nF X5R 10V C0402
C3816 100nF X5R 10V C0402
C3817 100nF X5R 10V C0402
C3818 100nF X5R 10V C0402
C3819 100nF X5R 10V C0402
C3820 100nF X5R 10V C0402
C3821 100nF X5R 10V C0402
C3822 100nF X5R 10V C0402
C3828 22uF X5R 6.3V C0603
C3829 10uF X5R 6.3V C0603
C3830 10uF X5R 6.3V C0603
C3831 1uF X5R 10V C0402
C3832 100nF X5R 10V C0402
C3833 100nF X5R 10V C0402
C3834 100nF X5R 10V C0402
C3835 100nF X5R 10V C0402
C3836 100nF X5R 10V C0402
C3837 100nF X5R 10V C0402
C3838 100nF X5R 10V C0402
C3839 100nF X5R 10V C0402
C3840 100nF X5R 10V C0402
C3841 100nF X5R 10V C0402
C3842 100nF X5R 10V C0402
C3843 100nF X5R 10V C0402
C3844 100nF X5R 10V C0402
C3845 100nF X5R 10V C0402
C3846 100nF X5R 10V C0402
C3854 100nF X5R 10V C0402
VCCA1V8_PMU
R3802 0R R0402 5%
C3823 10uF X5R 6.3V C0603
C3824 100nF X5R 10V C0402
C3825 100nF X5R 10V C0402
C3826 100nF X5R 10V C0402
C3848 10uF X5R 6.3V C0603
C3849 100nF X5R 10V C0402
C3850 100nF X5R 10V C0402
C3851 100nF X5R 10V C0402
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
VCC3V3_SYS
VCC1V8_DDR
U3801
VIN
LX
GND
EN
FB/OUT
NC/SY8089AAC
ETA3409A/TCS4201
SOT_23_5
L3800 NC/2.2uH IND_404026
FB=0.6V
C3855 10uF X5R 10V C0603
R3806 100K R0402 5%
C3856 100nF X5R 10V C0402
C3857 100pF C0G 50V C0402
R3807 2K 1% R0402
C3858 22uF X5R 6.3V C0603
C3859 100nF X5R 10V C0402
R3809 100K 1% R0402
VCC0V6_DDR
VCC_DDR
R3804 0R R0603 5% DNP
C3860 10uF X5R 10V C0603
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
VCC3V3_SYS
VCC3V3_PMU
C3827 1uF X5R 10V C0402 DNP
U3802
IN
OUT
GND
EN
BP
NC/PTS108E23E-18
SOT_23_5 DNP
R3808 10K 5% R0402 DNP
C3853 DNP C0402
C3852 DNP C0402
C3847 4.7uF X5R 6.3V C0603
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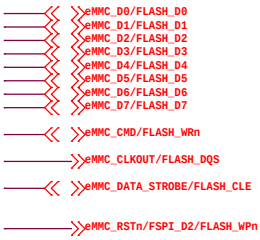
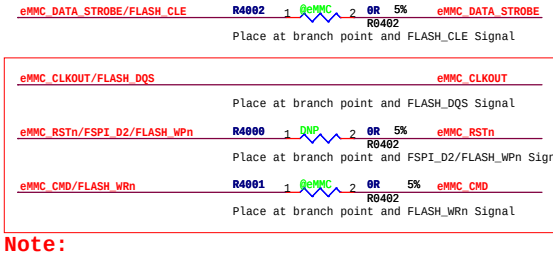
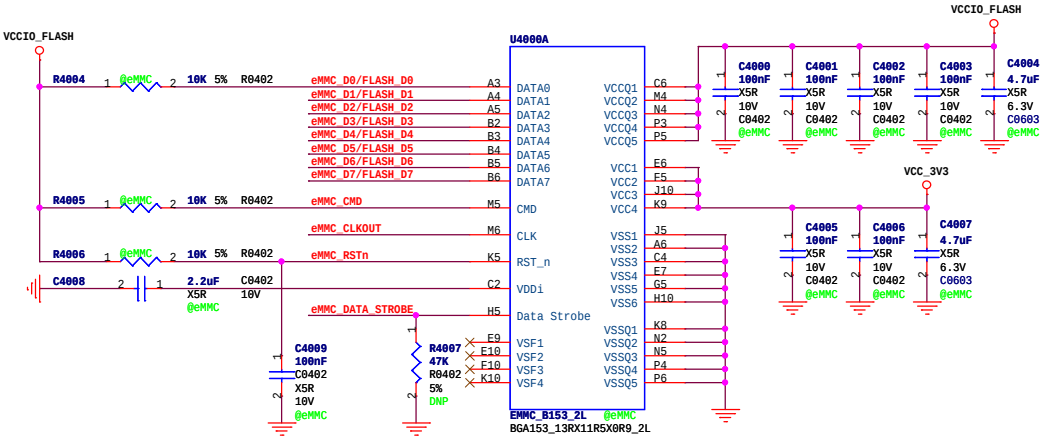
eMMC Flash

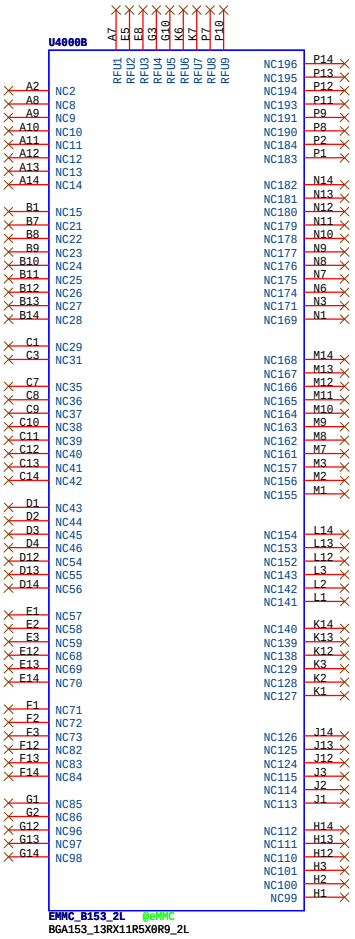




Note:

No need to double layout with Nand Flash, 0R resistor can be omitted





Note:

If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

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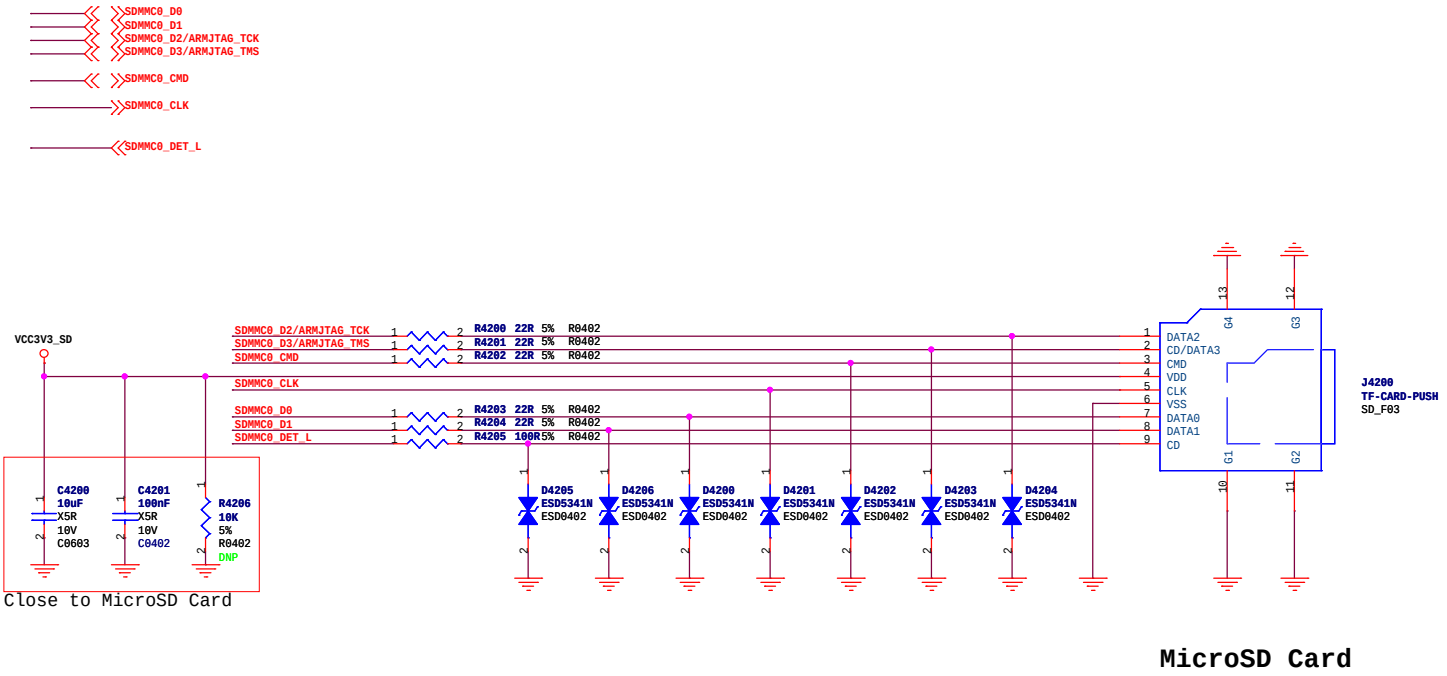
MicroSD Card



MicroSD Card

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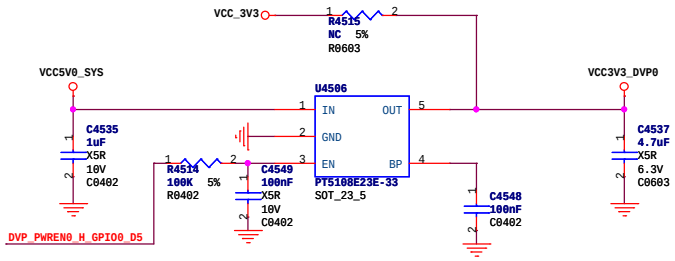
DVP_PWREN0_H_GPIO0_D5



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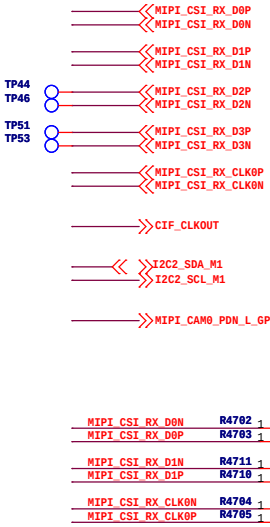
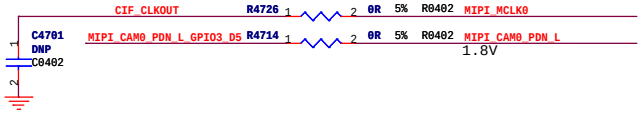
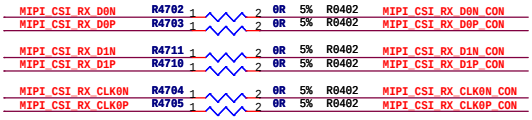
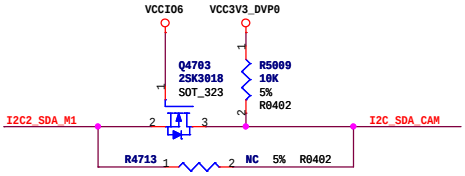
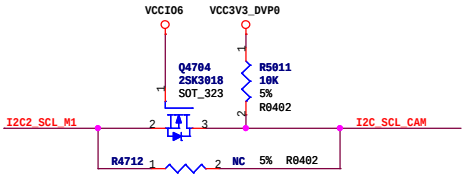
Camera0:MIPI_CSI_RX 2Lanes



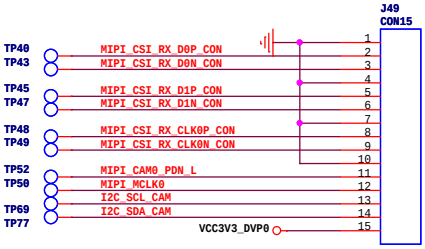


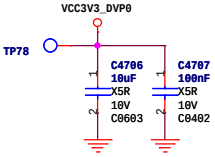






MIPI-CSI_RX CON





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HDMI2.0 TX

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT

HDMITX_SCL
HDMITX_SDA

HDMITX_CEC_M0
HDMI_TX_HPDIN

Cj<=0.4pF

U5000
ESD5344D
SON10_2R50X1R00X0R50

U5001 ESD5344D SON10_2R50X1R00X0R50

HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
HDMI_TX_HPD_PORT

VCC5V_HDMI_TX

ED5000 ESD5341N ESD0402
ED5001 ESD5341N ESD0402
ED5002 ESD5341N ESD0402
ED5003 ESD5341N ESD0402

C5000 1uF X5R 10V C0402

J5000 HDMI_TYPE_A HDMI\YKF45-7012-1

HDMI TX DDC

VCC_5V0
D5000 B5819WS SOD_123
VCC_3V3
R5000 10K 5% R0402
Q5000 2SK3018 SOT_323
R5001 1.8K 5% R0402
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
VCC_3V3
R5002 10K 5% R0402
Q5001 2SK3018 SOT_323
R5003 1.8K 5% R0402
HDMITX_SDA
HDMI_TXDDC_SDA_PORT

HDMI TX CEC

VCC_3V3
VCC_5V0
R5006 27K 5% R0402
Q5002 2SK3018 SOT_323
HDMITX_CEC_M0
HDMI_TX_CEC_PORT

HDMI TX HPD

HDMI_TX_HPDIN
R5005 1K 5% R0402
HDMI_TX_HPD_PORT
R5007 100K 5% R0402

VCC_5V0
VCC5V_HDMI_TX
D5001 B5819W SOD_123
R5004 DNP NC 5% R0402

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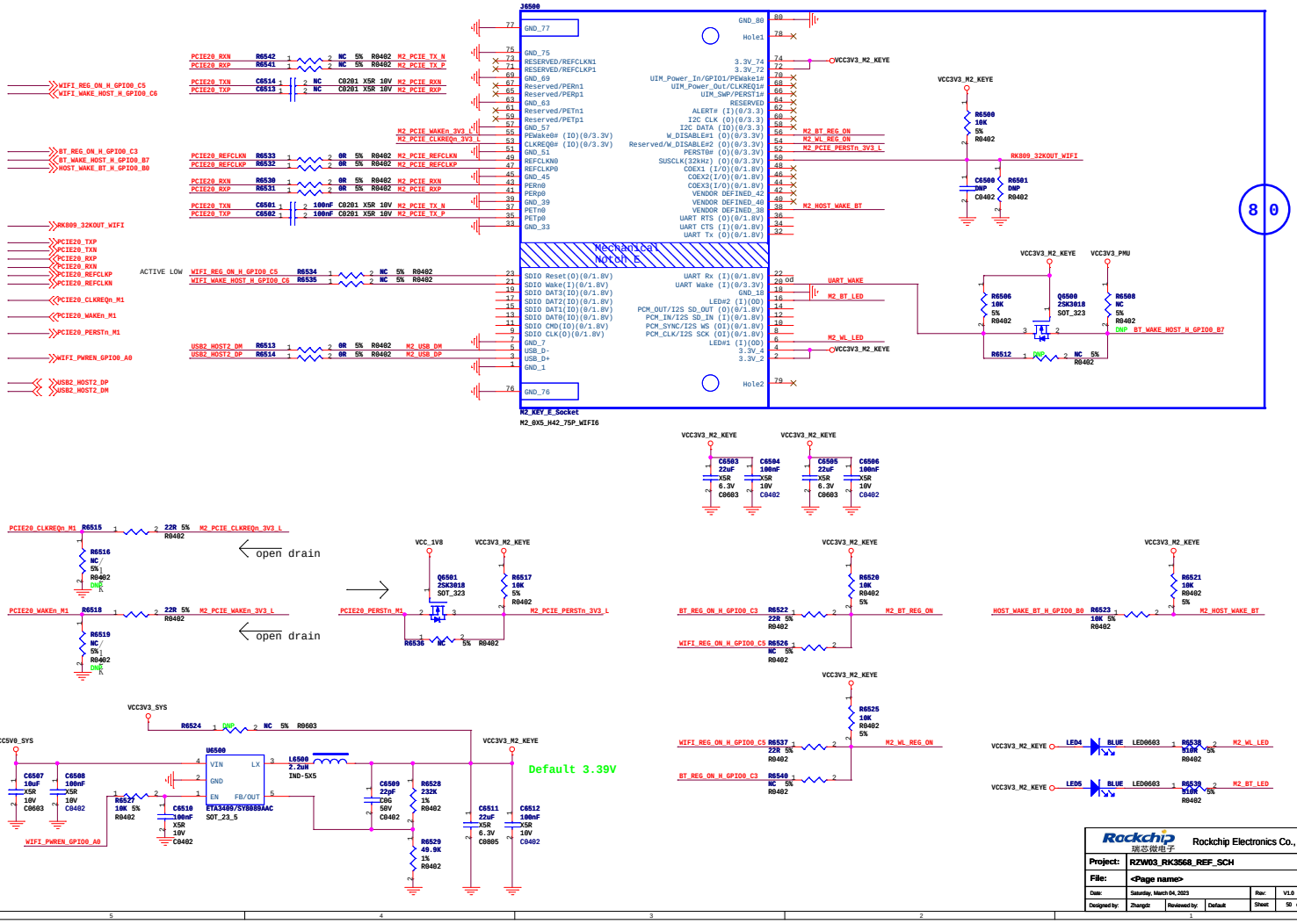
WIFI/BT-M.2_KEY_E



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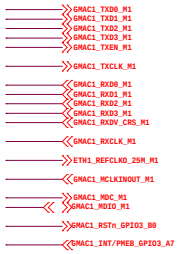
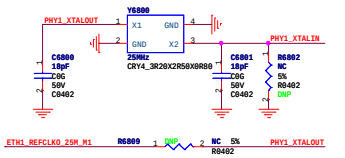
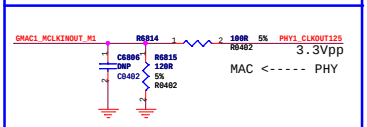
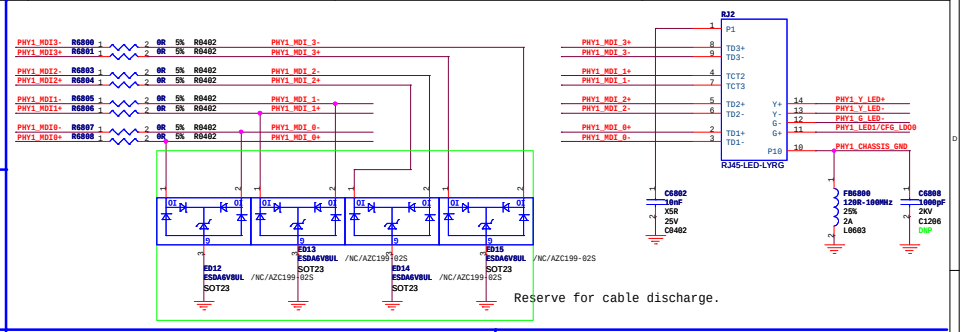
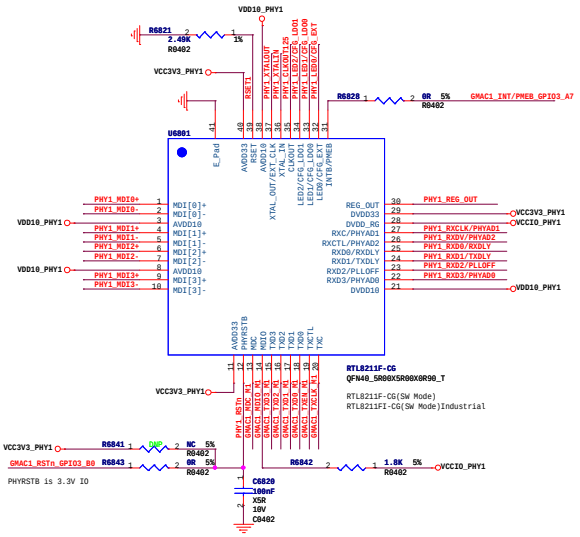
Giga PHY1

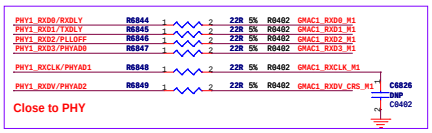


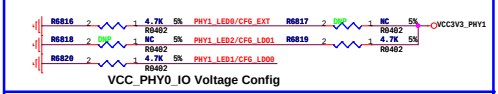


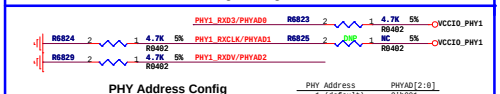


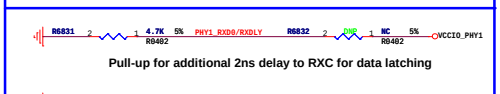


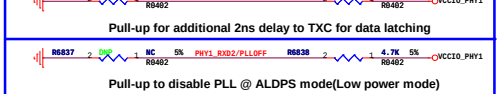


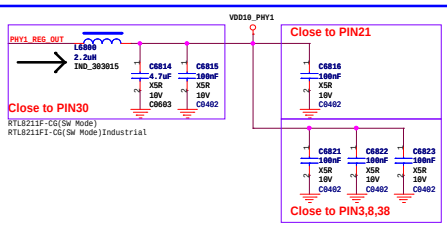




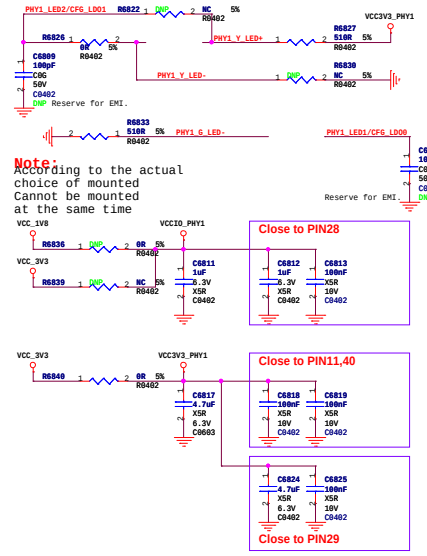








RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	



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Giga PHY0

GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
ETH0_REFCLKO_25M
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
GMAC0_RSTn_GPIO3_B7
GMAC0_INT/PMEB_GPIO3_C0

PHY0_XTALOUT — Y6700 (X1 GND X2) 25MHz CRY4_3R20X2R50X0R000 — PHY0_XTALIN
C6700 18pF C0G 50V C0402
C6701 18pF C0G 50V C0402
R6703 NC 5% R0402 DNP
ETH0_REFCLKO_25M — R6709 DNP NC 5% R0402 — PHY0_XTALOUT

GMAC0_MCLKINOUT — R6714 100R 5% R0402 — PHY0_CLKOUT125
C6706 DNP C0402
R6715 120R 5% R0402
3.3Vpp
MAC <----- PHY

PHY0_MDI3- R6700 0R 5% R0402 PHY0_MDI_3-
PHY0_MDI3+ R6701 0R 5% R0402 PHY0_MDI_3+
PHY0_MDI2- R6702 0R 5% R0402 PHY0_MDI_2-
PHY0_MDI2+ R6704 0R 5% R0402 PHY0_MDI_2+
PHY0_MDI1- R6705 0R 5% R0402 PHY0_MDI_1-
PHY0_MDI1+ R6706 0R 5% R0402 PHY0_MDI_1+
PHY0_MDI0- R6707 0R 5% R0402 PHY0_MDI_0-
PHY0_MDI0+ R6708 0R 5% R0402 PHY0_MDI_0+

ED16 ESDA6V8UL /NC/AZC199-02S SOT23
ED17 ESDA6V8UL /NC/AZC199-02S SOT23
ED18 ESDA6V8UL /NC/AZC199-02S SOT23
ED19 ESDA6V8UL /NC/AZC199-02S SOT23

RJ1 RJ45-LED-LYRG
PHY0_MDI_3+ PHY0_MDI_3- PHY0_MDI_1+ PHY0_MDI_1- PHY0_MDI_2+ PHY0_MDI_2- PHY0_MDI_0+ PHY0_MDI_0-
PHY0_Y_LED+ PHY0_Y_LED- PHY0_G_LED- PHY0_LED1/CFG_LDO0 PHY0_CHASSIS_GND
C6702 10nF X5R 25V C0402
FB6700 120R-100MHz 25% 2A L0603
C6708 1000pF 2KV C1206 DNP

Reserve for cable discharge.

VDD10_PHY0
R6721 2.49K 1% R0402
VCC3V3_PHY0
R6723 0R 5% R0402 GMAC0_INT/PMEB_GPIO3_C0 od
U6701
E_Pad
PHY0_MDI0+ PHY0_MDI0- PHY0_MDI1+ PHY0_MDI1- PHY0_MDI2+ PHY0_MDI2- PHY0_MDI3+ PHY0_MDI3-
MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]-
REG_OUT DVDD33 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10
PHY0_REG_OUT VCC3V3_PHY0 VCCIO_PHY0 PHY0_RXCLK/PHYAD1 PHY0_RXDV/PHYAD2 PHY0_RXD0/RXDLY PHY0_RXD1/TXDLY PHY0_RXD2/PLLOFF PHY0_RXD3/PHYAD0 VDD10_PHY0
AVDD33 RSET AVDD18 PHYRSTB XTAL_IN XTAL_OUT LED2/CFG_LDO1 CLKOUT LED1/CFG_LDO0 LED0/CFG_EXT INTB/PMEB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL RTL8211F-CG QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode) RTL8211FI-CG(SW Mode)Industrial
PHY0_RSTn GMAC0_MDC GMAC0_MDIO GMAC0_TXD3 GMAC0_TXD2 GMAC0_TXD1 GMAC0_TXD0 GMAC0_TXCTL GMAC0_TXCLK
VCC3V3_PHY0
R6741 DNP NC 5% R0402
R6742 1.8K 5% R0402 VCCIO_PHY0
GMAC0_RSTn_GPIO3_B7 R6743 0R 5% R0402
C6720 100nF X5R 10V C0402
PHYRSTB is 3.3V IO

PHY0_RXD0/RXDLY R6744 22R 5% R0402 GMAC0_RXD0
PHY0_RXD1/TXDLY R6745 22R 5% R0402 GMAC0_RXD1
PHY0_RXD2/PLLOFF R6746 22R 5% R0402 GMAC0_RXD2
PHY0_RXD3/PHYAD0 R6747 22R 5% R0402 GMAC0_RXD3
PHY0_RXCLK/PHYAD1 R6748 22R 5% R0402 GMAC0_RXCLK
PHY0_RXDV/PHYAD2 R6749 22R 5% R0402 GMAC0_RXDV_CRS
C6726 DNP C0402
Close to PHY

R6716 4.7K 5% R0402 PHY0_LED0/CFG_EXT R6717 DNP NC 5% R0402 VCC3V3_PHY0
R6718 DNP NC 5% R0402 PHY0_LED2/CFG_LDO1 R6719 4.7K 5% R0402
R6720 4.7K 5% R0402 PHY0_LED1/CFG_LDO0
VCC_PHY0_IO Voltage Config

R6724 DNP NC 5% R0402 PHY0_RXD3/PHYAD0 R6725 4.7K 5% R0402 VCCIO_PHY0
R6726 4.7K 5% R0402 PHY0_RXCLK/PHYAD1
R6729 4.7K 5% R0402 PHY0_RXDV/PHYAD2
PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

R6731 4.7K 5% R0402 PHY0_RXD0/RXDLY R6732 DNP NC 5% R0402 VCCIO_PHY0
Pull-up for additional 2ns delay to RXC for data latching

R6734 4.7K 5% R0402 PHY0_RXD1/TXDLY R6735 DNP NC 5% R0402 VCCIO_PHY0
Pull-up for additional 2ns delay to TXC for data latching

R6737 DNP NC 5% R0402 PHY0_RXD2/PLLOFF R6738 4.7K 5% R0402 VCCIO_PHY0
Pull-up to disable PLL @ ALDPS mode(Low power mode)

VDD10_PHY0
PHY0_REG_OUT — L6700 2.2uH IND_303015 — C6715 4.7uF X5R 10V C0603, C6716 100nF X5R 10V C0402
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
Close to PIN21
C6717 100nF X5R 10V C0402
Close to PIN3,8,38
C6723 100nF X5R 10V C0402
C6724 100nF X5R 10V C0402
C6725 100nF X5R 10V C0402

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	

PHY0_LED2/CFG_LDO1 R6722 DNP NC 5% R0402
R6727 0R 5% R0402
C6709 100pF C0G 50V C0402 DNP Reserve for EMI.
VCC3V3_PHY0
R6728 510R 5% R0402
PHY0_Y_LED+
PHY0_Y_LED-
R6730 NC 5% R0402 DNP
R6733 510R 5% R0402
PHY0_G_LED-
PHY0_LED1/CFG_LDO0
C6710 100pF C0G 50V C0402 DNP Reserve for EMI.

Note:
According to the actual choice of mounted Cannot be mounted at the same time

VCC_1V8 — R6736 DNP 0R 5% R0402 — VCCIO_PHY0
VCC_3V3 — R6739 DNP NC 5% R0402
C6711 4.7uF X5R 10V C0603
Close to PIN28
C6712 1uF X5R 10V C0402
C6713 100nF X5R 10V C0402

VCC_3V3 — R6740 0R 5% R0402 — VCC3V3_PHY0
C6718 4.7uF X5R 10V C0603
Close to PIN11,40
C6719 100nF X5R 10V C0402
C6714 100nF X5R 10V C0402
C6721 4.7uF X5R 10V C0603
C6722 100nF X5R 10V C0402
Close to PIN29

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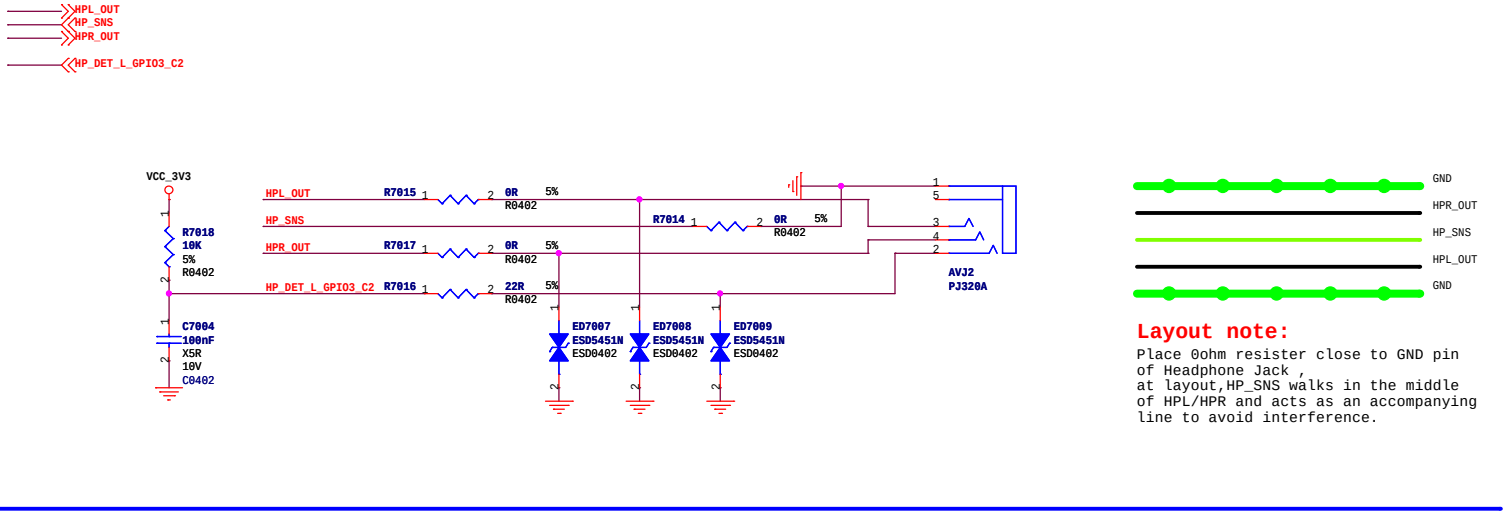

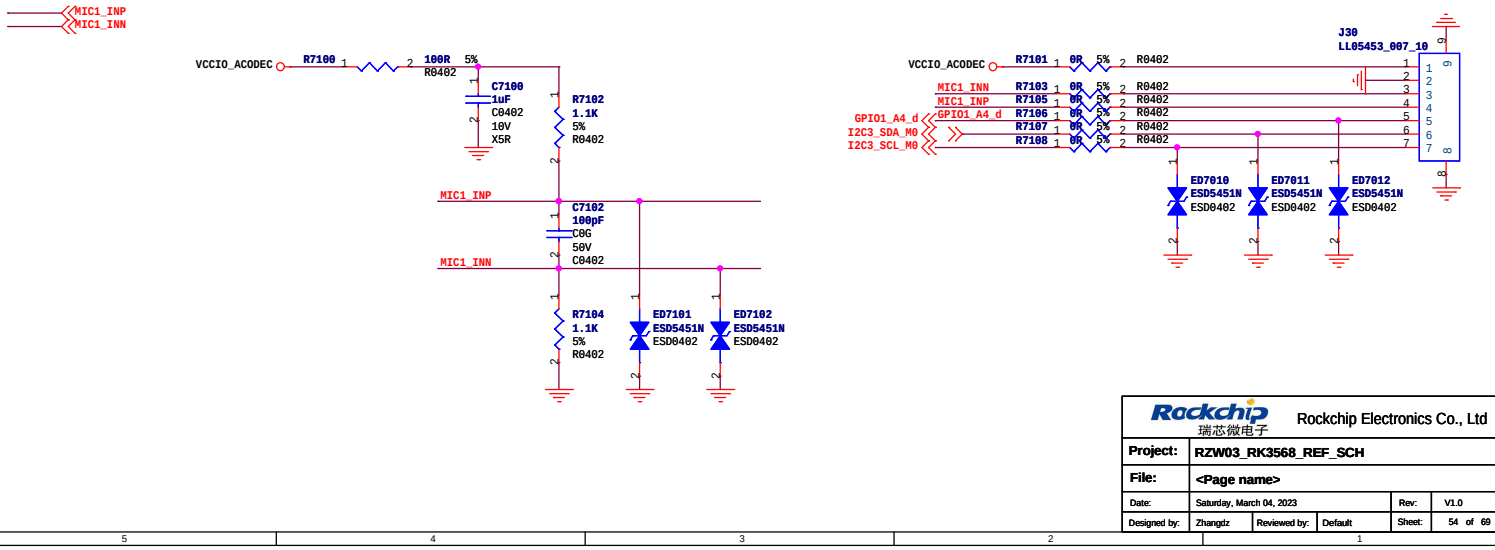

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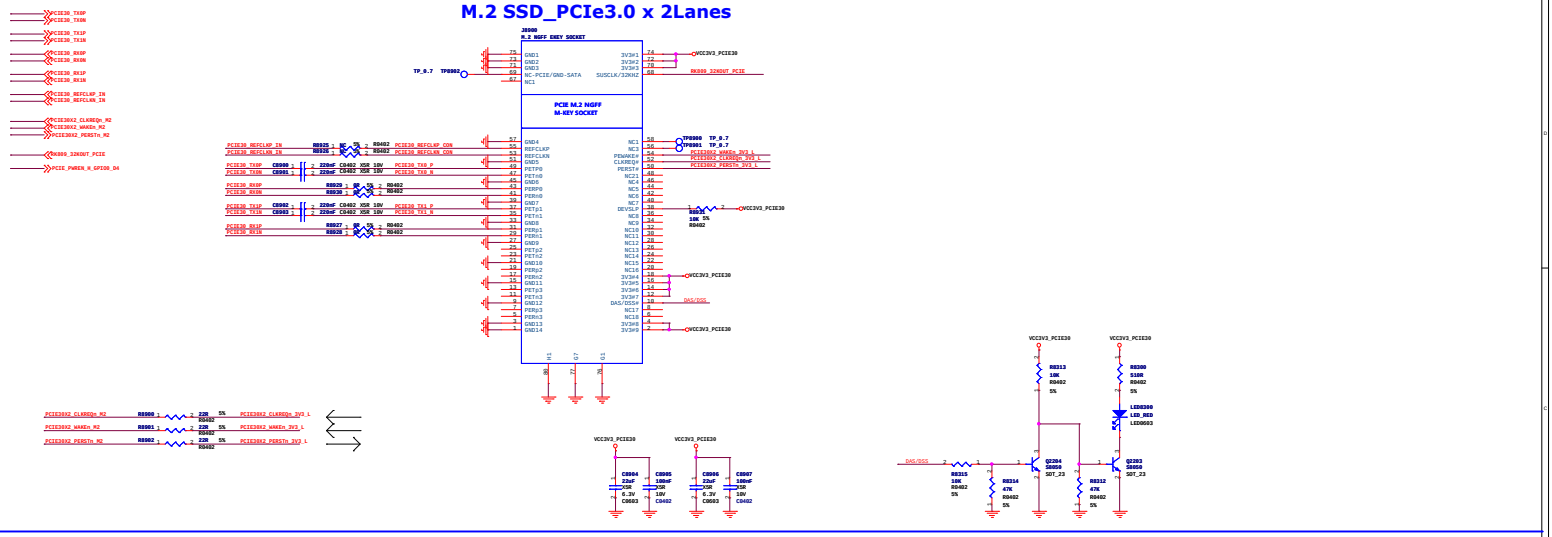
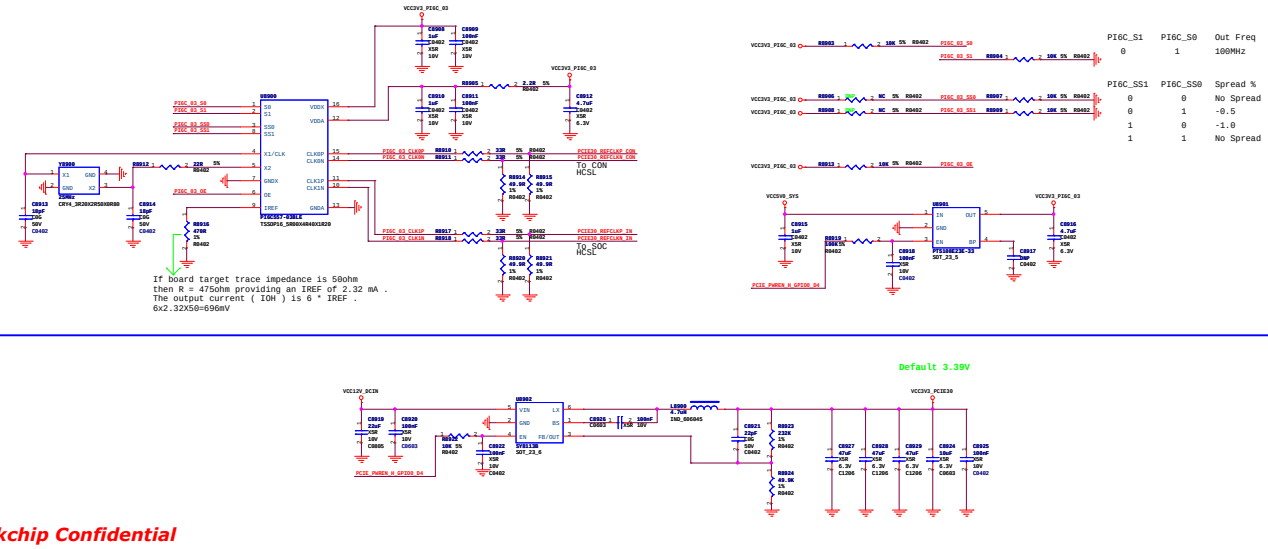
M.2 SSD_PCIe3.0 x 2Lanes





PI6C_S1	PI6C_S0	Out Freq
0	1	100MHz

PI6C_SS1	PI6C_SS0	Spread %
0	0	No Spread
0	1	-0.5
1	0	-1.0
1	1	No Spread

Default 3.39V

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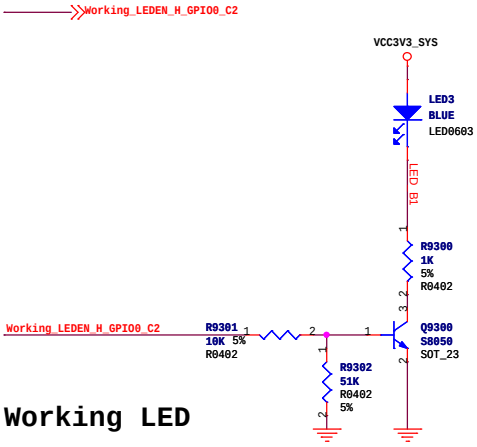

Working LED

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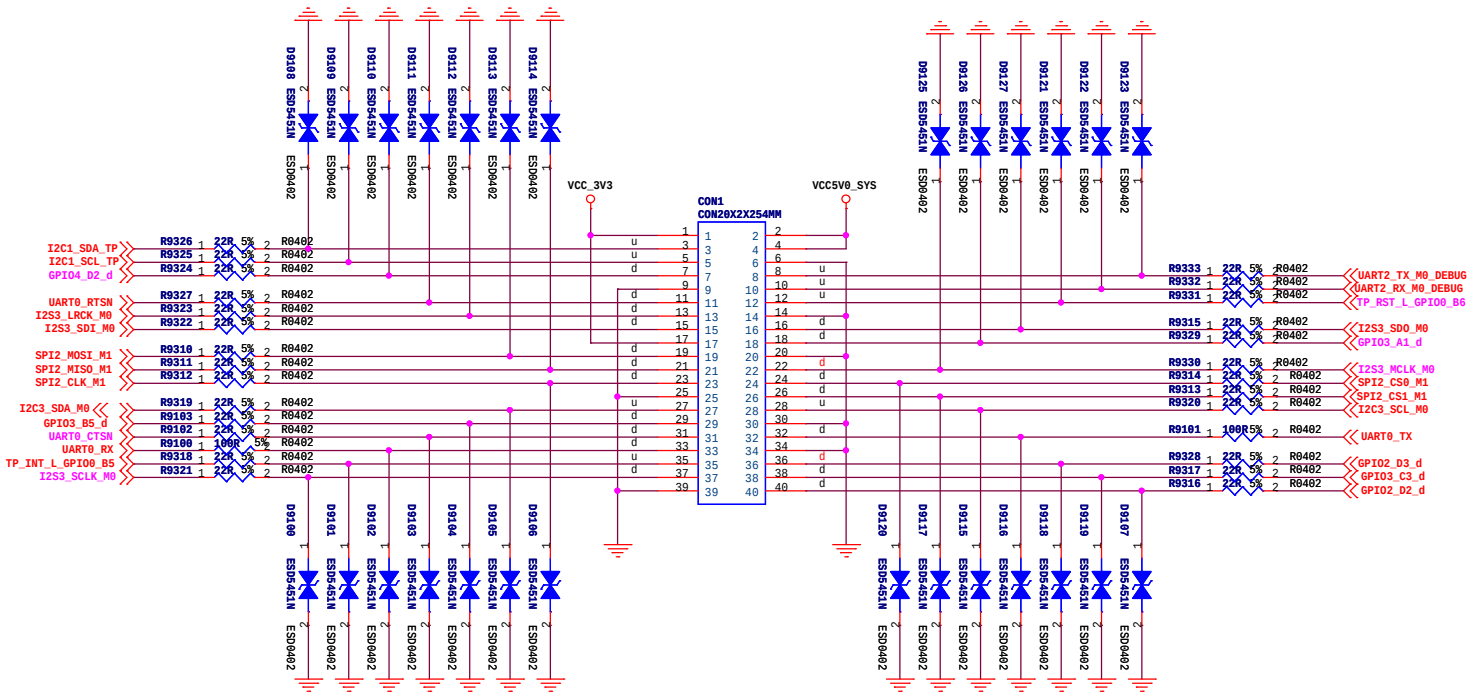

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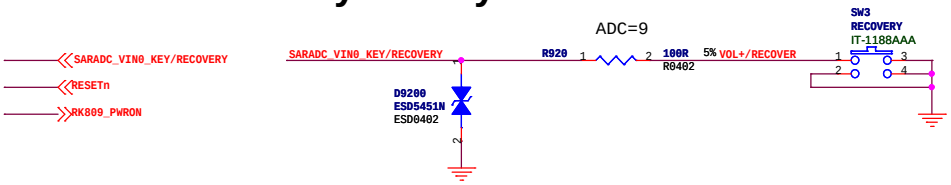
Key Array

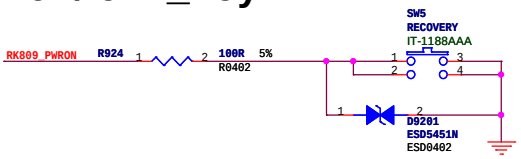


Note:

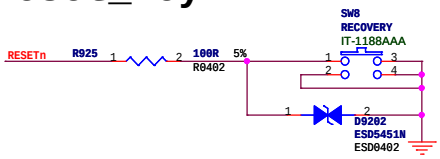
If there is no Key requirement,
It is suggested to reserve a
SW9200 Key to facilitate the
development debug

RECOVERY_Key function:
If SARADC_VIN0=0V
at after power on and reset,
then system will
enter into loader mode.

PowerOn/OFF_Key



Reset_Key



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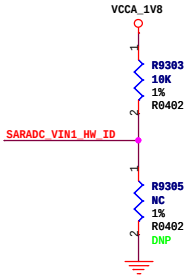
SARADC_VIN1_HW_ID

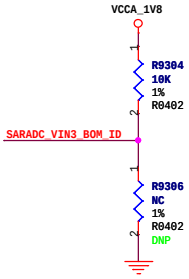
SARADC_VIN3_BOM_ID

HW_ID



SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW_ID12	DNP	10K

BOM_ID



SARADC_VIN3	Up Resistance	Down Resistance
BOM_ID0	10K	DNP
BOM_ID1	10K	110K
BOM_ID2	20K	100K
BOM_ID3	33K	100K
BOM_ID4	18K	36K
BOM_ID5	36K	51K
BOM_ID6	51K	51K
BOM_ID7	51K	36K
BOM_ID8	36K	18K
BOM_ID9	100K	33K
BOM_ID10	100K	20K
BOM_ID11	110K	10K
BOM_ID12	DNP	10K

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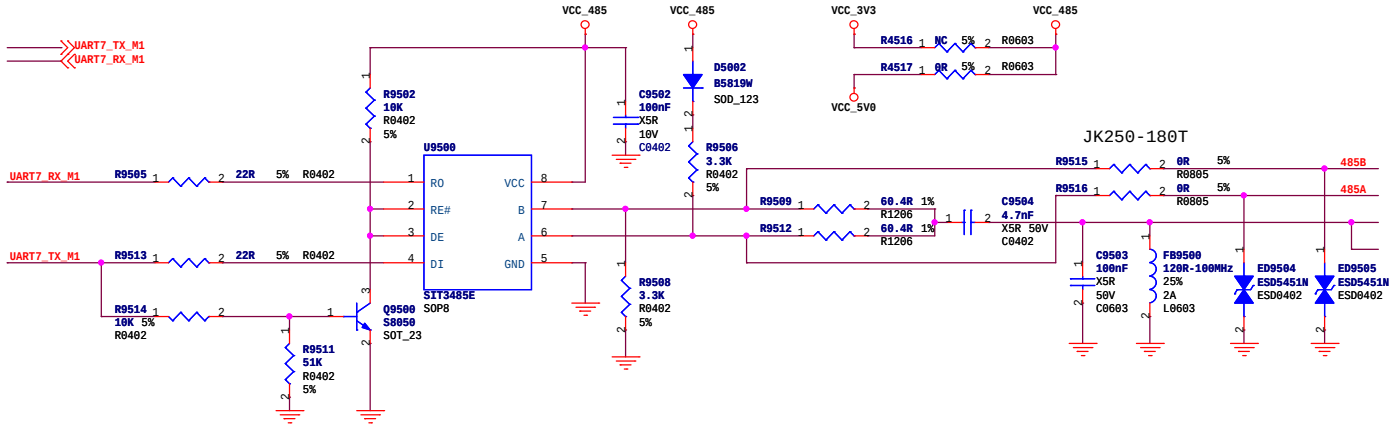
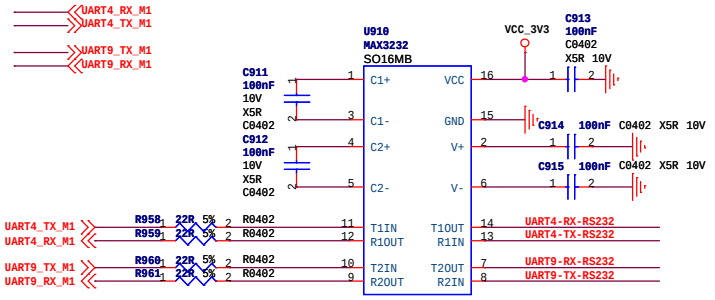
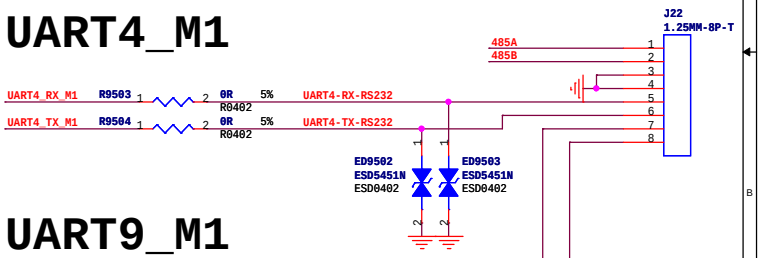
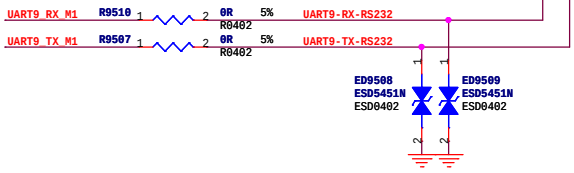




UART4_M1



UART9_M1



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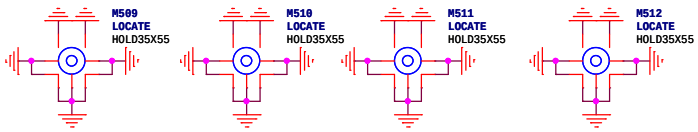

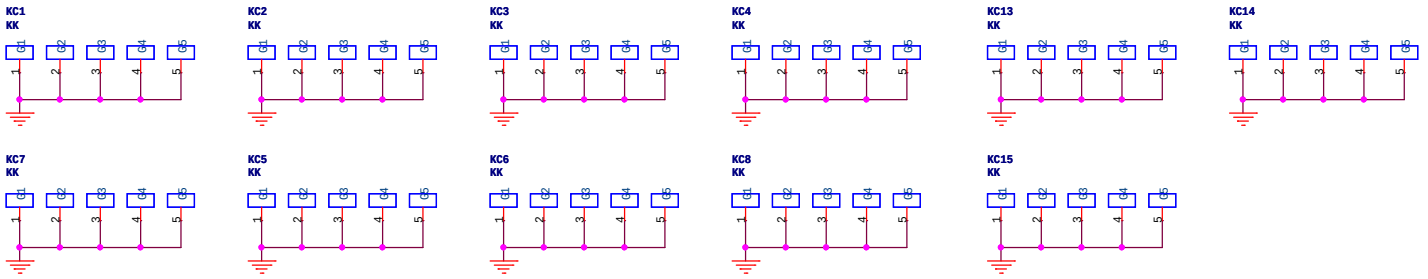

TOP Mark

BOTTOM Mark

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