



Global LCD Panel Exchange Center

Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications() Final Specifications

Module	17.3"(17.26") QHD 16:9 Color TFT-LCD with LED Backlight design	
Model Name	B173QTN01.4 (H/W:0A) Dell P/N:JYWWF	
Note (🗭)	LED Backlight with driving circuit design	

Customer	Date
Checked & Approved by	Date
Note: This Specification is without notice.	subject to change

Approved by	Date			
<u>Wen Hwa</u>	<u>12/13/2016</u>			
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AU Optronics corporation				





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10.1 EDID Description.....





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Record of Revision

Ver	sion and Date	Page	Old description	New Description	Remark
0.1	2016/11/28	All	First Edition for Customer		
0.2	2016/12/13	30		Update EDID	

B173QTN01.4 Document Version: 0.2

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1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



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2. General Description

B173QTN01.4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 QHD, 2560(H) x1440(V) screen and RGB 8-bits data driver with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B173QTN01.4 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

Items	Unit		Cnocif	ioationo	,	
			Specii	ications		
Screen Diagonal	[mm]	438.38				
Active Area	[mm]	382.08 X 2	14.92			
Pixels H x V		2560x3(RG	B) x1440			
Pixel Pitch	[mm]	0.14925X0.14925				
Pixel Format		R.G.B. island				
Display Mode	6	Normally White (TN)				
White Luminance (ILED=25mA) (Note: ILED is LED current)	[cd/m ²]	400 typ. (5 points average) 340 min. (5 points average)				
Luminance Uniformity		1.25 max. (5 points)				
Contrast Ratio		700 typ				
Response Time	[ms]	5 typ / 8 Ma	ıx			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.				
Power Consumption	[Watt]	10.1 max. (Include Log	ic and Blu p	ower)	
Weight	[Grams]	550 max.				
Physical Size	[mm]		Min.	Тур.	Max.	
Include bracket		Length	397.6	398.1	398.6	
		Width	252	252.5	253	
		Thickness	-	-	4.35	
Electrical Interface		4 Lane eDF	1.4	•	•	
Glass Thickness	[mm]	0.5				
Surface Treatment		Anti-Glare, Hardness 3H,				
Support Color		RGB 8-bit				





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Temperature Range		
Operating	[°C]	0 to +50
Storage (Non-Operating)	[°C]	-20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 $\!\!\!\!\!^{\circ}_{\circ}$ (Room Temperature) :

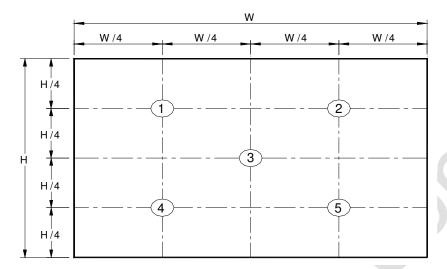
Item		Symbol	Conditions	Min.	Тур.	Max.	Unit	Note
White Lumir			5 points average	340	400	-	cd/m ²	1, 4, 5
Viewing Angle		$ heta_{ extsf{R}}$	Horizontal (Right)	60	70			
		$ heta_{ extsf{L}}$	CR = 10 (Left)	60	70	-	degree	
		ф н	Vertical (Upper)	50	60	-		4, 9
		φ _L	CR = 10 (Lower)	50	60	-		
Luminance Uniformity		δ _{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ _{13P}	13 Points	<u></u>	-	1.60		2, 3, 4
Contrast R	atio	CR		-	700	-		4, 6
Cross ta	lk	%				4		4, 7
Response ⁻	Гіте	T _{RT}	Rising + Falling	-	5	8	msec	4, 8
	Red	Rx		0.613	0.643	0.673		
	Hea	Ry		0.311	0.341	0.371		
Color /	Green	Gx 🕨		0.309	0.339	0.369	•	
Chromaticity	arcen	Gy		0.580	0.610 0.	0.640		
Coodinates	Blue	Bx	CIE 1931	0.123	0.153	0.183		4
	Diue	Ву		0.020	0.050	0.080	-	
	\//bit-	Wx		0.283	0.313	0.343		
	White	Wy		0.299	0.329	0.359		
NTSC		%		_	72	_		



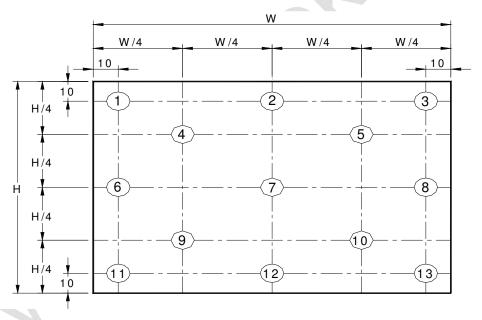


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Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{\text{W5}} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{\text{W13}} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

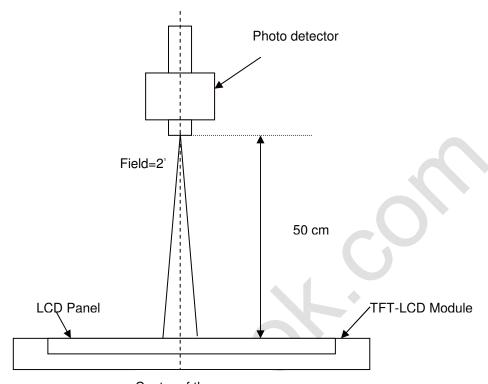


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Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Center of the screen

Note 5: Definition of Average Luminance of White (Y_L) :

Measure the luminance of gray level 63 at 5 points \cdot $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$ L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

Note 7: Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m₂)

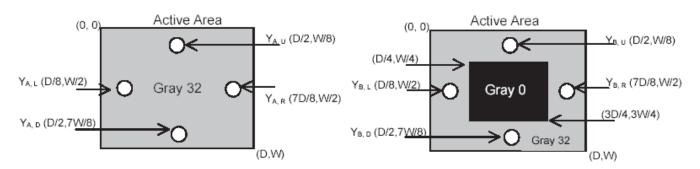
Y_B = Luminance of measured location with gray level 0 pattern (cd/m₂)



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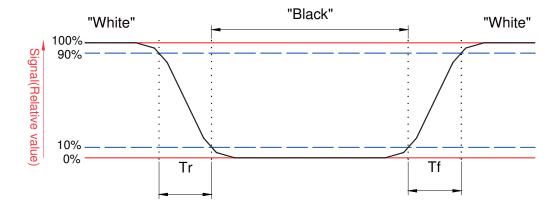
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Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



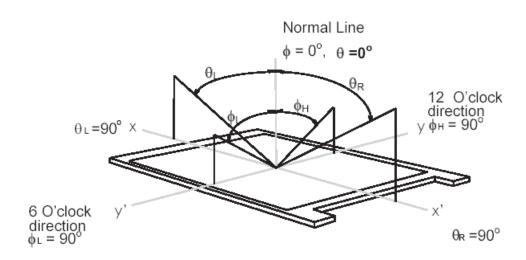




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Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio \geq 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



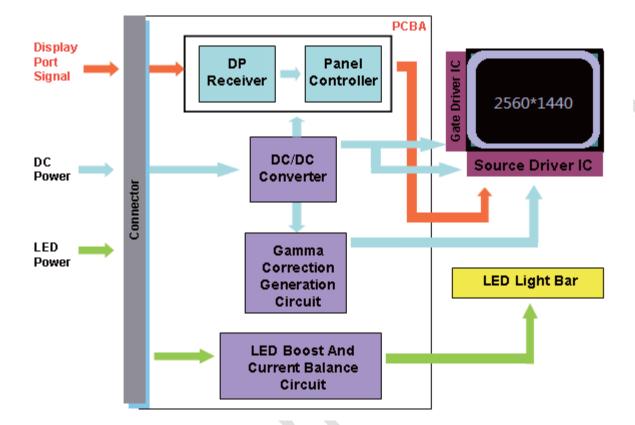




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3. Functional Block Diagram

The following diagram shows the functional block of the 17.3 inches wide Color TFT/LCD 40 Pin







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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item Symbol		Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

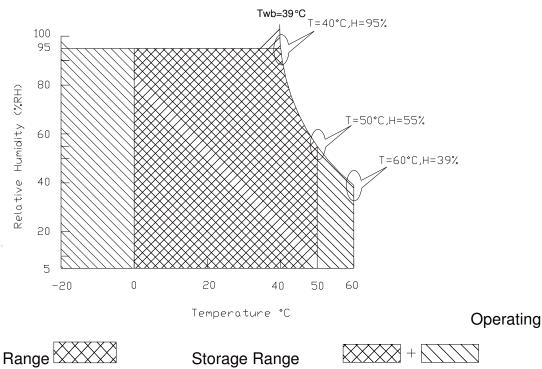
Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).

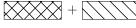
Note 5: The packing material of system forbid to involve ammonium component

Note 6: The reliability test conditions of system do not exceed the verified conditions of TFT module

Note 7: Be sure the panel test condition do not exceed the component limitation of TFT module(TN Liquid crystal, for example)



Storage Range





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5. Electrical Characteristics

5.1 TFT LCD Module

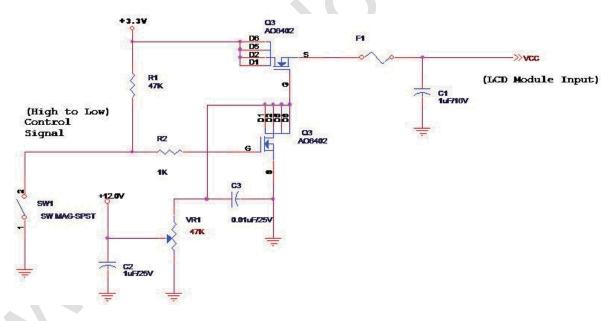
5.1.1 Power Specification

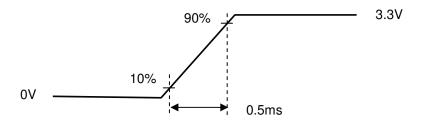
Input power specifications are as follows;

Symble	Parameter	Min	Тур	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	_	-	4.1	[Watt]	Note 1
IDD	IDD Current(RMS)	_	-	1367	[mA]	Note 1
lRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Mosaic pattern (PDD (max) = VDD(min) x IDD(max))

Note 2: Measure Condition





Vin rising time





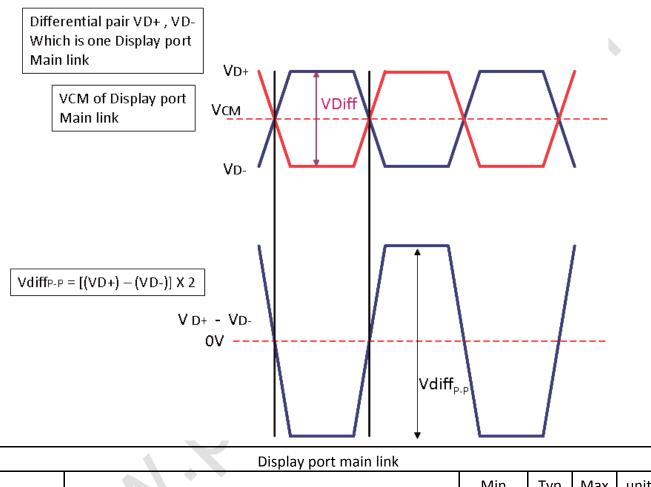
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5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Display Port main link signal:



	Display port main link							
		Min	Тур	Max	unit			
VCM	RX input DC Common Mode Voltage		0		V			
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	70		1320	mV			

Fallow as VESA display port standard V1.3



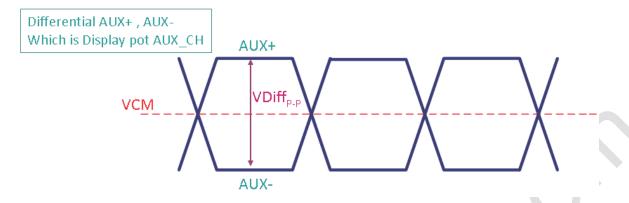


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Display Port AUX CH signal:



	Display port AUX_CH				
		Min	Тур	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	270		800	mV

Fallow as VESA display port standard V1.3

Display Port VHPD signal:

	Display port VHPD				
		Min	Тур	Max	unit
VHPD	HPD Voltage	2.25	_	3.6	V

Fallow as VESA display port standard V1.3





5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Тур	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	6.0	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	1	Hour	(Ta=25°C), Note 2 I _F =25 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Тур	Max	Units	Remark
LED Power Supply	VLED	7.0	12.0	21.0	[Volt]	
LED Enable Input High Level	WED EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level	VLED_EN	-	-	0.5	[Volt]	Define as
PWM Logic Input High Level	VPWM EN	2.5	-	5.5	[Volt]	Connector Interface
PWM Logic Input Low Level		-	-	0.5	[Volt]	(Ta=25°C)
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5		100	%	

Note 1: Recommend system pull up/down resistor no bigger than 10kohm





6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

		1								25	66	C
1st Line	R	G	В	R	G	В	 R	G	В	R	G	В
		•			•							
		•			•			•			•	
								· ·				
1440th Line	R	G	В	R	G	В	 R	G	В	R	G	В





6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-040E-12 or compatible
Mating Housing/Part Number	IPEX 20353-040T-11 or compatible

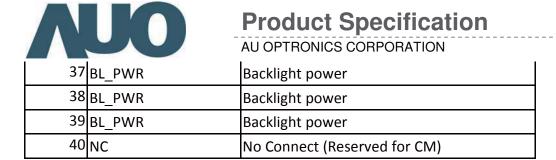


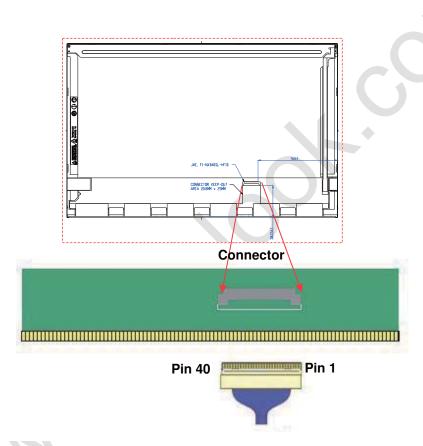


6.2.2 Pin Assignment (4 Lane)

PIN NO S	Symbol	Function
1	NVSR	NVSR
2 _F	H_GND	High Speed Ground
3 L	_ane3_N	Comp Signal Lane3
4 լ	_ane3_P	True Signal Link Lane 3
5 H	H_GND	High Speed Ground
6 լ	_ane2_N	Comp Signal Link Lane 2
7 L	_ane2_P	True Signal Link Lane 2
8 H	H_GND	High Speed Ground
9 լ	_ane1_N	Comp Signal Lane 1
10 լ	_ane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12 լ	_ane0_N	Comp Signal Link Lane 0
13 լ	_ane0_P	True Signal Link Lane 0
14 H	H_GND	High Speed Ground
15 /	AUX_CH_P	True Signal Auxiliary Ch.
16	AUX_CH_N	Comp Signal Auxiliary Ch.
17 H	H_GND	High Speed Ground
18 լ	_CD_VCC	LCD logic and driver power
19 լ	_CD_VCC	LCD logic and driver power
20 լ	_CD_VCC	LCD logic and driver power
21 լ	_CD_VCC	LCD logic and driver power
22 լ	_CD_Self_Test or NC	LCD Panel Self Test Enable (Optional)
23 լ	.CD GND	LCD logic and driver ground
24 լ	_CD GND	LCD logic and driver ground
25 լ	_CD GND	LCD logic and driver ground
26 լ	.CD GND	LCD logic and driver ground
27 F	HPD	HPD signale pin
28 E	BL_GND	Backlight_ground
29 E	BL_GND	Backlight_ground
30 E	BL_GND	Backlight_ground
31	BL_GND	Backlight_ground
32	BL_Enable	Backlight On / Off
33 [BL PWM DIM	System PWM signal Input
34 N	NC	No connect (Reserved for H-SYNC)
35	NC	No connect (Reverse for AUO TEST only)
36	BL_PWR	Backlight power







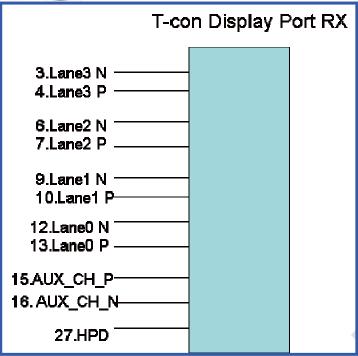
Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off. Internal circuit of **eDP inputs** are as following.





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6.3 Interface Timing

6.3.1 Timing Characteristics

For normal display, interface timings should match the 2560x1440 /120Hz manufacturing guide line timing.

Parar	Symbol	Min.	Тур.	Max.	Unit	
Frame	e Rate	-	- 120			Hz
Clock frequency		1/ T _{Clock}		499.6		MHz
	Period	T _V		1530		
Vertical	Active	T _{VD}		1440		T_{Line}
Section	Blanking	T _{VB}		90		
	Period	T _H		2720		
Horizontal Section	Active	T _{HD}		2560		T_{Clock}
	Blanking	T HB		160		

Note 1: The above is as optimized setting

Note 2: The maximum clock frequency = (2560+B)*(1440+A)*60<80MHz





G-Sync Function enable, interface timings should match the 1366x768 /60-120Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Тур.	Max.	Unit
Frame Rate		-	60.025		120.05	Hz
Clock fro	equency	1/ T _{Clock}	499.6		499.6	MHz
	Period	T _V	3060		1530	
Vertical	Active	T _{VD}	1440			${f T}_{\sf Line}$
Section	Blanking	T _{VB}	1620		90	
	Period	T _H	2720		2720	
Horizontal	Active	T _{HD}		2560	·	T _{Clock}
Section	Blanking	T HB	160		160	

Note 1: G Sync function enble frame rate frequency operating range: 60-120Hz

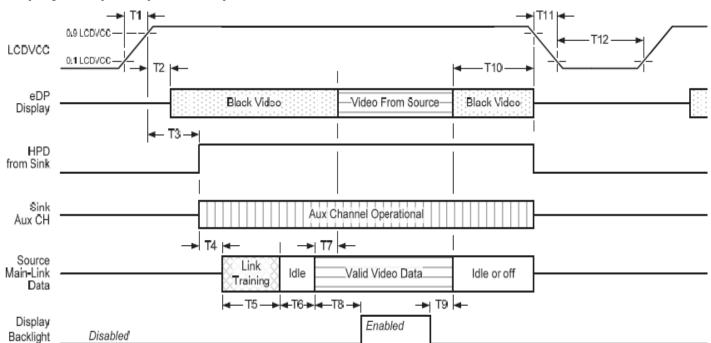




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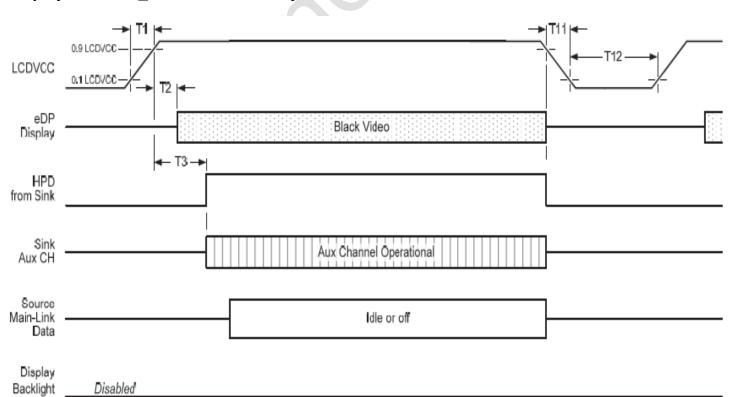
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only





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Display Port panel power sequence timing parameter:

Timing	December 41 and	Devel Ive	Limits			Notes
parameter	Description	Reqd. by	Min.	Тур.	Max.	Notes
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
Т2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
Т3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
Т5	link training duration	source				dependant on source link to read training protocol.
Т6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
Т7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
Т8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
Т9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

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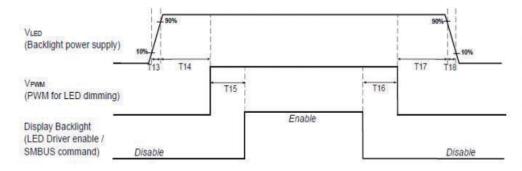




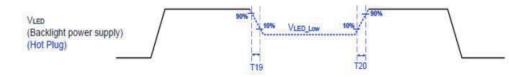


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Display Port panel B/L power sequence timing parameter:



Note: When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	85=8
T15	0	56
T16	0	1849
T17	10	2(0)
T18	0.5	10
T19	1*	20=0
T20	1*	95

Seamless change: T19/T20 = 5xT_{PWM}* *T_{PWM}= 1/PWM Frequency





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7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

Test method: Non-Operation

Acceleration: 1.5 G

• Frequency: 10 - 500Hz Random

Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

Test method: Non-Operation

Acceleration: 220 G, Half sine wave

Active time: 2 ms

Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV	Note 1
ESD	Air: ±15 KV	

Note1: According to EN 61000-4-2, ESD class B: Some performance degradation allowed. Self-recoverable.

No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

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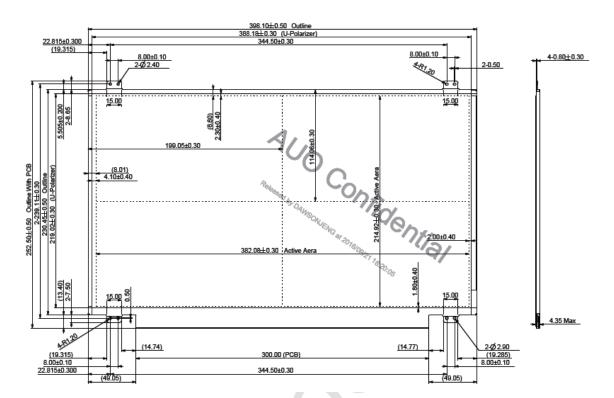




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8. Mechanical Characteristics

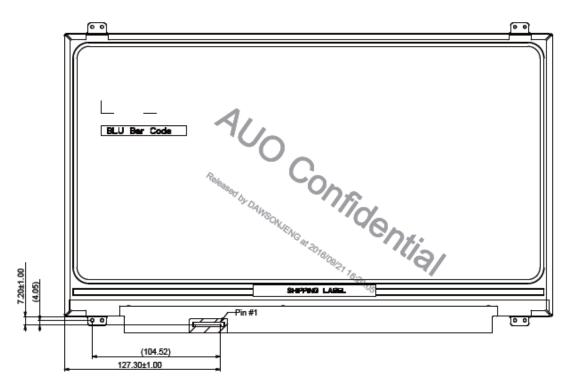
8.1 LCM Outline Dimension



B173QTN01.4 Document Version: 0.2







Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

B173QTN01.4 Document Version: 0.2

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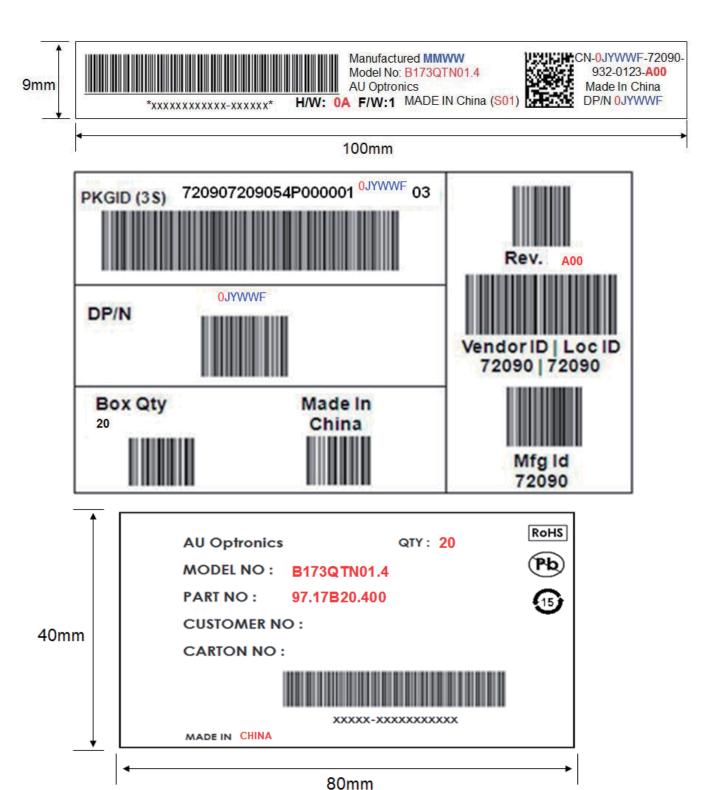




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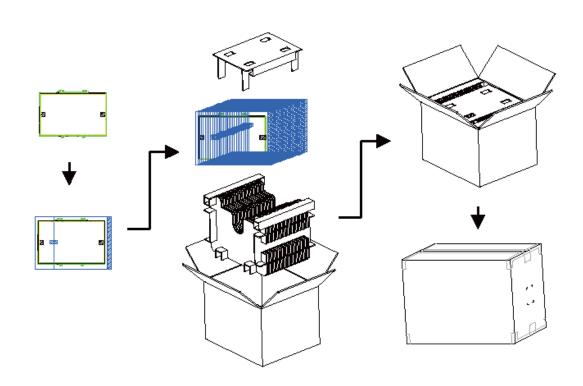
9. Shipping and Package

9.1 Shipping Label Format

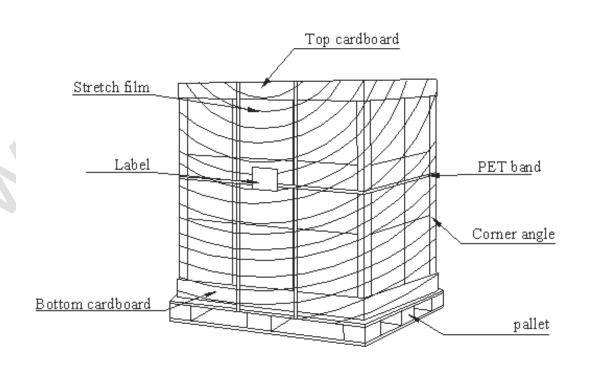








9.3 Shipping Package of Palletizing Sequence



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10. Appendix:

	Byte	Field Name and Comments	Value	Value	Valu
	(hex)	ried Name and Comments	(hex)	(binary)	(DE
	0	Header	00	00000000	0
	1	Header	FF	111111111	25
ا	2	Header	FF	11111111	25
Header	3	Header	FF	11111111	25
	4	Header	FF	11111111	25
	5	Header	FF	11111111	25
	6	Header	FF	11111111	25
	7	Header	00	00000000	C
	8	EISA manufacture code = 3 Character ID	06	00000110	6
	9	EISA manufacture code (Compressed ASCII)	AF	10101111	17
	0A	Panel Supplier Reserved – Product Code	96	10010110	15
ಕ	0B	Panel Supplier Reserved – Product Code	14	00010100	2
ion	0C	LCD module Serial No - Preferred but Optional ("0" if not used)	7D	01111101	12
Vendor / Product EDID Version	0D	LCD module Serial No - Preferred but Optional ("0" if not used)	0D	00001101	1
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0E	LCD module Serial No - Preferred but Optional ("0" if not used)	CB	11001011	20
월	0F	LCD module Serial No - Preferred but Optional ("0" if not used)	39	00111001	5
₩ М	10	Week of manufacture	00	00000000	0
	11	Year of manufacture	1A	00011010	2
	12	EDID structure version # = 1	01	00000001	1
	13	EDID structure version # = 1 EDID revision # = 4	04	00000001	4
	14	Video I/P definition			16
ers			A5	10100101	
ola) netk	15	Max H image size = ?? cm(Rounded to cm)	26	00100110	3
Display Parameters	16	Max V image size = ?? cm(Rounded to cm)	15	00010101	2
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) - 100 = 120	78	01111000	12
	18	Feature support	02	00000010	2
	19	Red/Green Low bit (RxRy/GxGy)	9D	10011101	15
	1A	Blue/White Low bit (BxBy/WxWy)	75	01110101	11
> (0	1B	Red X	A4	10100100	16
Panel Color Coordinates	1C	Red Y Ry = 0.???	57	01010111	8
O Sil	1D	Green X Rx = 0.???	56	01010110	8
orc	1E	Green Y Ry = 0.???	9C	10011100	15
Pal	1F	Blue X Rx = 0.???	27	00100111	3
	20	Blue Y Ry = 0.???	0C	00001100	1:
	21	White X $Rx = 0.$??	50	01010000	8
	22	White Y $Ry = 0.$??	54	01010100	8
S S	23	Established timings 1 (00h if not used)	00	00000000	C
stabl hed iming	24	Established timings 2 (00h if not used)	00	00000000	C
Establis hed Timings	25	Manufacturer's timings (00h if not used)	00	00000000	C
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01	00000001	1
	27	Standard timing ID1 (01h if not used)	01	00000001	1
	28	Standard timing ID2 (01h if not used)	01	00000001	1
	29	Standard timing ID2 (01h if not used)	01	00000001	1
	2A	Standard timing ID3 (01h if not used)	01	00000001	1
	2B	Standard timing ID3 (01h if not used)	01	00000001	1
	2C	Standard timing ID3 (0111 into used) Standard timing ID4 (01h if not used)	01	00000001	1
	2D	Standard timing ID4 (01h ir not used) Standard timing ID4 (01h if not used)	01	00000001	1
					1
dard	2E	Standard timing ID5 (01h if not used)	01	00000001	
Stand	2F	Standard timing ID5 (01h if not used)	01	00000001	1
	30	Standard timing ID6 (01h if not used)	01	00000001	1
	31	Standard timing ID6 (01h if not used)	01	00000001	1
	32	Standard timing ID7 (01h if not used)	01	00000001	1
	33	Standard timing ID7 (01h if not used)	01	00000001	1
	34	Standard timing ID8 (01h if not used)	01	0000001	1

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		AU OPTRONICS CORPORATION			
	36	Pixel Clock/10,000 (LSB)	28	00101000	40
		Pixel Clock/10,000	_		_
	37	(MSB)	C3	11000011	195
	38	Horizontal Active = ???? pixels (lower 8 bits)	00	00000000	0
	39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	A0	10100000	160
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	A0	10100000	160
	3B	Vertical Active = ??? lines	A0	10100000	160
	3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	5A	01011010	90
	3D 3E	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits) Horizontal Sync, Offset (Thfp) = ?? pixels	50 30	01010000 00110000	80 48
17	3F	Horizontal Sync, Oliset (Thip) = ?? pixels Horizontal Sync, Pulse Width = ??? pixels	20	00110000	32
Timing Descripter #1	40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	35	00110101	53
ript	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
esc	42	Horizontal Image Size =??? mm	7E	01111110	126
ďρ	43	Vertical image Size = ??? mm	D6	11010110	214
ning	44	Horizontal Image Size / Vertical image size	10	00010000	16
Ë	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
		Bit[7] 0: Non-interlace, 1: Interlace			
		Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate			
		Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3			
	47	==> fix=1A	1A	00011010	26
	48	Pixel Clock/10,000 (LSB)	28	00101000	40
	49	Pixel Clock/10,000 (MSB)	СЗ	11000011	195
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	00	00000000	0
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	A0	10100000	160
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	A0	10100000	160
	4D	Vertical Active = xxxx lines	A0	10100000	160
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	54	01010100	84
	4F	Vertical Active: Vertical Blanking (Tvbp) (upper4:4 bits)	56	01010110	86
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	30	00110000	48
#2	51	Horizontal Sync, Pulse Width = xxxx pixels	20	00100000	32
oter	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	35	00110101	53
scrip	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
Des	54	Horizontal Image Size =xxx mm	7E	01111110	126
l gri	55	Vertical image Size = xxx mm	D6	11010110	214
Timing Descripter #2 (=Timing Descripter #1)	56	Horizontal Image Size / Vertical image size	10	00010000	16
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
		Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital			
		composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3			
	59	==> fix=1A	1A	00011010	26
ter	5A	Flag	00	00000000	0
crip iffic	5B	Flag	00	00000000	0
Timing Descripter #3 Dell specific information	5C	Flag	00	00000000	0
lg [# sll s	5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
nim De jri	5E	Flag	00	00000000	0
F	5F	Dell P/N 1 st Character	4A	01001010	74

00

00000000

11110100

0

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	60	Dell P/N 2 nd Character	59	01011001	89
	61	Dell P/N 3 rd Character	57	01010111	87
	62	Dell P/N 4 th Character	57	01010111	87
	63	Dell P/N 5 th Character	46	01000110	70
		EDID Revision Bit[6:0] See charts below			
	64	Bit[7] 0: X-rev, 1: A-rev	80	10000000	128
	65	Manufacturer P/N	42	01000010	66
	66	Manufacturer P/N	31	00110001	49
	67	Manufacturer P/N	37	00110111	55
	68	Manufacturer P/N	33	00110011	51
	69	Manufacturer P/N	51	01010001	81
	6A	Manufacturer P/N	54	01010100	84
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	4E	01001110	78
	6C	Flag	00	00000000	0
	6D	Flag	00	00000000	0
	6E	Flag	00	00000000	0
	6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0
	70	Flag	00	00000000	0
4	71	Color Management	02	00000010	2
# #	72	Panel Structure	41	01000001	65
ipte	73	Frame Rate	2F	00101111	47
scri	74	Light Controller Interface and Luminance	28	00101000	40
De	75	Outdoor Features	00	00000000	0
Вu	76	Multi-Media Features	01	00000001	1
Timing Descripter #4	77	Multi-Media Features	00	00000000	0
	78	Special Features #1	00	00000000	0
	79	Special Features #2	0B	00001011	11
	7A	Special Features #3	01	0000001	1
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32

Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)

Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)



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