YIN FUNG KHONG

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A multilingual graduate in Computer Engineering with demonstration of leadership and attention to details, coordinated programs and events for student success. Seeking opportunities to leverage both engineering and leadership skills within the industry.

EDUCATION

California State University – Northridge (CSUN) ***Spring 2019***
- **M.S.** in Computer Engineering ***(3.95/4.0 CGPA)***
- Distinction Award, Outstanding Graduate Student

California State University – Northridge (CSUN) ***January 2018***
- **B.S.** in Computer Engineering ***(3.94/4.0 CGPA)***
- Summa Cum Laude (First Class Honors)

EXPERIENCE

Graduate Assistant | ***CSUN Dept of Electrical & Computer Engineering*** ***Sept 2018 – May 2019***
- Graded assignments and lab reports, and tabulate grades accordingly.
- Assisted in lab, answering questions related to homework assignments and laboratory experiments.

Graduate Intern | ***Intel Corporation (iCDG)*** ***June 2018 - Aug 2018***
- Designed and developed C# application for product's test data analysis.
- Implemented Machine Learning for pattern detection in test data.

SKILLS

Multilingual - fluent in *English, Mandarin, Bahasa Malaysia* and conversational in *Cantonese*

Programming - *VHDL Verilog MATLAB Java Python ARM C C#*

CRLA International Mentor Training Program Certification (IMPTC) – Certified Mentor Level I

PROJECTS

A Novel Approach for Efficient Implementation of Nucleus Detection and Segmentation Using Correlated Dual Color Space (IEEE SMC Conference) ***April 2019***
- Researching an efficient yet accurate algorithm in blood cell segmentation in microscopic blood images using digital image processing techniques, to improve and accelerate the diagnosis of different hematologic disorder.
- The research proposes a novel technique that involves the RGB and CMYK color spaces.

Blood Cells Detection using Circular Hough Transform in MATLAB ***Dec 2018***
- White Blood Cells detection and calculation on color blood test images.
- Morphological operation to process and filter image noise for further handling.
- Translated concept for implementation on real-time detection on FPGA.

Multi-Clock and Timers using ZedBoard Development Board ***Nov 2017***
- Implemented FSM on the FPGA for chess clocks and timers with error handlings.
- Added Seven-segment displays for two user's countdowns, with on-board LEDs.
- Implemented LFSR for pseudo-random number generation for Fischer chess clock.

Audio Codec using ZedBoard SoC Development Board ***May 2017***
- Integrated PL and PS of the board to implement functionality for audio streaming.
- Added frequency filtering and tones to the audio streaming output.
- Implemented onboard display and switches for better user experience and control.

INVOLVEMENTS / ACHIEVEMENTS

President, *Tau Beta Pi Engineering Honor Society* ***May 2017 – May 2019***
President, *Leaders in Engineering and Computer Science - Student Council* ***Nov. 2017 – May 2019***
President's Volunteer Service Award (PVSA) ***2016, 2017, 2018, 2019***
Best Leadership Award, *Tau Beta Pi Engineering Honor Society* ***2018***