Jack Yinger

Electrical and Computer Engineer

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Experience

Work

Microsoft *FPGA RTL Design Engineer*

June 2017 - Present

Working on Microsoft's Catapult FPGA Datacenter Accelerator program developing PCIe capabilities and contributing a broad range of features and fixes. At times working closely with the Software and Board teams.

Developed PCI Express Tester to stress transaction layer traffic. Broke large design into blocks, defined interface contracts between blocks, and delegated implementation of some blocks. Capable of full speed DMA, MMIO for control, and Function Level Reset handling.

Added board support for 3 generations of boards; adapting structure to work with new IPs while maintaining user interface compatibility.

Intel *Hardware & Software Engineer*

May 2013 - June 2017

Worked on systolic array processor designs for deep neural network inference; at the junction of algorithmic design and performant implementation.

Researched & Designed Systolic Array Matrix Multiplier for Sparse Neural Nets; Achieved state of the art performance, Published Peer Reviewed Paper: Customizable FPGA OpenCL Matrix Multiply Design Template for Deep Neural Networks.

Contributed features to a Systolic Array Neural Network product. Made microarchitectural optimizations and feature additions. Developed transpiler for optimizing neural models for execution on the systolic array.

Education

Oregon State University *BS Electrical & Computer Eng.*

September 2008 - April 2013

Studied: Discrete & Continuous Signal Processing & Filters, Phased Array Antenna Beamforming. Laser Engineering, Microwave Circuits and Antennas. Computer Architecture, Microprocessor System Design, Computer Science Fundamentals

Activities: IEEE Chapter Webmaster & Store Manager. Robotics Club University Rover Challenge Team Member.

Capabilities

Hardware

FPGA Logic Design

Development: System Verilog & Verilog. High Speed Logic Design; Pipelining, Interleaving. Timing Closure & Constraints. IP use.

Testing: SVUnit, Questasim/Modelsim,

Tools: Quartus, Bus Analyzers (PCIe, I2C)

SW/HW Interface

Design, Use, and Reverse Engineering

Software

Languages

Python, C/C++, TCL, Matlab, Haskell, Rust, etc.

Linux

Platform of choice at work & home. Use of Vim, Git, Grep, Bash, etc.

Leadership

Innate drive to set collaborators up for success and work as a team player.

Strong sense of ownership; ready to take responsibility even when the going is rough.