

Yinghua Hu

University of Southern California
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PRINCIPAL INTERESTS Hardware security and trust, supply chain security, computer-aided design, formal verification, logic encryption.

ACADEMIC BACKGROUND **University of Southern California** **Los Angeles, CA**
Ph.D. in Electrical Engineering 2017 - present
• Advisor: Prof. Pierluigi Nuzzo.
• Dissertation Title: Toward A Risk-Aware Design Methodology for Secure Logic Locking.

University of Southern California **Los Angeles, CA**
M.S. Electrical Engineering 2017 - 2019

Nankai University **Tianjin, China**
B.S. Electrical Engineering 2013 - 2017

AWARDS AND HONORS

- Charles L. Weber Memorial Outstanding Teaching Assistant Award (Honorable Mention), USC, Apr. 2021.
- Young Fellow, Design Automation Conference, July 2020.
- Outstanding Graduates Award, Nankai University, May, 2017.
- Samsung Scholarship, Samsung Electronics (top 1% out of 400 students), Dec. 2015.
- National Scholarship, Chinese Ministry of Education (top 1% out of 400 students), Dec. 2014.

PUBLICATIONS *Book Chapters*

1. **Y. Hu**, K. Yang, S. Nazarian, P. Nuzzo, “**SANSCrypt: Sporadic-Authentication-Based Sequential Logic Encryption**”, *VLSI-SoC: Design Trends*, Springer, 2021.

Conference Papers

8. Y. Zhang, **Y. Hu**, P. Nuzzo, P. A. Beerel, “**TriLock: IC Protection with Tunable Corruptibility and Resilience to SAT and Removal Attacks**”, *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Mar. 2022.
7. **Y. Hu**, Y. Zhang, K. Yang, D. Chen, P. A. Beerel, P. Nuzzo, “**Fun-SAT: Functional Corruptibility-Guided SAT-Based Attack on Sequential Logic Encryption**”, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, Dec. 2021.
6. S. Dutta Chowdhury, G. Zhang, **Y. Hu**, P. Nuzzo, “**Enhancing SAT-Attack Resiliency and Cost-Effectiveness of Reconfigurable-Logic-Based Circuit Obfuscation**”, *IEEE International Symposium on Circuits and Systems (ISCAS)*, May. 2021.

5. **Y. Hu**, K. Yang, S. Dutta Chowdhury, P. Nuzzo, “**Risk-Aware Cost-Effective Design Methodology for Integrated Circuit Locking**”, *IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Feb. 2021.
4. **Y. Hu**, K. Yang, S. Nazarian, P. Nuzzo, “**SANSCrypt: A Sporadic-Authentication-Based Sequential Logic Encryption Scheme**”, *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Oct. 2020.
3. **Y. Hu**, V. Venugopalan, A. Schmidt, J. Monson, M. French, P. Nuzzo, “**Security-driven Metrics and Models for Efficient Evaluation of Logic Encryption Schemes**”, *ACM-IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE)*, Oct. 2019.
2. V. Venugopalan, G. Kolhe, A. Schmidt, J. Monson, M. French, **Y. Hu**, P. A. Beerel, P. Nuzzo, “**System-Level Framework for Logic Obfuscation with Quantified Metrics for Evaluation**”, *IEEE Secure Development Conference (SecDev)*, Sept. 2019.
1. V. Venugopalan, G. Kolhe, A. Schmidt, J. Monson, M. French, **Y. Hu**, P. A. Beerel, P. Nuzzo, “**Quantifying Security and Overheads for Obfuscation of Integrated Circuits**”, *GOMACTech*, March 2019.

WORKING EXPERIENCE

Research Assistant Aug. 2017 - present
University of Southern California, Los Angeles, CA

- Research focused on hardware security solutions on the integrated circuit (IC) supply chains, including the design and formal verification of IC encryption solutions that prevent successful IC reverse engineering.

Software Engineering Intern May 2021 - Aug. 2021
Synopsys Inc., Mountain View, CA

- Worked on DSO.ai, the world’s first autonomous AI application for chip design.
- Developed features to calculate design similarities between different designs, allowing DSO.ai to leverage the design space search history of previous designs.
- Built a user interface to visualize design similarities among a group of customer designs, which is expected to help the team conveniently develop and debug new features of design similarity.

Teaching Assistant Jan. 2020 - May 2020
University of Southern California, Los Angeles, CA

- Course: EE577A (VLSI System Design), Spring 2020.
- Held weekly discussions and guided students on fully customized VLSI system design using Cadence tools.
- Received Honorable Mention for Charles L. Weber Memorial Outstanding Teaching Assistant.

MENTORING

Summer High School Intensive in Next-Generation Engineering
University of Southern California, Los Angeles, CA 2018 - 2020

- Mentored three local high school students to complete a hardware security related project for seven weeks.
- Helped the mentees prepare for relevant skill sets for college study and research.