0	CS3810 Assignment 08	
	Question 1:	
	1. lw\$1,8(\$2)	
	add \$4, \$1, \$3	
	without forwarding	
	1 2 3 4 5 6 7 8	
31/1	1 2 3 4 5 6 7 8 1 w \$1,8(\$2) IF D/R AIL DM RW add \$4,\$1,\$3 IF Stall D/R ALW DM RW	
	add \$4, \$1,\$3 IF Stall DIR ALW DM PW	
	(2) (1) (1) (1) (1) (1) (2) (1) (2) (1) (2) (2)	
	Operands (\$1,\$3) all available only at the end of first half of Rw	_
	Stage The Stage of	
No al Villa	with A in diag	
	with forwarding 2 3 4 5 6 7 8 9	
	1 w \$1,8(52) IF D/R ALU DM RW -> Calculates the effective	,
	SW +3-85+7) IF DIR Stall ALU DM RW addiess at ALU stage	_
	add \$4,\$1,\$3	10
	17 Operand in available at	9
	5th clock cycle.	
127E/3		
40 4	2. lw \$1,8(\$2)	
	Sw \$3, 8(\$1)	
	without forwarding 1 2 3 4 5 6 7 8 9 10	
	(w\$1,8(\$2) IF D/R ALU DM RW	
	SW \$3, 8(\$1) IF Stall Stall D/R ALU DM RW	
	\$1 & available only at 5th clock cycle (after	
	writing in register file)	
	with forwarding 1 2 3 4 5 6 7 8 9 10	
	SW \$3, 8(\$1) IF D/R ALV DM RW SW \$3, 8(\$1) IF D/R Stall ALV DM RW	
	SW \$3, 8(\$1) IF P/R Stall ALLY DM RW \$1 is landed at 4th cycle. To store the value	
0	of \$3 to 8(\$1), we have to wait until \$1 is	
	loaded with new value. After that, the value is	
	durity forwarded to ALV unit of swinstruction.	
	John John Mill of South Chion.	

	Question 2:
	1 0 0 0 1 1 12
	1123456789101112
	I, F D RR IA RW
	- EDRRIARW
	73 Stall F D Bubble PR IA Potam Rotum RW = 12 cycles
	In Stall + Rubble V PR 1/3 Upr VIV.
	It FORR IA DM PM RW
44	
	The overtover overall process takes 12 cycles to complete
	i) For a processor with register by passing, it takes & success
	time hatractions
	ii) For a processor with no register by passing, it takes 12 inst.
	7 4 5 6 7 8 9 10 1112
	TO DE PORT
12402	
100 100	12 F D DR IA DIM DIM RW
5 (5)	E D CO IA DM DM RW
	5 D DO LA DON DIM
	It F D RR LA DIM DIM
	For prob i:
	In p in the
. 1758	I3 F D RR IA RW
	No Register by passing

Question 3: O As branch consequence is determined in The 4th stage, so we can act: AVG AVGCPI = 20% . 4 + 80% -1 = 1.6 DIf a branch is taken, then instruction in the phases previously the 3xx 4th stage are gruashed. Then we can get: AVG CPI = 20% - 75% - 4 + 80% - 1 + 20% - 25% - 1 = 1.45 3) Since it is fetched, so I clock cycle is compulsory for branches AVACPI=20%-1+80%-1 @ As hardware analyst makes precise prediction for 90% of division, I di cycle is compulsory when correct calculation is made and 4 clock cycl are essential for AVGCPI=20%.90%.1+2%.10%.4+80%.1 incorrect calculation = 1.06