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# Modeling of Stacking Fault Expansion Velocity of Body Diode in 4H-SiC MOSFET

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**Abstract.** We present a model to explain forward voltage degradation of body diode in 4H-SiC MOSFET, and evaluate the velocity of SF expansion. First, by using in-situ photoluminescence (PL) observation, we investigated how a stacking fault (SF) expands from a basal plane dislocations (BPD) in the 4H-SiC epitaxial layer. Second, double-diffused MOSFETs were developed and measured before and after degradation. Then, the characteristics of the forward voltage degradation were modeled by a combination of PL imaging and electrical measurement, and the calculated characteristics are in good agreement with the measured ones. Finally, we tested the SiC MOSFETs under various stress conditions and evaluated the velocity of the SF expansion by calculation. These results indicate that the velocity of SF expansion increases with increasing forward current density and junction temperature.

## Introduction

SiC MOSFETs are used for advanced power applications due to their superior properties such as high breakdown voltage and low power loss. By using an internal p-i-n diode, called a body diode and formed parasitically in the MOSFET structure, as a free-wheeling diode instead of an external Schottky barrier diode (SBD), an external diode-less power module can be fabricated to reduce the cost and size of the power module [1,2]. However, in the p-i-n diode, the forward voltage degrades under forward current stress due to basal plane dislocations (BPDs) expansion to the stacking faults (SFs) induced by electron-hole recombination [3-8]. In this work, we present a model to explain forward voltage degradation of body diode in 4H-SiC MOSFET, and evaluate the velocity of SF expansion.

## Experimental procedure and device structure

First, we investigated how a SF expands from a BPD in the 4H-SiC epitaxial layer by using in-situ photoluminescence (PL) observation. Then, double-diffused MOSFETs were fabricated on the Si-face, $4^{o}$ off-axis toward the <11-20> direction, n-type 4H-SiC substrate. Figure 1 shows a schematic cross-section of the SiC MOSFET. The epi layer was 30 μm thick with an n-type doping concentration of $3 \times 10^{15}$ $cm^{-3}$. To evaluate the dependence of SF expansion velocity on current and temperature, we investigated the forward voltage degradation under various stresses by using PL imaging and electrical measurement.