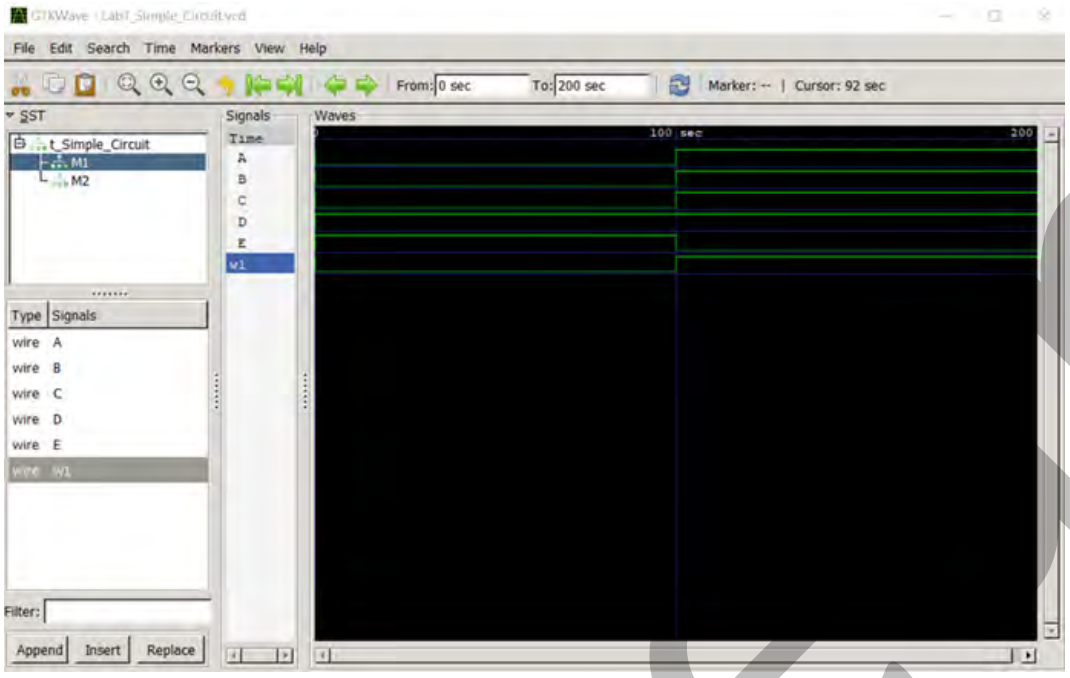
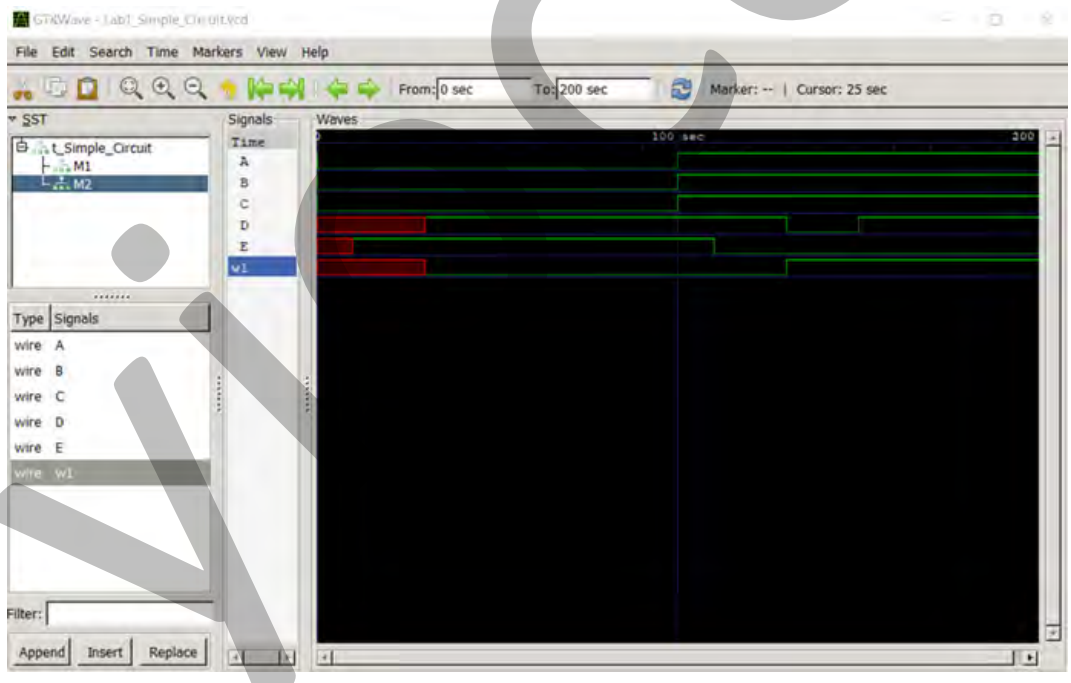
1 Give the waveform of the simulation result of 2A(a), including outputs D and E and internal connection w1, and explain the difference between the waveform of Simple_Circuit.v and that of Simple_Circuit_prop_delay.v.

Simple_Circuit.v



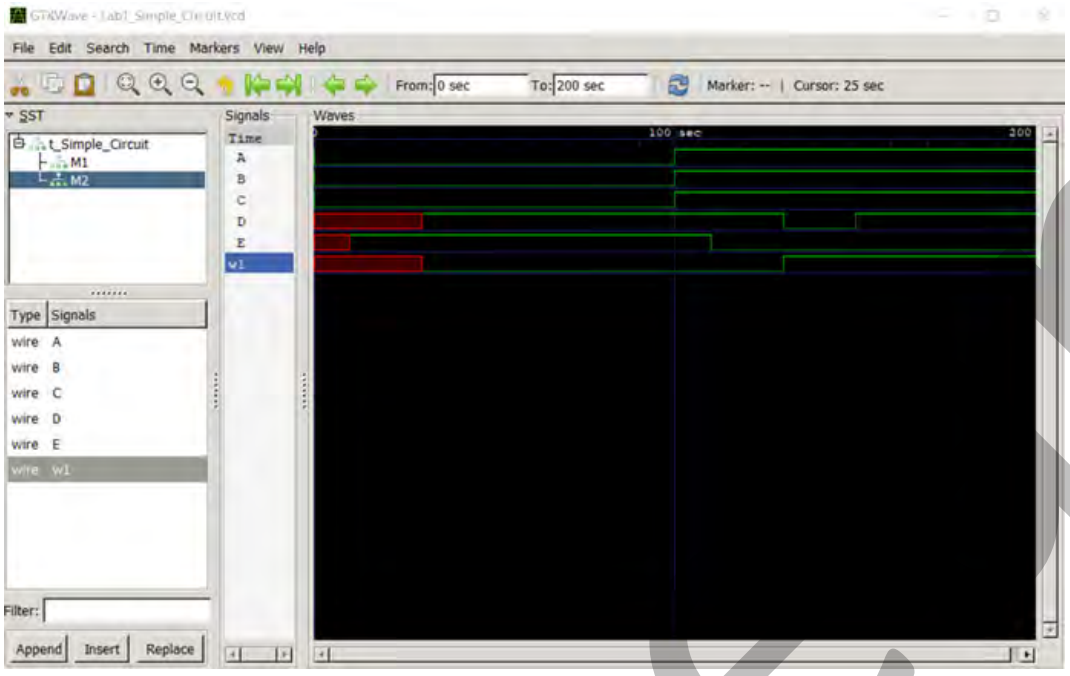
Simple_Circuit_prop_delay.v



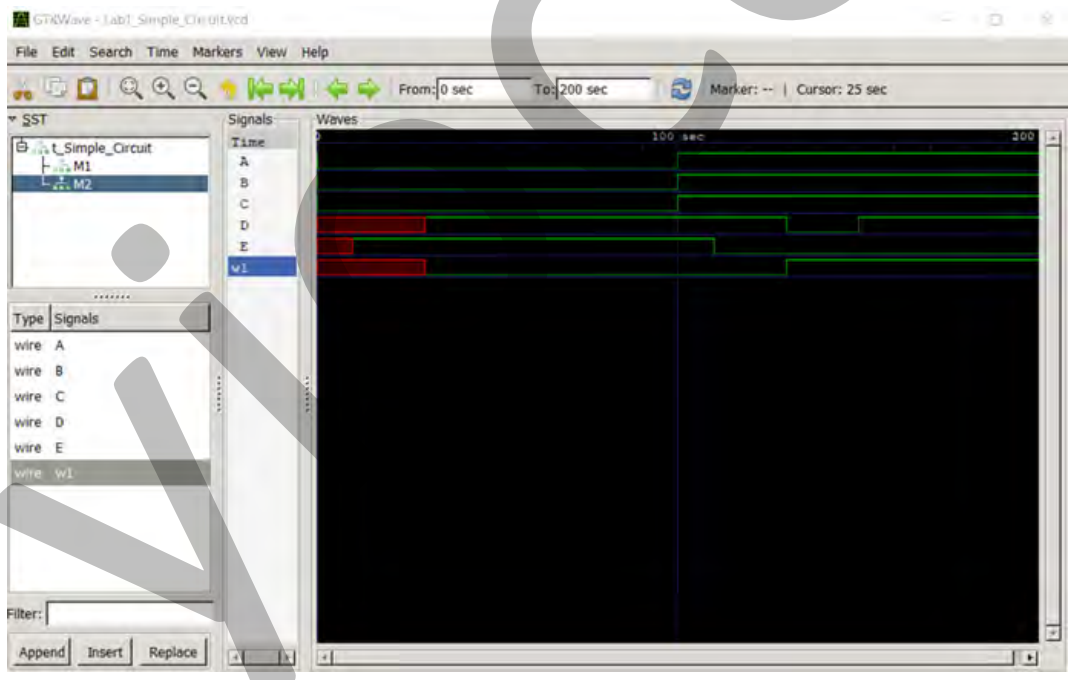
The Simple_Circuit_prop_delay.v circuit has propagation delays, which cause some gates to require more time to change values based on input changes. This is the major difference between this circuit and the other one. As you can see from the two waveforms, the propagation delay affects the output D, E, and the wire w1. To illustrate this, let's take the output E as an example. Since the propagation delay of a NOT gate is 10 time units, the output E will change its value 10 time units after the input C changes its value.

2 Give the waveform of the simulation result of 2A(b), and explain whether there is any difference between the waveforms of 2A(a) and 2A(b).

Simple_Circuit_prop_delay.v (After Swapping)



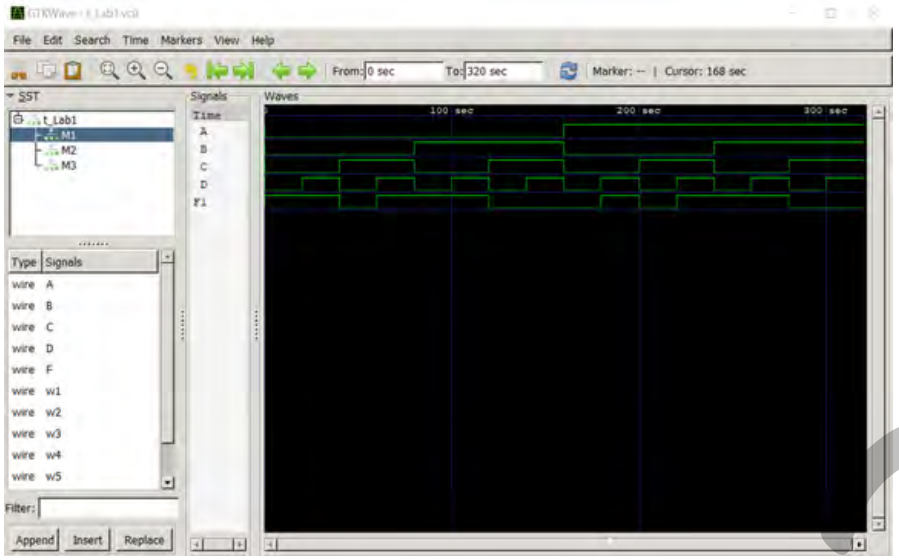
Simple_Circuit_prop_delay.v (Before Swapping)



The waveforms of the two circuits are identical. This is because HDL is a descriptive language and does not directly manipulate the circuit. Therefore, changing the order of statements in HDL does not affect the execution of the program, but only the content of the statements themselves.

3 Give the waveform of the simulation result in 2B(d), and explain whether the three modules are correct.

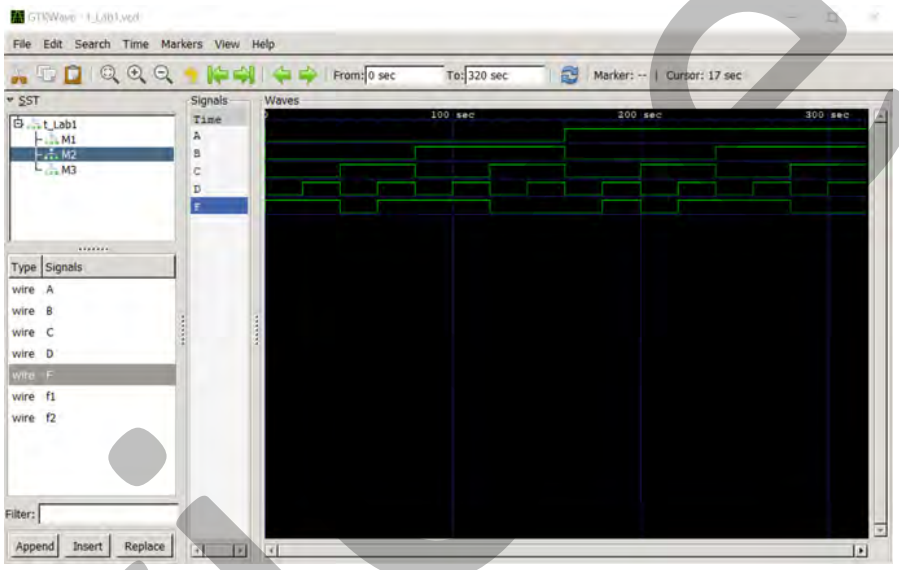
Lab1_gatelevel.v



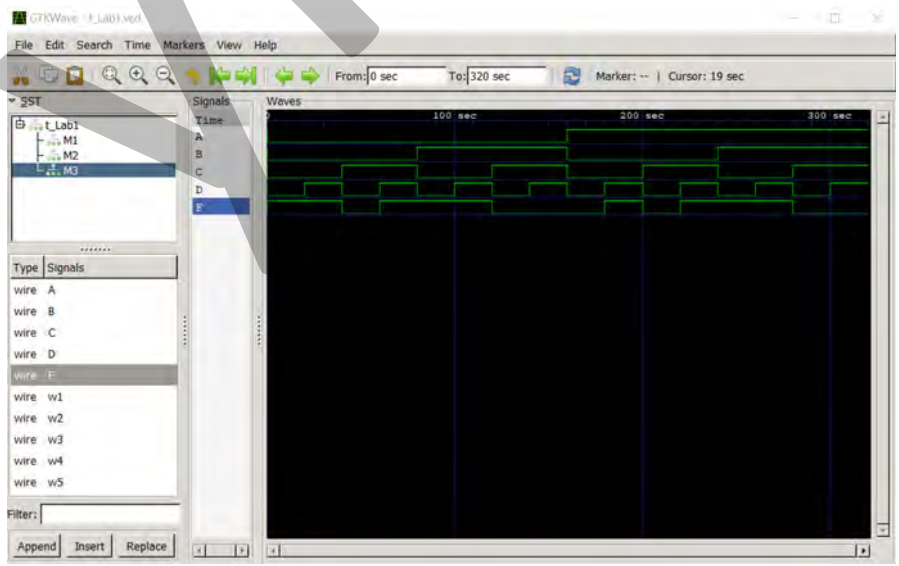
I changed the function to Sum-of-Minterms form to detect its accuracy and found out the results are identical to the waveform. Therefore, the results are correct.

F(A, B, C, D)
=(AB'+C)' + [B(A+C)+D']'
=C'(A'+B) + D(B'+A'C')
=A'C' + BC' + B'D + A'C'D
=A'C' + BC' + B'D
= Σ m (2, 6, 7, 8, 10, 14, 15)

Lab1_dataflow.v



Lab1_gatelevel_UDP.v



4 **Does the design of Figure 1 have the least gate input count for the function of the circuit? If yes, explain your reason; if not, derive the Boolean expression with least gate input count for the function, draw the logic diagram of the circuit by using AND, OR, NOT, NAND, and NOR gates, and write the gate input count of the circuit.**

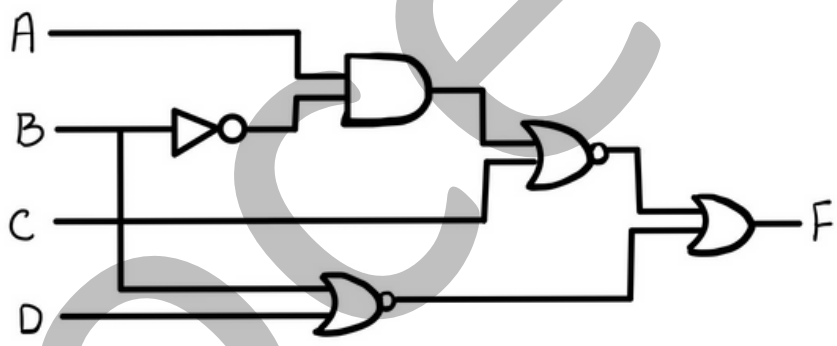
No, the gate input count (GIC) of the current circuit is 14.

Further Simplification of the Boolean equation by Boolean Algebra:

F(A, B, C, D)
=(AB'+C)' + [B(A+C)+D']'
=C'(A'+B) + D(B'+A'C')
=A'C' + BC' + B'D + A'C'D
=A'C' + BC' + B'D
=C'(A'+B) + B'D
=(C+AB')' + (B+D')'

GIC = 9

Logic diagram:



5 **Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab.**

This is my first experience writing and using Verilog, and it presented several challenges for me. Initially, I struggled with the unfamiliar syntax of HDL, which led to several errors in my program. Additionally, the three circuits I simulated in Part B were supposed to have identical lengths, but they appeared different. Upon further investigation, I discovered that I had mistakenly written NOR gates as XOR gates in my gate-level modeling, and I had also entered incorrect values in the truth table for my user-defined primitive. Despite this homework taking me three days to complete, I found this assignment to be incredibly valuable in deepening my understanding of Verilog syntax and descriptive methods. I am confident that this experience will make me better equipped to tackle future assignments, such as the upcoming Lab 3 homework.