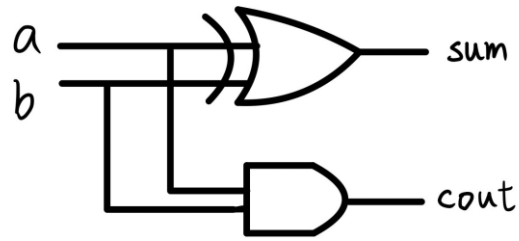
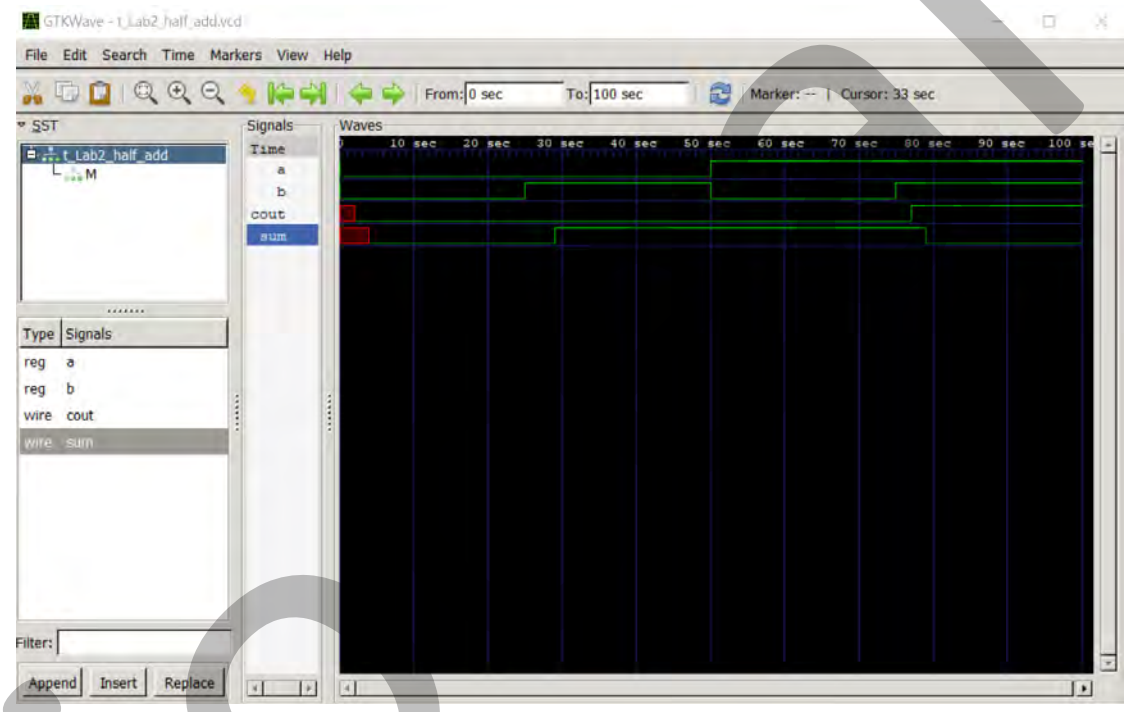
1. Draw the logic diagram of the half adder, attach the waveforms of the simulation results for this module tested in 2A(a)ii, describe the propagation delay of the circuit, and determine whether the waveforms are correct or not.





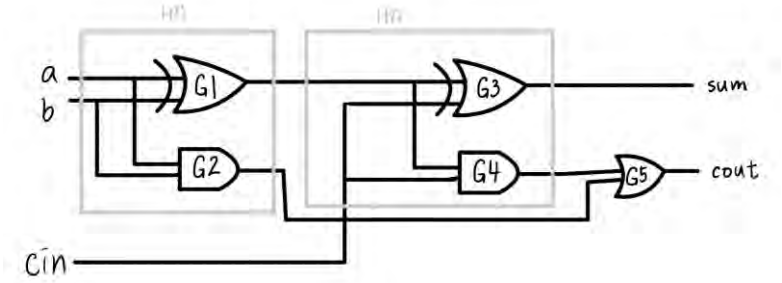
Propagation Delay of the Circuit

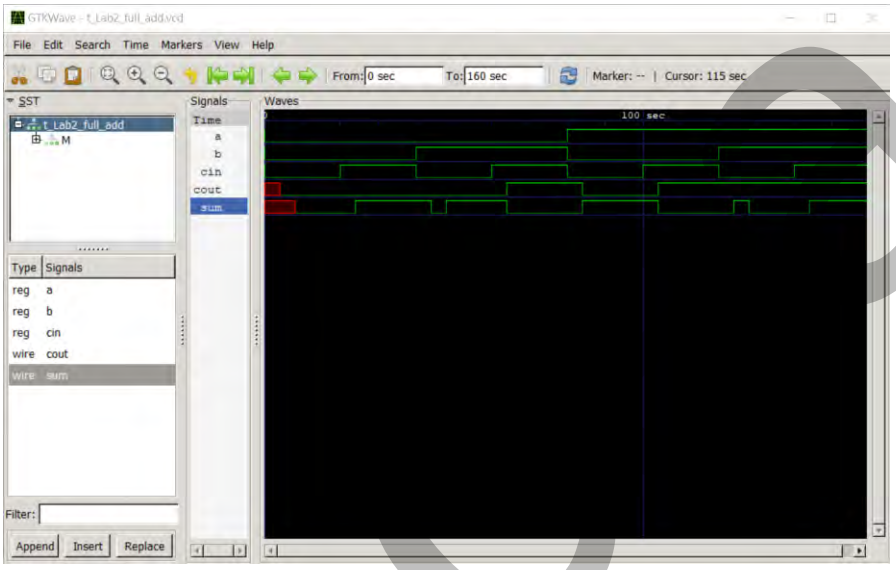
The propagation delay of sum is 4 time units, and the propagation delay of cout is 2 time units. Therefore, the total propagation delay of the half adder is approximately 6 ns.

Correctness of the Waveform

The waveform is correct and shows the expected behavior of a half adder. When A and B are both 0, the sum output S is also 0 and the carry output C is 0. When either A or B is 1, the sum output S is 1 and the carry output C is 0. When both A and B are 1, the sum output S is 0 and the carry output C is 1.

2. Draw the block diagram of the full adder by using half adder as basic blocks, attach the waveform of the simulation results tested in 2A(b)ii, describe the propagation delay of the circuit, and explain whether the waveforms are correct or not.





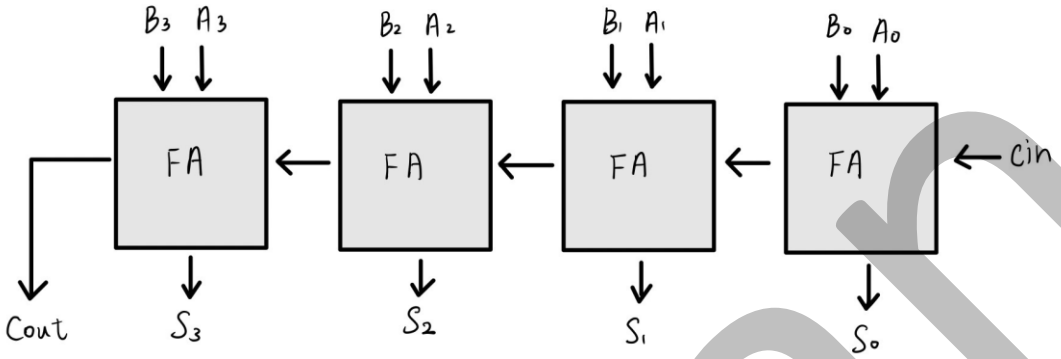
Propagation Delay of the Circuit

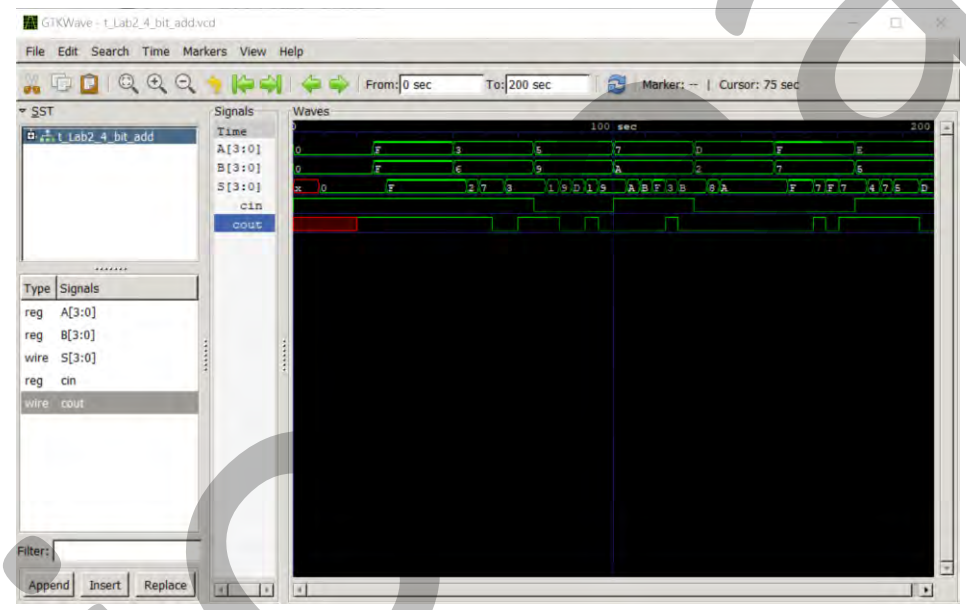
The propagation delay of sum is 8 time units (G1 + G3). On the other hand, the propagation delay of cout is 4 time units only (Max (G2, G4) + G5) since the initial value of b and cin are 0, which generates an output of 0 regard less of the other input of G2 and G4. However, if the initial value isn't 0, the delay of B would be longer.

Correctness of the Waveform

The waveforms appear to be correct. The sum output changes as expected when the input signals change, and the carry out output changes accordingly. The waveform for the carry out output shows that it changes only when there is a carry from the previous bit. The waveform for the sum output shows that it changes only when there is a change in the input signals, indicating that the circuit is working correctly. Also, the waveform results are correct since the truth table derived from the waveform is equivalent to the truth table we learned in the class.

3. Draw the block diagram of the 4-bit ripple-carry adder (RCA) by using full adders as basic blocks, attach the waveform of the simulation results tested in 2A(c)ii, describe the propagation delay of the circuit, and explain whether the waveforms are correct or not.





Propagation Delay of the Circuit

The propagation delay of cout is 16 time units:

4 pairs of full add = 4 × 4 = 16

The propagation delay of S is 32 time units:

4 pairs of full add = 4 × 8 = 32

Correctness of the Waveform

The waveforms in the simulation results appear to be correct. The sum and carry output waveforms match the expected values for each input test case. The propagation delay in the carry signal can be seen in the time taken for the carry output to stabilize after the input carry changes.

4. Derive the Boolean expressions of Pi, Gi, Ci, and Si for the 4-bit carry lookahead adder (CLA). Attach the waveforms of the simulation results for the three different modules of the 4-bit CLA tested in 2A(d)iv, describe the propagation delay of the module written in gate-level modeling, and explain whether the waveforms of the three modules are correct or not.

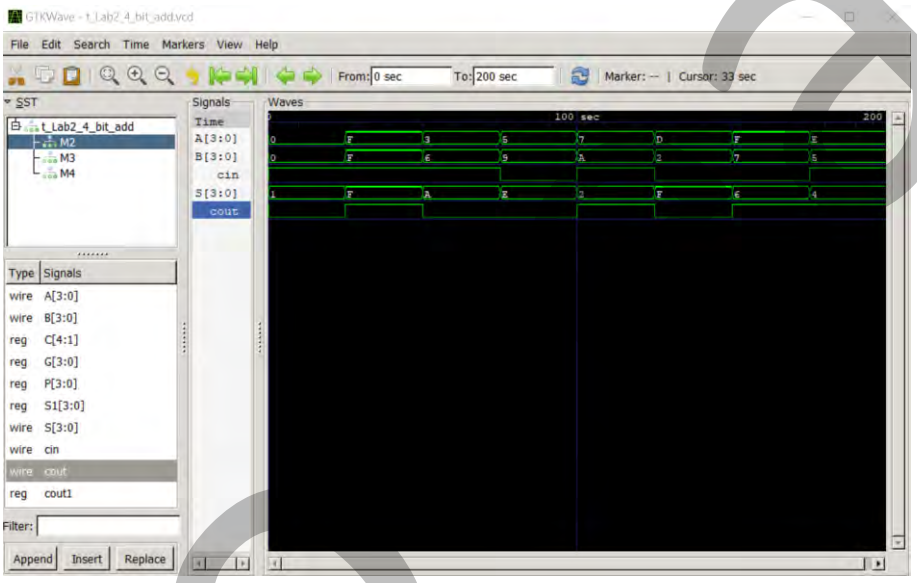
$$P_i = A_i \oplus B_i = A_i B_i' + A_i' B_i$$

$$G_i = A_i B_i$$

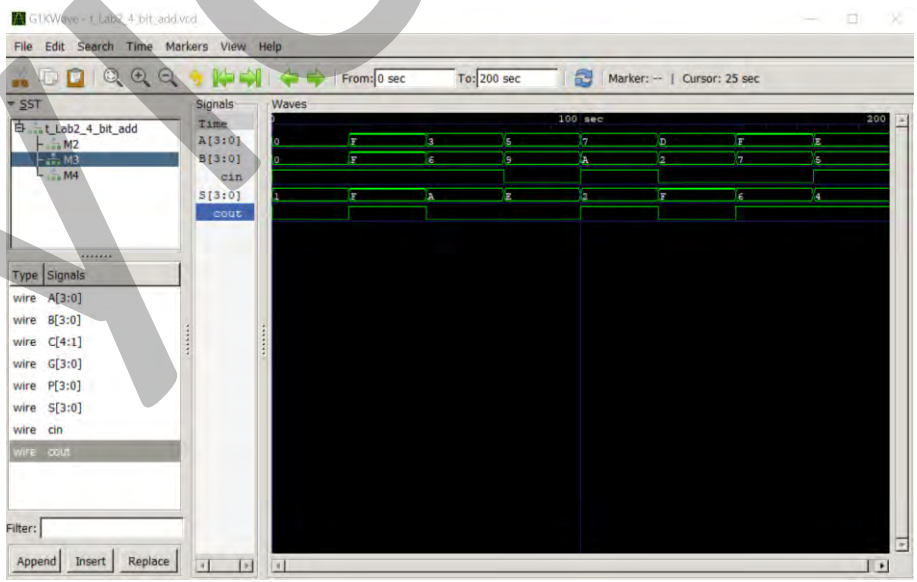
$$C_{i+1} = G_i + C_i P_i$$

$$S_i = C_i \oplus P_i = C_i P_i' + C_i' P_i$$

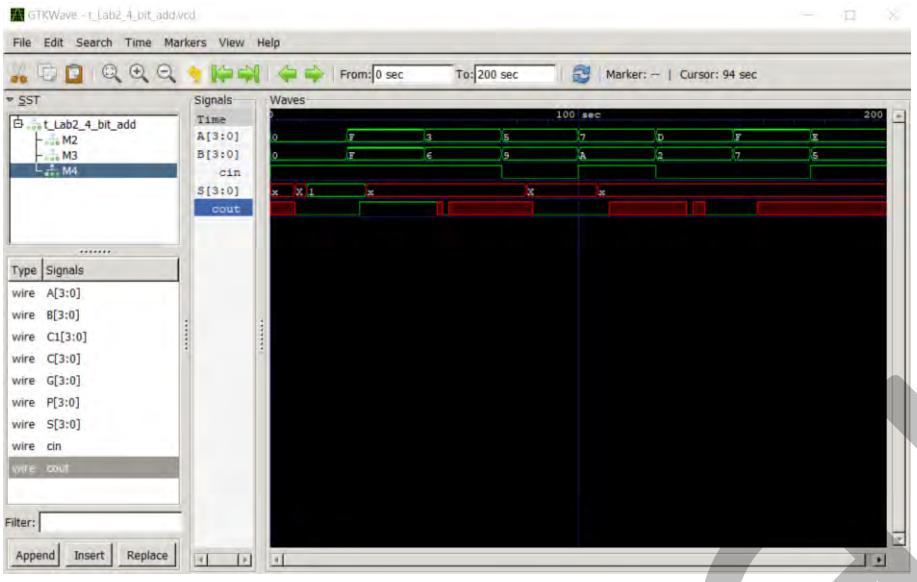
Lab2_4_bit_CLA_beh



Lab2_4_bit_CLA_df



Lab2_4_bit_CLA_gate



Propagation Delay of the Circuit

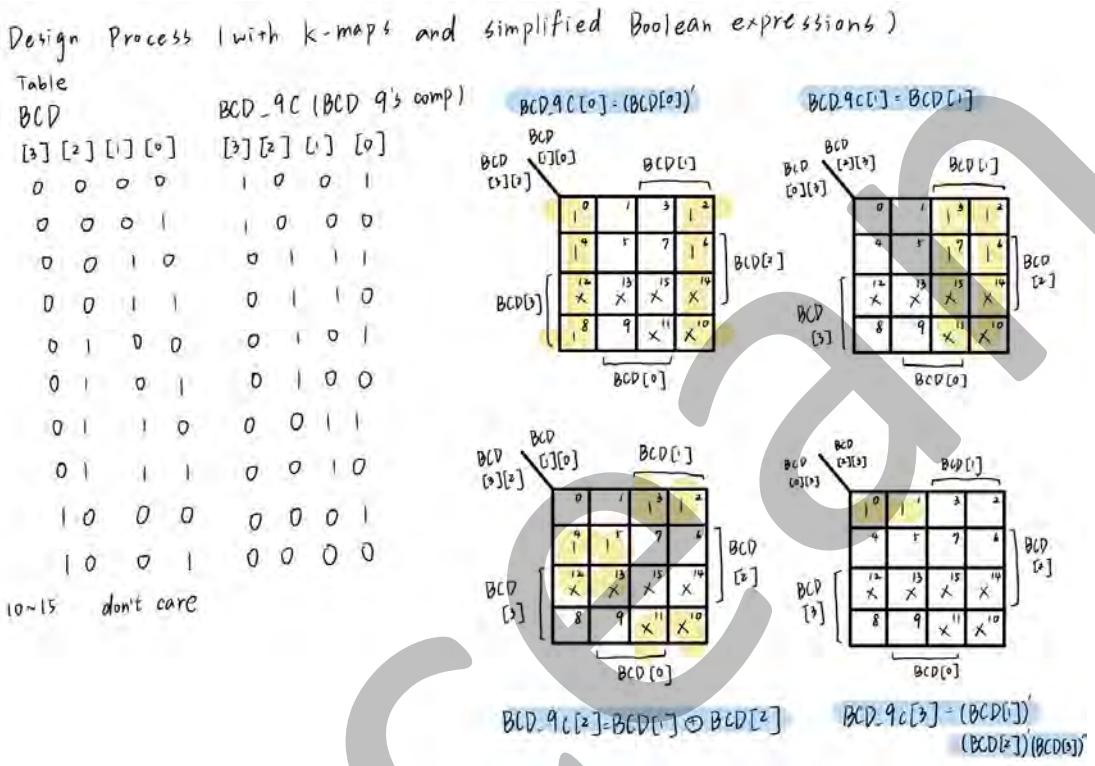
The total propagation delay of cout is 64 time units:

8 XOR gate and 16 AND, OR gate = (8 x 4) + (16 x 2) = 32 + 32 = 64

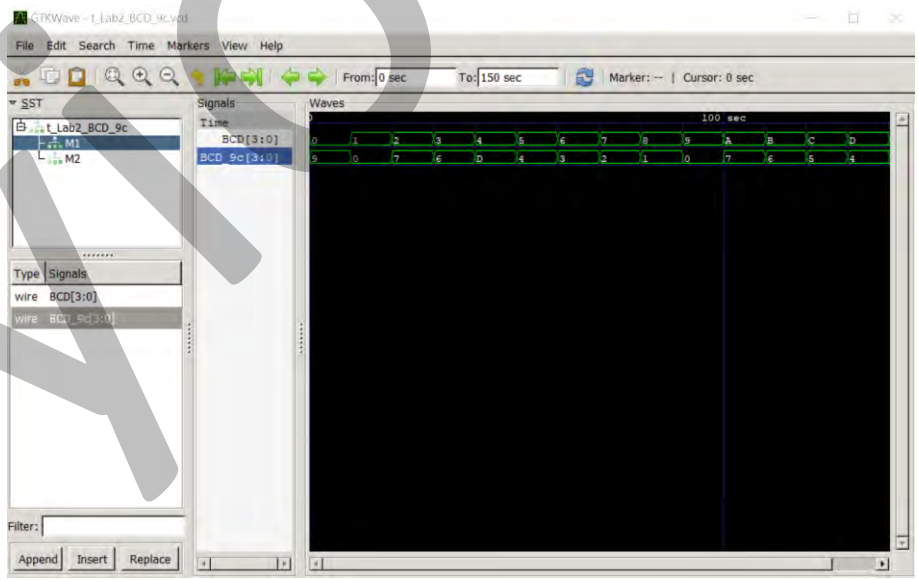
Correctness of the Waveform

The waveforms in the simulation results appear to be correct. The sum and carry output waveforms match the expected values for each input test case. The propagation delay in the carry signal can be seen in the time taken for the carry output to stabilize after the input carry changes.

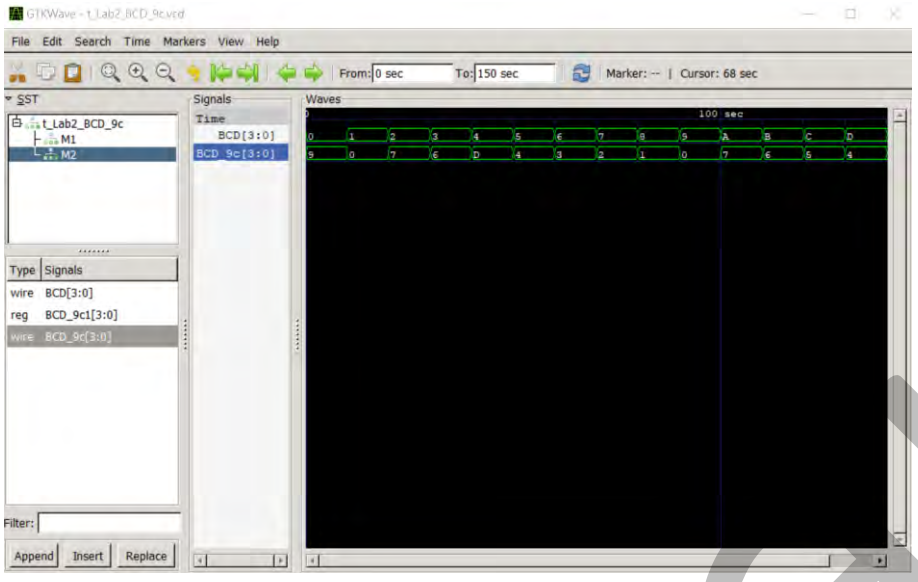
5. Describe the design process of the BCD 9's Complementer, including the Karnaugh maps and the derived simplified Boolean expressions in sum-of-products form. Attach the waveforms of the simulation results for the two different modules tested in 2B(a)iii, and explain whether the waveforms are correct or not.



Lab2_BCD_9c_df



Lab2_BCD_9c_beh

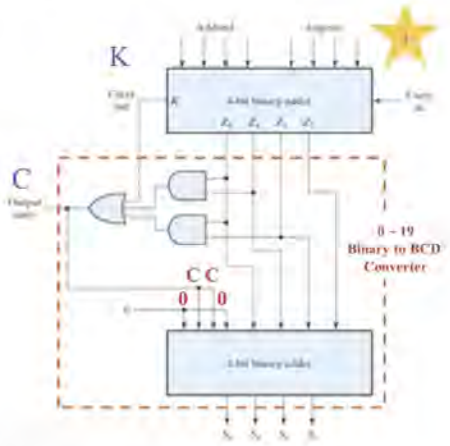


Correctness of the Waveform

The waveforms in the simulation results appear to be correct. The output number waveforms match the expected values for each input test case.

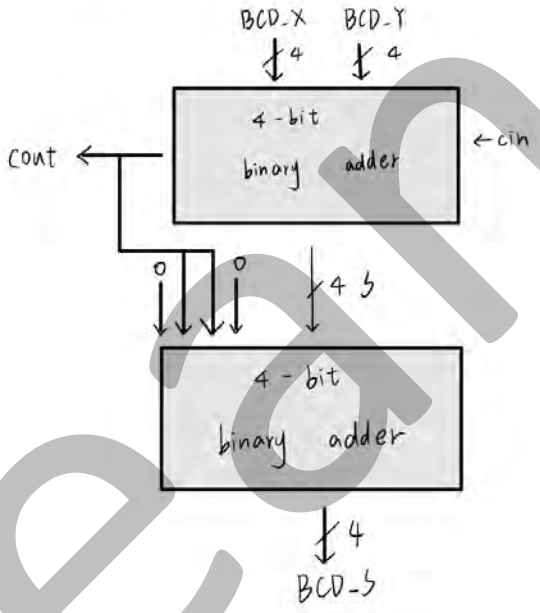
6. Describe the design process of the 1-digit BCD Adder and draw the block diagram of the circuit. Attach the waveforms of the simulation results for the two different modules tested in 2B(b)iii, and explain whether the waveforms are correct or not.

Design Process

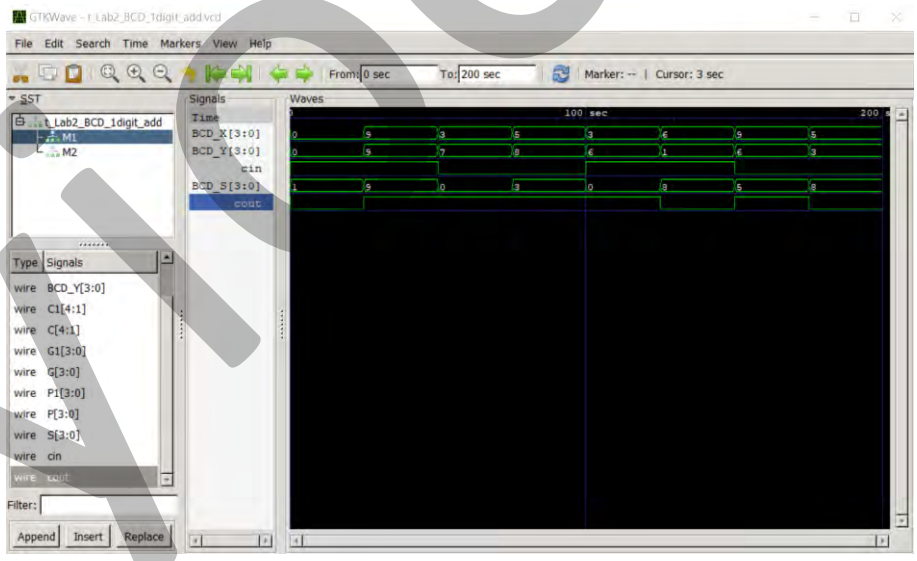


My design is using this circuit which mentions in the lecture. And use the Boolean expression we have derived in the CLA to complete.

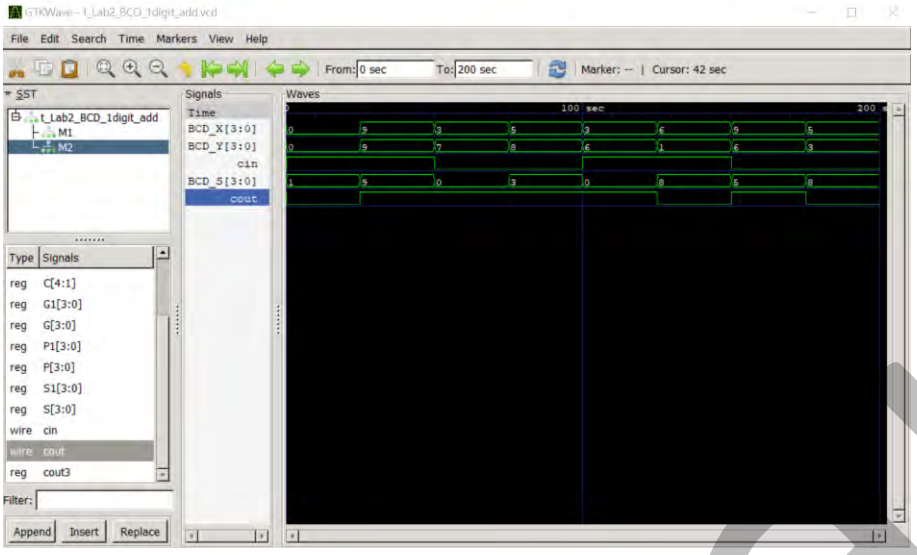
Black diagram



Lab2_BCD_1digit_add_df



Lab2_BCD_1digit_add_beh

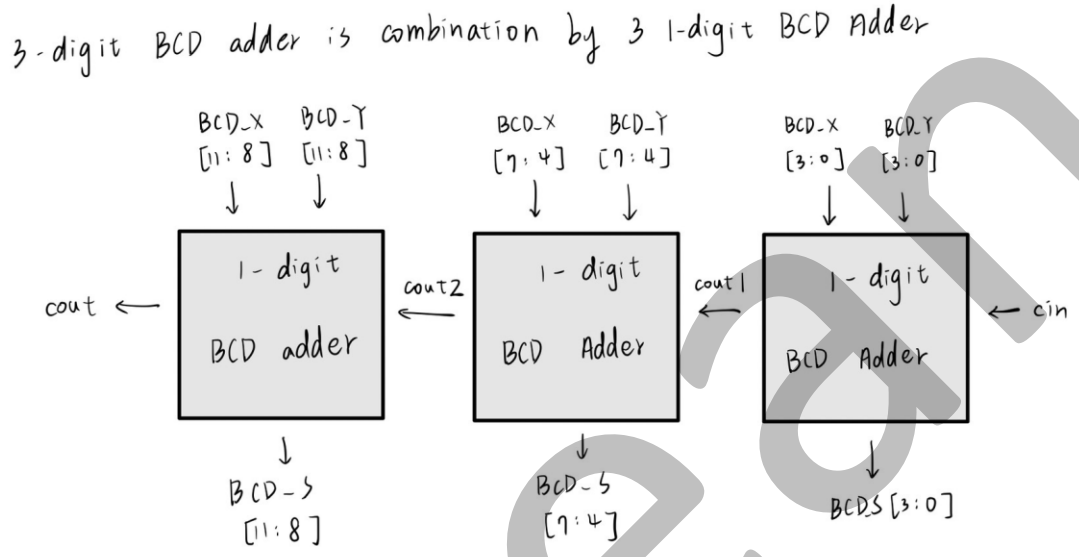


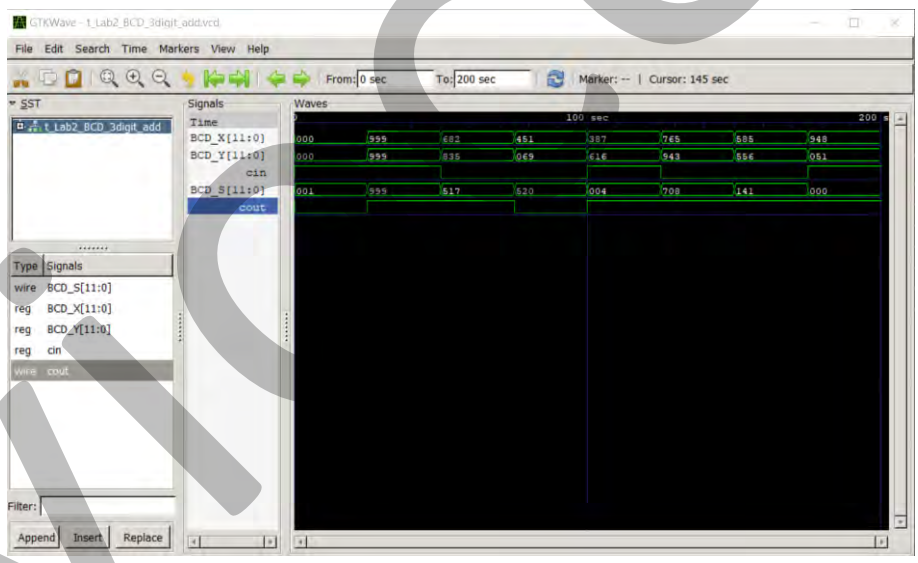
Correctness of the Waveform

The waveforms in the simulation results appear to be correct. The output number and carry out waveforms match the expected values for each input test case.

7. Describe the design process of the 3-digit BCD Adder and draw the block diagram of the circuit. Attach the waveforms of the simulation results for the module tested in 2B(c)ii, and explain whether the waveforms are correct or not.

Design Process and Black diagram





Correctness of the Waveform

The waveforms in the simulation results appear to be correct. The output number and carry out waveforms match the expected values for each input test case.

8. Describe the design process of the 3-digit BCD Adder-Subtractor and draw the block diagram of the circuit. Attach the waveforms of the simulation results for the module tested in 2B(d)ii, and explain whether the waveforms are correct or not.

Design Process and Black diagram

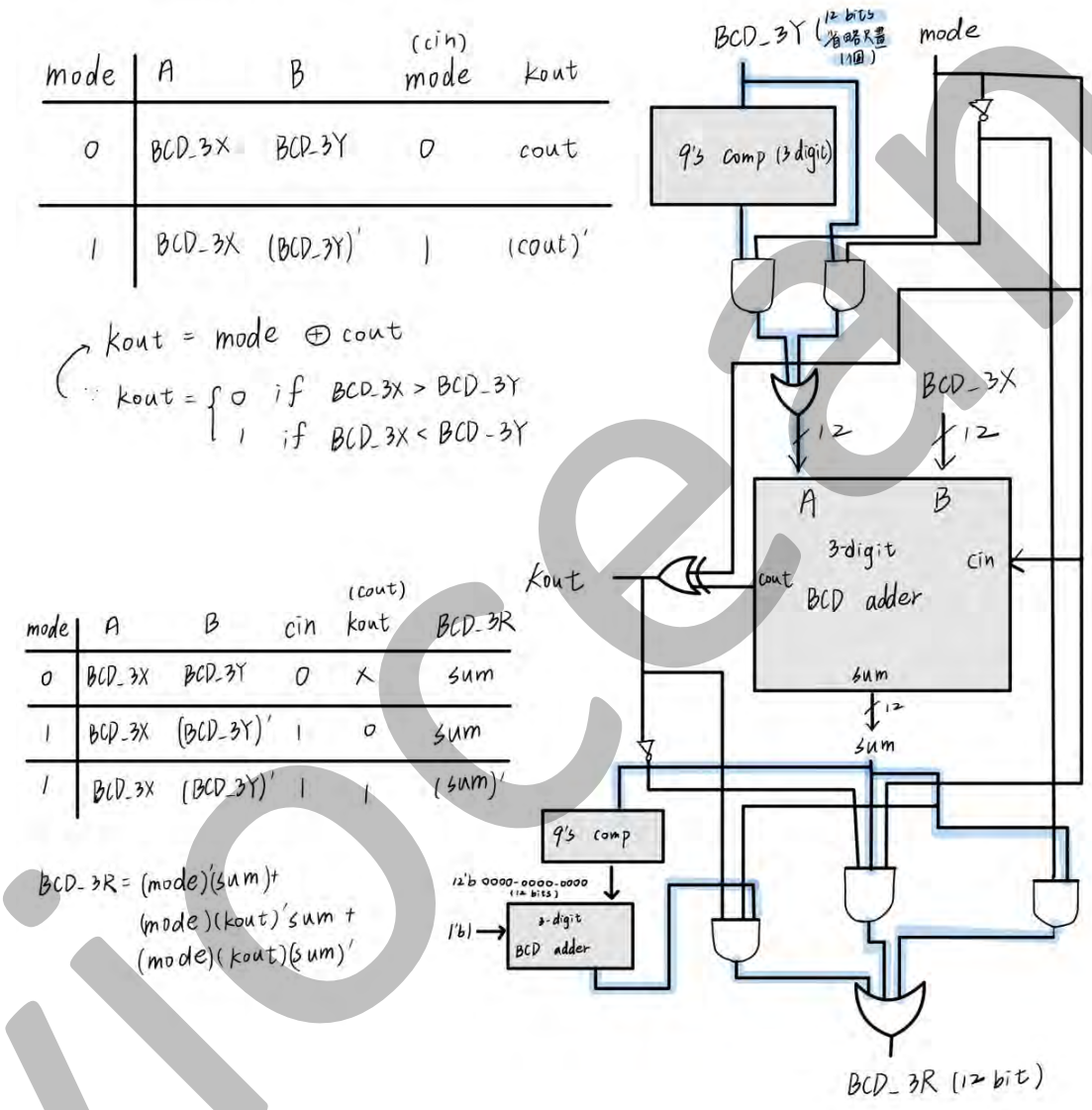
mode	A	B	(cin) mode	kout
0	BCD_3X	BCD_3Y	0	cout
1	BCD_3X	(BCD_3Y)'	1	(cout)'

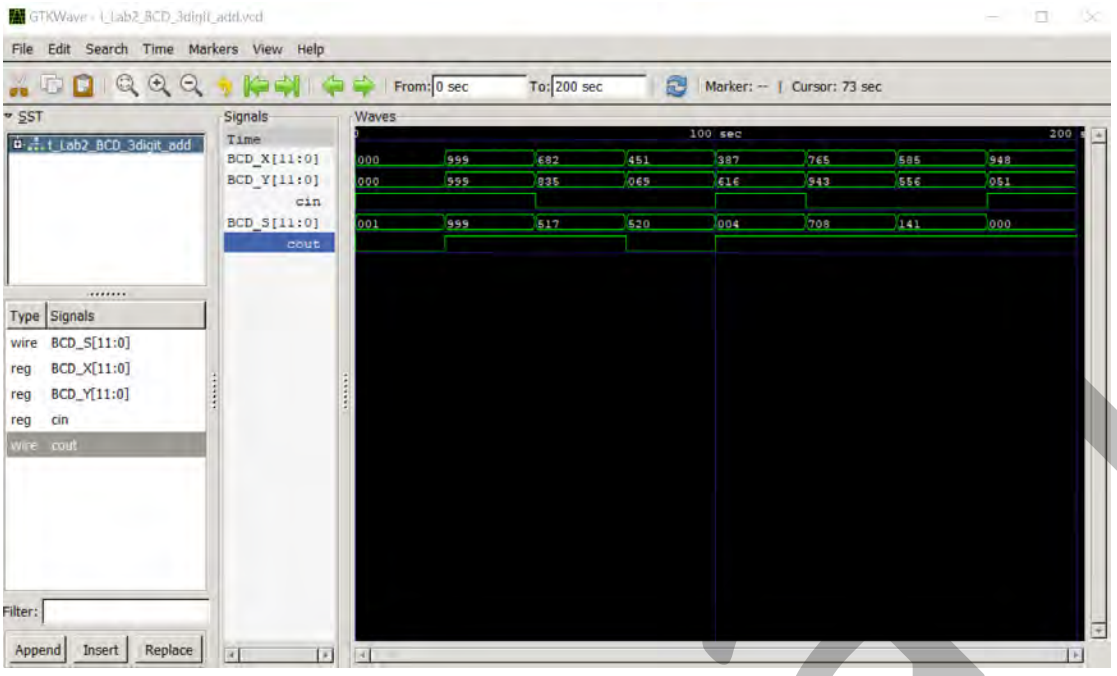
kout = mode ⊕ cout

$$kout = \begin{cases} 0 & \text{if } BCD\_3X > BCD\_3Y \\ 1 & \text{if } BCD\_3X < BCD\_3Y \end{cases}$$

mode	A	B	cin	(cout) kout	BCD_3R
0	BCD_3X	BCD_3Y	0	X	sum
1	BCD_3X	(BCD_3Y)'	1	0	sum
1	BCD_3X	(BCD_3Y)'	1	1	(sum)'

BCD_3R = (mode)'(sum) + (mode)(kout)'sum + (mode)(kout)(sum)'





Correctness of the Waveform

The waveforms in the simulation results appear to be correct. The output number and carry out waveforms match the expected values for each input test case.

9. Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab.

   Throughout this lab unit, I have gained valuable knowledge about designing digital logic circuits using Verilog code. I have successfully modeled and simulated various logic circuits, such as adders, decoders, and BCD 9's complementers.

   Despite some challenges, such as understanding the concept of propagation delay and ensuring the syntax and structure of the Verilog code were accurate, I persevered and learned from my mistakes. I found coding the BCD circuit particularly challenging, but it provided an excellent opportunity to improve my coding skills and learn more about combinational circuits.

   Overall, this lab unit has enhanced my abilities in digital logic circuit design, Verilog coding, and simulation testing. The skills and knowledge gained through this experience will undoubtedly prove invaluable in my future endeavors.