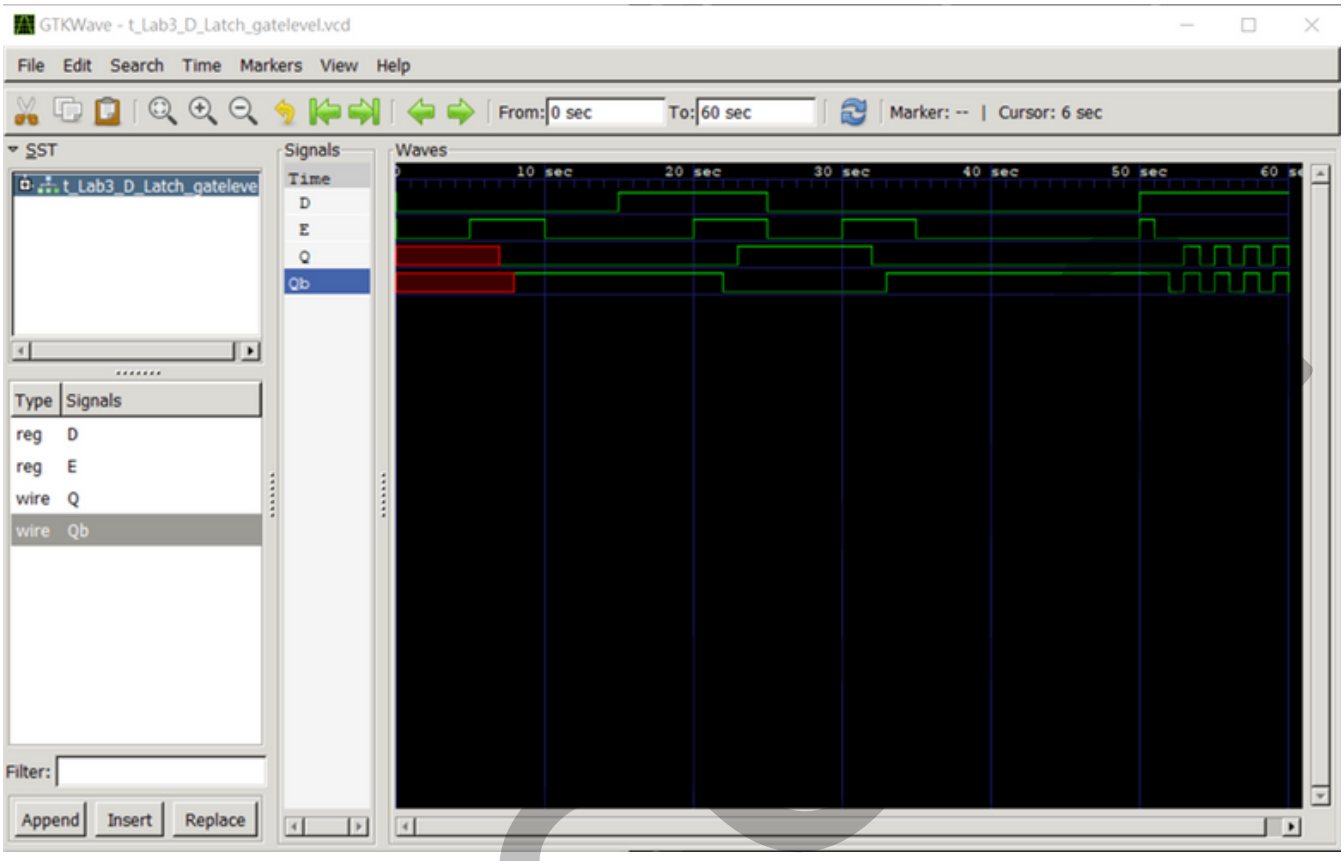
1 **Give the waveform of the simulation results in 2A, and explain whether it is correct or not. If there is a situation where the output oscillates between 0 and 1, please briefly explain the reason.**



According to the Truth Table and Characteristic Table on the right side, and considering the propagation delay issue, we can determine that the waveform is correct. The reason for the oscillation is that in the state where D=1 and E=1, it only lasts for 1 second. The gates in the latch have propagation delay, and before the input E is fully calculated, it changes, causing both Q and Qb to become 1 at 53 seconds, resulting in an indeterminate state.

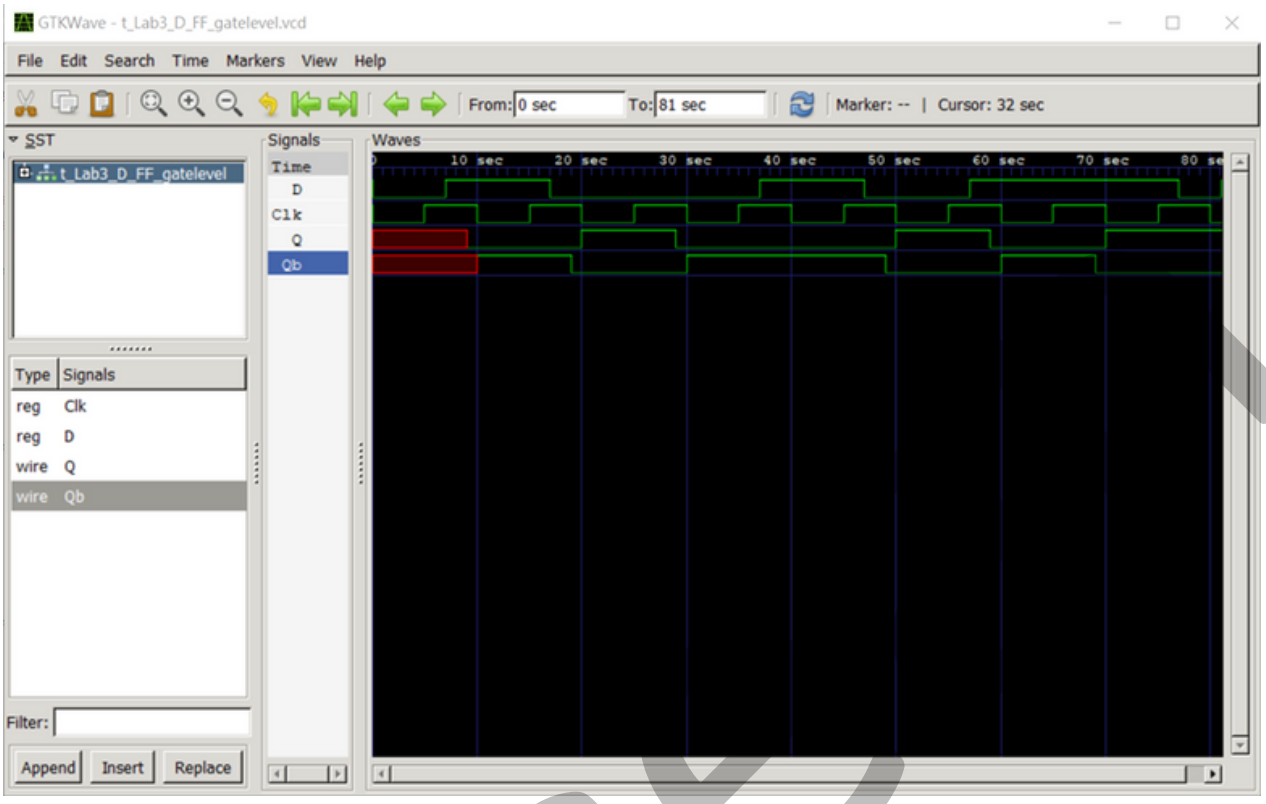
Truth table

Times	D	E	Q^+	Qb^+
0	0	0	–	–
5	0	1	0	1
10	0	0	0	1
15	1	0	0	1
20	1	1	1	0
25	0	0	1	0
30	0	1	0	1
35	0	0	0	1
50	1	1	1	0
51	1	0	1	0

D latch characteristic Table

E	D	Next state
0	X	No change
1	1	Set ($Q^+=1$)
1	0	Resct ($Q^+=0$)

2 Give the waveform of the simulation results in 2B, observe when the flip flop changes state, and explain whether the waveform is correct or not.



According to the Truth Table and Characteristic Table on the right side, and considering the propagation delay issue, we can determine that the waveform is correct. The D flip-flop sets the next stage of Q to the value of D. Therefore, by observing the waveform, we can see that the waveform of Q fluctuates in accordance with the value of D.

Truth Table

D	Q^+	$\bar{Q}^+$
0	0	1
1	1	0
0	0	1
1	1	0
0	0	1
1	1	0
0	0	1
1	1	0

characteristic Table

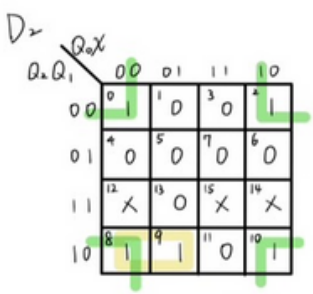
D	Q^+
0	0
1	1

3 **Describe the design of the Mealy type synchronous sequential circuit in 2C by using D flip flops based on the design procedure of synchronous sequential circuits. Derive the flip flop input equations and output equation, and draw the logic circuit diagram of the circuit by using D flip flops as basic building blocks. Then, give the waveform of the simulation results in 2C, explain how you design your testbench, show the state transitions and outputs for the input stimuli, and determine whether each of the two circuit modules designed by you is correct or not.**

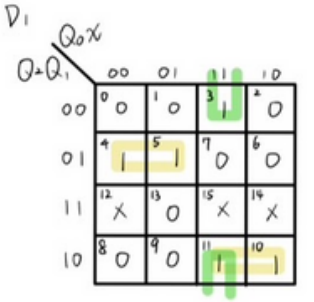
Designing Process

present state	Next state x=0	Next state x=1	Output x=0	Output x=1
S_0	S_4	S_1	1	0
S_1	S_5	S_2	1	0
S_2	S_3	S_3	0	1
S_3	S_0	S_0	0	1
S_4	S_5	S_5	0	1
S_6	–	S_0	–	0

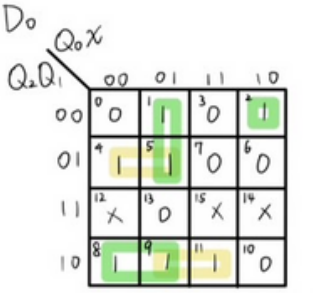
present state $Q_2\ Q_1\ Q_0$	x=0 $Q_2^+\ Q_1^+\ Q_0^+$	x=0 Z	x=1 $Q_2^+\ Q_1^+\ Q_0^+$	x=1 Z
S_0 0 0 0	1 0 0	1	0 0 1	0
S_1 0 0 1	1 0 1	1	0 1 0	0
S_2 0 1 0	0 1 1	0	0 1 1	1
S_3 0 1 1	0 0 0	0	0 0 0	1
S_4 1 0 0	1 0 1	0	1 0 1	1
S_5 1 0 1	1 1 0	1	0 1 1	0
S_6 1 1 0	—		0 0 0	0



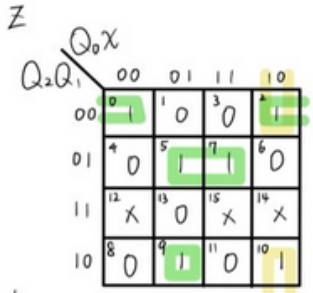
$D_2 = Q_1'X' + Q_2Q_1'Q_0'$



$D_1 = Q_2'Q_1Q_0' + Q_2Q_1'Q_0 + Q_1'Q_0X$

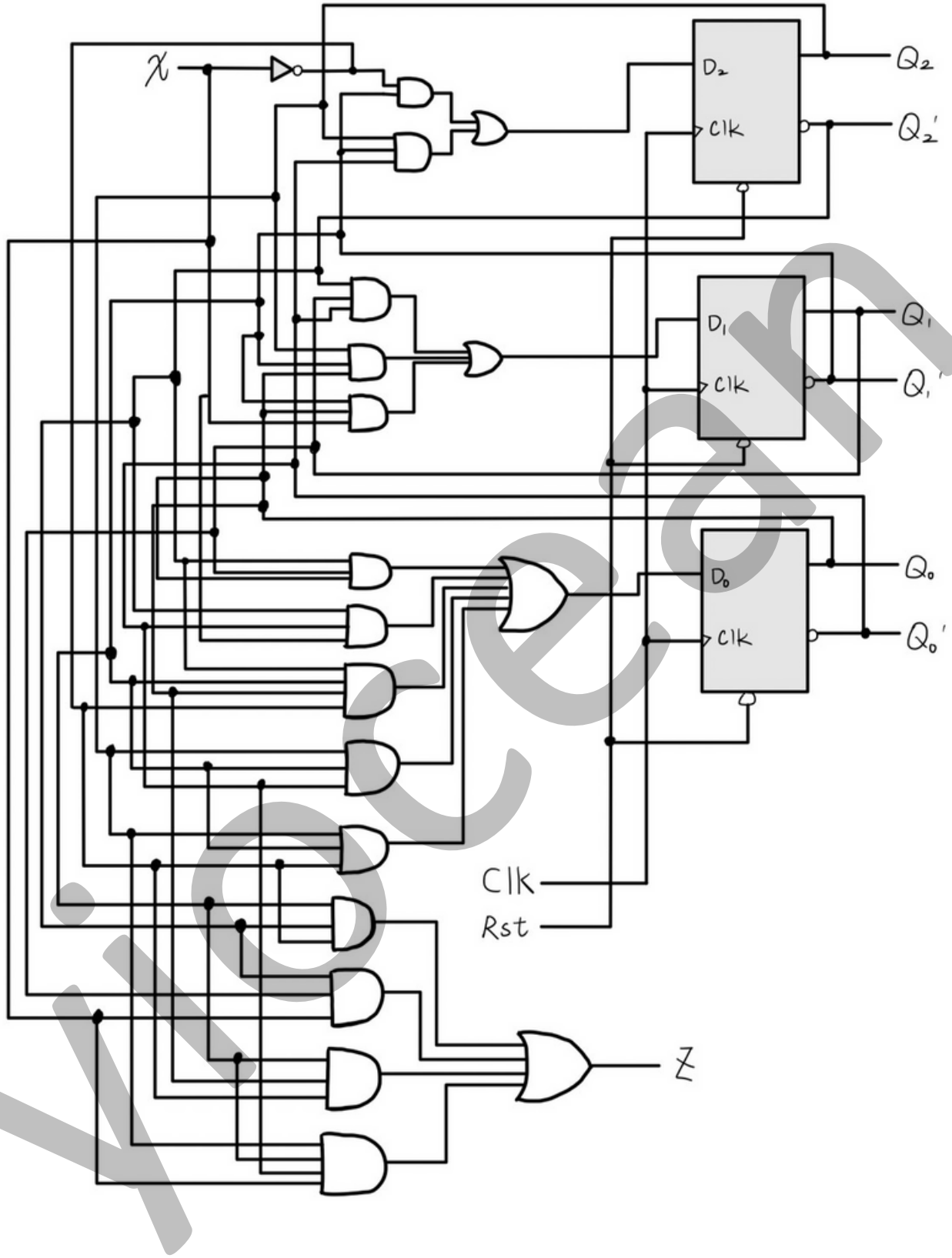


$D_0 = Q_2'Q_1Q_0' + Q_2'Q_0'X + Q_1'Q_1'Q_0X' + Q_2Q_1'Q_0' + Q_2Q_1'X$

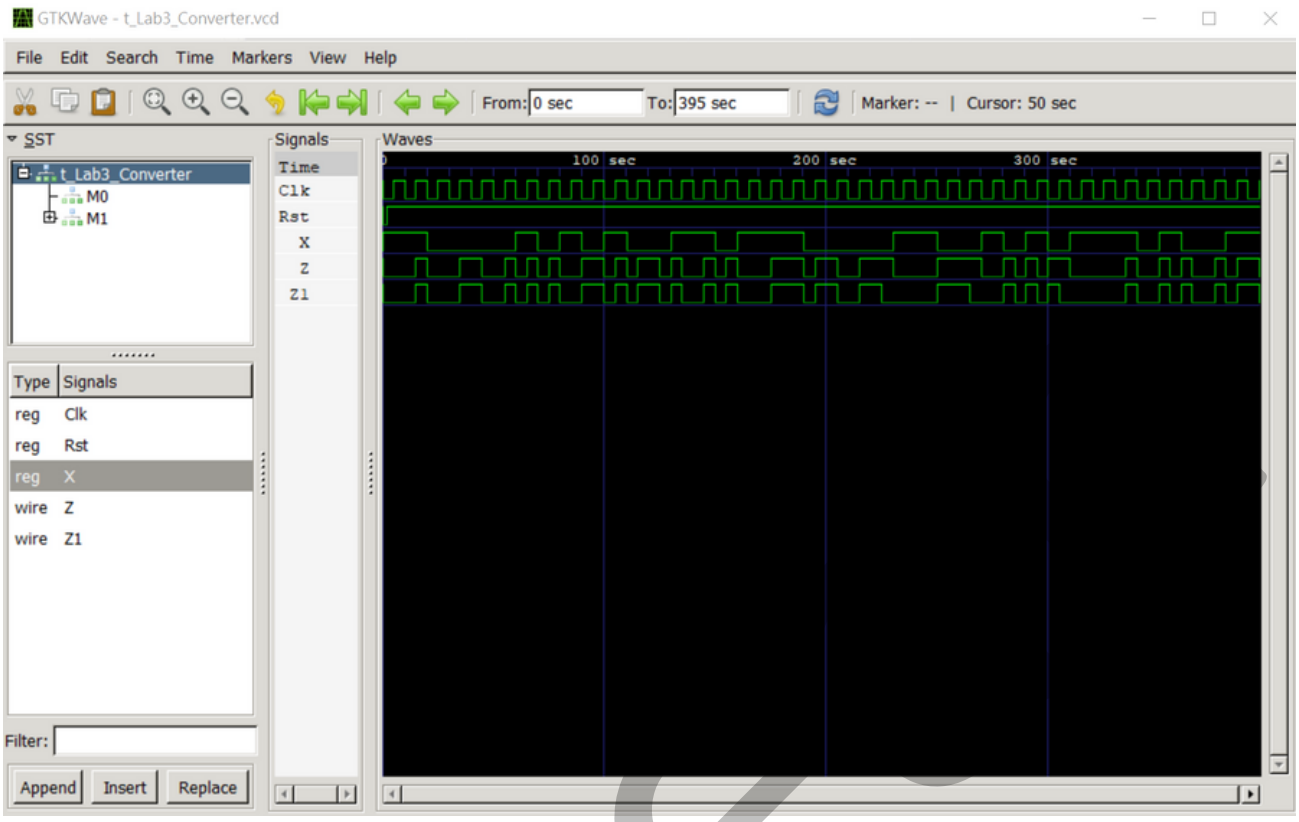


$Z = Q_2'Q_1'X' + Q_2'Q_1X + Q_1'Q_0X' + Q_2Q_1'Q_0'X$

3 **logic circuit diagram**



3 waveform



Z : Lab3_Converter_state_diagram
Z1 : Lab3_Converter_structure

Test Bench Design Describe and outputs for the input stimuli

Since the task requires converting Excess-3 code to BCD code, it is necessary to test whether the conversion is correct by using the Excess-3 codes 0011 to 1100 (0 to 9 in decimal), which correspond to the BCD codes 0000 to 1001 (0 to 9 in decimal). Therefore, the Test Bench needs to be written using the Excess-3 codes 0011 to 1100 (0 to 9 in decimal) for testing.

Correctness of the waveform

The aspect we need to focus on is the situation when CLK equals 0. According to the design method of the Test Bench mentioned above and the corresponding table of Excess-3 codes to BCD on the right side, we can conclude that the waveform is correct.

Decimal	Binay (BCD) 8 4 2 1	Excess-3 Code
0	0 0 0 0	0011
1	0 0 0 1	0100
2	0 0 1 0	0101
3	0 0 1 1	0110
4	0 1 0 0	0111
5	0 1 0 1	1000
6	0 1 1 0	1001
7	0 1 1 1	1010
8	1 0 0 0	1011
9	1 0 0 1	1100

4 Describe what you have learned from this lab unit and discuss the problems or difficulties encountered in this lab.

During this lab, I had the opportunity to implement sequential circuits using HDL. This hands-on experience greatly enhanced my understanding of the inner workings of circuits like the D-Latch and D Flip-Flop. Although it took me some time to grasp the intricacies of the Verilog code for the Mealy Type circuit, the overall experience proved to be highly beneficial for me.