Sensor to ADC—analog interface design

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Introduction

The sensor output voltage span seldom equals the analog-to-digital converter (ADC) input voltage span. Sensor data is lost and/or ADC dynamic range is not fully utilized because the spans are unequal, start at different DC voltages, or both. In Figure 1(a) the spans are equal but offset. This situation requires level shifting to move the sensor output voltage up by one volt so the spans match. In Figure 1(b) the spans are unequal, but no offset exists. This situation requires amplification of the sensor output to match the spans. When the spans are unequal and offset, as is often the case, level shifting and amplification are required to match the spans.

The spans must be matched to achieve optimum performance because mismatched spans lose sensor data or require an expensive increase in ADC dynamic range (higher bit converters). The op amp is the best analog circuit available for matching the spans because it level shifts and amplifies the input voltage to make the spans equal. The op amp is so versatile that it level shifts and amplifies the input signal simultaneously.

A similar but different problem exists in the digital-to-analog converter (DAC)/actuator interface. The DAC output voltage span must match the actuator input voltage span to achieve maximum performance. The procedure for matching the DAC output span to the actuator input span can be quite different from the procedure for matching the sensor output span to the ADC input span. The DAC/actuator interface will be covered in a later issue of this journal. Sensor outputs are usually low-level signals, thus care must be taken to preserve their signal-to-noise ratio. Actuator input signals may require significant power, thus robust op amps are required to drive some actuators.

If you don't have a good working knowledge of circuits and op amp equations, please refer to the "Understanding Basic Analog…" series of application notes available from Texas Instruments. Application Note SLAA068, entitled, "Understanding Basic Analog—Ideal Op Amps," develops the ideal op amp equations based on a set of ideal op amp assumptions that are tabulated in Table 1 for your reference.

Table 1. Ideal system parameter values

PARAMETER NAME	PARAMETER SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	a	∞

The circuit design gets complicated when amplification and level shifting are required. To simplify this article, the op amp equations used here are taken directly from Application Note SLOA030, entitled, "Single Supply Operational Amplifier Design Techniques."

Design procedure

A step-by-step design procedure that results in the proper op amp selection and circuit design begins on the following page. This design procedure works best when the op amp has almost ideal performance so that ideal op amp equations are applicable. The latest generation of rail-to-rail op amps makes the ideal assumption more valid than it ever was. No design procedure can anticipate all possible situations, and depending on the op amp selected, procedure modifications may have to be made to account

Figure 1. Example of spans that require correction

(a)

(b)
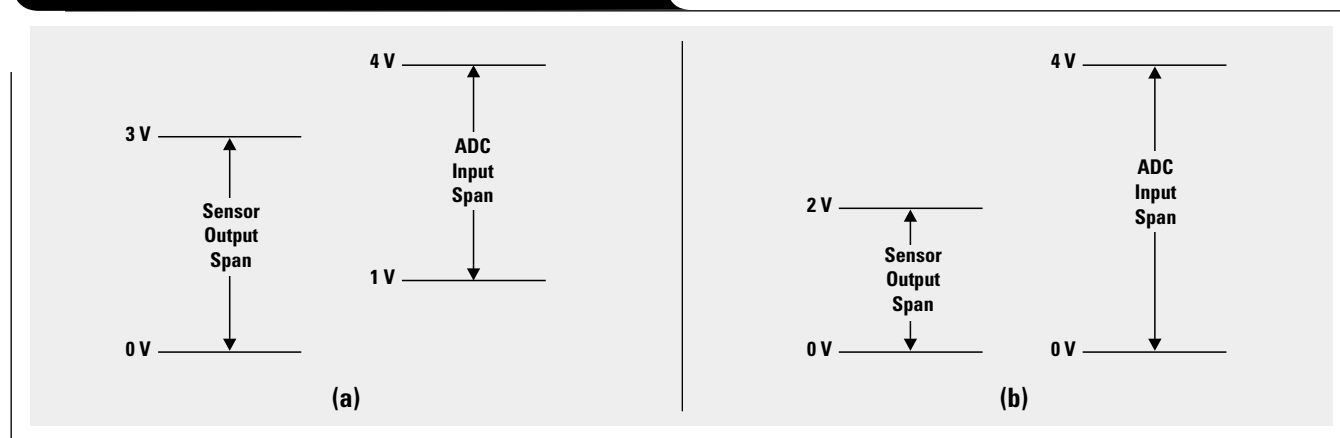
for op amp bias current, input offset voltage, or other parameters.

1. The sensor's output voltage range determines the op amp's required input voltage range (V_{IN1} to V_{IN2}).
2. The ADC's input voltage range determines the op amp's required output voltage swing (V_{OUT1} to V_{OUT2}).
3. Scan the sensor and ADC specifications, and put the data into the format of input/output pairs—V_{IN1}, V_{OUT1} and V_{IN2}, V_{OUT2}.
4. $\Delta V_{OUT}/\Delta V_{IN}$ determines the op amp gain. This is a good point to consider the effect of the input offset voltage.
5. Determine the output impedance of the sensor; this impedance sets the input impedance requirement for the op amp circuit. This is a good point to consider the effect of input bias current.
6. Determine the input impedance of the ADC; this impedance sets the output impedance requirement for the op amp circuit. This is a good point to consider the effect of op amp output impedance.
7. Characterize the reference voltage available, including initial tolerances and drift.
8. Consider noise, power, current drain, frequency response, and other variables that might affect the design.
9. Use the data to form simultaneous equations, and obtain the equation for the op amp circuit.
10. Use the op amp equation to determine the resistor values.
11. Build the circuit and test it.

## Design example—reading the specifications

The sensor in this example is a diode temperature sensor (see Figure 2). The diode in this sensor is selected because it has a specified output voltage of 650 mV at 25°C ambient temperature. The sensor output voltage changes –2 mV/°C, and the application requires the sensor to measure temperatures ranging from –25°C to +100°C. Based on the application, the diode voltage is calculated as 650 – 150 = 500 mV at 100°C, and 650 + 100 = 750 mV at –25°C. This data is translated as V_{IN1} = 500 mV, V_{IN2} = 750 mV.

Systems engineering selected the TLV2544 ADC for this design. The analog input range for this ADC is 0 to 5 V. The sensor signal should completely fill the ADC input span; hence, the ADC input data is translated as the op amp output data V_{OUT1} = 0 V, and V_{OUT2} = 5 V (the circuit uses a single 5-V power supply). The highest temperature corresponds to the lowest ADC output number, so the input and output voltages are coupled as V_{IN1} = 500 mV at V_{OUT1} = 0 V, and V_{IN2} = 750 mV at V_{OUT2} = 5 V. This completes step one.

Determining the op amp input and output voltage ranges

The TLV247x product family is a candidate for the op amp slot, so its specifications are compared against the input and output requirements to determine suitability for the job. The common-mode input voltage range for the TLV247x is from –0.2 V to +5.2 V when V_{CC} = 5 V, and because this range exceeds the input signal range of V_{IN1} = 500 mV to V_{IN2} = 750 mV, the input voltage range

Figure 2. Diode temperature sensor
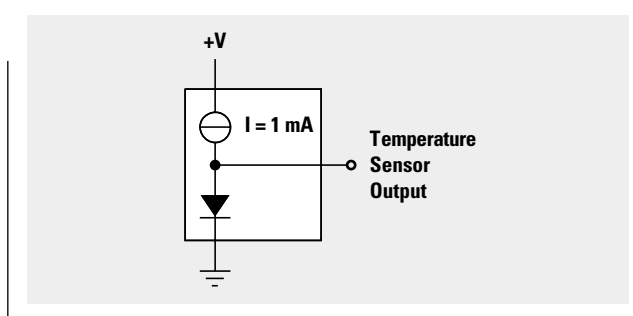
is adequate. The high-level output voltage capability of the TLV247x with a 2-kΩ load is 4.85 V minimum and 4.96 V nominal. The TLV247x low-level output voltage with a 2-kΩ load is 150 mV maximum and 70 mV nominal. I am not a fan of nominal data sheet specifications, but since the load is approximately 20 kΩ (this assumes that conversion and sampling are not coincident), the majority of the units built will be closer to the nominal output voltages than the guaranteed specifications.

The TLV2544 is a 12-bit ADC, and the voltage value of each bit is calculated below as 1.22 mV/bit.

$$\frac{\text{Input}}{\text{Resolution}} = \frac{5}{2^{12}-1} = 1.22 \frac{\text{mV}}{\text{Bit}} \tag{1}$$

The converter loses 150 mV + 150 mV = 300 mV of range because the op amp output voltage swing is limited when using guaranteed specifications. This translates into a loss of 246 bits out of 4095 bits because the full input range of the ADC is not used. The actual error will be closer to 50 mV + 30 mV = 80 mV (allowing for a larger load), and this translates into a loss of 66 bits out of 4095 bits.

The 5-V power supply feeds the op amp and ADC, and this guarantees that some range will be lost because no op amp can drive current into a load without incurring a voltage drop. The only way to preserve the converter's dynamic range is to power the op amp from a larger power supply. When converter cost was exorbitant, op amps driving 5-V ADCs were run from ±12-V power supplies, but this isn't required now in the day of moderately priced converters. Let the circuit be designed for an output range of 0 V to 5 V, knowing that the guaranteed range is 150 mV to 4.85 V and that the accuracy loss has to be accepted.

The op amp gain and impedances

The amplifier gain is approximately 5/0.25 = 20; and the TLV247x, with an open-loop gain in excess of 100,000, can accurately amplify with a closed-loop gain of 20 (especially at the low frequencies involved in temperature measurement). The op amp's input offset voltage (2.2 mV maximum) is multiplied by the gain, so the offset voltage presented to the converter input is 44 mV. This introduces a 36-bit error into the system.

The output impedance of the sensor is essentially the output impedance of a forward-biased diode. The equation

Continued from previous page

for a forward-biased diode is given below, where r_e is the diode resistance and I_{BIAS} is given in mA.

$$r_e = \Theta\frac{26}{I_{BIAS}} = 26\,\Omega \qquad (2)$$

The diode resistance, 26 Ω, forms a voltage divider with the op amp input resistance. The TLV247x input resistance is 10^{12} Ω nominal, but let's assume that circuit resistors lower the input resistance to 20 kΩ. A voltage divider is formed by the sensor output resistance and the circuit input resistance (see Equation 3). The diode resistance introduces a 1.3-mV error that is approximately one bit, so the diode resistance is neglected.

$$Error = \frac{R_{IN}}{R_{IN} + R_{DIODE}} = \frac{20,000}{20,000 + 26} = .9987 \qquad (3)$$

The input bias current (300 pA maximum) introduces an error by causing a voltage drop across the parallel combination of the feedback and input resistor. Assuming 20-kΩ input resistance and a gain of 20, the voltage drop at the converter input is $(400 \times 10^3)(300 \times 10^{-12}) = 0.12$ mV, or less than one bit. The input current error is neglected.

The input impedance of the converter is very high most of the time, but it is 20 kΩ minimum when sampling. The output resistance of the TLV247x is 1.8 Ω nominal. The op amp output resistance and converter input resistance form a voltage divider that introduces a .09-mV error, which is less than one bit; thus the op amp output impedance is neglected.

Selecting a reference

The reference is an input to the ADC, therefore any noise or disturbance on the reference input shows up as an error. The reference input is decoupled with a .01-µF capacitor to reduce noise. A reference diode is used because the power supply (5 V) has too much noise and drift to be used as a reference. A 2.5-V stable temperature-compensated reference diode is selected for the design. This diode has an initial tolerance of ±10 mV and a total drift of 10 mV. The converter range sacrificed to the diode inaccuracy is 25 bits.

Selecting the op amp

The TLV247x is a CMOS op amp, so it has low power and current drain. The op amp noise is low for a CMOS device, and it shouldn't cost one bit in accuracy. The biggest anticipated noise problem comes from the cable carrying the sensor voltage to the op amp input. Shielding the sensor input (by tying one end of the shield to ground) can reduce this noise, and if a ground plane circuit board is used, conducted noise should not be a problem. Temperature is a slowly changing variable, so the op amp frequency response is not important. The TLV247x satisfies all the requirements and justifies the ideal op amp assumption, so it is selected for the design.

Figure 3. Op amp circuit yielding $V_{OUT} = 20\,V_{IN} - 10$
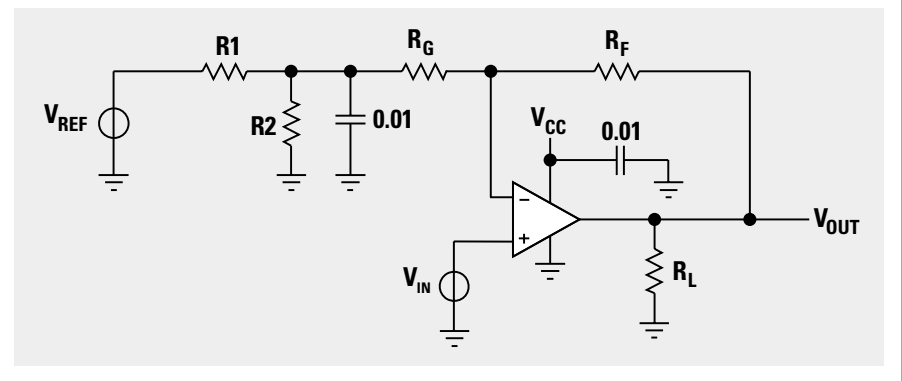
Simultaneous equations

The equation of an op amp is the equation of a straight line; therefore, there are four potential solutions to the problem. One solution is correct for the problem at hand, and the method of finding that solution is to solve simultaneous equations because their solution yields the magnitude and sign of the slope and zero axis intercept (m, b). Use the input/output data to make the following two equations.

$$0 = .5m + b \qquad (4)$$

$$5 = .75m + b \qquad (5)$$

Equation 4 yields m = –2b. Substituting Equation 4 into Equation 5 yields Equation 6.

$$-\frac{m}{2} = 5 - .75m \qquad (6)$$

Equation 6 defines the slope as m = 20 and the zero axis intercept as b = –10. Substituting these values back into Equations 4 and 5 proves that the algebra is correct. The equation for an op amp has the form $V_{OUT} = mV_{IN} + b$; thus, substituting the values obtained from Equation 6 yields Equation 7.

$$V_{OUT} = 20V_{IN} - 10 \qquad (7)$$

Determining the resistor values

The op amp circuit that yields the transfer function given in Equation 7 is shown in Figure 3, and the transfer function for that circuit is given in Equations 8, 9, and 10.

$$V_{OUT} = V_{IN}\left(\frac{R_F + R_G + R_1\|R_2}{R_G + R_1\|R_2}\right)\cdots\cdots \qquad (8)$$

$$\cdots - V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1\|R_2}\right)$$

$$m = \frac{R_F + R_G + R_1\|R_2}{R_G + R_1\|R_2} \qquad (9)$$

$$|b| = V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 + R_2}\right) \qquad \textbf{(10)}$$

Some simplification is desired prior to making the final calculations. If $R_G \gg (R_1 + R_2)$ then $(R_1 + R_2)$ and $R_1 \| R_2$ can be neglected, and Equations 9 and 10 reduce to Equations 11 and 12.

$$m = 20 = \frac{R_F + R_G}{R_G} \qquad \textbf{(11)}$$

$$|b| = \left(\frac{R_2}{R_1 + R_2}\right)\frac{R_F}{R_G} \qquad \textbf{(12)}$$

Let $R_G = 27$ kΩ; then Equation 11 yields $R_F = 513$ kΩ. Select $R_F = 510$ kΩ because it is the closest standard 5% value. Substituting the resistor values for R_F and R_G into Equation 12 yields $R_1 = .888R_2$. Select $R_2 = 270$ Ω and $R_1 = 240$ Ω. The error incurred by neglecting R_1 and R_2 is approximately $.51/27 = .018$; this error is much less than the resistor tolerances.

The resistors are selected from the 5% values, but that does not mean that they have to have 5% tolerances. The resistor tolerances in a 12-bit circuit are normally 1% or smaller because 1% metal film resistors have excellent drift and end-of-life tolerances.

Adjustments

Resistors with a 1% tolerance have about a 3% tolerance at the end of their life. A 3% tolerance equates to about 5-bit accuracy, so the circuit must be adjusted to obtain an initial accuracy close to 12 bits. R_2 is split into R_{2A} and R_{2B} as shown in Figure 4. If R_{2A} is 220 Ω and R_{2B} is a 100-Ω pot, the reference voltage can be adjusted from 1.19 V to 1.32 V, and this yields an adjustment range of approximately 14%.

The reference adjustment is easy to implement with a DAC. The inverting gain is $R_F/R_G = 19$. If R_F is changed to a fixed resistor, $R_{FA} = 470$ kΩ, and a pot, $R_{FB} = 100$ kΩ, the gain adjustment range is approximately 10%. The gain is hard to adjust with a DAC because a resistor value must be changed, but sometimes a DAC and multiplier are used to give a variable gain.

Set the gain first and the reference voltage second to minimize interaction between the adjustments.

Build and test

After the calculations are completed, build and test the circuit. The circuit should be built with off-the-shelf components, not with selected or hand-delivered samples. Sometimes samples must be used to build the circuit because samples are the only parts available. There is some element of risk using samples, so retesting is in order when components become available from production.

The performance test results should be closer to nominal than the extremes because randomly selected components should have close-to-nominal values. If the data is skewed from nominal, troubleshoot the circuit until you find the reason for the skew. Skewed data is often an indicator of an error in the calculations. Also, test for conditions well beyond the design specifications. Look for problems like latch-up, find out what happens when the input voltage goes out of range, and check the noise performance. The prudent engineer tests extensively and makes changes prior to production.

Summary

Start the design with a review of the design specifications, sensor specifications, and potential component specifications. Use the sensor and ADC specifications to formulate the op amp input and output voltages. Calculate the effects of the input and output impedances; insure that op amp imperfections don't interfere with the design; and select the reference, ADC, and op amp. Use simultaneous equations to determine what equation the op amp must implement. Use the op amp equation to select a circuit configuration from the reference, and calculate the resistor values using the reference equations. Build and test the circuit, and if the results are good, you are done.

References

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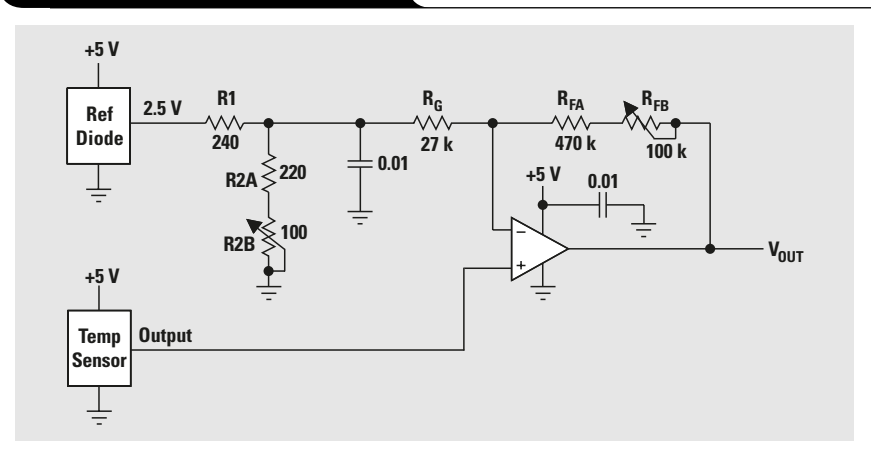| Document Title	TI Lit. #
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Figure 4. Final circuit diagram

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