FM28V100

1Mbit Bytewide F-RAM Memory

Features

1Mbit Ferroelectric Nonvolatile RAM

- Organized as 128Kx8
- High Endurance 100 Trillion (10^{14}) Read/Writes
- NoDelay™ Writes
- Page Mode Operation to 33MHz
- Advanced High-Reliability Ferroelectric Process

Superior to Battery-backed SRAM Modules

- No battery concerns
- Monolithic reliability
- True surface mount solution, no rework steps
- Superior for moisture, shock, and vibration

SRAM Replacement

- JEDEC 128Kx8 SRAM pinout
- 60 ns Access Time, 90 ns Cycle Time

Low Power Operation

- 2.0V – 3.6V Power Supply
- Standby Current 90 µA (typ)
- Active Current 7 mA (typ)

Industry Standard Configurations

- Industrial Temperature -40° C to +85° C
- 32-pin “Green”/RoHS Package

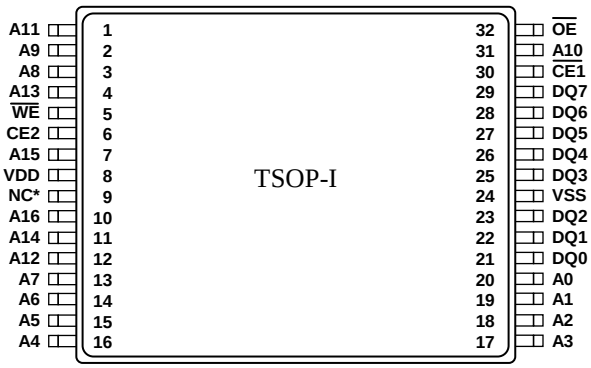
General Description

The FM28V100 is a 128K x 8 nonvolatile memory that reads and writes like a standard SRAM. A ferroelectric random access memory or F-RAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 10 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and very high write endurance make F-RAM superior to other types of memory.

In-system operation of the FM28V100 is very similar to other RAM devices and can be used as a drop-in replacement for standard SRAM. Read and write cycles may be triggered by toggling a chip enable pin or simply by changing the address. The F-RAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the FM28V100 ideal for nonvolatile memory applications requiring frequent or rapid writes in the form of an SRAM.

Device specifications are guaranteed over the industrial temperature range -40°C to +85°C.

Pin Configuration



* Reserved for A17 on 2Mb

Ordering Information	
FM28V100-TG	32-pin “Green”/RoHS TSOP
FM28V100-TGTR	32-pin “Green”/RoHS TSOP, Tape & Reel

This product conforms to specifications per the terms of the Ramtron standard warranty. The product has completed Ramtron’s internal qualification testing and has reached production status.

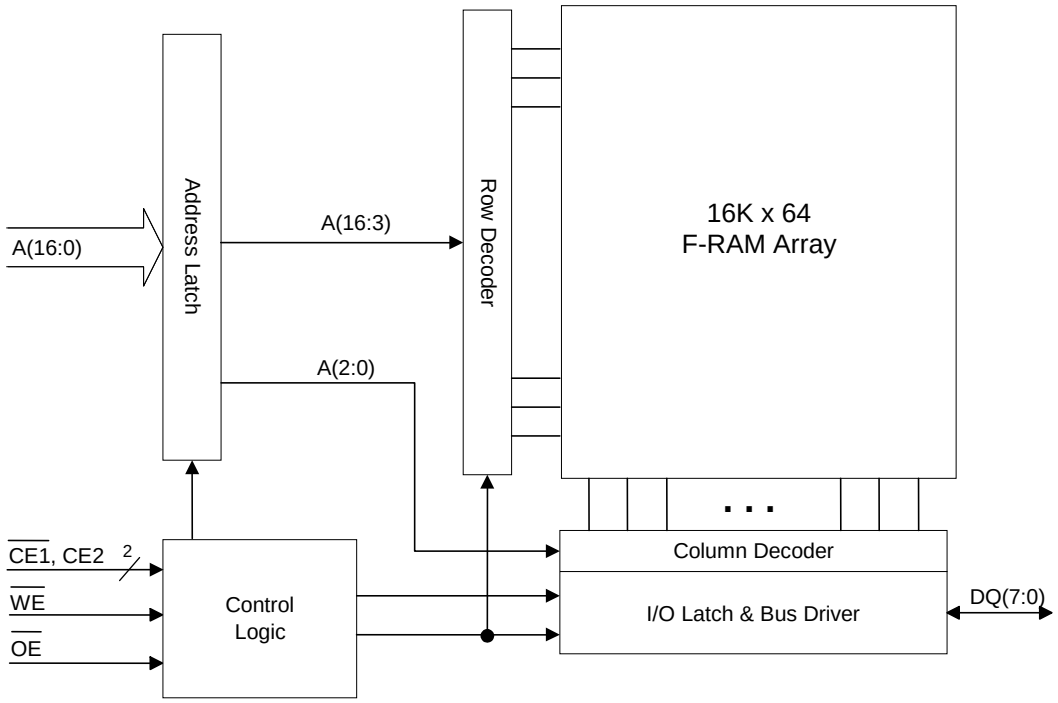


Figure 1. Block Diagram

Pin Descriptions

Pin Name	Type	Pin Description
A(16:0)	Input	Address inputs: The 17 address lines select one of 131,072 bytes in the F-RAM array. The address value is latched on the falling edge of /CE1 (while CE2 high) or the rising edge of CE2 (while /CE1 low). Addresses A(2:0) are used for page mode read and write operations.
/CE1, CE2	Input	Chip Enable inputs: The device is selected and a new memory access begins on the falling edge of /CE1 (while CE2 high) or the rising edge of CE2 (while /CE1 low). The entire address is latched internally at this point. The CE2 pin is pulled up internally.
/WE	Input	Write Enable: A write cycle begins when /WE is asserted. The rising edge causes the FM28V100 to write the data on the DQ bus to the F-RAM array. The falling edge of /WE latches a new column address for fast page mode write cycles.
/OE	Input	Output Enable: When /OE is low, the FM28V100 drives the data bus when valid data is available. Deasserting /OE high tri-states the DQ pins.
DQ(7:0)	I/O	Data: 8-bit bi-directional data bus for accessing the F-RAM array.
NC	-	No Connect: This pin has no internal connection.
VDD	Supply	Supply Voltage
VSS	Supply	Ground

Functional Truth Table [1]

/CE1	CE2	/WE	A(16:3)	A(2:0)	Operation
H X	X L	X X	X X	X X	Standby/Idle
↓ L	H ↑	H H	V V	V V	Read
L	H	H	No Change	Change	Page Mode Read
L	H	H	Change	V	Random Read
↓ L	H ↑	L L	V V	V V	/CE-Controlled Write [2]
L	H	↓	V	V	/WE-Controlled Write [2, 3]
L	H	↓	No Change	V	Page Mode Write [4]
↑ L	H ↓	X X	X X	X X	Starts Precharge

Notes:

1) H=Logic High, L=Logic Low, V=Valid Address, X=Don't Care.
2) For write cycles, data-in is latched on the rising edge of /CE1 or /WE of the falling edge of CE2, whichever comes first.
3) /WE-controlled write cycle begins as a Read cycle and A(16:3) is latched then.
4) Addresses A(2:0) must remain stable for at least 15 ns during page mode operation.

Overview

The FM28V100 is a bytewide F-RAM memory logically organized as 131,072 x 8 and is accessed using an industry standard parallel interface. All data written to the part is immediately nonvolatile with no delay. The device offers page mode operation which provides higher speed access to addresses within a page (row). An access to a different page is triggered by toggling a chip enable pin or simply by changing the upper address A(16:3).

Memory Operation

Users access 131,072 memory locations with 8 data bits each through a parallel interface. The F-RAM array is organized as 16,384 rows and each row has 8 column locations (bytes), which allows fast access in page mode operation. Once an initial address has been latched by the falling edge of /CE1 (while CE2 high) or the rising edge of CE2 (while /CE1 low), subsequent column locations may be accessed without the need to toggle a chip enable. When either chip enable pin is deasserted, a precharge operation begins. Writes occur immediately at the end of the access with no delay. The /WE pin must be toggled for each write operation.

Read Operation

A read operation begins on the falling edge of /CE1 (while CE2 high) or the rising edge of CE2 (while /CE1 low). The /CE-initiated access causes the address to be latched and starts a memory read cycle if /WE is high. Data becomes available on the bus after the access time has been satisfied. Once the address has been latched and the access completed, a new access to a random location (different row) may begin while both chip enables are still active. The minimum cycle time for random addresses is t_{RC}. Note that unlike SRAMs, the FM28V100's /CE-initiated access time is faster than the address cycle time.

The FM28V100 will drive the data bus only when /OE is asserted low and the memory access time has been satisfied. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When /OE is inactive, the data bus will remain hi-Z.

Write Operation

Writes occur in the FM28V100 in the same time interval as reads. The FM28V100 supports both /CE- and /WE-controlled write cycles. In both cases, the address is latched on the falling edge of /CE1 (while CE2 high) or the rising edge of CE2 (while /CE1 low).

In a /CE-controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when the device is activated with a chip enable. In this case, the device begins the memory cycle as a write. The FM28V100 will not drive the data bus regardless of the state of /OE as long as /WE is low. Input data must be valid when the device is deselected with a chip enable. In a /WE-controlled write, the memory cycle begins when the device is activated with a chip enable. The /WE signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if /OE is low, however it will hi-Z once /WE is asserted low. The /CE- and /WE-controlled write timing cases are shown on page 12. In the *Write Cycle Timing 2* diagram, the data bus is shown as a hi-Z condition while the chip is write-enabled and before the required setup time. Although this is drawn to look like a mid-level voltage, it is recommended that all DQ pins comply with the minimum V_{IH}/V_{IL} operating levels.

Write access to the array begins on the falling edge of /WE after the memory cycle is initiated. The write access terminates on the deassertion of /WE, /CE1, or CE2, whichever comes first. A valid write operation requires the user to meet the access time specification prior to deasserting /WE, /CE1, or CE2. Data setup time indicates the interval during which data cannot change prior to the end of the write access.

Unlike other truly nonvolatile memory technologies, there is no write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Page Mode Operation

The FM28V100 provides the user fast access to any data within a row element. Each row has eight column locations (bytes). An access can start anywhere within a row and other column locations may be accessed without the need to toggle the CE pins. For page mode reads, once the first data byte is driven onto the bus, the column address inputs A(2:0) may be changed to a new value. A new data byte is then driven to the DQ pins. For page mode writes, the first write pulse defines the first write access. While the device is selected (both chip enables asserted), a subsequent write pulse along with a new column address provides a page mode write access.

Precharge Operation

The precharge operation is an internal condition in which the state of the memory is prepared for a new access. Precharge is user-initiated by driving at least one of the chip enable signals to an inactive state. The chip enable must remain inactive for at least the minimum precharge time t_{PC}.

Precharge is also activated by changing the upper addess A(16:3). The current row is first closed prior to accessing the new row. The device automatically detects an upper order address change which starts a precharge operation, the new address is latched, and the new read data is valid within the t_{AA} address access time. Refer to the *Read Cycle Timing 1* diagram on page 9. Likewise a similar sequence occurs for write cycles. Refer to the *Write Cycle Timing 3* diagram on page 11. The rate at which random addresses can be issued is t_{RC} and t_{WC}, respectively.

Endurance

The FM28V100 is capable of being accessed at least 10^{14} times – reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis. The F-RAM architecture is based on an array of rows and columns. Rows are defined by A16-A3 and column addresses by A2-A0. The array is organized as 16K rows of 8-bytes each. The entire row is internally accessed once whether a single byte or all eight bytes are read or written. Each byte in the row is counted only once in an endurance calculation.

The user may choose to write CPU instructions and run them from a certain address space. The table below shows endurance calculations for 256-byte repeating loop, which includes a starting address, 7 page mode accesses, and a CE precharge. The number of bus clocks needed to complete an 8-byte transaction is 8+1 at lower bus speeds, but 9+2 at 33MHz due to initial read latency and an extra clock to satisfy the device's precharge timing constraint t_{PC}. The entire loop causes each byte to experience only one endurance cycle. F-RAM read and write endurance is virtually unlimited even at 33MHz system bus clock rate.

Table 1. Time to Reach 100 Trillion Cycles for Repeating 256-byte Loop

Bus Freq (MHz)	Bus Cycle Time (ns)	256-byte Transaction Time (µs)	Endurance Cycles/sec.	Endurance Cycles/year	Years to Reach 10^{14} Cycles
33	30	10.56	94,690	2.98×10^{12}	33.5
25	40	12.8	78,125	2.46×10^{12}	40.6
10	100	28.8	34,720	1.09×10^{12}	91.7
5	200	57.6	17,360	5.47×10^{11}	182.8

SRAM Drop-In Replacement

The FM28V100 has been designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require the CE pins to toggle for each new address. Both CE pins may remain active indefinitely while V_{DD} is applied. When both CE pins are active, the device automatically detects address changes and a new access begins. It also allows page mode operation at speeds up to 33MHz.

A typical application is shown in Figure 3. It shows a pullup resistor on /CE1 which will keep the pin high during power cycles assuming the MCU/MPU pin tri-states during the reset condition. The pullup resistor value should be chosen to ensure the /CE1 pin tracks V_{DD} yet a high enough value that the current drawn when /CE1 is low is not an issue. Although not required, it is recommended that CE2 be tied to V_{DD} if the controller provides an active-low chip enable.

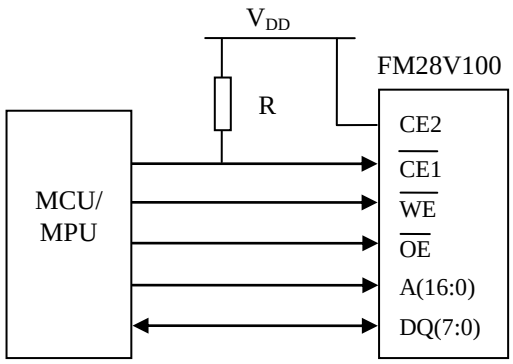


Figure 3. Typical Application using Pullup Resistor on /CE1

For applications that require the lowest power consumption, the CE signals should be active only during memory accesses. Due to the external pullup resistor, some supply current will be drawn while /CE1 is low. When /CE1 is high, the device draws no more than the maximum standby current I_{SB}.

Note that if /CE1 is grounded and CE2 tied to V_{DD}, the user must be sure /WE is not low at powerup or powerdown events. If the chip is enabled and /WE is low during power cycles, data corruption will occur. Figure 4 shows a pullup resistor on /WE which will keep the pin high during power cycles assuming the MCU/MPU pin tri-states during the reset condition. The pullup resistor value should be chosen to ensure the /WE pin tracks V_{DD} yet a high enough value that the current drawn when /WE is low is not an issue. A 10Kohm resistor draws 330uA when /WE is low and V_{DD}=3.3V.

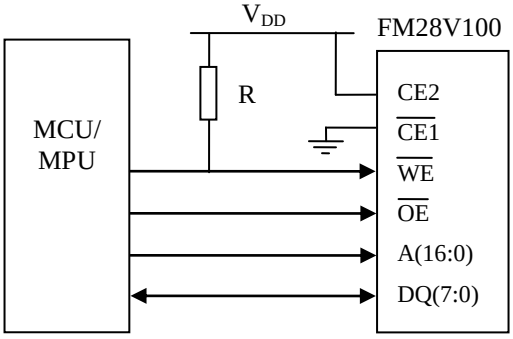


Figure 4. Use of Pullup Resistor on /WE

The FM28V100 is backward compatible with the 1Mbit FM20L08 and 256Kbit FM18L08 devices.

PCB Layout Recommendations

A 0.1uF decoupling capacitor should be placed close to pin 8 (V_{DD}) and the ground side of the capacitor should be connected to either a ground plane or low impedance path back to pin 24 (V_{SS}). It is best to use a chip capacitor that has low ESR and has good high frequency characteristics.

If the controller drives the address and chip enable from the same timing edge, it is best to keep the address routes short and of equal length. A simple RC circuit may be inserted in the chip enable path to provide some delay and timing margin for the FM28V100's address setup time t_{AS}.

As a general rule, the layout designer may need to add series termination resistors to controller outputs that have fast transitions or routes that are > 15cm in length. This is only necessary if the edge rate is less than or equal to the round trip trace delay. Signal overshoot and ringback may be large enough to cause erratic device behavior. It is best to add a 50 ohm resistor (30 – 60 ohms) near the output driver (controller) to reduce such transmission line effects.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +4.5V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +4.5V and $V_{IN} < V_{DD}+1V$
T_{STG}	Storage Temperature	-55°C to +125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	260° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (AEC-Q100-002 Rev. E) - Charged Device Model (AEC-Q100-011 Rev. B) - Machine Model (AEC-Q100-003 Rev. E)	 2kV 1.25kV 200V
	Package Moisture Sensitivity Level	MSL-3

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to +85° C, V_{DD} = 2.0V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply	2.0	3.3	3.6	V	
I_{DD}	V_{DD} Supply Current		7	12	mA	1
I_{SB}	Standby Current – CMOS		90	150	µA	2
I_{LI}	Input Leakage Current			±1	µA	3
I_{LO}	Output Leakage Current			±1	µA	3
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3		0.3 V_{DD}	V	
V_{OH1}	Output High Voltage (I_{OH} = -1 mA, V_{DD}=2.7V)	2.4			V	
V_{OH2}	Output High Voltage (I_{OH} = -100 µA)	V_{DD}-0.2			V	
V_{OL1}	Output Low Voltage (I_{OL} = 2 mA, V_{DD}=2.7V)			0.4	V	
V_{OL2}	Output Low Voltage (I_{OL} = 150 µA)			0.2	V	
R_{IN}	Address Input Resistance (CE2) For V_{IN} = V_{IH} (min) For V_{IN} = V_{IL} (max)	 40 1			 KΩ MΩ	4

Notes

1. V_{DD} = 3.6V, CE cycling at minimum cycle time. All inputs at CMOS levels (0.2V or V_{DD}-0.2V), all DQ pins unloaded.
2. V_{DD} = 3.6V, /CE1 at V_{DD} or CE2 at V_{SS}, and all other pins at CMOS levels (0.2V or V_{DD}-0.2V).
3. V_{IN}, V_{OUT} between V_{DD} and V_{SS}.
4. The input pull-up circuit is stronger (>40KΩ) when the input voltage is above V_{IH} and weak (>1MΩ) when the input voltage is below V_{IL}.

Read Cycle AC Parameters (T_A = -40° C to +85° C, C_L = 30 pF, unless otherwise specified)

Symbol	Parameter	V_{DD} 2.0 to 2.7V		V_{DD} 2.7 to 3.6V		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	105	-	90	-	ns	
t_{CE}	Chip Enable Access Time	-	70	-	60	ns	
t_{AA}	Address Access Time	-	105	-	90	ns	
t_{OH}	Output Hold Time	20	-	20	-	ns	
t_{AAP}	Page Mode Address Access Time	-	40	-	30	ns	
t_{OHP}	Page Mode Output Hold Time	3	-	3	-	ns	
t_{CA}	Chip Enable Active Time	70	-	60	-	ns	
t_{PC}	Precharge Time	35	-	30	-	ns	
t_{AS}	Address Setup Time (to /CE1, CE2 active)	0	-	0	-	ns	
t_{AH}	Address Hold Time (/CE-controlled)	70	-	60	-	ns	
t_{OE}	Output Enable Access Time	-	25	-	15	ns	
t_{HZ}	Chip Enable to Output High-Z	-	10	-	10	ns	1
t_{OHZ}	Output Enable High to Output High-Z	-	10	-	10	ns	1

Write Cycle AC Parameters (T_A = -40° C to +85° C, unless otherwise specified)

Symbol	Parameter	V_{DD} 2.0 to 2.7V		V_{DD} 2.7 to 3.6V		Units	Notes
		Min	Max	Min	Max		
t_{WC}	Write Cycle Time	105	-	90	-	ns	
t_{CA}	Chip Enable Active Time	70	-	60	-	ns	
t_{CW}	Chip Enable to Write Enable High	70	-	60	-	ns	
t_{PC}	Precharge Time	35	-	30	-	ns	
t_{PWC}	Page Mode Write Enable Cycle Time	40	-	30	-	ns	
t_{WP}	Write Enable Pulse Width	22	-	18	-	ns	
t_{AS}	Address Setup Time (to /CE1, CE2 active)	0	-	0	-	ns	
t_{AH}	Address Hold Time (/CE-controlled)	70	-	60	-	ns	
t_{ASP}	Page Mode Address Setup Time (to /WE low)	8	-	5	-	ns	
t_{AHP}	Page Mode Address Hold Time (to /WE low)	20	-	15	-	ns	
t_{WLC}	Write Enable Low to Chip Disabled	30	-	25	-	ns	
t_{WLA}	Write Enable Low to A(16:3) Change	30	-	25	-	ns	
t_{AWH}	A(16:3) Change to Write Enable High	105	-	90	-	ns	
t_{DS}	Data Input Setup Time	20	-	15	-	ns	
t_{DH}	Data Input Hold Time	0	-	0	-	ns	
t_{WZ}	Write Enable Low to Output High Z	-	10	-	10	ns	1
t_{WX}	Write Enable High to Output Driven	5	-	5	-	ns	1
t_{WS}	Write Enable to CE-Active Setup Time	0	-	0	-	ns	1,2
t_{WH}	Write Enable to CE-Inactive Hold Time	0	-	0	-	ns	1,2

Notes

1 This parameter is characterized but not 100% tested.

2 The relationship between CE's and /WE determines if a /CE- or /WE-controlled write occurs.

Power Cycle Timing (T_A = -40° C to +85° C, V_{DD} = 2.0V to 3.6V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{VR}	V_{DD} Rise Time	50	-	µs/V	1
t_{VF}	V_{DD} Fall Time	100	-	µs/V	1
t_{PU}	Power Up (V_{DD} min) to First Access Time	250	-	µs	
t_{PD}	Last Access to Power Down (V_{DD} min)	0	-	µs	

Notes

1 Slope measured at any point on V_{DD} waveform.

Data Retention (T_A = -40°C to + 85°C)

Parameter	Min	Max	Units	Notes
Data Retention	10	-	Years	

Capacitance (T_A = 25° C , f=1 MHz, V_{DD} = 3.3V)

Symbol	Parameter	Min	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (DQ)	-	8	pF	1
C_{IN}	Input Capacitance	-	6	pF	1

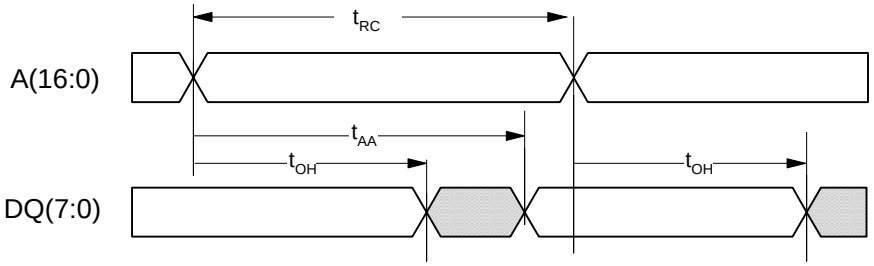
Notes

1. This parameter is characterized and not 100% tested.

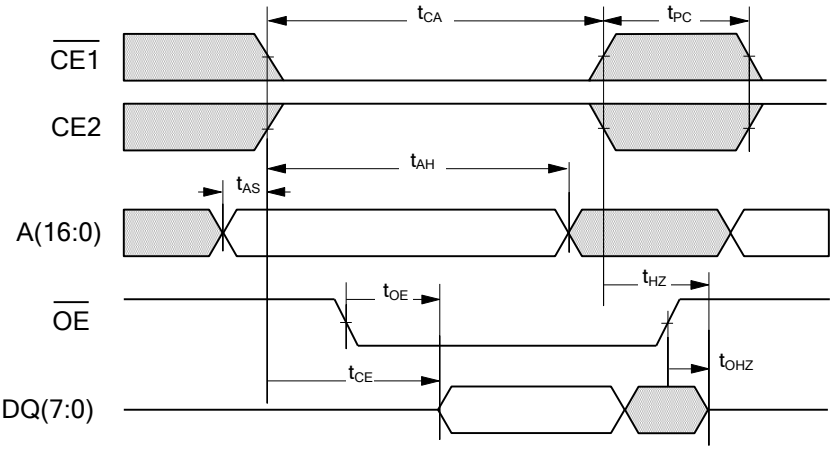
AC Test Conditions

Input Pulse Levels	0 to 3V
Input rise and fall times	3 ns
Input and output timing levels	1.5V
Output Load Capacitance	30 pF

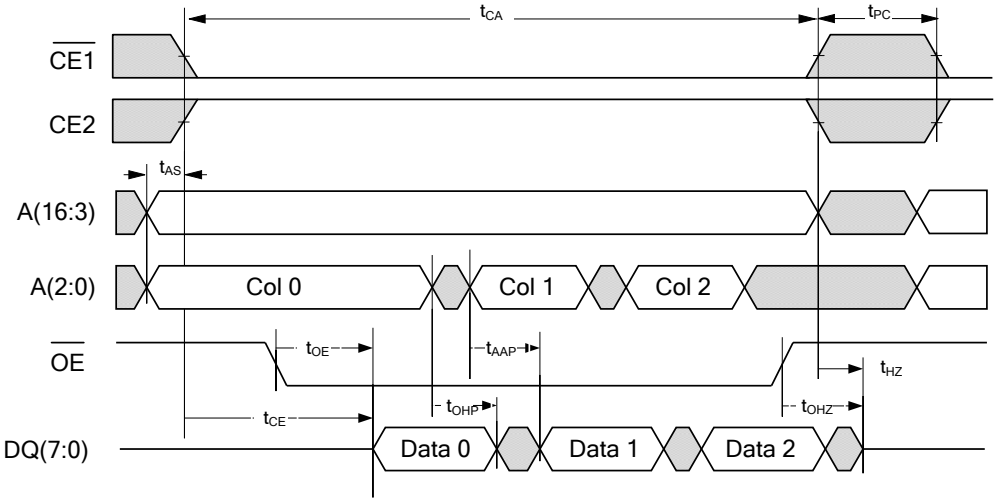
Read Cycle Timing 1 (/CE1 low, CE2 high, /OE low)



Read Cycle Timing 2 (/CE-controlled)

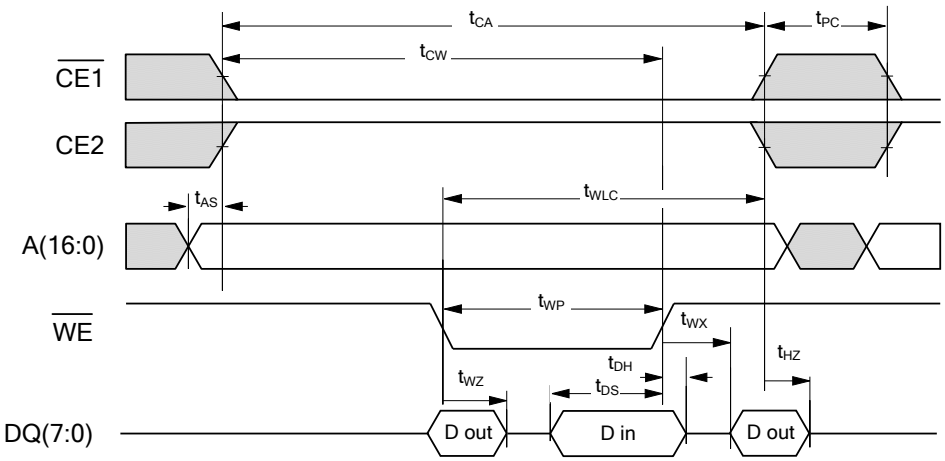


Page Mode Read Cycle Timing

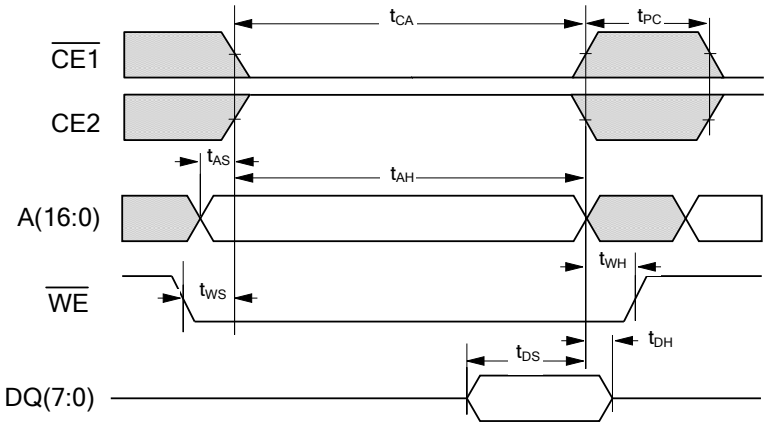


Although sequential column addressing is shown, it is not required.

Write Cycle Timing 1 (/WE-Controlled) Note: /OE is low only to show effect of /WE on DQ pins

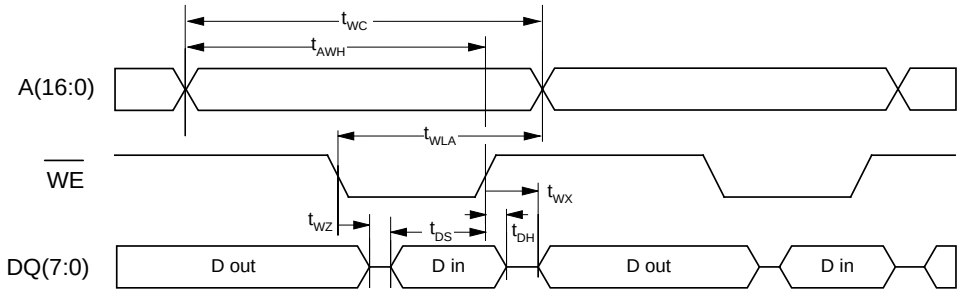


Write Cycle Timing 2 (/CE-Controlled)

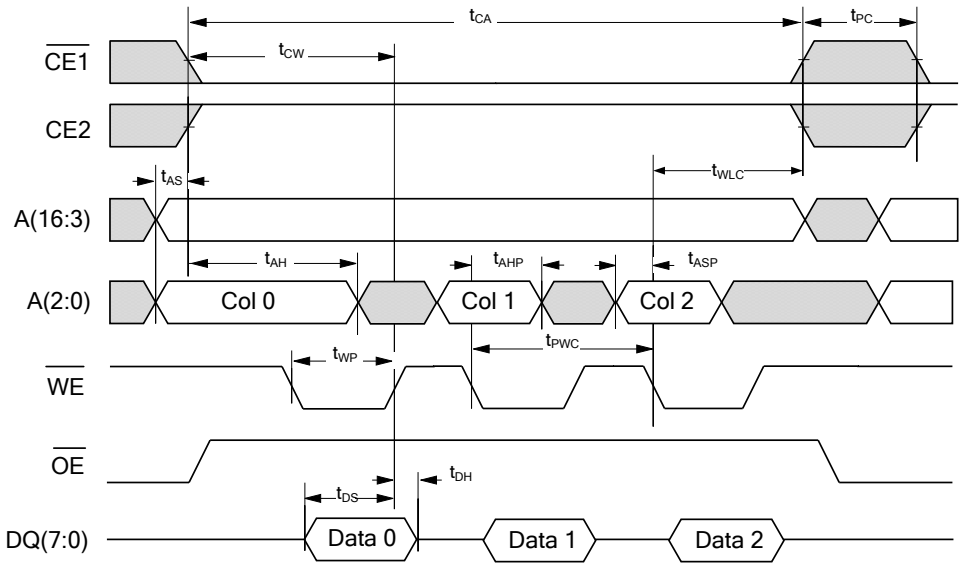


NOTE: See Write Operation section for detailed description (page 4).

Write Cycle Timing 3 (/CE1 low, CE2 high) Note: /OE is low only to show effect of /WE on DQ pins

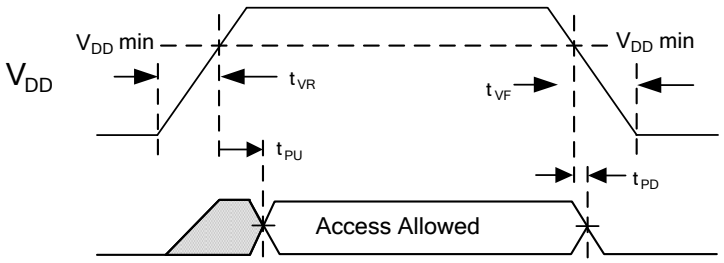


Page Mode Write Cycle Timing



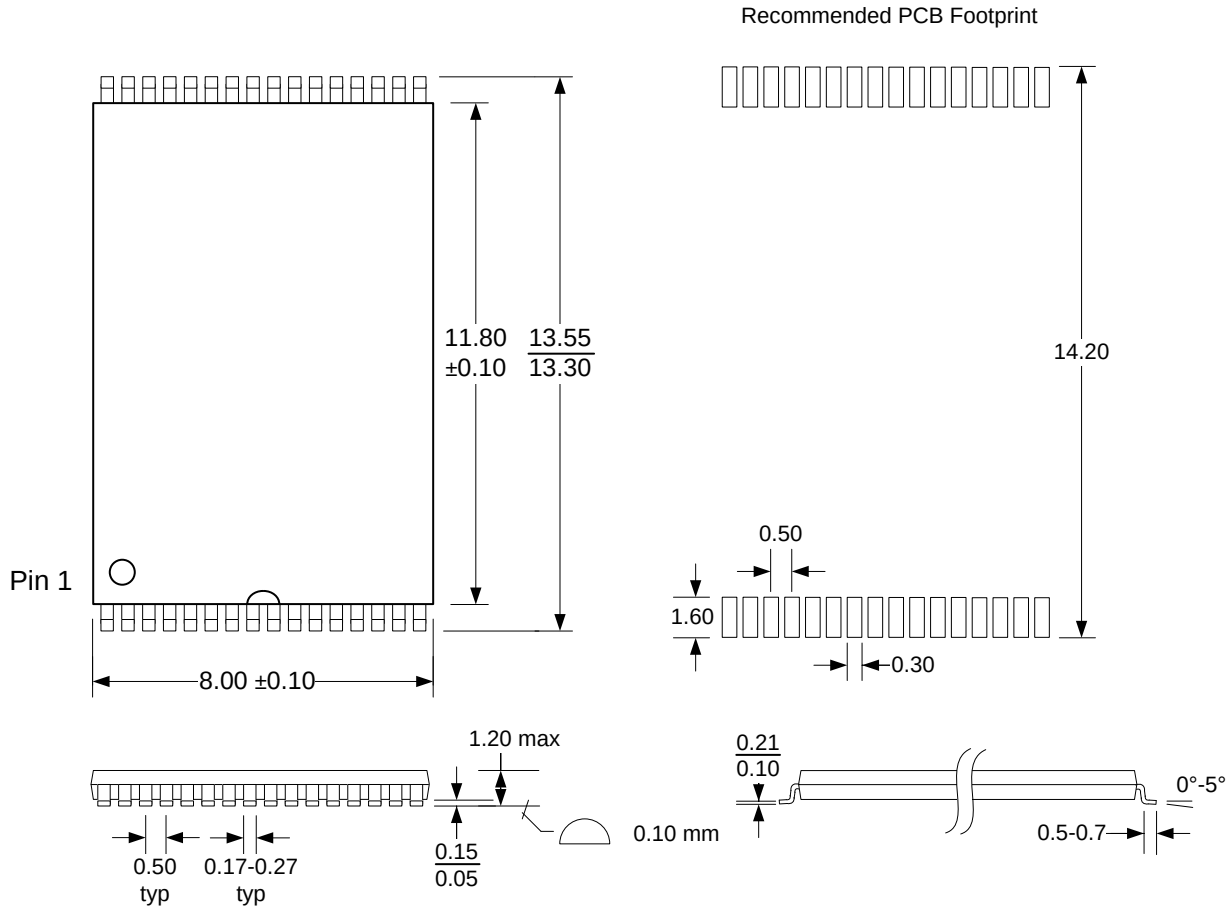
Although sequential column addressing is shown, it is not required.

Power Cycle Timing

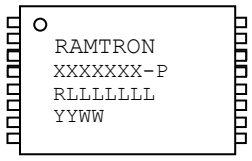


Mechanical Drawing

32-pin Shrunk TSOP-I (8.0 x 13.4 mm)
All dimensions in millimeters



TSOP Package Marking Scheme



Legend:
XXXXXX= part number, P= package/option (T=TSOP "Green")
R=rev code, YY=year, WW=work week, LLLLLLL= lot code

Example: FM28V100, "Green"/RoHS TSOP-I package,
Rev. A, Year 2010, Work Week 18, Lot 9482296

```
RAMTRON
FM28V100-TG
A9482296TG
1018
```

Revision History

Revision	Date	Summary
1.0	10/10/2008	Initial release.
1.1	3/25/2009	Added tape & reel ordering information. Added ESD ratings. Removed software write protect feature.
1.2	5/25/2010	Changed MSL package rating. Expanded explanation of precharge operation. Updated lead temperature rating in Abs Max table. Changed package marking scheme.
3.0	4/24/2012	Changed to Production status.

Document History

Document Title: FM28V100 1Mbit (128Kx8) Bytewide F-RAM Memory
Document Number: 001-86202

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3912933	GVCH	02/25/2013	New Spec

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