電子系統層級設計與驗證

Homework 4

Power Measurement

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日期：114/05/27

（一）實驗結果

(1) Without clock gating technique/latches/AND gates

Area：

```
****************************************
Report : area
Design : GCD
Version: U-2022.12
Date   : Tue May 27 09:09:40 2025
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /cad/CBDK/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)

Number of ports:                          269
Number of nets:                           427
Number of cells:                          174
Number of combinational cells:            134
Number of sequential cells:                27
Number of macros/black boxes:               0
Number of buf/inv:                         34
Number of references:                       2

Combinational area:               644.918412
Buf/Inv area:                      75.499202
Noncombinational area:            419.126401
Macro/Black Box area:               0.000000
Net Interconnect area:          21840.108582

Total cell area:                 1064.044813
Total area:                     22904.153395
1
```

Power：

```
****************************************
Report : Averaged Power
  -hierarchy
Design : GCD
Version: U-2022.12
Date   : Tue May 27 09:11:31 2025
****************************************


                                    Int      Switch   Leak     Total
Hierarchy                           Power    Power    Power    Power    %
-------------------------------------------------------------------------------
GCD                                 1.90e-05 2.26e-05 3.83e-06 4.55e-05 100.0
  Datapath (Datapath)               1.60e-05 1.51e-05 3.46e-06 3.46e-05  76.0
    B (Register_2)                  4.38e-06 1.87e-06 5.24e-07 6.77e-06  14.9
    FU1 (Sub)                       7.75e-07 1.13e-06 7.72e-07 2.68e-06   5.9
      sub_336 (Sub_DW01_sub_0)      7.75e-07 1.13e-06 7.72e-07 2.68e-06   5.9
    R (Register_1)                  4.17e-06 1.24e-06 5.20e-07 5.93e-06  13.0
    M1 (MUX3)                       5.16e-07 2.55e-06 3.44e-07 3.41e-06   7.5
    FU2 (Compare)                   4.71e-07 1.94e-06 3.67e-07 2.77e-06   6.1
    M2 (MUX2_0)                     1.85e-07 5.80e-07 1.98e-07 9.64e-07   2.1
    M3 (MUX2_1)                     2.15e-07 1.23e-06 2.15e-07 1.66e-06   3.7
    A (Register_0)                  5.29e-06 4.55e-06 5.23e-07 1.04e-05  22.8
  Controller (Controller)           3.05e-06 7.51e-06 3.67e-07 1.09e-05  24.0
1
```

Simulation time :

```
i =          x, time =             411000, A =  15, B =   9, Outport =   3
$finish called from file "GCD_tb_gate.v", line 59.
$finish at simulation time              410904
         V C S   S i m u l a t i o n   R e p o r t
Time: 410904 ps
CPU Time:      0.280 seconds;       Data structure size:   0.3Mb
Tue May 27 09:11:12 2025
CPU time: 2.975 seconds to compile + .258 seconds to elab + .511 seconds to link + .320 seconds in simulation
```

(2) With clock gating technique

Area：

```
****************************************
Report : area
Design : GCD
Version: U-2022.12
Date   : Tue May 27 09:17:35 2025
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /cad/CBDK/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)

Number of ports:                          278
Number of nets:                           412
Number of cells:                          153
Number of combinational cells:            107
Number of sequential cells:                30
Number of macros/black boxes:               0
Number of buf/inv:                         28
Number of references:                       2

Combinational area:               505.209608
Buf/Inv area:                      60.681602
Noncombinational area:            448.761600
Macro/Black Box area:               0.000000
Net Interconnect area:          17640.087982

Total cell area:                  953.971208
Total area:                     18594.059191
1
```

Power :

```
****************************************
Report : Averaged Power
  -hierarchy
Design : GCD
Version: U-2022.12
Date   : Tue May 27 09:19:09 2025
****************************************


                                        Int      Switch   Leak     Total
Hierarchy                               Power    Power    Power    Power    %
-----------------------------------------------------------------------------
GCD                                     1.03e-05 1.89e-05 3.43e-06 3.26e-05 100.0
  Datapath (Datapath)                   7.22e-06 1.14e-05 3.06e-06 2.17e-05  66.5
    B (Register_2)                      1.26e-06 9.95e-07 3.85e-07 2.64e-06   8.1
      clk_gate_Q_reg (SNPS_CLOCK_GATE_HIGH_Register_2)
                                        4.23e-07 6.40e-07 6.79e-08 1.13e-06   3.5
    FU1 (Sub)                           7.75e-07 1.13e-06 7.72e-07 2.68e-06   8.2
      sub_336 (Sub_DW01_sub_0)          7.75e-07 1.13e-06 7.72e-07 2.68e-06   8.2
    R (Register_1)                      1.11e-06 6.08e-07 3.81e-07 2.09e-06   6.4
      clk_gate_Q_reg (SNPS_CLOCK_GATE_HIGH_Register_1)
                                        4.00e-07 5.41e-07 6.76e-08 1.01e-06   3.1
    M1 (MUX3)                           5.35e-07 2.61e-06 3.44e-07 3.49e-06  10.7
    FU2 (Compare)                       4.71e-07 1.94e-06 3.68e-07 2.77e-06   8.5
    M2 (MUX2_0)                         1.85e-07 5.72e-07 1.98e-07 9.55e-07   2.9
    M3 (MUX2_1)                         2.15e-07 1.23e-06 2.15e-07 1.66e-06   5.1
    A (Register_0)                      2.67e-06 2.33e-06 4.00e-07 5.40e-06  16.5
      clk_gate_Q_reg (SNPS_CLOCK_GATE_HIGH_Register_0)
                                        6.07e-07 1.44e-06 7.06e-08 2.11e-06   6.5
  Controller (Controller)               3.05e-06 7.53e-06 3.67e-07 1.09e-05  33.5
1
```

Simulation time :

```
i =          x, time =             411000, A =  15, B =   9, Outport =   3
$finish called from file "GCD_tb_gate.v", line 59.
$finish at simulation time              410904
          V C S   S i m u l a t i o n   R e p o r t
Time: 410904 ps
CPU Time:      0.290 seconds;       Data structure size:   0.3Mb
Tue May 27 09:18:40 2025
CPU time: 2.970 seconds to compile + .256 seconds to elab + .504 seconds to link + .329 seconds in simulation
```

(3) With latches

Area：

```
****************************************
Report : area
Design : GCD
Version: U-2022.12
Date   : Tue May 27 09:56:28 2025
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /cad/CBDK/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)

Number of ports:                          305
Number of nets:                           480
Number of cells:                          193
Number of combinational cells:            135
Number of sequential cells:                43
Number of macros/black boxes:               0
Number of buf/inv:                         33
Number of references:                       2

Combinational area:               649.857613
Buf/Inv area:                      76.204802
Noncombinational area:            565.891202
Macro/Black Box area:               0.000000
Net Interconnect area:          23426.783081

Total cell area:                 1215.748815
Total area:                     24642.531896
1
```

Power：

```
****************************************
Report : Averaged Power
  -hierarchy
Design : GCD
Version: U-2022.12
Date   : Tue May 27 10:00:54 2025
****************************************


                                        Int      Switch   Leak     Total
Hierarchy                               Power    Power    Power    Power    %
-----------------------------------------------------------------------------
GCD                                     2.13e-05 2.64e-05 4.35e-06 5.20e-05 100.0
  Datapath (Datapath)                   1.78e-05 1.59e-05 3.93e-06 3.77e-05  72.4
    B (Register_2)                      4.37e-06 1.86e-06 5.24e-07 6.76e-06  13.0
    D1 (D_latch_0)                      7.53e-07 2.24e-07 2.30e-07 1.21e-06   2.3
    D2 (D_latch_1)                      6.69e-07 7.28e-08 2.31e-07 9.73e-07   1.9
    FU1 (Sub)                           6.69e-07 1.05e-06 7.87e-07 2.51e-06   4.8
      sub_373 (Sub_DW01_sub_0)          6.69e-07 1.05e-06 7.87e-07 2.51e-06   4.8
    R (Register_1)                      4.17e-06 1.24e-06 5.20e-07 5.93e-06  11.4
    M1 (MUX3)                           6.04e-07 2.94e-06 3.37e-07 3.88e-06   7.5
    FU2 (Compare)                       4.71e-07 1.93e-06 3.68e-07 2.77e-06   5.3
    M2 (MUX2_0)                         1.85e-07 5.80e-07 1.98e-07 9.64e-07   1.9
    M3 (MUX2_1)                         2.15e-07 1.23e-06 2.15e-07 1.66e-06   3.2
    A (Register_0)                      5.72e-06 4.76e-06 5.24e-07 1.10e-05  21.2
  Controller (Controller)               3.45e-06 1.05e-05 4.18e-07 1.43e-05  27.6
1
```

Simulation time :

```
i =          x, time =             411000, A =  15, B =   9, Outport =   3
$finish called from file "GCD_tb_gate.v", line 59.
$finish at simulation time              410948
          V C S   S i m u l a t i o n   R e p o r t
Time: 410948 ps
CPU Time:      0.260 seconds;       Data structure size:   0.3Mb
Tue May 27 09:56:50 2025
CPU time: 3.105 seconds to compile + .252 seconds to elab + .473 seconds to link + .293 seconds in simulation
```

(4) With AND gates

Area：

```
****************************************
Report : area
Design : GCD
Version: U-2022.12
Date   : Tue May 27 10:18:59 2025
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    slow (File: /cad/CBDK/CBDK_TSMC90GUTM_Arm_f1.0/CIC/SynopsysDC/db/slow.db)

Number of ports:                          271
Number of nets:                           446
Number of cells:                          191
Number of combinational cells:            151
Number of sequential cells:                27
Number of macros/black boxes:               0
Number of buf/inv:                         33
Number of references:                       2

Combinational area:               704.894415
Buf/Inv area:                      74.793602
Noncombinational area:            419.126401
Macro/Black Box area:               0.000000
Net Interconnect area:          23426.783081

Total cell area:                 1124.020816
Total area:                     24550.803897
1
```

Power：

```
****************************************
Report : Averaged Power
  -hierarchy
Design : GCD
Version: U-2022.12
Date   : Tue May 27 10:19:58 2025
****************************************


                                        Int      Switch   Leak     Total
Hierarchy                               Power    Power    Power    Power    %
------------------------------------------------------------------------------
GCD                                     2.05e-05 2.77e-05 4.11e-06 5.23e-05 100.0
  Datapath (Datapath)                   1.72e-05 1.94e-05 3.74e-06 4.03e-05  77.1
    M3 (MUX2_1)                         2.15e-07 1.23e-06 2.15e-07 1.66e-06   3.2
    FU1 (Sub)                           1.46e-06 2.17e-06 7.41e-07 4.37e-06   8.4
      sub_351 (Sub_DW01_sub_0)          1.46e-06 2.17e-06 7.41e-07 4.37e-06   8.4
    FU2 (Compare)                       4.71e-07 1.93e-06 3.68e-07 2.77e-06   5.3
    R (Register_1)                      4.17e-06 1.24e-06 5.20e-07 5.93e-06  11.3
    A (Register_0)                      5.20e-06 4.43e-06 5.21e-07 1.01e-05  19.4
    B (Register_2)                      4.37e-06 1.86e-06 5.24e-07 6.76e-06  12.9
    M1 (MUX3)                           6.17e-07 2.98e-06 3.65e-07 3.96e-06   7.6
    M2 (MUX2_0)                         1.85e-07 5.80e-07 1.98e-07 9.64e-07   1.8
  Controller (Controller)               3.25e-06 8.35e-06 3.69e-07 1.20e-05  22.9
1
```

Simulation time :

```
i =          x, time =             411000, A =  15, B =   9, Outport =   3
$finish called from file "GCD_tb_gate.v", line 59.
$finish at simulation time              410948
           V C S   S i m u l a t i o n   R e p o r t
Time: 410948 ps
CPU Time:      0.260 seconds;       Data structure size:   0.3Mb
Tue May 27 10:19:25 2025
CPU time: 3.595 seconds to compile + .221 seconds to elab + .403 seconds to link + .295 seconds in simulation
```

結果比較：

GCD	Area of GCD circuit	Average Power of GCD circuit	Average Power of registers	Energy of GCD circuit
Without clock gating technique/latches/AND gates	1064.044813	4.55e-05	2.31e-05	1.870050e-11
With clock gating technique	953.971208	3.26e-05	1.013e-05	1.339860e-11
With latches	1215.748815	5.20e-05	2.369e-05	2.137200 e-11
With AND gates	1124.020816	5.23e-05	2.279e-05	2.149530e-11

(二)實驗心得

上星期在課堂中老師教我們一些功率的重要觀念，例如功率多寡對電路的影響，以及如何降低功率的方法，而 clock gating 是一個很實用的辦法，它可以大幅減少使用 MUX 的數量,進而減少面積和功率,從實驗結果可以一窺究竟。Latches 和 AND gates 的方式，它們都是讓 FU 需要運算時才讓 value 進來，觀念上是要減少數值變動而產生的 dynamic power，但是從 GCD power 結果看到居然不減反增,造成反效果,這通常可能是因為在電路中加入額外的 cell 本來就要付出 cost,理所當然的增加面積和功率，而當增加的功率大於這個 component 本身設計帶來

功率減小的幅度時，這項設計其實可以考慮剔除。但縱使在 GCD 電路中 Latches 和 AND gates 不能帶來成效，但是說不定在其他電路它可以使得功率變小，所以這次練習的機會讓我知道要如何設計一些基本的低功率電路。