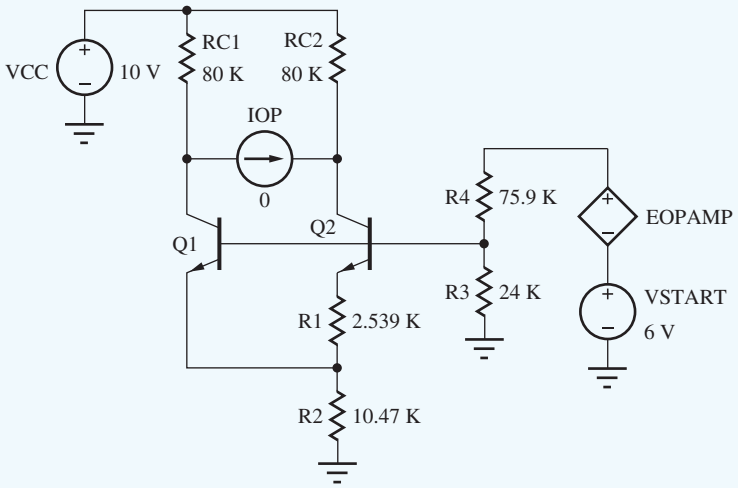
appears across zero-value current source IOP. The gain is set to 10^6. Source VSTART may be needed in some versions of SPICE to help the circuit start up. Another help is to sweep VCC from 0 to 10 V. (Remember that $V_O = 0$ is a valid operating point.) SPICE simulation produces $V_{BG} = 1.204$ V and $V_{\text{PTAT}} = 63.52$ mV and $V_O = 5.01$ V. With BF = 100 and VAF = 75 V, the values are $V_{BG} = 1.201$ V, $V_{\text{PTAT}} = 63.52$ mV and $V_O = 5.03$ V.



EXERCISE: Redesign the reference in Ex. 16.6 using $A_{E2} = 20A_{E1}$.

ANSWER: 3.30 kΩ, 10.5 kΩ, 24.0 kΩ, 75.9 kΩ, 80 kΩ

16.7 THE CURRENT MIRROR AS AN ACTIVE LOAD

We encountered use of transistors as replacements for the load resistors in amplifiers in Chapters 14 and 15. In this section, we find that one of the most important applications of the current mirror[4] is as a replacement for the load resistors of differential amplifier stages in IC operational amplifiers. This elegant application of the current mirror can greatly improve amplifier voltage gain while maintaining the operating-point balance necessary for good common-mode rejection and low offset voltage. When used in this manner, the current mirror is referred to as an **active load** because the passive load resistors have been replaced with active transistor circuit elements.

16.7.1 CMOS DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

Figure 16.31 shows a CMOS differential amplifier with an active load; the load resistors have been replaced by a PMOS current mirror. Let us first study the quiescent operating point of this circuit and then look at its small-signal characteristics.

dc Analysis

Assume for the moment that the amplifier is voltage balanced (in fact, it will turn out that it *is* balanced). Then, bias current I_{SS} divides equally between transistors M_1 and M_2, and I_{D1} and I_{D2} are each equal to $I_{SS}/2$. Current I_{D3} must equal I_{D1} and is mirrored as I_{D4} at the output of the PMOS

[4] In addition to its role as a current source.

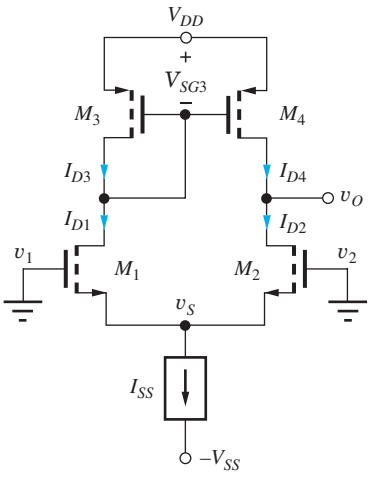


Figure 16.31 CMOS differential amplifier with PMOS active load.

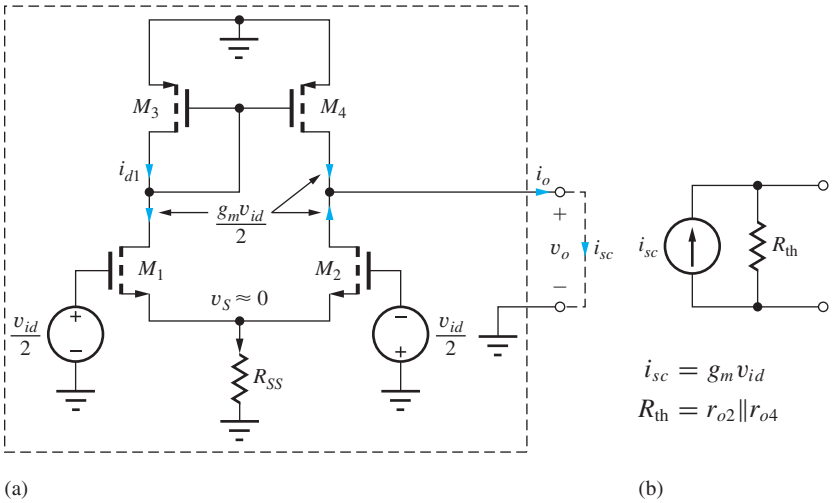


Figure 16.32 (a) CMOS differential amplifier with differential-mode input. (b) The circuit is a one port and can be represented by its Norton equivalent circuit.

current mirror. Thus, I_{D3} and I_{D4} are also equal to $I_{SS}/2$, and the current in the drain of M_4 is exactly the current required to satisfy M_2.

The mirror ratio set by M_3 and M_4 is precisely unity when $V_{SD4} = V_{SD3}$ and hence $V_{DS1} = V_{DS2}$. Thus, the differential amplifier is completely balanced at dc when the quiescent output voltage is

$$V_O = V_{DD} - V_{SD4} = V_{DD} - V_{SG3} = V_{DD} - \left(\sqrt{\frac{I_{SS}}{K_p}} - V_{TP}\right) \tag{16.57}$$

Q-Points

The drain-source voltages of M_1 and M_2 are

$$V_{DS1} = V_O - V_S = V_{DD} - \left(\sqrt{\frac{I_{SS}}{K_p}} - V_{TP}\right) + \left(V_{TN} + \sqrt{\frac{I_{SS}}{K_n}}\right)$$

or

$$V_{DS1} = V_{DD} + V_{TN} + V_{TP} + \sqrt{\frac{I_{SS}}{K_n}} - \sqrt{\frac{I_{SS}}{K_p}} \cong V_{DD} \tag{16.58}$$

and those of M_3 and M_4 are

$$V_{SD3} = V_{SG3} = \sqrt{\frac{I_{SS}}{K_p}} - V_{TP} \tag{16.59}$$

(Remember that $V_{TP} < 0$ for p-channel enhancement-mode devices.)

The drain currents of all the transistors are equal:

$$I_{DS1} = I_{DS2} = I_{SD3} = I_{SD4} = \frac{I_{SS}}{2} \tag{16.60}$$

Small-Signal Analysis

Now that we have found the operating points of the transistors, we can proceed to analyze the small-signal characteristics of the amplifier, including differential-mode gain, differential-mode input and output resistances, common-mode gain, CMRR, and common-mode input and output resistances.

Differential-Mode Signal Analysis

Analysis of the ac behavior of the differential amplifier begins with the differential-mode input applied in the ac circuit model in Fig. 16.32. Upon studying the circuit in Fig. 16.32, we realize that

it is a two-terminal network and can be represented by its Norton equivalent circuit consisting of the short-circuit output current and Thévenin equivalent output resistance. With the output terminals short circuited, the NMOS differential pair produces equal and opposite currents with amplitude $g_{m2}v_{id}/2$ at the drains of M_1 and M_2. Drain current i_{d1} is supplied through current mirror transistor M_3 and is replicated at the output of M_4. Thus, the total short-circuit output current is

$$\mathbf{i_o} = 2\frac{g_{m2}\mathbf{v_{id}}}{2} = g_{m2}\mathbf{v_{id}} \tag{16.61}$$

The current mirror provides a single-ended output but with a transconductance equal to the full value of the C-S amplifier!

The Thévenin equivalent output resistance will be found using the circuit in Fig. 16.33 in which the internal output resistances of M_2 and M_4 are shown next to their respective transistors. In the next sub section, we will show that R_{th} is equal to the parallel combination of r_{o2} and r_{o4}:

$$R_{\text{th}} = r_{o2} \| r_{o4} \tag{16.62}$$

The differential-mode voltage gain of the open-circuited differential amplifier is simply the product of i_{sc} and R_{th}:

$$A_{dm} = g_{m2}(r_{o2} \| r_{o4}) = \frac{\mu_{f2}}{1 + \dfrac{r_{o2}}{r_{o4}}} \cong \frac{\mu_{f2}}{2} \tag{16.63}$$

Equation (16.63) indicates that the gain of the input stage of the amplifier approaches one half the intrinsic gain of the transistors forming the differential pair. We are now within a factor of 2 of the theoretical voltage gain limit for the individual transistors!

Output Resistance of the Differential Amplifier

The origin of the output resistance expression in Eq. (16.63) can be thought of conceptually in the following (although technically incorrect) manner. At node 1 in Fig. 16.33, r_{o4} is connected directly to ac ground at the positive power supply, whereas r_{o2} appears connected to virtual ground at the sources of M_2 and M_1. Thus, r_{o2} and r_{o4} are effectively in parallel. Although this argument gives the correct answer, it is not precisely correct. Because the differential amplifier with active load no longer represents a symmetric circuit relative to the test signal applied to the output, the node at the sources of M_1 and M_2 *is not* truly a virtual ground.

Exact Analysis

A more precise analysis can be obtained from the circuit in Fig. 16.34. The output resistance r_{o4} of M_4 is indeed connected directly to ac ground and represents one component of the output resistance.

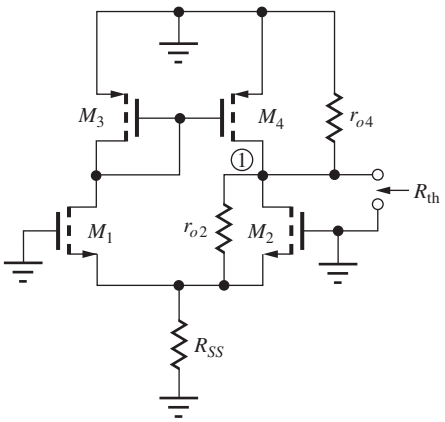


Figure 16.33 Simple CMOS op amp with active load in the first stage.

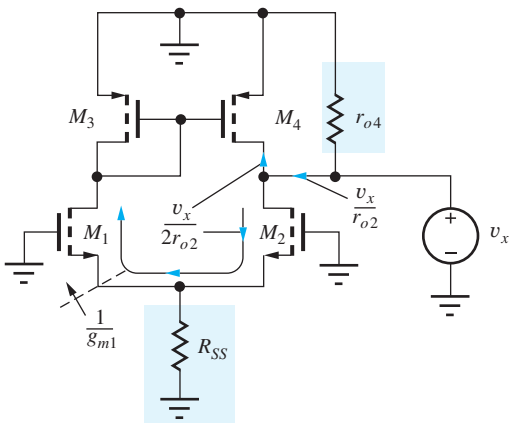


Figure 16.34 Output resistance component due to r_{o2}.

However, the current from v_x due to r_{o2} is more complicated. The actual behavior can be determined from Fig. 16.34, in which R_{SS} is assumed to be negligible with respect to $1/g_{m1}$ ($R_{SS} \gg 1/g_{m1}$).

Transistor M_2 is operating as a common-source transistor with an effective resistance in its source of $R_S = 1/g_{m1}$. Based on the results in Table 14.3, the resistance looking into the drain of M_2 is

$$R_{o2} = r_{o2}(1 + g_{m2}R_S) = r_{o2}\left(1 + g_{m2}\frac{1}{g_{m1}}\right) = 2r_{o2} \tag{16.64}$$

Therefore, the drain current of M_2 is equal to $v_x/2r_{o2}$. However, the current goes around the differential pair and into the current mirror at M_3. The current is replicated by the mirror to become the drain current of M_4. The total current from source v_x becomes $2(v_x/2r_{o2}) = v_x/r_{o2}$.

Combining this current with the current through r_{o4} yields a total current of

$$\mathbf{i}_\mathbf{x}^\mathbf{T} = \frac{\mathbf{v_x}}{r_{o2}} + \frac{\mathbf{v_x}}{r_{o4}} \qquad \text{and} \qquad R_{od} = r_{o2} \| r_{o4} \tag{16.65}$$

The equivalent resistance at the output node is, in fact, exactly equal to the parallel combination of the output resistances of M_2 and M_4.

EXERCISE: Find the Q-points of the transistors in Fig. 16.31 if $I_{SS} = 250\ \mu A$, $K_n = 250\ \mu A/V^2$, $K_p = 200\ \mu A/V^2$, $V_{TN} = -V_{TP} = 0.75$ V, and $V_{DD} = V_{SS} = 5$ V. What are the transconductance, output resistance, and voltage gain of the amplifier if $\lambda = 0.0133\ V^{-1}$?

ANSWERS: (125 μA, 4.88 V), (125 μA, 1.87 V); 250 μS, 314 kΩ, 78.5

Common-Mode Input Signals

Figure 16.35 is the CMOS differential amplifier with a common-mode input signal. The common-mode input voltage causes a common-mode current i_{oc} in both sides of the differential pair consisting of M_1 and M_2. The common-mode current (i_{oc}) in M_1 is mirrored at the output of M_4 with a small error since no current can appear in r_{o4} with the output shorted. In addition, the small voltage difference developed between the drains of M_1 and M_2 causes a current in the differential output resistance ($2r_{o2}$) of the pair that is then doubled by the action of the current mirror.

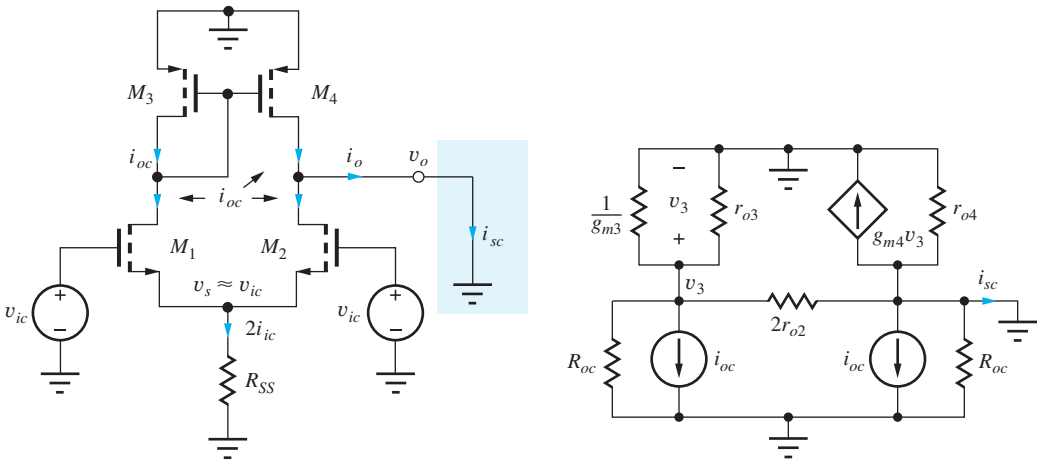


Figure 16.35 (a) CMOS differential amplifier with common-mode input. (b) Small-signal model.

An expression for the short-circuit output current can be found using the small-signal model for the circuit in Fig. 16.35(b). The differential pair with common-mode input is represented by the model from Sec. 15.1.15 with

$$\mathbf{i_{oc}} \cong \frac{\mathbf{v_{ic}}}{2R_{SS}} \qquad R_{od} = 2r_{o2} \qquad R_{oc} = 2\mu_f R_{SS} \tag{16.66}$$

With the output short circuited, we have a one-node problem. Solving for v_3,

$$\mathbf{v_3} = \frac{-\mathbf{i_{oc}}}{g_{m3} + g_{o3} + \dfrac{g_{o2}}{2} + G_{oc}} \qquad \text{and} \qquad \mathbf{i_{sc}} = -\left(\mathbf{i_{oc}} + g_{m4}\mathbf{v_3} - \frac{g_{o2}}{2}\mathbf{v_3}\right) \tag{16.67}$$

which together with Eq. (16.66) yields

$$\mathbf{i_{sc}} = -\frac{g_{o3} + g_{o2}}{g_{m3} + g_{o3} + \dfrac{g_{o2}}{2} + G_{oc}}\mathbf{i_{oc}} \cong -\frac{1 + \dfrac{r_{o3}}{r_{o2}}}{\mu_{f3}}\left(\frac{\mathbf{v_{ic}}}{2R_{SS}}\right) \tag{16.68}$$

where it is assumed that $g_{m4} = g_{m3}$ and $G_{oc} \ll g_{o3}$. The Thévenin equivalent output resistance is exactly the same as found in the previous section, $R_{\text{th}} = r_{o2} \| r_{o4}$. Thus, the common-mode gain is

$$A_{cm} = \frac{\mathbf{i_{sc}} R_{\text{th}}}{\mathbf{v_{ic}}} = -\frac{\left(1 + \dfrac{r_{o3}}{r_{o2}}\right)}{2\mu_{f3}R_{SS}}(r_{o2} \| r_{o4}) \tag{16.69}$$

where $\mu_{f3} \gg 1$ has been assumed. The common-mode rejection ratio is

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| = \frac{2\mu_{f3}g_{m2}R_{SS}}{\left(1 + \dfrac{r_{o3}}{r_{o2}}\right)} \cong \mu_{f3}g_{m2}R_{SS} \quad \text{for} \quad r_{o3} \cong r_{o2} \tag{16.70}$$

which is improved by a factor of approximately μ_{f3} over that of the pair with a resistor load!

EXERCISE: Evaluate Eq. (16.70) for $K_p = K_n = 5$ mA/V^2, $\lambda = 0.0167$ V^{-1}, $I_{SS} = 200$ μA, and $R_{SS} = 10$ MΩ.

ANSWER: 6.00×10^6 or 136 dB

In the last exercise, we find that the CMRR predicted by Eq. (16.70) is quite large, whereas typical op amp specs are 80 to 100 dB. We need to look deeper. In reality, this predicted level will not be achieved, but will be limited by mismatches between the devices in the circuit.

Mismatch Contributions to CMRR

In this section, we explore the techniques used to calculate the effects of device mismatches on CMRR. Figure 16.36 presents the small-signal model for the differential amplifier with mismatches in transistors M_1 and M_2 in which we assume

$$g_{m1} = g_m + \frac{\Delta g_m}{2} \qquad g_{m2} = g_m - \frac{\Delta g_m}{2} \qquad g_{o1} = g_o + \frac{\Delta g_o}{2} \qquad g_{o2} = g_o - \frac{\Delta g_o}{2} \tag{16.71}$$

In this analysis, M_3 and M_4 are still identical. We desire to find the short-circuit output current $i_{sc} = (i_{d1} - i_{d2})$ in which i_{d1} is replicated by the current mirror. Let us use our knowledge of the gross behavior of the circuit to simplify the analysis. We have $v_{d2} = 0$, since we are finding the short-circuit output current, and based on previous common-mode analyses, we expect the signal at v_{d1} to be small. So let us assume that $v_{d1} \cong 0$. With this assumption, and noting that the two gate-source voltages are identical,

$$\mathbf{i_{sc}} = \mathbf{i_{d1}} - \mathbf{i_{d2}} = (g_{m1} - g_{m2})\mathbf{v_{gs}} - (g_{o1} - g_{o2})\mathbf{v_s} = \Delta g_m \mathbf{v_{gs}} - \Delta g_o \mathbf{v_s} \tag{16.72}$$

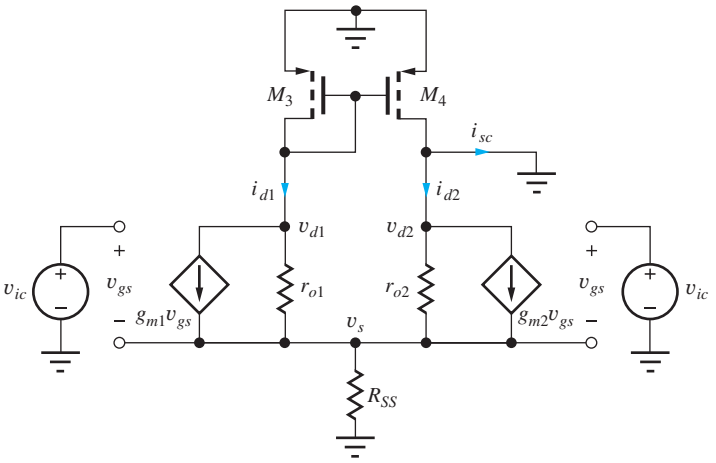


Figure 16.36 CMOS differential amplifier in which M_1 and M_2 are no longer matched.

To evaluate this expression, we need to find source voltage v_s and gate-source voltage v_{gs}. Writing a nodal equation for v_s with $v_{gs} = v_{ic} - v_s$, $v_{d1} = 0$ and $v_{d2} = 0$, yields

$$\left(g_m + \frac{\Delta g_m}{2} + g_m - \frac{\Delta g_m}{2}\right)(\mathbf{v_{ic}} - \mathbf{v_s}) = \left(g_o + \frac{\Delta g_o}{2} + g_o - \frac{\Delta g_o}{2} + G_{SS}\right)\mathbf{v_s}$$

in which we may be surprised to see all the mismatch terms cancel out! Thus, for common-mode inputs, v_s and v_{gs} are not affected by the transistor mismatches:[5]

$$\mathbf{v_s} \cong \frac{2g_m R_{SS}}{1 + 2g_m R_{SS}}\mathbf{v_{ic}} \cong \mathbf{v_{ic}} \quad \text{and} \quad \mathbf{v_{gs}} \cong \frac{1 + 2g_o R_{SS}}{1 + 2g_m R_{SS}}\mathbf{v_{ic}} \cong \left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right)\mathbf{v_{ic}} \tag{16.73}$$

since $2g_m R_{SS} \gg 1$. The short-circuit output current goes through the Thévenin output resistance $R_{\text{th}} = r_{o2} \| r_{o4}$ to produce the output voltage, and

$$A_{cm} = \frac{\mathbf{i_{sc}} R_{\text{th}}}{\mathbf{v_{ic}}} = \left[\Delta g_m \left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right) - \Delta g_o\right](r_{o2} \| r_{o4}) \tag{16.74}$$

The CMRR is then

$$\begin{aligned} \text{CMRR}^{-1} &= \left|\frac{A_{cm}}{A_{dm}}\right| = \left|\frac{A_{cm}}{g_m (r_{o2} \| r_{o4})}\right| \\ &= \left[\frac{\Delta g_m}{g_m}\left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right) - \frac{\Delta g_o}{g_o}\frac{1}{\mu_f}\right] \end{aligned} \tag{16.75}$$

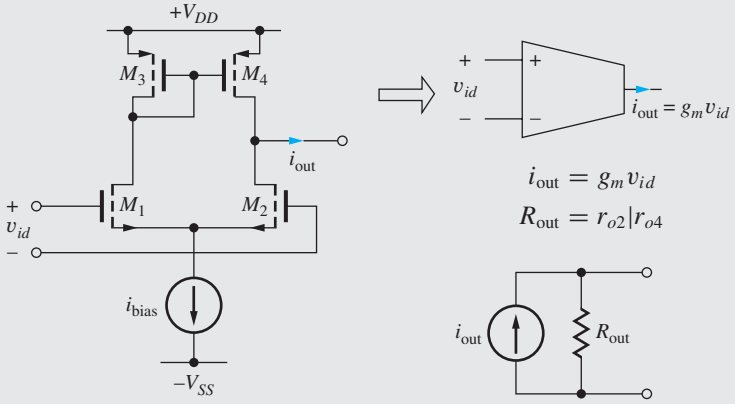
For very large R_{SS}, we see that CMRR is now limited by the transistor mismatches and value of the intrinsic gain. For example, a 1 percent mismatch with an intrinsic gain of 500 limits the individual terms in Eq. (16.75) to 2×10^{-5}. Since we cannot predict the signs on the $\Delta g/g$ terms, the expected CMRR is 2.5×10^4 or 88 dB. This is much more consistent with observed values of CMRR.

[5] An exact analysis without assuming that $v_{d1} = 0$ shows that a negligibly small change actually occurs.

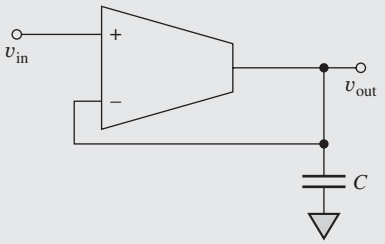
ELECTRONICS IN ACTION

G_m-C Integrated Filters

The design of integrated circuit filters is complicated by the lack of well-controlled resistive components in most mainstream CMOS processes. One approach to overcome this is the use of G_m-C filter topologies based on the operational transconductance amplifier (OTA). The OTA is characterized by both a high-input and high-output impedance. A simple form of an OTA is the CMOS differential amplifier from Fig. 16.31. The high-impedence output ($R_{\text{out}} = r_{o2} \| r_{o4}$) is a small-signal current given by the product of the differential pair g_m and the differential input voltage v_{id}. Typically, commercial OTA designs include additional devices to improve output resistance and voltage swing.



Equivalent schematic symbol for operational transconductance amplifier (OTA).



$$V_{\text{out}} = \frac{I_{\text{out}}}{sC} = (V_{\text{out}} - V_{\text{in}})\frac{g_m}{sC}$$

$$A_v(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{1}{1 + s\dfrac{C}{g_m}}$$

Single pole G_m-C low-pass filter.

A simple low-pass filter formed with an OTA and a capacitor is shown above. The transfer characteristic is also included and indicates that the upper cutoff frequency occurs at $f_H = g_m/2\pi C$. One of the more useful characteristics of the G_m-C filter approach is the ease with which the characteristics can be tuned. Recalling that g_m is a function of the differential pair current, we see that the cutoff frequency of the filter is easily modified by adjusting the bias current. It is also very important to note that this circuit is a continuous-time filter that requires no resistors!

A second-order version (a biquad topology) is shown on the next page. This circuit permits the adjustment of cutoff frequency with constant Q, and still requires no resistors. High-pass, band-pass, and band-reject are also readily derived from this basic form. Because of their compatibility with standard CMOS processes and excellent power efficiency, G_m-C filters are frequently used in low power in communication circuits, A/D converter anti-alias filters, noise shaping, and many other applications.