A Novel High Speed Current Mirror CompensationTechnique And Application

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Abstract:
In this paper, we propose a very simple but powerful method of bandwidth enhancement for general CMOS current-mirror circuits. By introducing a compensation resistor between the gates of the primary transistor pair of the current-mirror can lead to a significant bandwidth enhancement. Both simulated and measured results are presented in this paper.

1. Introduction

Current-mirrors are one of the most indispensable building blocks of analog circuits. In this paper we propose a new compensation technique to enhance the bandwidth of the current-mirror without distorting the dc characteristics of the original circuits. Analysis of the effect of biasing current, parasitic capacitance together with optimisation techniques are discussed in every section.

2. Basic Current Mirror

The most widely used CMOS current-mirrors are probably the simple[1], high-swing cascode[5], regulated cascode[4], and Wilson current-mirrors[1].

The simple two transistor current-mirror as shown in fig. 1, with R=0Ω(R is the compensation resistor which will be in introduced later) and $M_1 = M_2$, has a first order response of the form,

$$H(S) = \frac{g_{m2}}{g_{m1}} \frac{1}{1 + SC/g_{m1}} \qquad (1.a)$$

$$\omega_o = g_{m1} / 2C_{gs} \qquad (1.b)$$

where

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} |I|} \qquad (1.c)$$

$$C = 2C_{gs} = 2(\tfrac{2}{3} C_{ox} WL) \qquad (1.d)$$

I is the DC biasing current, g_m is the transconductance , and C is the combination of the two gate-source capacitors. Both transistors are assumed to operate in their saturation regions. The input and output capacitors and conductances are neglected. Obviously, assuming the mirror is a first order lowpass system then it will always be underdamped. Due to the capacitive loading of M_2, the current-mirror bandwidth is only half that of $M_1(M_1=M_2)$. Essentially, from eq. 1.b, the bandwidth is half the f_t of the MOSFET. The bandwidth reduction would be even worse if M_2 were much larger than M_1. For this simple configuration, a method of improving frequency performance is to increase the DC biasing current. However, this will tend to trade off power consumption. Since g_m is proportion to $\sqrt{I}$, the bandwidth improvement is not very effective. Another drawback of using high bias current is the mobility degradation[1]. The speed improvement is not proportional to the increment of bias current. In fact the improvement of g_m reduces rapidly with large V_{gs}. Taking into account these second order effects, the mobility μ can be approximated by the following relationship.

$$\mu = \mu_o [1 - \frac{1}{E_{cr} t_{ox}} (V_{gs} - V_t)] \qquad (1.e)$$

Where μ_o is the mobility at zero electric field, t_{ox} is the oxide thickness, and E_{cr} is the critical electrical field. Thus, large changes in biasing current cause large variation in V_{gs}, reducing the changes in bandwidth as discussed earlier.

3. Novel High Frequency Compensation Scheme

By introducing a compensation resistor between the gate of M1 and M2 as shown in fig. 1, the first order lowpass current-mirror is transposed into a second order lowpass with one zero and two poles as described by the following transfer function.

$$H(S) = \frac{g_{m2}}{C_2} \frac{(S + 1/RC_1)}{S^2 + \frac{C_1 + C_2}{RC_1C_2} S + \frac{g_{m1}}{RC_1C_2}} \qquad (2.a)$$

with a zero

$$Z_1 = -1/RC_1 \qquad (2.b)$$

and a complex pole pairs

$$P_{1,2} = \frac{C_1 + C_2}{2RC_1C_2} \left[-1 \pm \sqrt{1 - \frac{4g_{m1}RC_1C_2}{(C_1 + C_2)^2}} \right] \qquad (2.c)$$

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From a control theory prospective, eq. 2.a can be compared with a standard one zero, one complex pole pair system of the type shown below,

$$H(S) = \frac{\omega_o^2}{Z}\frac{(S+Z)}{S^2+2\varsigma\omega_o S+\omega_o^2} \quad (3.a)$$

Comparing coefficients of eq. 2.a with eq. 3.a yields

$$\omega_o = \sqrt{g_{m1}/RC_1C_2} \quad (3.b)$$

$$Z = 1/RC_1 \quad (3.c)$$

$$\varsigma = \frac{C_1+C_2}{2\sqrt{g_{m1}RC_1C_2}} \quad (3.b)$$

As the zero moves in along the negative real axis toward the origin, the time to the first peak of the step response changes monotonically while the percentage of overshoot increases monotonically. The most adverse effect can be observed when the zero moves closer to the origin than the real part of the complex pole pair. Overall, the addition of a zero makes the system faster and more oscillatory as the zero moves in the negative axis toward the origin. It is worth noting that when $R=1/g_{m1}$, the zero in eq. 3.c cancels one of the pole yielding a 1st order system with a frequency response determined by $\omega_o = g_{m1}/C_{gs}$ which is twice of the frequency in eq. 1.b; hence, the compensated current-mirror is operating at twice the bandwidth of the uncompensated and theoretically now at the f_t of the MOSFETs.

4. Compensation of Cascode Current Mirror

Fig. 2 shows the high-swing cascode current-mirror[4]. V_b ensures all of the transistors are operating in their saturation region. For $R=0\Omega$, the current-mirror in fig. 2 has the following small signal transfer function,

$$H(S) = \frac{g_{m1}}{C_T}\frac{g_{m2}}{C_2}\frac{1}{S^2+\frac{g_{m2}}{C_2}S+\frac{g_{m1}}{C_T}\frac{g_{m2}}{C_2}} \quad (4.a)$$

$$P_{1,2} = \frac{g_{m2}}{2C_2}\left[-1 \pm \sqrt{1-\frac{4g_{m1}/C_T}{g_{m2}/C_2}}\right] \quad (4.b)$$

$$\omega_o = \sqrt{\frac{g_{m1}}{C_T}\frac{g_{m2}}{C_2}} \quad (4.c)$$

$$\varsigma = \frac{1}{2}\sqrt{\frac{g_{m2}/C_2}{g_{m1}/C_T}} \quad (4.d)$$

where g_{m1} and g_{m2} are the transconductance of the lower and upper pair transistors, C_T is the combined gate-drain capacitance's of the lower pair transistors and C_2's are the gate-drain capacitance of the upper pair transistors. Eq. 4.a is a two pole system. By carefully choosing the ratio of the g_m's and dimension of the transistors, the amount of overshoot can be designed.

It is apparent that by increasing the size of M2 to reduce the overshoot leads to bandwidth reduction. Any capacitive compensation by augmenting C_T or C_2 will also reduce the bandwidth. Further, for low voltage design, g_m's and capacitances , hence the transistor sizes can not simply be fixed based on the frequency response. The DC voltage and current gain dominate the design procedure. The output swing which determines the output dynamic range is vital and has become a more important design criteria for circuit implementation. For analog signal processing, g_m's can be tuned via bias current.

An alternative method of tuning the frequency behaviour is again to introduce a resistor between the primary pair transistors in the current-mirror as shown in fig. 2. A detailed small signal analysis of the circuit yields the following transfer function

$$H(S) = \frac{g_{m1}}{C_1}\frac{g_{m2}}{C_3}\frac{(S+1/RC_1)}{S^3+\left[\frac{2C_3+g_{m2}RC_1}{RC_1C_3}\right]S^2+\left[\frac{2g_{m2}}{RC_1C_3}\right]S+\frac{g_{m1}g_{m2}}{RC_1^2C_3}} \quad (5.b)$$

where $C_1=C_{gs1}=C_{gs2'}$, $C_3=C_{gs2}=C_{gs2'}$, $g_{m1}=g_{m1'}$ and $g_{m2}=g_{m2'}$

The zero and poles can be approximated as

$$Z_1 = \frac{1}{RC_1} \quad (5.c)$$

$$P_1 = -\Re_1\left(1+\sqrt{1-g_{m1}/C_1\Re_1}\right) \quad (5.d)$$

$$P_2 = -\frac{1}{2}[\Re_1(1+\sqrt{1-g_{m1}/C_1\Re_1})+ \Re_2(1-\sqrt{1-4g_{m2}/\Re_2^2})] \quad (5.e)$$

$$P_3 = -\Re_2\left(1+\sqrt{1-4g_{m2}/\Re_2^2}\right) \quad (5.f)$$

where

$$\Re_1 = \frac{g_{m2}}{2C_3+g_{m2}RC_1} \quad (5.g)$$

$$\Re_2 = \frac{2C_3+g_{m2}RC_1}{2RC_1C_3} \quad (5.h)$$

The introduction of resistor R creates a new pole, P_3, and zero, Z_1. As the resistor value increases from zero to a large value, the new P_3 and Z_1 move from negative infinity towards the centre of the axes. At the same time, the intrinsic P_1 and P_2(eq. 4.b) approach each other and converge to a point when $R = 2C_3/g_{m2}C_1$. A further increase of R will lead to a complex pole pair which converge again at the centre of the axes. A maximum bandwidth is obtained when the zero cancels the low frequency pole.

5. Current Mirror Design Examples

In this section, we present the SPICE simulation results. All of the simulations are based on Northern Telecoms's 0.8μ BICMOS process. To illustrate the speed enhancement of the simple 2-transistor current- mirror, lets consider the graph shown in fig. 3. In this plot, we quantitatively investigate the speed improvement by resistive compensation compared to that through augmenting

bias current for a given design. The vertical axis is the one percent settling time for a 10μA step input current. As can be seen, with R=0, along the vertical axis, the speed improvements through augmenting bias currents reduces due to g_m proportional to $\sqrt{I}$ and mobility degradation. However, with resistive compensation for a given biasing current, the settling time reduces as the resistor value R increases. It is worth noting that the settling time for a bias of 40μA with R=4.25KΩ is less than that achieved with the non-compensated circuit(R=0Ω) and a biasing current of more than 320 μA. A power reduction of more than eight folds for the same speed is thus achieved with the compensated design. For this example, any further increase of biasing current beyond 320μA will only marginally improve the settling time in the uncompensated current-mirror(R=0).

Fig. 4 shows the settling time variation for a high swing cascode current-mirror[5]. To satisfy high swing, M1 has to be designed with large g_m. For better matching, the channel length must be much larger than minimum design rules of the process allowed; hence, $L_1 \geq L_2$. The result again demonstrates that an optimal value of R can be chosen to minimise the settling time.

Fig. 5 shows another example that of a regulated cascode current-mirror[4]. The regulated cascode current-mirror achieves high output resistance and high output swing by having a servo controlled cascode gate. Without going through the same detailed analysis, fig. 5 also shows the SPICE simulation results. It is clear from all the simulations presented with different circuit topologies that the resistive compensation technique enhances the speed and bandwidth of current-mirrors.

6. Tunability

For many high frequency applications, particularly in filter applications, manual or automatic tuning is required for precision. The tuning scheme normally involves changing DC bias current which in turn alters the g_m, and hence the frequency response. As indicated by eq. 3.b, the changes of g_m of the current-mirrors will led to the changes of ζ which can be compensated by tuning R. A transistor with drain and source connected across the resistor R, with gate voltage as control variable, will enable the resistor value to be tuneable in the predesigned range. Fig. 6 shows the step response of a simple tunable current-mirror. Alternatively, a single MOSFET operating in its triode region may be employed for tuning.

7. Current-mode Applications

In applications where current-mirrors are present, the resistive compensation technique can be applied to increase bandwidth and speed. So far continuous-time applications have been derived, but the technique is equally applicable to sampled-data applications such as switched-current filters, where short settling time is very important. A second generation switched-current memory cell and its step response are shown in fig. 7. The basic operation of the cell is as follows. Essentially, the circuit acts as a analog memory. During ϕ_1(Vs is HIGH) the input current is sampled by M1. During ϕ_2(Vs is LOW), the amount of current flowing through M1 will be held constant[7]. M3 is a gain stage which regulates the gate of cascode transistor M2 to reduce the output conductance of the cell[7]. Resistive compensation has been applied to the switch current memory cell to enhance the speed. With the same analysis as presented in section 2, it can be shown that by choosing suitable R values, we can optimise the speed of the current memory cell quite significantly. Other application of the resistive compensation technique includes continues time filter[8] and current feedback operational amplifiers[8].

8. Measurement Result

To confirm the validity of the resistive compensation technique in practice, a simple compensated current-mirror was fabricated in a 3μ high voltage(12.5V) CMOS process as part of a multi-chip projects. The devices dimensions were quite large since the components were essential for high current applications. The f_t of the transistor was about 2MHz. However as expected the current gain-bandwidth of the non-compensated current-mirror was measured to be about 1MHz. By introducing a 10KΩ compensation resistor, the bandwidth doubled to 2MHz as shown by the measured curve in fig. 8 and the curve reveals monotonic behaviour without any high frequency instability.

9. Conclusion

We have revealed a new elegant method of enhancing general current mirror bandwidth. Supported with analytic, SPICE simulation and measurement results, this topology enables us to extent the bandwidth without sacrificing other design parameters such as output swing, large signal gain, and power consumption. We are also looking into the many others possible applications. This technique may be applied to bipolar technology, but because of base current this will currupt the DC conditions. In fact a similar technique has been used as base current scaling in a bipolar mirrors.

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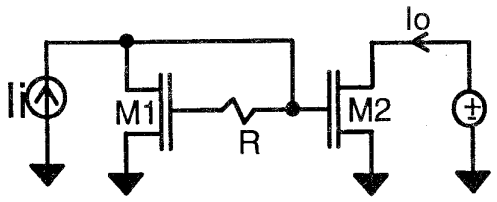

Fig 1. Basic current mirror

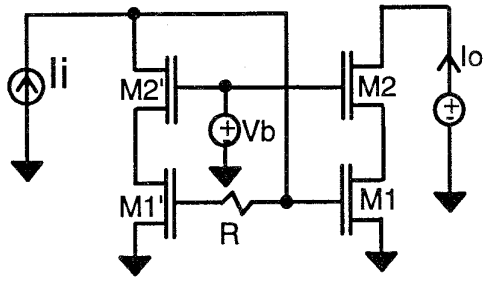

Fig 2. High-swing cascode current mirror

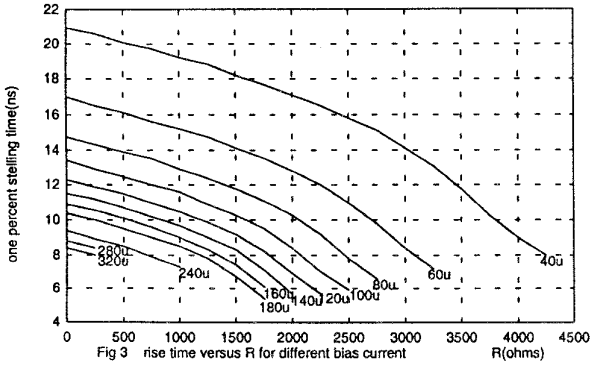

Fig 3 rise time versus R for different bias current

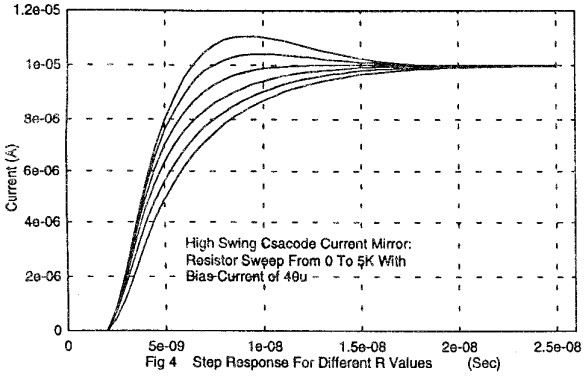

Fig 4 Step Response For Different R Values (Sec)

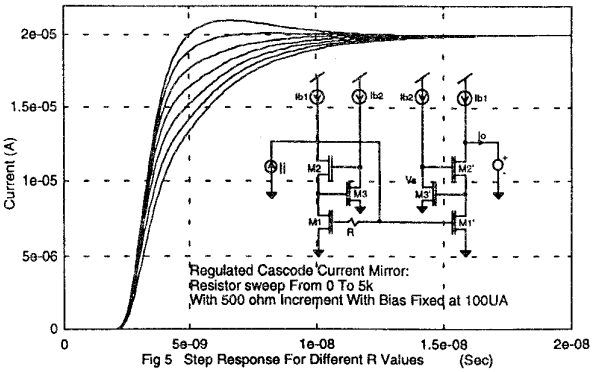

Fig 5 Step Response For Different R Values (Sec)

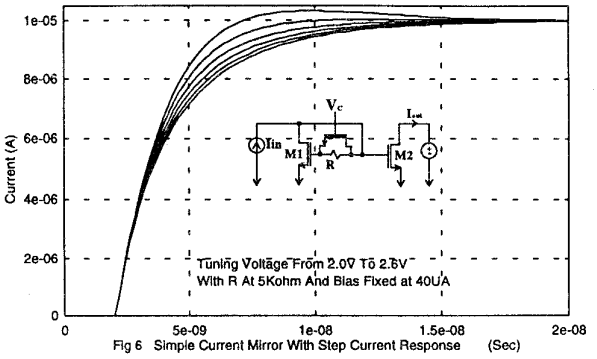

Fig 6 Simple Current Mirror With Step Current Response (Sec)

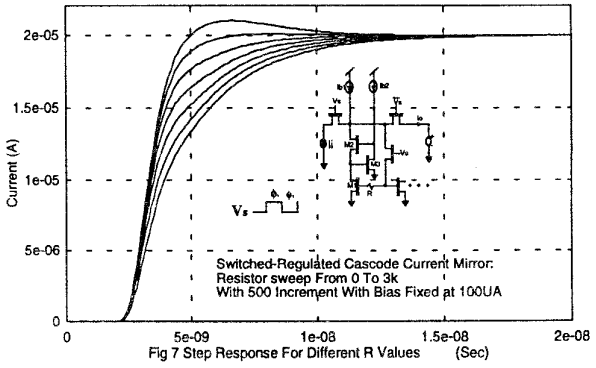

Fig 7 Step Response For Different R Values (Sec)

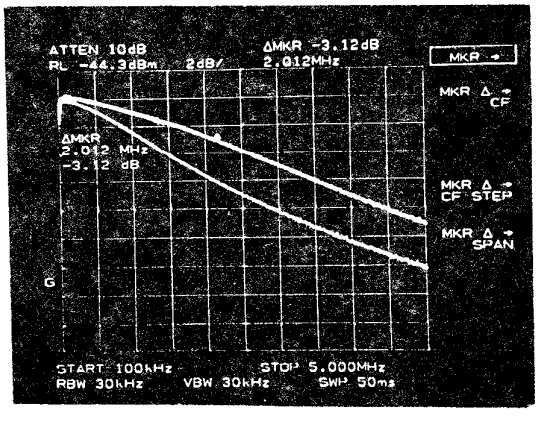

Fig 8 Simple Current-Mirror Frequency Response