[Paper] High Accuracy CMOS cap multiplier

Wednesday, 10 December, 2025 11:37 PM

High Accuracy ...

High Accuracy CMOS Capacitance Multiplier

Salvatore Pennisi

DEES (Dipartimento Elettrico Elettronico e Sistemistico) University of Catania, Viale Andrea Doria, 6
I-95125 CATANIA – ITALY - Phone: +39-095-7382318; Fax: +39-095-330793; email: spennisi@dees.unict.it

ABSTRACT

This paper presents a CMOS circuit suitable to magnify the value of a grounded unit capacitance. The multiplication factor is achieved through the gain of current mirrors and its maximum value is solely limited by power consumption constraints. Circuit solutions are then developed to reduce power dissipation and to enable the detection of small unit capacitances. Thanks to its inherent simplicity, the circuit is also characterized by wide-band operations. An on-chip tuning technique is also included which allows the value of the obtained capacitance to be adjusted by about ±70%. Simulations of a design example are provided.

1. INTRODUCTION

In short, u need big capacitance

Analog integrated systems often require the implementation of high-valued capacitors characterized by good accuracy and linearity. This is however an onerous task since linear capacitors –realized with two polysilicon layers– exhibit a relatively small specific capacitance. Furthermore, in some sensor applications it can be useful to deal with capacitance values higher than those normally given by the capacitive sensors. In all these circumstances, a circuit behaving as a capacitance multiplier becomes very useful.

Aka the cap connected between output and input of the op amp (gain elem.)

Cos the big cap load, become no gain at relatively low freq (low pass RC)
Research official ans why current mirror can handle hi freq

Active capacitive multipliers have been developed in the past, employing both voltage- or current-mode techniques [1-3]. Solutions using voltage amplifiers as active elements (exploiting the well-known Miller effect) can achieve high multiplication factors but are limited in frequency since the voltage gain includes a relatively low frequency pole, moreover they require the availability of both capacitor terminals. Current-mode techniques provide high-frequency performance but, as will be clear later, with reduced values of multiplication factors. In this last case, negative Current Conveyors (CCII-) [4], current mirrors and current amplifiers [5] have been used as active elements. To explain the operating principle of current-mode capacitive multiplication, consider the feedback configuration which uses a common-drain (or common-collector) transistor and a current mirror with current ratio equal to k, as schematically illustrated in Fig. 1.

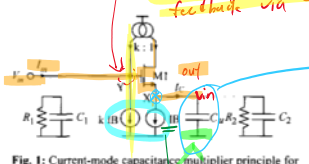

Fig. 1: Current-mode capacitance multiplier principle for a grounded capacitor C.

In our discussions we assume that the capacitor to be multiplied is grounded, as this situation is the most general one.

Considering an ideally unitary voltage gain between the gate and source terminals of the transistor, simple analysis shows that the input impedance, $Z_{in}=V_{in}/I_{in}$, is equal to $1/skC_x$. Thus, the value of the capacitance connected between the source terminal and ground is effectively multiplied by the current gain k. The main advantage of this scheme (and of many of the current-mode ones) relies on its simplicity. Moreover, the linearity and the high bandwidth of the current transfer gain, realized with current mirrors, is reflected on the obtained capacitance value. Of course, unavoidable nonidealities affect the circuit behavior. Basically, we have to consider the finite impedance at the gate of M1 due to the generator kI_B and the output of the current mirror (that we model with a resistor R_1 in parallel with a parasitic capacitance C_1), the output resistance of the source follower transistor ($1/g_{ms}$), and the output impedance of the current generator I_B (R_2 in parallel with C_2). Moreover, the pole in the current mirror transferfunction, ω_{kc}, limits the high-frequency operations. After considering these nonidealities we get

$$Z_{in} = \frac{1+s/\omega_M}{k}\,\frac{1+sC_x/g_{ms}}{\frac{1}{R_2}+s(C_x+C_2)} \,//\, \frac{1}{sC_1} // R_1 \qquad (1)$$

and the equivalent circuit of this impedance is modeled in Fig. 2. It is seen that resistances R_1 and R_2 affect the low-frequency circuit behaviour. However, since R_2 is divided by k its effect is usually the dominating one and can dramatically reduce the operating frequency bandwidth

0-7803-7596-3/02/$17.00 ©2002 IEEE

for large values of k. At high frequencies the limitation is due to the lowest pole among those introduced by the voltage and current transfers (g_m/C_x and ω_{kc}, respectively). Moreover, the minimum usable value of C_x is limited by capacitor C_2, while C_1 causes an offset error. Finally, it is apparent that any error of the current mirror ratio turns directly into a gain error.

In order to improve the above solution, we propose in this paper a novel implementation of capacitance multiplier which reduces the effects of many of the nonidealities discussed above, thus allowing the detection and amplification of smaller unit capacitors and enhancing the frequency performance. To improve flexibility, an electronic tuning technique is also added enabling the on-chip variation of the multiplication factor. This last property is, for instance, essential to compensate for process tolerances in continuous-time filters or integrated sensor applications.

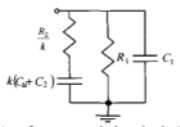

Fig. 2: Low-frequency equivalent circuit of the input impedance of circuit in Fig. 1.

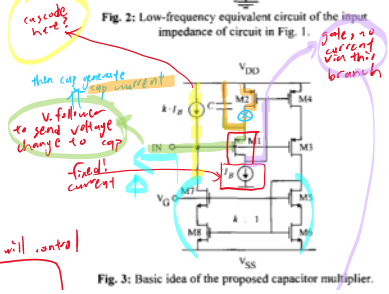

Fig. 3: Basic idea of the proposed capacitor multiplier.

this current mirror which lastly feeds the amplified current back to the input terminal.

Note that to minimize the effects of the finite drain impedance of M2, we connect the gate of M3 to the input terminal, instead to a constant voltage. In this manner, M2 and M4 operate under the same electrical and topological conditions, thus improving the accuracy by which the current from the capacitor is sensed and allowing the amplification of very small unit capacitances. The AC schematic in Fig. 4 is useful to visualize this concept. The circuit represents the input section of the proposed circuit removing the unit capacitor. Assume that transistors M2 and M4 are ideal voltage-controlled current-sources and that their finite output impedance is modeled by z_{o2} and z_{o4}, with $z_{o2}=z_{o4}$ as M2 and M4 are implementing a unitary current mirror. After applying V_{in}, the output current provided by M3 should be ideally zero because no capacitance has to be sensed. Actually, V_{in} causes the small-signal current I (about equal to V_{in}/z_{o2}) to flow through z_{o2}, this current must be supplied by M2 (remember that M1 is forced to conduct the fixed current I_B). Due to the mirror action, current I is replicated by M4 and, since V_{in} is also applied to the gate of M3, it is perfectly canceled by the current generated onto z_{o4}. Thus, we get $I_3=0$. In conclusion, current I_3 is effectively the one flowing through the unit capacitor C, irrespective of the actual impedance which subsists in parallel with C.

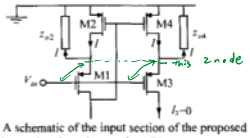

Fig. 4: A schematic of the input section of the proposed circuit (removing the unit capacitor C.)

It can be noticed that, without using this technique, the finite output impedance of M2 would strongly limit circuit operations at low frequency. Indeed, being the current on a capacitor proportional to the frequency, for angular frequencies much lower than $1/(|z_{o2}|C)$ the current through C would be much lower than that flowing through z_{o2} and therefore its contribution to I_3 would be hardly

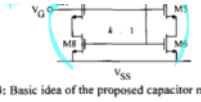

Fig. 3: Basic idea of the proposed capacitor multiplier.

2. THE PROPOSED SOLUTION

The proposed circuit is shown in Fig. 3. The input transistor, M1, acts as a voltage follower and at its source terminal the grounded unit capacitor, C, is connected. Since the current through M1 is constant (it is set by the bias current generator I_B) the current flowing through C is sensed by transistor M2, it is then mirrored through M4 and delivered to the current mirror M5-M7. The capacitance factor is set by the transistor aspect ratios of

It can be noticed that, without using this technique, the finite output impedance of M2 would strongly limit circuit operations at low frequency. Indeed, being the current on a capacitor proportional to the frequency, for angular frequencies much lower than $1/(|z_{g2}|C)$ the current through C would be much lower than that flowing through z_{g2} and therefore its contribution to I_3 would be hardly detectable. On the other hand, the equivalent output resistance at the drain of M7 can be made very large using cascoding techniques, thereby minimizing its adverse effect at low frequencies.

Another attractive feature of the circuit is its very small resistance exhibited at the source of M1, whose expression is approximately $1/g_{m7}r_{d7}$. This, as already stated, improves the high-frequency performance.

The circuit main drawback is the high power dissipation that is proportional to the multiplication factor. Indeed, the small-signal multiplication factor, k, applies also to the quiescent current of the mirror M5-M8.

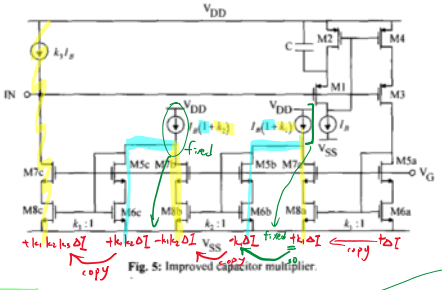

Fig. 5: Improved capacitor multiplier.

When a large factor k is needed, this constitutes a serious problem. To avoid the above limitation, we adopt the solution in Fig. 5, where the small-signal current gain is obtained through the cascade of three current-mirror stages (M5a-M7a, M5b-M7b, and M5c-M7c). The i-th current mirror provides a current gain equal to k_i so that the overall multiplication factor is $k = k_1 k_2 k_3$, but the quiescent current of the input section of each current mirror (i.e., transistors M5-M6) is always the same and equal to I_B. Therefore, the total current dissipation of the circuit is

$$I_{Q,TOT} = (1 + k_1 + k_1 k_2 + k_1 k_2 k_3) I_B \quad (2)$$

instead of $(2 + k_1 k_2 k_3) I_B$.

Finally, a tuning subsection can be incorporated in the circuit. The most simple is perhaps the one which exploits triode-biased transistors (MT1-MT2) as source degeneration of a (generic unitary current mirror (M5-M8), as illustrated in Fig. 6 [6]. If the tuning voltage, V_{TUNE}, is zero the mirror operates under balanced conditions, because the conductance of MT2 equals that of MT1, and I_{out} equals I_{in}. If V_{TUNE} is negative (positive) the conductance of M8 is lower (greater) than that of M7 and I_{out} is lower (greater) than I_{in}. Therefore, their current ratio can be varied by means of V_{TUNE}.

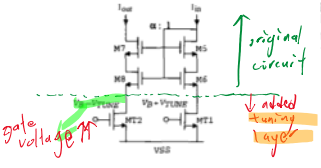

Fig. 6: Tuning technique using triode-biased transistors MT1-MT2.

Note that the achieved current ratio, also applies to the quiescent currents in addition the small signal component. Therefore, we have to vary the bias current of the output branch according to the tuning voltage applied [6]. For this reason it is convenient to apply this technique to the last current mirror in Fig. 5, M5c-M8c, and consequently only to its bias current generator $k_3 I_B$.

3. SIMULATIONS

The circuit in Fig. 5 was simulated with SPICE and using the models of a 0.8-μm CMOS process. Transistors dimensions and bias settings are summarized in Table I. A typical behavior of the module and phase of the input impedance is plotted in Fig. 7 curves a, where we set C=1pF and k=8 (k_1= k_2= k_3=2). It can be noticed that the impedance is predominantly capacitive within a limited frequency range. Note that this range is strongly reduced if the gate of M3 is connected to a constant voltage as shown by curves b in the same figure (and using the same other settings).

A quantification of the frequency range where the capacitance multiplication occurs and the related accuracy, can be made by considering the three parameters defined below. The first two are related to the bandwidth at −1° with respect to −90° and are respectively the lower, f_{rL}, and higher, f_{rH}, limit frequencies. The second parameter is defined as

$$C_M = \left[Z_{in}(f^*) 2\pi f \right]^{-1} \quad (3)$$

where f^* is an arbitrary frequency internal to the −1° bandwidth. Equation (3) gives a capacitance value which is nominally equal to kC. For instance, the curves a in Fig. 7 yield f_{rL}=4.40 kHz, f_{rH} =132kHz and C_M=7.85pF, with a percentage error compared to the ideal capacitance value (8 pF) of −1.9%. As already noted, the circuit may

be useful in two different contests. The first concerns the realization of high capacitance values, otherwise impractical to be fabricated, and the second is to detect and amplify very small capacitances, like those provided by integrated sensors. To examine the circuit performances within these two frameworks and to understand their fundamental limitations we set different unit capacitors ranging from 50 fF to 10 pF and four different multiplication factors, all obtained using $k_1=k_2=k_3$. These results are summarized in Table II, and the case for C=10 pF is also illustrated in Fig. 8. It is seen that there is an offset and a gain error. Offset is caused by the parasitic capacitance in parallel to Z_{in} (about 25fF) and its effect becomes negligible for large values of kC. The gain error is constant (about -2.5%) and is due to the transfer gain of the current mirrors. We see that increasing k reduces the -1^{o}-bandwidth. Moreover, increasing C by a factor of 10 produces approximately the same decrease in $f_{1^{o}L}$. In conclusion, we can obtain an accurate magnification of unit capacitances as low as 100fF, and the easy realization of equivalent capacitances in the range of several nanofarads. The tuning technique was finally applied. In brief, by varying V_{TUNE} from +0.3V to -0.4V, C_M modifies by about ±70%.

Component	Value
M1, M3	10/0.8
M2, M4	4/0.8
M5abc, M6abc	20/1.2
M7a, M8a	k_1·20/1.2
M7b, M8b	k_2·20/1.2
M7c, M8c	k_3·20/1.2
I_B	2 µA
VDD-VSS	3 V
VG	1.5 V
VB	1.6 V

Table 1. Transistors dimensions and bias settings.

C	k	$f_{1^{o}L}$ (kHz)	$f_{1^{o}H}$ (kHz)	C_M	$E\%(C_M)$
50fF	1	11.7	333	75.6fF	+51
	8	58.4	219	449fF	+12
	125	59.7	118	6.15pF	–1.6
	1000	44.5	67.0	47.3pF	–5.4
100fF	1	7.10	263	124fF	+24
	8	34.3	179	839fF	+4.9
	125	36.5	92.2	12.2pF	–2.1
	1000	28.6	51.3	96.1pF	–3.9
1pF	1	0.864	199	1.00pF	0.0
	8	4.40	132	7.85pF	–1.9
	125	5.56	59.1	122pF	–2.4
	1000	5.22	27.3	972pF	–2.8
10pF	1	0.088	120	10.2pF	+2.0
	8	0.459	92.1	78.0pF	–2.6
	125	0.609	46.4	1.22nF	–2.6
	1000	0.621	21.5	9.73nF	–2.7

Table 2. Circuit performance under different settings.

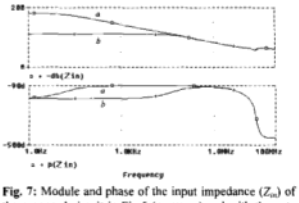

Fig. 7: Module and phase of the input impedance (Z_{in}) of the proposed circuit in Fig.5 (curves a) and with the gate of M3 biased at constant voltage (curves b). C = 1pF and k = 8 were set in both cases.

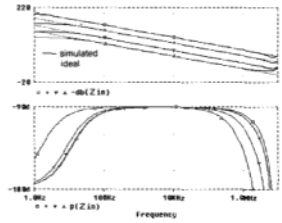

Fig. 8: Magnitude and phase of the input impedance (Z_{in}) of the circuit in Fig.5 with C=10pF and k = 1, 8, 125, 1000.

4. REFERENCES

[1] A.D'Amico, C. Di Natale, M. Mariucci, G. Baccarani, M. Faccio, G. Ferri, F. Maloberti, P. Malcovati, G. Stochino, "Active capacitance multiplication for sensor application" - Sensors and Microsystems - *Proc. Second Italian Conference of Sensors and Microsystems*, Roma, Feb.1997.

[2] G.Di Cataldo, G.Ferri, S.Pennisi, "Active capacitance multiplication by current conveyors" *Proc. IEEE ISCAS'98*. Monterey, May. 1998.

[3] G. Rincon-Mora, "Active Capacitor Multiplier in Miller-Compensated Circuits" *IEEE Trans. on Solid-State Circuits*, Vol. 35 N.1 Jan. 2000.

[4] A. Sedra, K. Smith, "A Second-Generation Current Conveyor and Its Applications", *IEEE Trans. on Circuit Theory*, CT-17, pp. 132-133, February 1970.

[5] G. Palmisano, G. Palumbo, S. Pennisi, *CMOS Current Amplifiers*, Boston/Dordrecht/London, Kluwer Academic Publishers, 1999.

[6] G. Palmisano, S. Pennisi, "New CMOS Tunable Transconductor for Filtering Applications", *Proc. IEEE ISCAS'01*, Sydney, Vol. 1, pp. 196-199, May 2001.