Current mirror op amp equations

Sunday, 4 January 2026 4:28 pm

Cascode_symmetrical...

6-7-1 Symmetrical CMOS OTA

The circuit schematic of the CMOS OTA with symmetrical input stage is given in Fig. 6-45. The differential pair is formed by input transistors T1 and T2. They drive their output currents in two transistors, T3 and T4, which are connected as diodes.

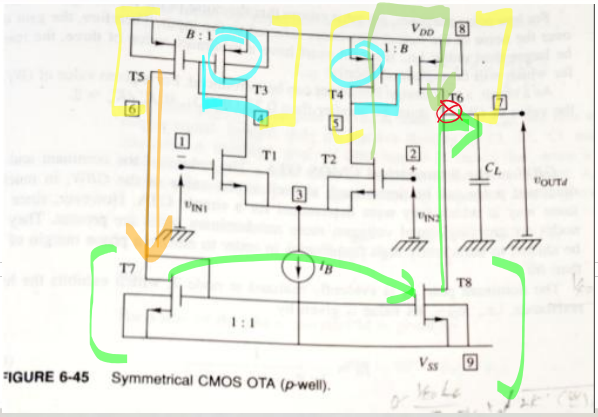
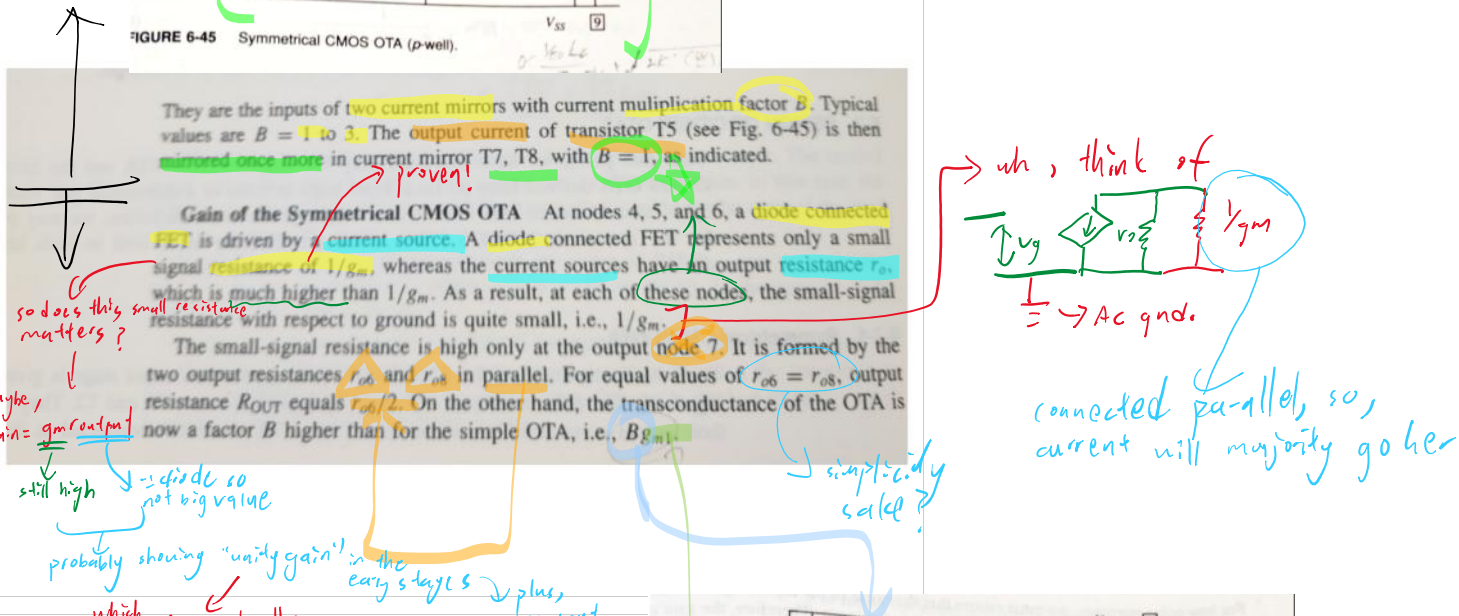


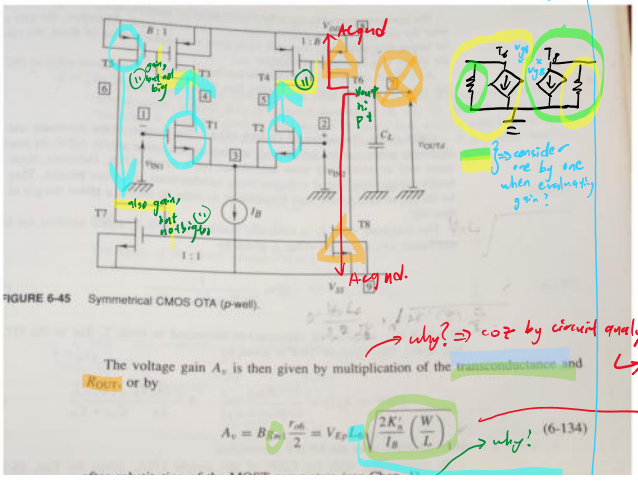
FIGURE 6-45 Symmetrical CMOS OTA (*p*-well).

They are the inputs of two current mirrors with current muliplication factor B. Typical values are $B = 1$ to 3. The output current of transistor T5 (see Fig. 6-45) is then mirrored once more in current mirror T7, T8, with $B = 1$, as indicated.

Gain of the Symmetrical CMOS OTA At nodes 4, 5, and 6, a diode connected FET is driven by a current source. A diode connected FET represents only a small signal resistance of $1/g_m$, whereas the current sources have an output resistance r_o, which is much higher than $1/g_m$. As a result, at each of these nodes, the small-signal resistance with respect to ground is quite small, i.e., $1/g_m$.

The small-signal resistance is high only at the output node 7. It is formed by the two output resistances r_{o6} and r_{o8} in parallel. For equal values of $r_{o6} = r_{o8}$, output resistance R_{OUT} equals $r_{o6}/2$. On the other hand, the transconductance of the OTA is now a factor B higher than for the simple OTA, i.e., Bg_{m1}.



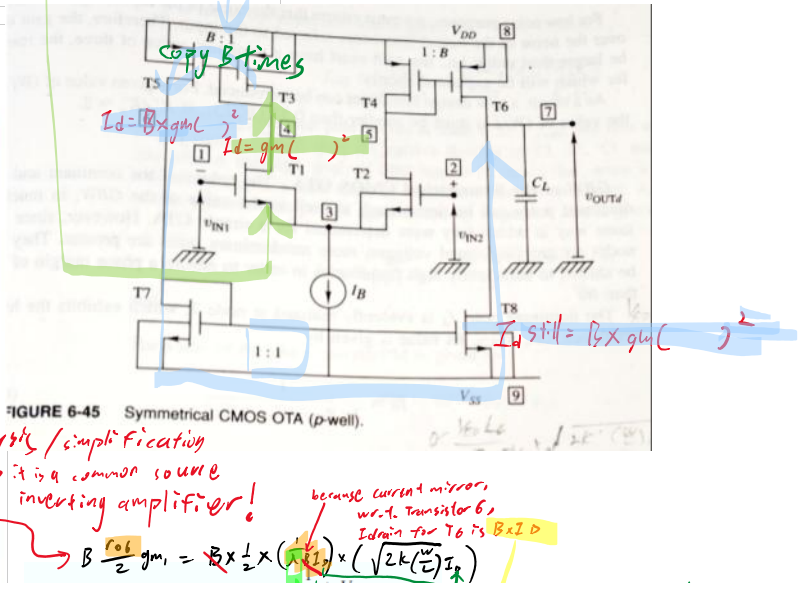


The voltage gain A_v is then given by multiplication of the transconductance and R_{OUT} or by

$$A_v = Bg_m \frac{r_{o6}}{2} = V_{EB} I_B \sqrt{\frac{2K_n'}{I_B}\left(\frac{W}{L}\right)_1} \quad (6\text{-}134)$$

why? ⇒ coz by circuit analysis / simplifying

↳ it is a common source inverting amplifier!



$$B\frac{r_{o6}}{2} g_{m1} = B \times \frac{1}{2} \times \left(\sqrt{2k\left(\frac{W}{L}\right) I_B}\right) \times \left(\sqrt{2k\left(\frac{W}{L}\right) I_B}\right)$$

because current mirror, w.r.t. Transistor 6, Id min for T6 is B x I D

R_{OUT} or by

$$A_v = B g_m \frac{r_{o6}}{2} = V_{EB} I_B \sqrt{\frac{2K_n'}{I_B}\left(\frac{W}{L}\right)_1} \quad (6\text{-}134)$$

after substitution of the MOST parameters (see Chap. 1).

Note that factor B is not present in the expression of the gain A_v. The transconductance increases B times, whereas R_{OUT} decreases B times. Yet, in comparison with A_v in Eq. (6-3*a*), an additional design factor appears in Eq. (6-134), which is L_1. Its value can be taken as larger than L_L. The voltage gain A_v can thus be increased by increasing the value of r_{o6} or L_1. With this additional degree of freedom, the output resistance R_{OUT} and the voltage gain A_v can be increased without affecting the OTA transconductance.

Up until this point, the total gain A_v of the OTA has been considered. The gain of the first stage A_{v1} alone is important as well, as it determines the noise performance of the OTA. It is given by the ratio of $(v_5 - v_4)/v_{IN1}$, if v_{IN2} is grounded. It is found by inspection (see Sec. 6-1) to be

$$A_{v1} = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{K_n'}{K_p'}}\sqrt{\frac{(W/L)_1}{(W/L)_3}} \quad (6\text{-}135)$$

inverting amplifier!

$$B\frac{r_{o6}}{2} g_{m1} = B \times \frac{1}{2} \times \left(\frac{1}{\lambda I_B}\right) \times \left(\sqrt{2k\left(\frac{W}{L}\right) I_B}\right)$$

Output resistance: $r_o = \frac{1}{g_o} = \frac{\frac{1}{\lambda}+V_{DS}}{I_D} \cong \frac{1}{\lambda I_D}$

In the Shichman–Hodges model used above, output resistance is given as:

$$r_O = \frac{1+\lambda V_{DS}}{\lambda I_D} = \frac{1}{I_D}\left(\frac{1}{\lambda}+V_{DS}\right) = \frac{V_E L/\Delta L + V_{DS}}{I_D}$$

where V_{DS} = drain-to-source voltage, I_D = drain current and λ = channel-length modulation parameter. Without channel-length modulation (for $\lambda = 0$), the output resistance is infinite. The channel-length modulation parameter usually is taken to be inversely proportional to MOSFET channel length L, as shown in the last form above for r_O.[3]

$$\lambda \approx \frac{\Delta L}{V_E L}$$

where V_E is a fitting parameter, although it is similar in concept to the Early Voltage for BJTs. For a 65 nm process, roughly $V_E \approx 4$ V/μm.[3] (A more elaborate approach is used in the EKV model.[4]). However, no simple formula used for λ to date provides accurate length or voltage dependence of r_O for modern devices, forcing use of computer models, as discussed briefly next.

For low noise purposes, we must ensure that the noise of the input stage is dominant over the noise of the output transistors referred to the input. Therefore, the gain must be larger than unity, i.e., the gain must have a minimum value of three, the reasons for which will be explained shortly.

As a result, a new design constraint can be introduced. For a given value of $(W/L)_1$, the value of $(W/L)_3$ must be smaller than $0.22\,(W/L)_1$, if $K_n'/K_p' \approx 2$.

GBW of the Symmetrical CMOS OTA The values of the dominant and nondominant poles can be determined, as well as the value of the *GBW*, in much the same way in which they were determined for a simple OTA. However, since more nodes are carrying signal voltages, more nondominant poles are present. They must be shifted to sufficiently high frequencies in order to ensure a phase margin of more than 60°.

The dominant pole f_d is evidently realized at node 7, which exhibits the highest resistance, i.e., R_{OUT}. Its value is given by

$$f_d = \frac{1}{2\pi R_{OUT}(C_{n7}+C_L)} \quad (6\text{-}136)$$

in which C_{n7} includes all capacitances connected to node 7, due to the OTA (see Fig. 6-45). The value of *GBW* is given by

$$GBW = A_v f_d = \frac{Bg_{m1}}{2\pi(C_{n7}+C_L)} = B\frac{\sqrt{2K_n' I_B}\sqrt{(W/L)_1}}{2\pi} \frac{1}{C_{n7}+C_L} \quad (6\text{-}137)$$

after substitution of the MOST parameters.

In comparison with the *GBW* of the simple OTA, given by Eqs. (6-7*a*) and (6-7*b*), the *GBW* of the symmetrical OTA is B times larger. Note, however, that the total current consumption is $(B + 1)$ times larger as well. The value of *GBW* is thus increased, but at the expense of more current consumption.

On the other hand, let us not forget that the increased symmetry of the input stage is an additional advantage, which has not yet been represented by numbers. This will be done later. In order to be able to effectively use this value of *GBW*, the nondominant poles are evaluated first. The calculation of the phase margin will show that the factor of B can never be made large.

Phase Margin PM of the Symmetrical CMOS OTA Nondominant poles occur at all other nodes, i.e., at nodes 4, 5, and 6, due to the capacitances on these nodes. Nodes 4 and 5 carry small signals, which have the same amplitude but the opposite phase. Therefore, the poles at nodes 4 and 5 are the same. Together, they form one single nondominant pole f_{nd5} (see also App. 6-1).

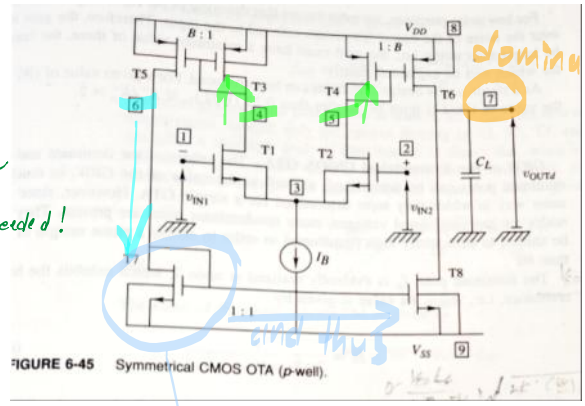


FIGURE 6-45 Symmetrical CMOS OTA (*p*-well).

It is found by inspection and is given by

$$f_{nd5} \approx \frac{g_{m3}}{2\pi C_{n5}} = \frac{\sqrt{2K_p' I_B}\sqrt{(W/L)_4}}{2\pi} \frac{}{C_{n5}} \tag{6-138}$$

The other nondominant pole occurs at node 6, i.e., f_{nd6}, but acts on only half of the output signal. Indeed, only the current flowing in T3, T5, T7, and T8 is subject to this pole. A thorough analysis (see App. 6-1) shows that, when a pole acts on only half of the signal, a zero must be added at twice the frequency. A pole-zero doublet is thus created. This pole is again found by inspection and is given by

$$f_{nd6} \approx \frac{g_{m7}}{2\pi C_{n6}} = \frac{\sqrt{2K_n' I_B}\sqrt{B(W/L)_7}}{2\pi} \frac{}{C_{n6}} \tag{6-139}$$

and

$$f_{z6} = 2f_{nd6}$$

The value of the phase margin PM is given by

$$\text{PM} = 90^\circ - \varphi_{n5} - \varphi_{n6} \tag{6-140}$$

with $$\varphi_{n5} = \arctan\frac{GBW}{f_{nd5}} = \arctan BA_{v1}\frac{C_{n5}}{C_L + C_{n7}}$$

and $$\varphi_{n6} = \arctan\frac{GBW}{f_{nd6}} - \arctan\frac{GBW}{2f_{nd6}}$$

$$= \arctan\sqrt{\frac{B(W/L)_1}{(W/L)_7}}\frac{C_{n6}}{C_L + C_{n7}} - \arctan\frac{1}{2}\sqrt{\frac{B(W/L)_1}{(W/L)_7}}\frac{C_{n6}}{C_L + C_{n7}}$$

after substitution of GBW, f_{nd5}, and f_{nd6}. Also $K_n' \approx 2K_p'$ and gain A_{v1} has been taken from Eq. (6-135).

It can be concluded that the phase margin PM can be increased by

- decreasing node capacitances C_{n5} and C_{n6}
- decreasing B
- increasing $(W/L)_7$

(provided we keep constant $A_{v1} = 3$ and constant C_L).

It is not acceptable to decrease B too much. Factor B is normally increased to increase the slew rate (as we will see later in this section). A good compromise is $B = 3$. For a given C_L, this leaves us thus only $(W/L)_7$ to play with to ensure sufficient phase margin.

However the phase margin is not very sensitive to $(W/L)_7$ because φ_6 is only a very weak function of $(W/L)_7$. As a result, other design plans may be more suitable, as explained later.

Example 6-13

Take a symmetrical OTA with $I_B = 10\ \mu\text{A}$, $B = 3$, $V_{EP} = 8.3\ \text{V}/\mu\text{m}$, $L_6 = 10\ \mu\text{m}$, $L_1 = 5\ \mu\text{m}$ and $W_1 = 50\ \mu\text{m}$ ($K_n' = 20\ \mu\text{A/V}^2$, $K_p' = 10\ \mu\text{A/V}^2$). Calculate the gains and the GBW for $C_L = 10$ pF.

Find the PM for $(W/L)_7 = 10$ and $A_{v1} = 3$ if $C_{n5} = C_{n6} = 1$ pF. Repeat for $B = 1$.

Solution. The resulting values are $R_{OUT} = 2.77\ \text{M}\Omega$, the OTA transconductance $Bg_{m1} = 190\ \mu\text{S}$ and $A_v = 524$. For $C_L = 10$ pF (C_{n7} is negligible), $GBW = 0.3$ MHz. The PM $= 90^\circ - \varphi_{n5} - \varphi_{n6} = 90^\circ - 42^\circ - 4.9^\circ = 43.1^\circ$. For $B = 1$, the respective values are $R_{OUT} = 8.3\ \text{M}\Omega$, $Bg_{m1} = 63.3\ \mu\text{S}$, but $A_v = 524$ is the same. For $C_L = 10$ pF, $GBW = 0.1$ MHz. The PM $= 90^\circ - 16.7^\circ - 2.85^\circ = 70.4^\circ$.

Design Plan The design plan is very similar to the plan for a simple OTA. Again, it is carried out in two steps. The GBW is determined at the dominant node, which is the output node, as given by Eq. (6-137). Second, the phase margin is determined by the two nondominant poles at the two other nodes.

Assume that C_L is given. For a given current I_B, a given $(V_{GS1} - V_T)$, and a given GBW, the size of the input transistor $(W/L)_1$ is obtained from Eq. (6-137). The sizes of the transistors $(W/L)_4$ and $(W/L)_7$ must be such that the phase margin, given in Eq. (6-140), is sufficiently large. Two extra variables are added, i.e., the gain of the first stage A_{v1} and the current multiplier B.

As a result, we have four variables I_B, $(W/L)_1$, $(W/L)_4$, and $(W/L)_7$ to satisfy four specifications: GBW, PM, A_{v1}, and B, provided C_L is given. An exact solution can thus be found.

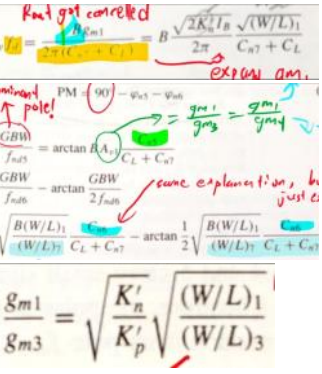
We can also relax the specifications. After all, B is present because of the slew rate and A_{v1} is present because of the noise. Let us first calculate these characteristics exactly before we make a decision about the design plan.

Slew Rate Again, for the symmetrical OTA, the slew rate is determined by the load capacitance. The current available to charge this capacitance is now BI_B. The slew rate is given by

$$SR = B\frac{I_B}{C_L + C_{n7}} \tag{6-141}$$

It is B times larger than the slew rate for the simple OTA, which yields a considerable advantage. Remember, however, that the current consumption was $(B + 1)$ times larger as well.

Noise Performance The total output noise voltage power $\overline{dv_{out}^2}$ is the sum of the equivalent input noise voltage powers $\overline{dv_{in}^2}$ of each transistor, multiplied by their gain



squared. The equivalent input noise voltage power $\overline{dv_{in}^2}$ is then obtained by division of the total gain squared. This yields

$$\overline{dv_{in}^2} = 2\overline{dv_1^2} + 2\left(\frac{g_{m4}}{g_{m1}}\right)^2 \overline{dv_4^2} + \frac{2}{B^2}\left[\left(\frac{g_{m6}}{g_{m1}}\right)^2 \overline{dv_6^2} + \left(\frac{g_{m7}}{g_{m1}}\right)^2 \overline{dv_7^2}\right] \tag{6-142}$$

Substitution of all $\overline{dv_{in}^2}$ by their expression $8kTdf/3g_{mi}$ yields

$$y = \frac{\overline{dv_{in}^2}}{\overline{dv_1^2}} = 2 + 2\frac{g_{m4}}{g_{m1}} + \frac{2}{B^2}\left[\frac{g_{m6}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right] \tag{6-143a}$$

Note that the total equivalent input noise has been normalized to the equivalent input noise of one input transistor only. This is the so-called excess noise y.

Remembering that $g_{m1}/g_{m4} = A_{v1}$ and that $g_{m6}/g_{m4} = B$, the previous expression becomes

$$y = 2\left\{1 + \frac{1}{A_{v1}}\left[1 + \frac{1}{B}\left(1 + \sqrt{\frac{K_n'(W/L)_7}{K_p'(W/L)_5}}\right)\right]\right\} \tag{6-143b}$$

The total equivalent input noise can thus be reduced to the equivalent input noise of only the two input transistors, provided the gain of the first stage A_{v1} is large. Since this impairs the stability, as shown by Eq. (6-140), a compromise is taken for A_{v1}, such as three to five. Increasing B helps, but it also reduces the phase margin. A good compromise for B is one to three.

Example 6-14

Calculate the excess noise and the total input noise voltage for the amplifier of Fig. 6-45, from Example 6-13 with $B = 1$ in unity gain configuration (i.e., output connected to a noninverting input terminal). Also, calculate the maximum signal-to-noise S/N ratio for a sinusoidal output with a ±2.5 V supply voltage.

Solution. Since $(W/L)_1 = 10$ and $A_{v1} = 3$, Eq. (6-135) yields $(W/L)_3 = 2.2$; also, $(W/L)_5 = (W/L)_3 = 2.2$ because $B = 1$. Hence, the total equivalent input noise voltage power is $y = 5.3$ times that of only the input transistor. For this transistor T1, $g_{m1} = 63.3\ \mu$S, which yields $\overline{dv_1^2} = 1.75 \times 10^{-16}$ V^2/Hz and $\overline{dv_{in}^2} = 9.3 \times 10^{-16}$ V^2/Hz. For a bandwidth of 0.1 MHz with a single-pole characteristic, the noise bandwidth is $\pi/2$ times as much (see Chap. 5), or 0.16 MHz. The equivalent

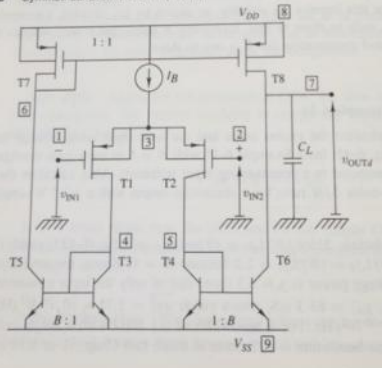
input noise is thus 1.5×10^{-10} V^2 or 12 μV$_{RMS}$. The peak output amplitude for a sine waveform is 2.5 V and its RMS value is $2.5/\sqrt{2} = 1.77$ V$_{RMS}$. As a result, the maximum S/N ratio is 1.5×10^5, or 103 dB.

BICMOS Alternatives In a BICMOS process with an n-well, the symmetrical OTA can be realized, as shown in Fig. 6-46. To obtain better matching, the sources of the input devices are connected to their common well. The input devices are MOSTs, because of the high input impedance and the high SR/GBW ratio. The nMOST current mirrors have been replaced by *npn* transistor mirrors.

The advantages of using a BICMOS process are as follows. First, the minimum voltage across a bipolar transistor is only a few hundred mV's, allowing a larger output swing. Second, the transconductance of a bipolar transistor is smaller. This causes the impedances at nodes 4 and 5 to be smaller. At these nodes, however, the capacitance is higher because of the collector-to-substrate capacitances. As the main nondominant pole is determined at these nodes, it will depend on the actual values used, whether the phase margin is smaller or not.

However, the noise performance will always be worse. The gain A_{v1} will probably be less than unity, giving rise to a large contribution by all transistors (see Eq. (143b)). In the CMOS circuit, we can effectively limit the noise contributions to the noise of two input transistors only, which is the best that can be achieved with any differential circuit.

FIGURE 6-46 Symmetrical BICMOS OTA (n-well).



used ideal voltage source in my case!

Note that current mirrors can be substituted by more complicated mirrors to increase the symmetry. Since this primarily involves the use of cascode transistors, we devote a separate section to this possibility.

6-7-2 Cascode Symmetrical CMOS OTA

In order to increase the open-loop gain and the symmetry, cascode transistors can be added. Of course, cascodes can be added in any OTA circuit. As an example, let us add cascodes in the symmetrical CMOS OTA discussed in the previous section. The circuit schematic is given in Fig. 6-47. Transistors M7 to M10 are cascode transistors. They are biased by a separate biasing network consisting of transistors M15 to M18, the current in which is set by current source I_B and transistor M14.

same!

Gain The only high impedance point in this circuit is the output node. All other such points are at a resistance level of $1/g_m$. The output resistance R_{OUT} consists of a resistance toward transistor M8, called $R_{OUT8} (= 1/g_{OUT8})$, and one toward M10, called $R_{OUT10} (= 1/g_{OUT10})$. It is given by

same thing but written in 1/Rout only

$$R_{OUT} = \frac{1}{g_{OUT8} + g_{OUT10}} \quad (6\text{-}144)$$

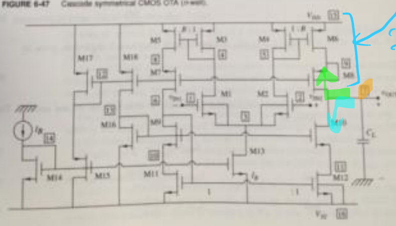
= Rout8 // Rout10 → $\frac{R_8 R_{10}}{R_8 + R_{10}}$ vs $\frac{1}{\frac{1}{R_8}+\frac{1}{R_{10}}} = \frac{1}{\frac{R_8+R_{10}}{R_8 R_{10}}}$ same!

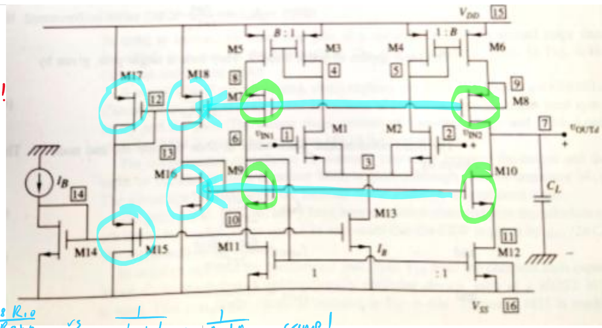
with

$$g_{OUT8} = \frac{g_{ds8} g_{ds6}}{g_{m8}}$$

cascode current mirror Rout equations!

FIGURE 6-47 Cascode symmetrical CMOS OTA (n-well).





and

$$g_{OUT10} = \frac{g_{ds10} g_{ds11}}{g_{m10} + g_{mb10}}$$

The gain A_{v0} is thus given by

$$A_{v0} = g_{m1} R_{OUT} \quad (6\text{-}145)$$

→ as explained above!

try to increase all those gm in denominator to make gout8 and gout10 small

Note that this circuit is realized in an n-well CMOS process. The n-well bulk of pMOST M8 is connected to its source. This is not possible for nMOST M10, however. As a result, g_{mb10} appears in the expression of g_{OUT10}. Also, note that both g_{OUT8} and g_{OUT10} can be made very small, yielding a very large output resistance R_{OUT}. This is a direct result of the use of the cascode transistors M8 and M10.

↳ ie, roz all the go in nominator is fixed somehow,

GBW and Phase Margin PM Since there is only one high impedance node, the GBW is simply given by

$$GBW = \frac{B(g_{m1} + g_{mb1})}{2\pi(C_L + C_{n7})} \quad (6\text{-}146)$$

→ dominant pole!

nwell used now but pwell used earlier

which is the same expression for the symmetrical OTA, except for the addition of g_{mb1}. In order to be able to effectively use this value of GBW, the nondominant poles and the phase margin PM must be evaluated.

Nondominant poles occur at all other nodes, i.e., at nodes 4, 5, 8, 9, 6, and 11. Nodes 4 and 5 carry signals with the same amplitude but opposite phase. Therefore, nodes 4 and 5 form one single nondominant pole f_{nd5} (see App. 6-1), given by

$$f_{nd5} \approx \frac{g_{m4}}{2\pi C_{n5}} \quad (6\text{-}147)$$

→ $R = \frac{1}{g_m}$

The same applies to nodes 8 and 9. They form a single pole, given by

$$f_{nd9} \approx \frac{g_{m8}}{2\pi C_{n9}} \quad (6\text{-}148)$$

→ roz gate voltage of M8 is fixed. and, ro6 way bigger

The other nondominant poles occur at node 6, node 10, and node 11. They are given by

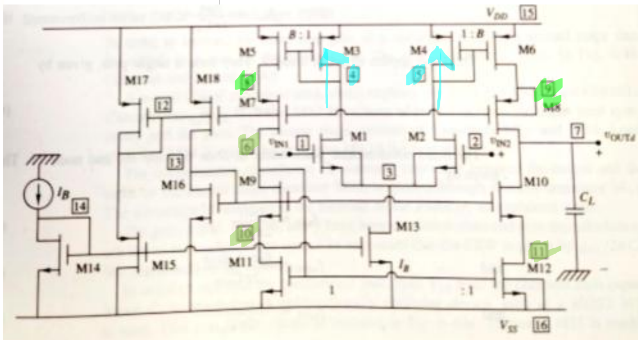
$$f_{nd6} \approx \frac{g_{m11}}{2\pi C_{n6}} \quad (6\text{-}149)$$

and

$$f_{nd10} \approx \frac{g_{m9} + g_{mb9}}{2\pi C_{n10}}(1 + G_{11}) \quad (6\text{-}150)$$

and

$$f_{nd11} \approx \frac{g_{m10} + g_{mb10}}{2\pi C_{n11}} \quad (6\text{-}151)$$



in which G_1 is the loopgain (at high frequencies) around transistor T11. As a result, the phase shift due to f_{nd10} is the smaller one and can be neglected.

All three poles act on only half of the output signal. All three generate a zero at double the frequency (see App. 6-1), and therefore their contribution to the phase margin can be made negligible.

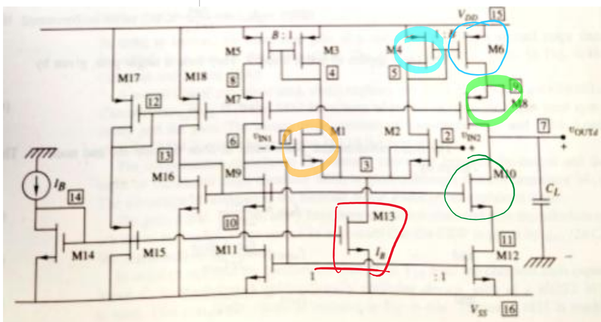
We can conclude that the phase margin PM is determined mainly by poles f_{nd5} and f_{nd9}.

Design Plan The design is very similar to the design for the symmetrical OTA, and is carried out in two steps. First, the GBW is determined at the output node. Second, the phase margin is determined mainly by the nondominant poles on nodes 5 and 9. The sizes of the transistors $(W/L)_4$ and $(W/L)_8$ must be such that the phase margin is sufficiently large.

As a result, we have six variables; namely I_B, $(W/L)_1$, $(W/L)_4$, $(W/L)_6$, $(W/L)_8$ and $(W/L)_{10}$, to satisfy the four specifications GBW, PM, A_{v0}, and $R_{..}$ provided C_L is given. Obviously, we have more variables than constraints. We can now choose other $(V_{GS} - V_T)$ values. We can also involve the slew rate, the noise, and a few other specifications.

We will not calculate the values for slew rate and noise, as they are exactly the same values obtained for the symmetrical OTA (see Sec. 6-7-1). The cascode transistors should not contribute to the noise, assuming they are properly designed (see Sec. 4-5-4).

Such a cascode symmetrical CMOS OTA has been realized. Its essential features are discussed in Sec. 6-9-1 and its dimensions are presented in App. 6-2.



6-7-3 Symmetrical Miller CMOS OTA With High PSRR

(not used this time, but considerable in the future!)

In order to increase the open-loop gain of a symmetrical OTA, a second stage can be added, as it was for the Miller OTA. The new schematic is given in Fig. 6-48 (Steyaert and Sansen 1990).

A p-well CMOS process is used, which explains why the input devices are nMOSTs. Cascode transistors M11 and M12 have been added to increase the input load symmetry and the gain. The second stage consists of transistors M13 and M14. Load transistor M14 is driven by transistor M3 of the first stage.

The compensation capacitance C_c normally connected between the output and the input of the second stage transistor M13, is guided through cascode transistor M11. The advantage of doing so is the increase of the $PSRR_{SS}$, as explained next.

The gain, GBW, PM, SR, and y have been discussed often and thus the calculations are left to the reader. There cannot be any doubt that the GBW is given by $g_{m1}/2\pi C_c$. We now focus on the $PSRR_{SS}$.

In order to suppress the feedforward path from V_{SS} over the compensation capacitance C_c to the output, a unidirectionally operating device, such as a MOST M11 is used. That part of the circuit is repeated in Fig. 6-49a. Transistor M11 is readily

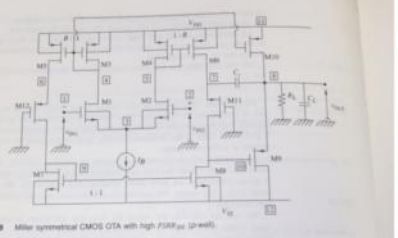


FIGURE 6-48 Miller symmetrical CMOS OTA with high $PSRR_{SS}$ (p-well).

recognized. Its biasing is left out, but it must ensure that the MOST always operates in saturation. The parasitic capacitance from the gate of M13 to V_{SS} is denoted by C_{n1SS}.

For analysis, the transistor is substituted by its small-signal equivalent circuit, shown in Fig. 6-49b. Note that the parasitic capacitance to ground C_p at the drain of the MOST cannot be neglected.

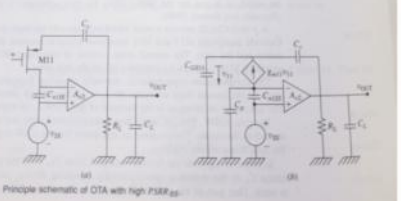


FIGURE 6-49 Principle schematic of OTA with high $PSRR_{SS}$.

Straightforward analysis of this circuit yields

$$\frac{v_{out}}{v_{SS}} = \frac{C_p}{C_c}\left(1 + j\frac{f}{f_{11}}\right) \tag{6-152}$$

with

$$f_{11} = \frac{g_{m11}}{2\pi(C_c + C_{GS11})}$$

if

$$A_{v2} > \frac{C_{n1SS} + C_p}{C_c}\left(1 + j\frac{f}{f_{11}}\right)$$

which is normally no problem.

For a large f_{11}, g_{m11} must also be large, but then C_p increases as well. Let us take for M11 a transistor that is equal in size to M1. In this case, $f_{11} \approx GBW$. If $C_{1nSS} = 0.2$ pF, and $C_p = 0.1$ pF, then the gain v_{OUT}/v_{SS} is 0.1, or -20 dB. This condition is easy to fulfill if $A_{v2} > 0.3$, which should not present a problem.

The high frequency $PSRR_{SS.GBW}$ is then given by

$$PSRR_{SS.GBW} = \frac{C_c}{C_p} \tag{6-153}$$

which is 10 if $C_c = 1$ pF and $C_p = 0.1$ pF. In comparison with unity for the Miller CMOS OTA, a factor of 10 has been gained by insertion of transistor M11. While it is always better to add the transistor, an extra node is added to the circuit, and this means that extra calculations will be necessary for the phase margin.

Such a symmetrical Miller CMOS OTA has been realized. Its features are discussed in Sec. 6-9-1 and its dimensions and characteristics are given in App. 6-2.