Comparative study on low-power high-performance flip-flops

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Reg. nr.: LiTH-ISY-EX-3432-2003

Linköping 2003

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Master Thesis
Division of Electronic Devices
Department of Electrical Engineering
Linköping University

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Reg. nr: LiTH-ISY-EX-3432-2003

Titel
Title

Jämförande studie av högpreserande lågeffektsvippor

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Sammanfattning
Abstract
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Nyckelord
Keyword
flip flops, latches, low power, standard cell, cell library, energy delay space

Abstract

This thesis explores the energy-delay space of eight widely referred flip-flops in a 0.13µm CMOS technology. The main goal has been to find the smallest set of flip-flop topologies to be included in a "high performance" flip-flop cell library covering a wide range of power-performance targets. Based on the comparison results, transmission gate-based flip-flops show the best power-performance trade-offs with a total delay (clock-to-output + setup time) down to 105ps. For higher performance, the pulse-triggered flip-flops are the fastest (80ps) alternatives suitable to be included in a flip-flop cell library. However, pulse-triggered flip-flops consume significantly larger power (about 2.5x) compared to other fast but fully dynamic flip-flops such as TSPC and dynamic TG-based flip-flops.

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Chapter 1

1. Introduction

Over the past decade, power consumption of VLSI chips has constantly been increasing. Moore's Law drives VLSI technology to continuous increases in transistor densities and higher clock frequencies. The trends in VLSI technology scaling in the last few years show that the number of on-chip transistors increase about 40% every year. And operation frequency of VLSI systems increases about 30% every year. Although capacitances and supply voltages scale down meanwhile, power consumption of the VLSI chips is increasing continuously. On the other hand, cooling systems can not improve as fast as the power consumption increases. Therefore in the very close future chips are expected to have limitations of cooling system and solving this problem will be expensive and inefficient.

For high performance VLSI chip-design, the choice of the back-end methodology has a significant impact on the design time and the design cost. Making every single gate from scratch is not necessarily the best method. Instead, a sufficient set of pre-designed standard cells can be utilized as building blocks to design most of the functional blocks. Semiconductor manufacturers offer standard cell libraries, which are also supported by CAD tools in automated design flows including the final physical auto-placement and routing. However, the selection of the standard cells as well as their performance is often limited. Despite the performance limitations, standard cell libraries could be useful even in design of high performance VLSI chips. Often, only a smaller portion of the chips include performance-critical units, and the rest of the design could be maximally automated to reduce the design time

without degrading the targeted performance. In addition, the concept of cell library can be extended to even support the full-custom part of the chip. Custom (in house) cell libraries can be made and shared by the designers of the performance critical units. This results in a sharp decrease in the number of cells to be created and verified reducing the total chip layout time significantly. Hence, development of an efficient cell library for high performance chips is essential.

A cell library includes a number of cells with different functionalities, where each cell may be available in several sizes and with different driving capability. Two central categories of cells included in cell libraries are flip-flops and latches. These are extremely important circuit elements in any synchronous VLSI chip. They are not only responsible for correct timing, functionality, and performance of the chips, but also their clocked devices consume a significant portion of the total active power. Based on the comparison of the power breakdown for different elements in VLSI chips, latches and flip-flops are the major source of the power consumption in synchronous systems. Latches and flip-flops have a direct impact on power consumption and speed of VLSI systems. Therefore study on low-power and high performance latches and flip-flops is inevitable.

A universal flip-flop with the best performance, lowest power consumption, and highest robustness against noise would be an ideal component to be included in cell libraries. However, it will be shown in this thesis, that increasing the performance of flip-flops generally involves significant power and robustness trade-offs. Therefore, a set of different latches and flip-flops with different performances are essential to limit the use of more power consuming and noise-sensitive elements only for smaller portion of the chips with performance-critical units. This eliminates global and unnecessary increase in power consumption as well as robustness degradations, which would result in overall decrease in noise margin requiring extra careful and time consuming design.

The goal of this work is to find a small set (ideally the smallest set) of flip-flop topologies to be included in a library covering a wide range of power-performance targets. Our strategy has been to first explore the capabilities of conventional and simpler transmission-gate (TG) based flip-flop topologies, before including other types of flip-flops.

Among a large number of flip-flops that have been proposed in the past [1-7], we have selected some of the widely used and/or referred topologies. Section 2 shows eight flip-flops we have incorporated in our initial benchmark including static and dynamic edge-triggered mater-slave as well as semi-dynamic pulsed flip-flops.

In contrast to many previously published results [5], [7], a wide power-performance space for each of the eight flip-flops has been explored. By sizing, useful operating ranges of the flip-flops have been identified. The design-space exploration not only enables a true comparison, but also it reveals potentially large overlaps in operating

range of the flip-flops. This in turn provides an opportunity to reduce the number of different circuit topologies in a flip-flop library.

The factors which are desirable in latches and flip-flops are as follows:

- High speed
- Low power consumption
- Robustness and noise stability
- Small area and less number of transistors
- Supply voltage scalability
- Low glitch probability
- Large internal race immunity
- Insensitivity to clock edge
- Insensitivity to process variables
- Less internal activity when data activity is low

According to the requirements of the system, the designer has to consider all these parameters while choosing a structure for flip-flops. What makes this decision even harder is that usually most of these parameters are not independent from each other. Trade-offs between desired parameters, make this decision a multi-dimensional optimization problem for high-performance systems. A multi-dimensional optimization problem for a non-linear system that usually has hundreds of variables, is unfortunately impossible to solve within the limited design time.

The idea for this thesis is to explore the energy-delay space for different structure of flip-flops. This will give us a good understanding of different structures and make the decisions easier for the designers.

1.1 Flip-flops and Latches

Building a sequential machine requires memory elements which read a value, save it for some time and then write that stored value somewhere else even if the element's input value has subsequently changed. A Boolean logic gate can compute values, but its output value will change shortly after its input changes. Each alternative circuit used as a memory element has its own advantages and disadvantages.

A generic memory element has as internal memory and some circuitry to control access to the internal memory. Access to the internal memory is controlled by the *clock* input. The memory element reads its *data* input value when instructed by the *clock* and stores that value in its memory. The output reflects the stored value, probably after some delay. In CMOS circuits the memory is formed in two ways. The first approach uses positive feedback or regeneration. Here, one or more output signals are intentionally connected back to the inputs. This results in a class of elements called multivibrator circuits. The second approach to build memory

function in circuits is to use charge storage as a means to store signal values. This approach, which is very popular in MOS world, requires regular refreshing as charge tends to leak away with time.

Memory elements differ in many key respects:

- Exactly what form of clock signal causes the input data value to be read
- How the behavior of data around the read signal from clock affects the stored value
- When the stored value is presented to the output
- Whether there is ever a combinational path from the input to the output

Introducing a terminology for memory elements requires caution. Many terms are used in slightly or grossly different ways by different people. However, in this thesis Dietmeyer's convention is chosen, dividing memory elements into two major types[1]:

- **Latches** are transparent while the internal memory is being set from the data input and the possible changes of the input value can be transmitted to the output.
- **Flip-flops** are not transparent; reading the input value and changing the flip-flop's output are two separate events.

Figure 1 illustrates the differences at the output of a positive-edge-triggered flip-flop and an active-high latch. As it can be seen in this figure, possible changes of input can be seen at the output of the latch while it is transparent. Within the flip-flop and latch classification many subclasses exist. Some of these classifications will be discussed in section 1.5.
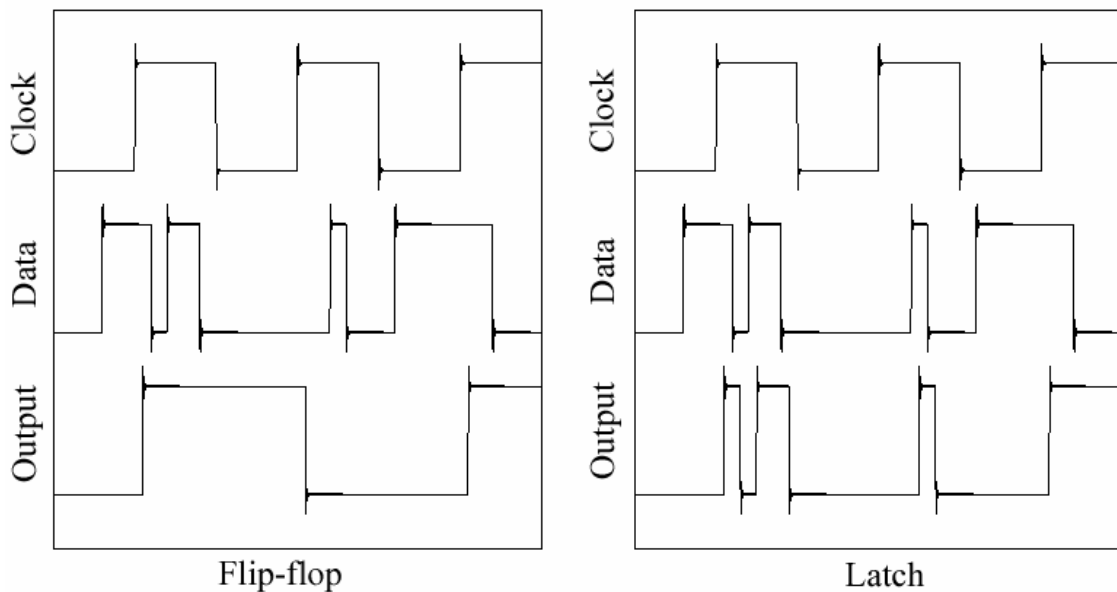
Figure 1 -Positive-edge-triggered flip-flops and active-high latches

Transparent nature of the latches can cause some severe problems. Consider the simple circuit of figure 2. As long as the clock is high (assuming that the latch is active or open when clock signal is high) the output of the latch oscillates back and forth between the 0 and 1 states. This phenomenon is called a race condition and can only be avoided by making the pulse width of the clock smaller than the propagation delay of the loop. Since the loop delay in this example is small and probably smaller than the pulse width, this situation has a major chance of occurring. The result of this repetitive toggling is that the output is undetermined when the clock goes low. One way to avoid a race is to exploit a flip-flop instead of the latch.
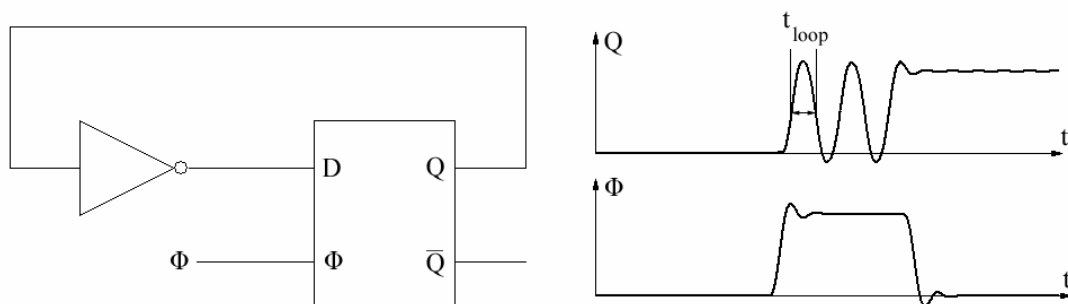
Figure 2 -Race problem in latch based designs (during transparency period)

1.2 Timing and delay definitions for flip-flops

The performance of a flip-flop is qualified by three important timings and delays: propagation delay (Clock-to-Output), setup time and hold time. They reflect in the system level performance of the flip-flops. Setup time and hold time define the relationship between the clock and input data. (Figure 3)

1.2.1. Propagation delay

Propagation delay (Clock-to-Output) is the time delay after arrival of clock's active edge that output is considered stable. Clock-to-Output equals the time it takes for the output to change after the occurrence of the clock edge.
Usually propagation delay differs for low-high transitions and high-low transitions. So propagation delay of the flip-flop is by definition maximum value of these two delays:

$$t_{Clock-to-Output} = \max(t_{Clock-to-Output_{LH}}, t_{Clock-to-Output_{HL}})$$
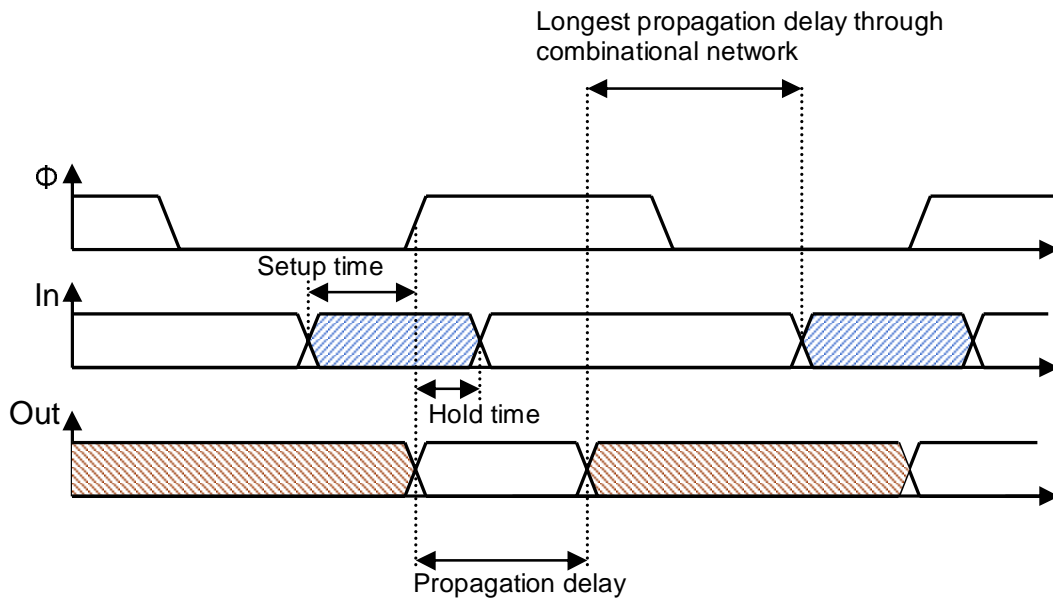
Figure 3 -Timing definitions

1.2.2. Setup time

In order to function correctly, the edge-triggered flip-flop requires the input to be stable some time before the clock's active edge. This period is called the setup time of the flip-flop. The data value must remain stable around the time clock signal changes value to ensure that the flip-flop retains the proper value.

As setup time may differ for low-high transitions and high-low transitions, setup time is by definition maximum of the values obtained for low-high and high-low transitions:

$$t_{setup} = \max(t_{setup_{LH}}, t_{setup_{HL}})$$

1.2.3. Hold time

Flip-flop design requires the state of the input to be held for some time after the clock edge. The time after the clock edge that the input has to remain stable is called the hold time. Basically hold time can be negative meaning that data can be changed even before clock edge and still previous value will be stored. Hold time is by definition maximum of the values obtained for low-high and high-low transitions:

$$t_{hold} = \max(t_{hold_{LH}}, t_{hold_{HL}})$$

The definitions of setup times, hold times and propagation delays are illustrated in the timing diagram of figure 3. In these definitions, propagation delay, setup time and hold time are considered as independent variables. However what happens in reality shows that these parameters are not independent from each other, figure 4. For instance, propagation delay is strongly related to the data arrival time. As it is illustrated in figure 4 and 5, propagation delay expands as data arrives later. When data arrival time is very close to clock edge, the Clock-to-Output delay increases drastically. In this case flip-flop is very close to function incorrectly or to enter an unstable operation point called metastability. There are several approaches for setup-time definition that have been used in literature:

- Setup-time is the time period before clock edge which causes 5% increase in Clock-to-Output. This definition is illustrated in figure 5 [5].

- Setup-time is the time period before clock edge which minimizes the total delay imposed by flip-flop to the system. As it is discussed in section 1.3 total delay of flip-flop is usually considered as sum of propagation delay and setup time. [7]
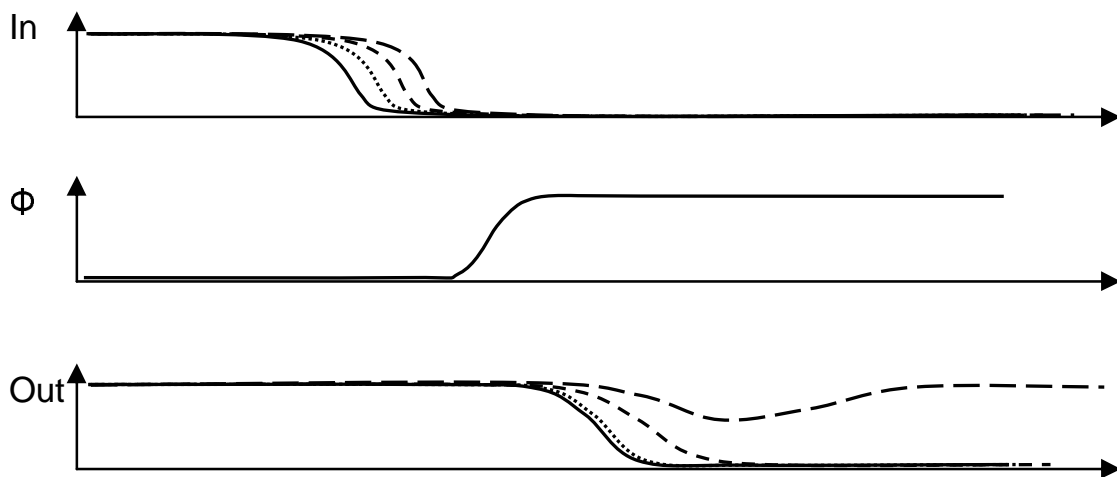
Figure 4 -Timing definitions, What happens in reality
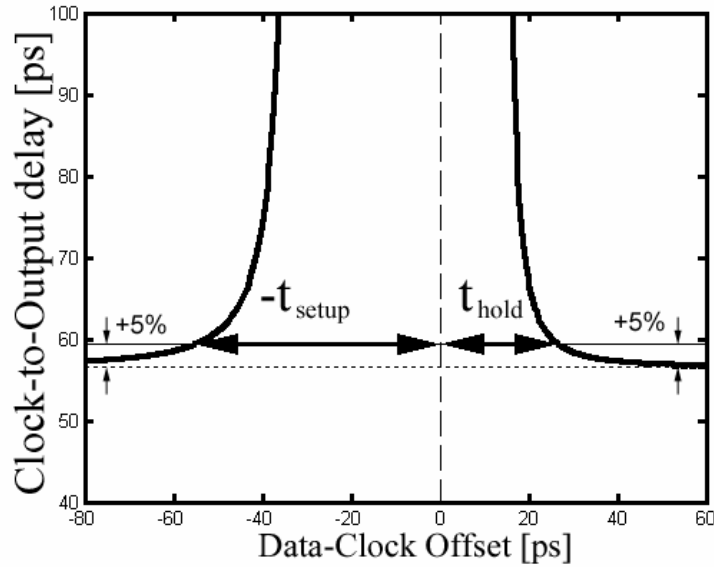
Figure 5 -Clock-to-Output versus data arrival time

In this thesis the first approach (5% increase in propagation delay) will be used for the simulations and measurements.

1.3 Correct operation of flip-flops within the digital environment

The flip-flop environment in digital systems, figure 6, has to satisfy two conditions for correct operation.
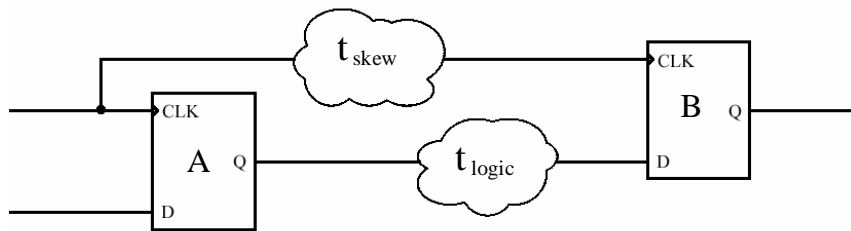
Figure 6 -Flip-flops at the logic boundaries

- The clock period must be greater or equal to the sum of worst case propagation delay of the flip-flop A, flip-flop setup-time B, maximum combinational logic delay, and relative clock skew between two series flip-flops' clock signal.

$$T_{clk} \geq t_{Clock-to-Output\,max} + t_{setup} + t_{Logic} + t_{skew}$$

8

According to the definition for the setup time, maximum propagation delay of the flip-flop is 5% more than the propagation delay of the flip-flop when data arrives much earlier than clock edge.

$$T_{clk} \geq 1.05 t_{Clock-to-Output} + t_{setup} + t_{Logic} + t_{skew}$$

- To avoid internal race in the system, the worst race conditions are considered. The worst case happens when there is no logic between two series flip-flops. Minimum propagation delay of the flip-flop must be greater or equal to the sum of flip-flop's hold time and relative clock skew between two flip-flops' clock.

$$t_{Clock-to-Output} \geq t_{hold} + t_{skew}$$

1.4 Failure mechanisms in flip-flops

1.4.1 Race-through

This failure which was mentioned in section 1.1 can also appear for edge triggered flip-flops built using a pair of latches driven on opposite clock phases [21]. Consider the model of an edge-triggered flip-flop shown in figure 7. Ideally the flip-flop should exhibit the setup and hold times of its master latch with respect to the rising edge of *clk*, and should cause data to appear on the output with the delay times of the slave latch with respect to the same *clk* edge. The latch is supposed to hold the value sampled on the rising clock edge until the next rising clock edge. It will do so, however, only if the delay time of the master latch is greater than the hold time of the slave. If this condition is not met, data will race-through to output, changing it on the inactive clock edge. This condition must be guaranteed solely by correct construction of the flip-flop and is independent of external parameters. The flip-flop can fail in a more subtle way. If setup time of the master latch is small and propagation delay of the master latch is large, then the behavior of the Output may no longer be governed solely by the properties of the slave latch. Data can race-through both latches on the active clock edge and may even cause multiple transitions on the Output. This undesirable behavior of the flip-flop can be avoided by assuming larger setup time for the flip-flop (larger than master latch's setup time), at the cost of increased cycle time.

t_{sM} : Master latch's setup-time

t_{hM} : Master latch's hold-time

t_{cCQM} : Master latch's contamination time
at Q after Clock edge

t_{dDQM} : Master latch's delay time
at Q after data changes

t_{cCQS} and t_{dCQS} : Slave latch's contamination
and delay time at Q after Clock edge

t_{hS} : Slave latch's hold-time
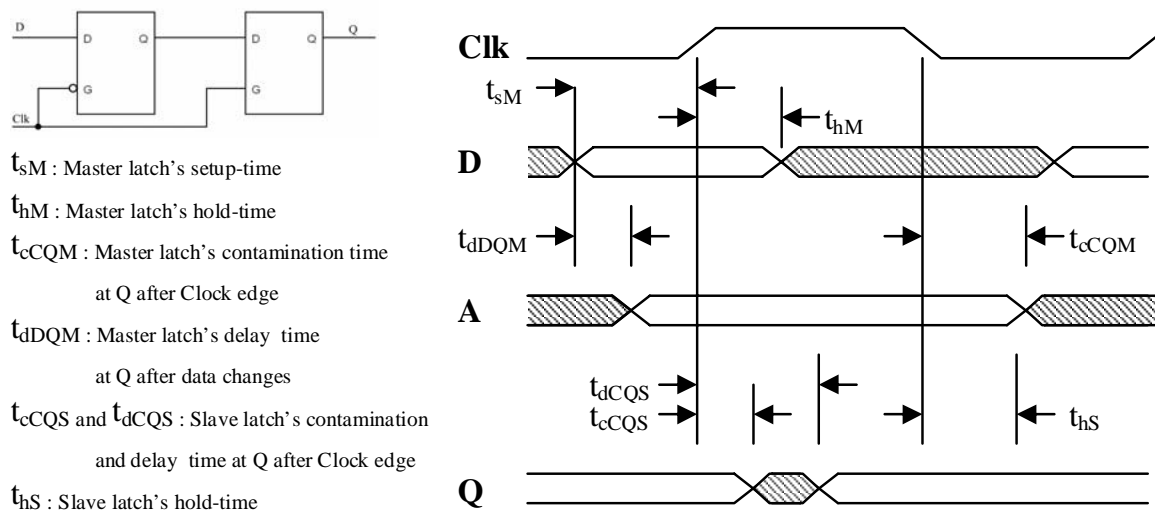
Figure 7 -Internal timing in a master-slave flip-flop

1.4.2   Dynamic node discharge

The storage capacitances of the dynamic latches and flip-flops must be periodically refreshed, otherwise the charge on these nodes will leak away by leakage currents, resulting invalid data [21]. A common situation is shown in figure 8. A "1" stored on the input capacitance of the pass-gate latch will eventually leak low because of the reverse leakage current of the N+/P junction (drain-bulk of NMOS).
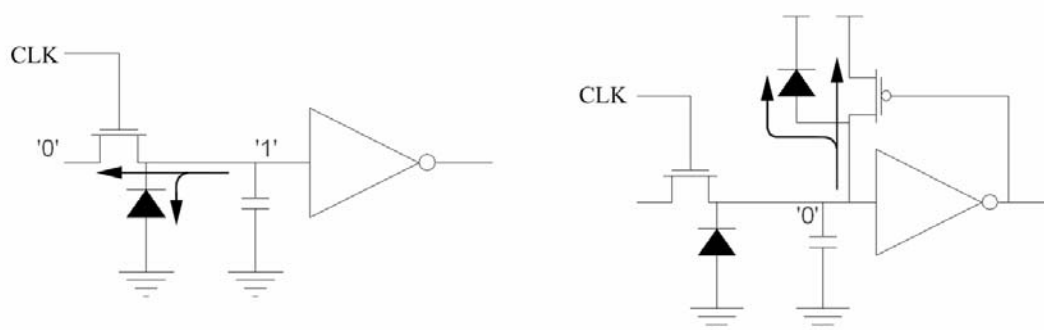
Figure 8 -Loss of data in dynamic latches

1.4.3   Power supply noise

Dynamic storage suffers from another potential problem illustrated in figure 9 [21]. In this case input signal D makes a transition while clock signal is high changing internal node X to high and pulling output Q low. Meanwhile clock signal goes low and D returns to high, leaving X storing its high dynamically, as indicated as dashed line. If a noise spike arrives on supply voltage VDD while X is floating and if this spike is greater than PMOS's threshold voltage this transistor will turn on and pull Q high causing an erroneous result.
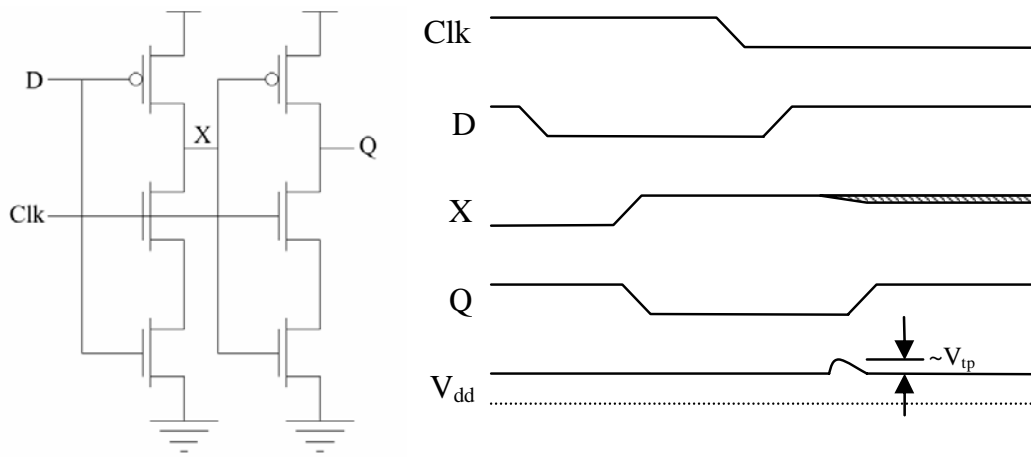
Figure 9 - Erroneous output due to power supply noise

1.4.4   Clock slope

Degraded clock waveform may cause failure in flip-flops [21]. Basically the flip-flop fails if the slow clock edge extends the master latch's propagation delay beyond the slave's hold time, as shown in figure 10.
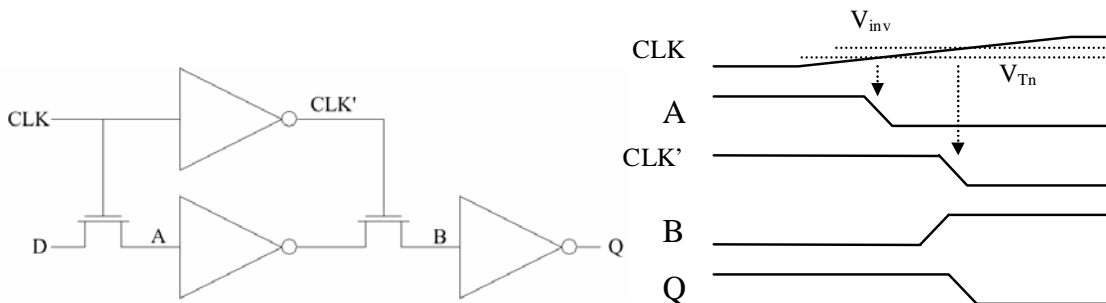
Figure 10 - An example of clock-slope failure

1.4.5   Charge sharing

Charge sharing is perhaps the best known cause of failure in dynamic flip-flops and latches. This phenomenon occurs when two capacitors at different voltages become connected, for example, by turning on a transistor. Charge sharing can cause an unexpected behavior in dynamic circuits [20].

1.5 Classifications of flip-flops

Within the name of Flip-flops, many subclasses exist. These classifications are mostly based on the behavior of clock signal and input signal and flip-flop's output. In this section some of these classifications will be discussed.

1.5.1   Master-Slave and Pulse triggered latch

As discussed in section 1.1 latches are transparent while the clock level is active and any change at the input is reflected at the output after a nominal delay. Data is accepted continuously until the clock goes inactive and latch closes. One way to avoid the race situation discussed in section 1.1 is to use flip-flops instead of latches in the system. A flip-flop can be designed as a latch pair in series which work in different phases of clock. One of the latches is transparent high and the other one is transparent low. This structure is called master-slave flip-flop as shown in figure 11. Ideally, master latch gives the flip-flop's setup time and slave latch gives the propagation delay of the flip-flop. However, to avoid failures like race-trough in flip-flops, the setup time of the flip-flop is greater than the master latch's setup time.
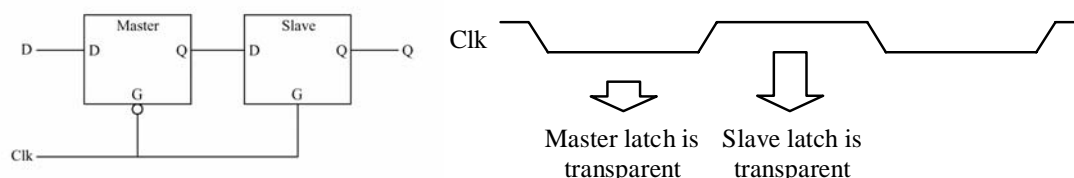
Figure 11 - Master-slave flip-flops

Another alternative for flip-flop structure is to use a pulse triggered latch. The idea is using very sharp pulses as clock signal of the latch, so that this latch can be seen as a flip-flop and transparency of the latch is only for a very short time which can be considered forbidden time interval. Input data is supposed to be stabled during the forbidden time interval. A pulse triggered latch is also a two stage flip-flop where the first stage is a pulse generator and the second stage is a latch. The needed sharp pulse is usually constructed using clock signal combined with the delayed clock signal. Figure 12 shows an overview of a pulse triggered latch. In the shown waveform stable data/output is shown with black color.
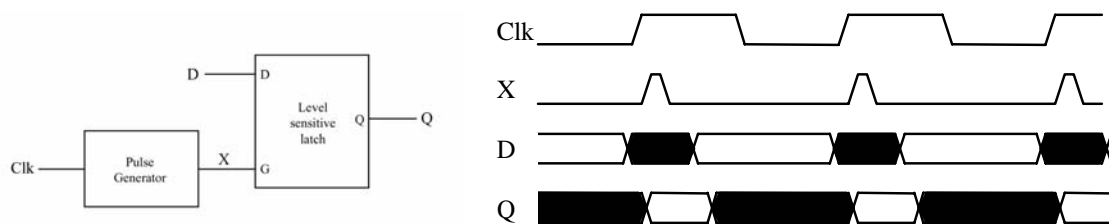
Figure 12 - Pulse triggered latch

1.5.2   Dynamic and Static

Static flip-flops are a group of flip-flops that can preserve their stored value even if the clock is stopped. In contrast, in dynamic flip-flops the stored value will be destroyed if it is not refreshed for a while (figure 13). Basically dynamic flip-flops can achieve higher speed and lower power consumption. However this family of flip-flops suffers from serious potential failures. Storage loss because of leakage currents, power supply noise and etc. are possible in dynamic flip-flops and must be considered by the designers.

As discussed briefly in section 1.4.2 discharge of dynamic nodes is because of reverse leakage current in NP junctions and subthreshold leakage in MOS transistors.

Subthreshold leakage varies exponentially with gate-source voltage in pass-gate transistors. Even a few tenths of a volt between gate and source, caused by for example noise or power supply network voltage drops, can give rise to large subthreshold currents. Even if the gate-source voltage is held exactly at 0, subthreshold leakage will cause loss of dynamic data. At high die temperatures commonly encountered in chip operation, junction leakage can become comparable to subthreshold leakage. Junction leakage usually sets the maximum time a dynamically stored value can be retained. NP junction leakage currents are usually

modeled by considering area and perimeter of the diffusion terminal separately. For modern processes, currents are in the range of a few fA/µm² for the area leakage and a few fA/µm for the perimeter at room temperature. Leakage current increases by roughly a factor of two for each 10ºC temperature increase; therefore it is two orders of magnitude higher for typical junction operation temperature.

Static latch   Dynamic latch
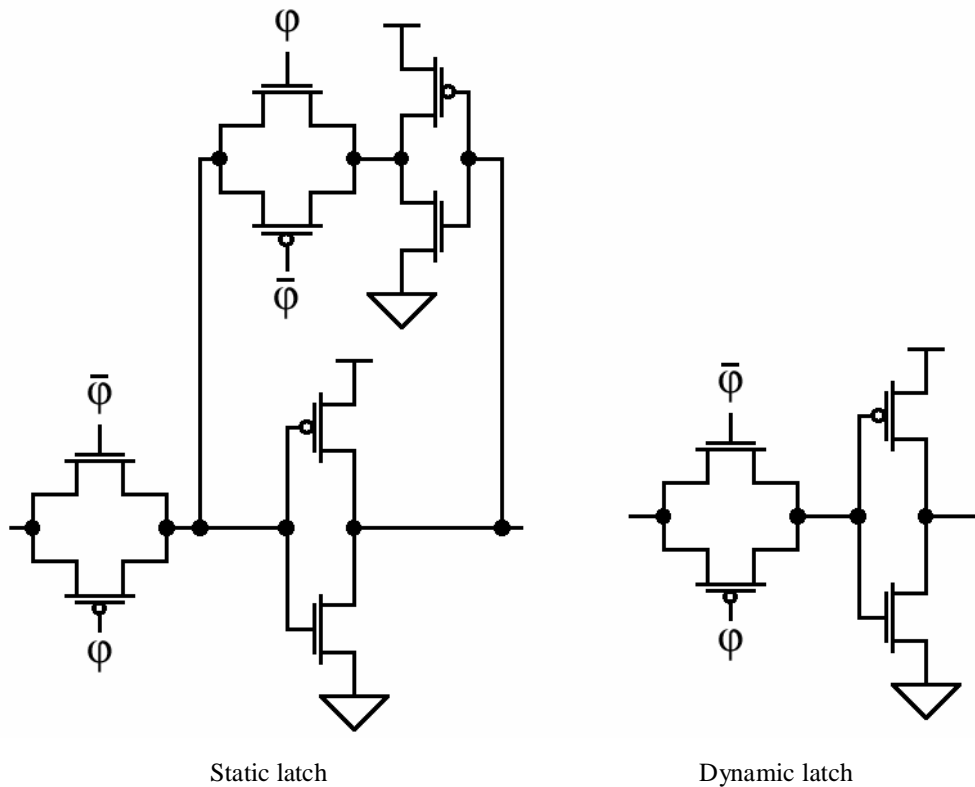
Figure 13 - Static and dynamic latch

Millisecond storage retention time is usually not a problem when chip is operating normally; However when chip is in testing mode it becomes a serious problem. In many modern testing modes are inevitable. For example if I_{DDQ} tests (measurements of quiescent power supply current of the chip) are required for a chip, it requires stopping the clocks (all the activities) in the system, which will be problematic for systems containing dynamic flip-flops [19].

The dynamic charge decay can become much more serious than a loss of correct logic values. As charge leaks in a dynamic node, the voltage on CMOS input after this node gradually changes. So for a considerable time the input voltage of the gate after dynamic node can be in forbidden region where NMOS and PMOS transistor are both on. This will consume considerable static current which in some cases can cause damages in the chip.

Most of the dynamic flip-flops can be converted to static flip-flops using keepers for the dynamic nodes.

1.5.3   Single clock phase flip-flop and multi-clock phase flip-flop

Another classification for flip-flops is according to the needed clock phases. As discussed previously in master-slave flip-flops two latches are used in series which work in different clock phases. So naturally two clock phases are needed for master-slave flip-flops if master and slave latches have similar structures. However in some cases changing the structure of the two latches can reduce the number of needed clocks to only one.

True Single Phase Clock (TSPC) flip-flops can usually be operating at higher speeds than two clock phase flip-flops [12], [15], [18]. Because of the skew time between two phases of the clock will add up to the delay of the two clock phase flip-flops, degrading the performance of these flip-flops.

1.5.4   Single-edge-triggered flip-flop and double-edge-trigger flip-flop

In some systems double-edge-triggered flip-flops are required. Unlike single-edge-triggered flip-flops, they capture data on both edges of a clock. A block diagram of a double-edge-triggered flip-flop is shown in figure 14. A positive and a negative edge-triggered flip-flop both sample the D input, and the appropriate flip-flop is selected for the output by a clocked multiplexer.
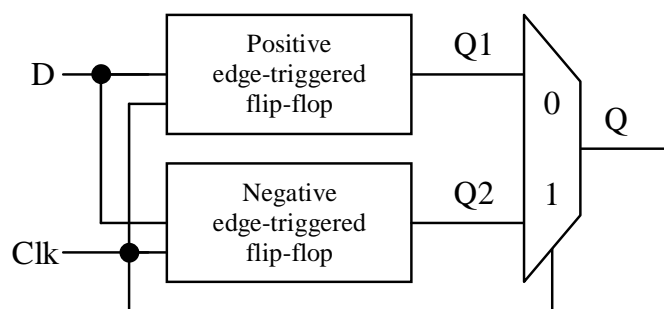
Figure 14 - Double-edge-triggered flip-flops

Double-edge triggered flip-flops can be beneficial for low-power systems [16]. In general they result in a more efficient system because every power-dissipating clock

edge is used to advantage. Master-slave flip-flops are shown to perform slightly better in double-edge-triggered mode than their single-edge-triggered counterparts. However this strategy requires careful control of the clock's duty cycle to ensure that the combinational logic has adequate time to operate during both the clock high and the clock low cycles.

1.5.5   Single ended flip-flop and differential flip-flop

A single clock phase edge-triggered flip-flop can be built by using differential structures. Generally differential flip-flops require both true and complement inputs and produce both true and complement outputs (figure 15). In cases where true and complement signals are available and they are synchronous differential structure can show better performance than single-ended structures. The performance of differential flip-flops will be degraded if the input signals are not synchronous [3] , [17].
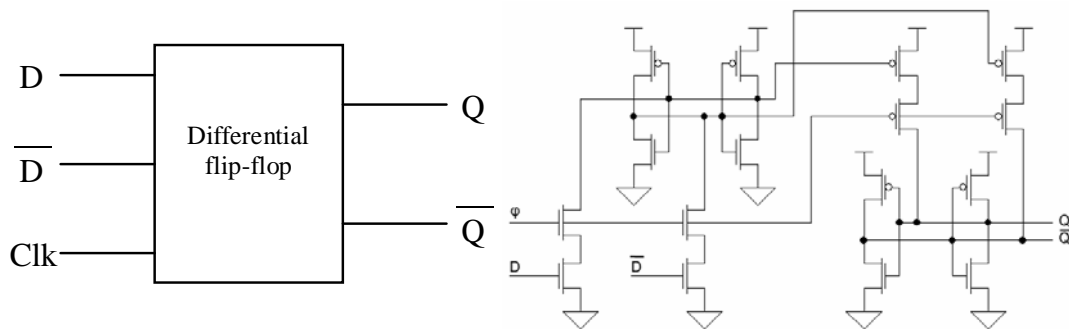
Figure 15 - Differential flip-flops

1.7 Energy metrics

The energy consumed by the flip-flops depends on the input data activity. When the input data activity is changing, the energy consumption will usually vary linearly as it is shown in figure 16.
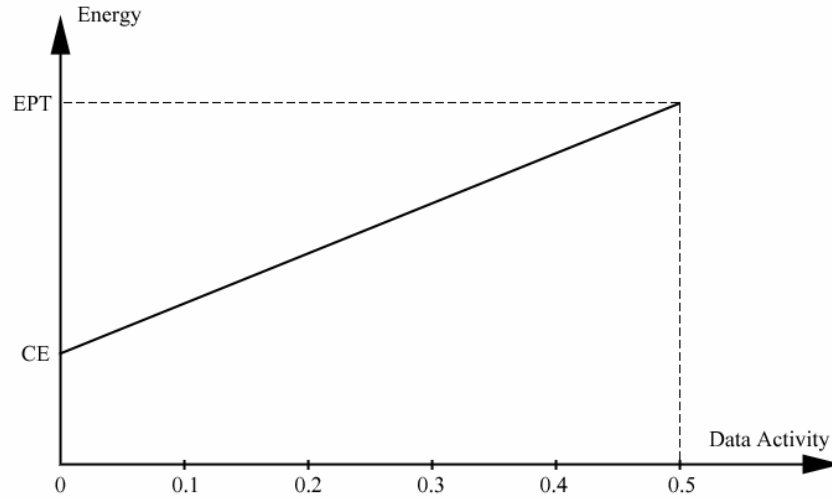
Figure 16 - Energy consumption vs. data activity

Energy-per-transition and clock-energy are two measures that will be used in our simulations. When input data activity is maximum acceptable value, 50% of clock's activity, Energy consumption of the flip-flop will be almost equal to Energy-per-transition. When input data activity is zero the energy consumption will be equal to Clock-energy.

1.7.1 Energy-per-transition

Energy-per-transition metric is defined as the total energy consumed by a flip-flop during one clock cycle while a transition occurs in flip-flop's state:

$$E = \int_{t_0}^{t_0+T} V_{DD} i_{V_{DD}}(\tau)d\tau = V_{DD} \int_{t_0}^{t_0+T} i_{V_{DD}}(\tau)d\tau = V_{DD}\overline{I_{V_{DD}}}$$

1.7.2 Clock-Energy

Clock energy is defined as the total energy consumed by a flip-flop during one clock cycle when the data activity is zero and flip-flop's state is preserved constant. Clock-energy for zero-state and one-state can be different. Therefore for more accurate calculations the average value of energy consumption for zero-state and one-state is considered.

1.8 Energy-Delay space

A well-known convention for comparing digital circuits is considering both delay and energy consumption. Comparing power-delay product is one of these methods, which is considered as a quality measure for a circuit. Trade-offs between power consumption and delay can be evaluated by this measure.

Plotting energy consumption versus delay can also be a good measure of comparison for digital circuits. Figure 17 shows the energy-delay space for 9T TSPC flip-flop. The star shaped points are optimal points of operation for this flip-flop. Other points are not optimum because there is another point with less energy or less delay among the measurements. An estimated curve for the optimum points is drawn in figure 17.
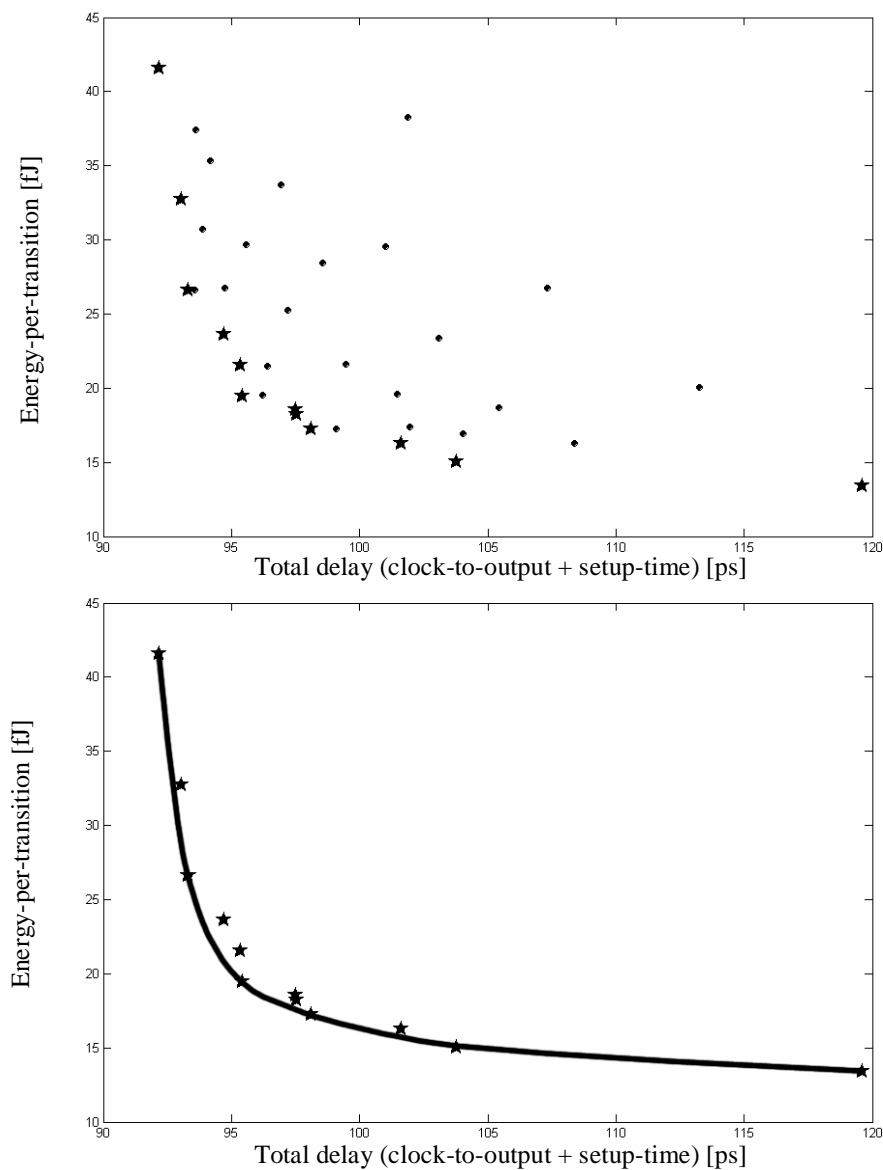
Figure 17 - Energy-delay space for 9T TSPC flip-flop

Chapter 2

2. Flip-flop topologies

As was described in section 1, many flip-flop topologies have been proposed in the past. For our comparative study, some of widely used and/or referred topologies in our initial benchmark have been selected. Four static master-slave flip-flops are included in our test bench. Figure 18 shows the classic transmission-gate based flip-flop (TGMS) [3]. Figure 21 shows second topology, which is a modified clocked inverter (mC²MOS) [9], where the dynamic master-slave C²MOS flip-flop is modified to a pseudo-static C²MOS flip-flop by adding a C²MOS feedback at the outputs. Another variation of TGMS is the flip-flop shown in figure 22, which is derived from PowerPC 603 master slave flip-flop [8]. In PowerPC 603 the interrupting feedback in the storage elements is based on C²MOS inverters. Fourth master-slave flip-flop (figure 27) is based on the traditional SR-latch build by cross coupled NAND/NOR gates [3], [6].

The next two flip-flops (figures 25, 26) are pulse-triggered latches. They are based on a single latch, which is transparent within a short time (during a pulse) on the edge of the clock. Figure 25 shows a hybrid-latch flip-flop element (HLFF) [10], and figure 26 shows a semi-dynamic flip-flop (SDFF) [11]. Both of the pulse-triggered topologies require and include pulse generators.

Further, there are two fully dynamic flip-flops in our benchmark; the TSPC flip-flop [12] in figure 23 and the dynamic transmission gate flip-flop [3], [4] in figure 19. These fast flip-flops (with floating nodes) are extra sensitive to noise and leakage currents. However, we have included their performance level as a reference to evaluate other flip-flops. Eight different structures for the flip-flops are chosen for

comparison. These structures are widely used in different applications and standard-cell libraries.

2.1 Transmission-gate latch based master-slave flip-flop (TGMS)
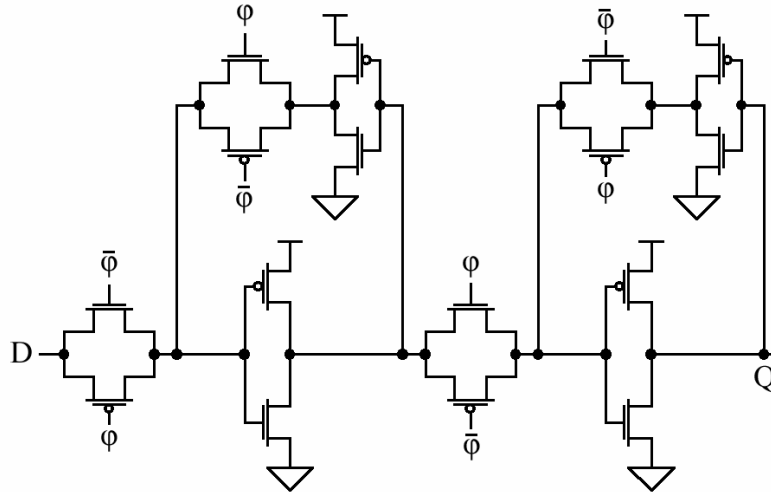
Figure 18 - Transmission gate flip-flop (TGMS)

This flip-flop is realized by using two transmission gate based latches operating on complementary clocks [3], [4], [6]. Several varieties of the transmission gate based are available. For example the feedback transmission gate may be eliminated or even PMOS transistors may be removed for transmission gates. However in our simulations we will only consider typical transmission gate based latch shown in figure 18. Later on dynamic version of this flip-flop will be compared to TSPC structure, figure 19. Although this structure has high-speed and consumes low power, it is sensitive to overlap of the clocks. This flip-flop malfunctions if the clocks overlap for a length of time.
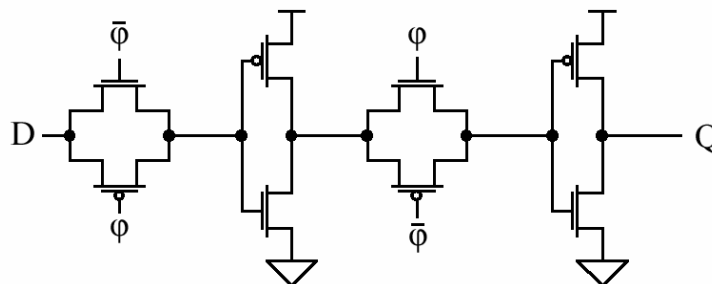
Figure 19 - Dynamic transmission-gate flip-flop (TGMS-dyn)

2.2 Modified C²MOS master-slave flip-flop (mC²MOS)
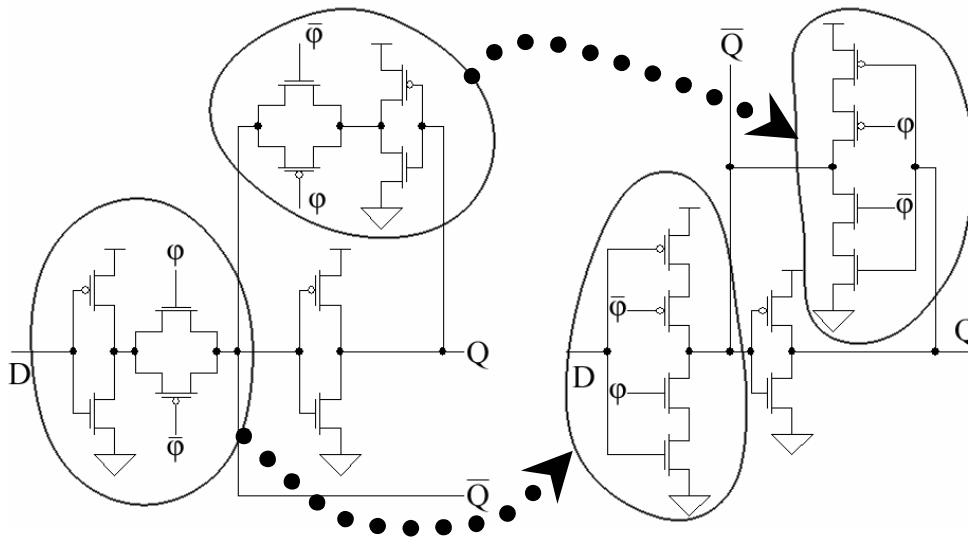
Figure 20 - Transmission gate latch and C²MOS latch

By eliminating the connections at the confluence of the inverter and transmission gate for transmission-gate based latches (figure 20a), the latch in figure 20b may be constructed without loss of functionality. This eliminates a metal connection, resulting in a smaller latch [3], [9]. This structure is called C²MOS latch because of the clocked inverters used in it. Flip-flop constructed using C²MOS latch is shown in figure 21. Unlike transmission gate flip-flop, this structure is insensitive to overlap of the clocks.
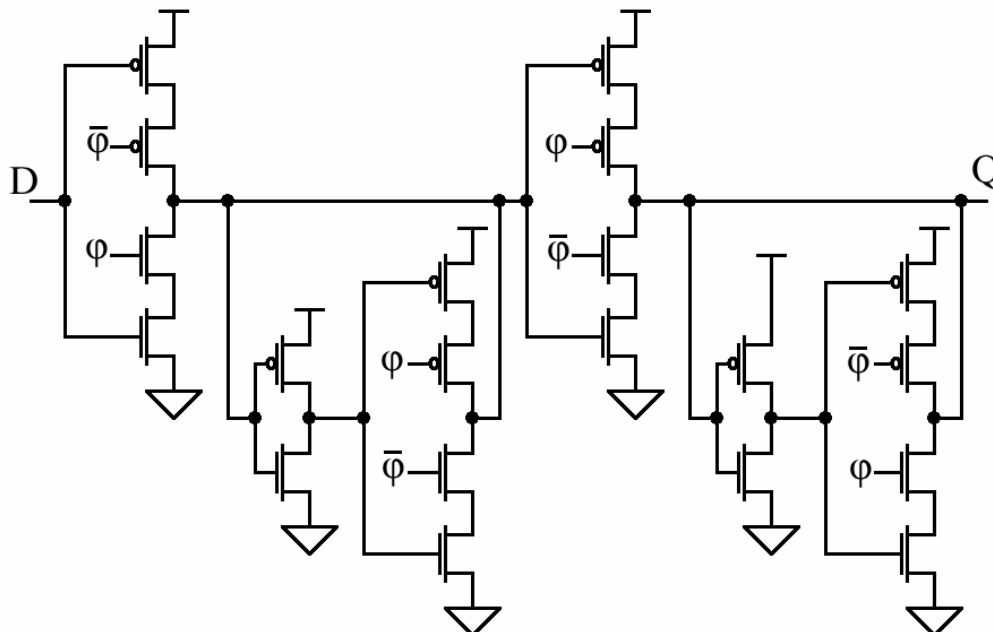
Figure 21 - mC²MOS flip-flop

2.3 PowerPC 603

This structure is a combination of TGMS flip-flop and mC²MOS flip-flop. The feedback transmission gate is changed with a clocked inverter (figure 22) [3], [8].
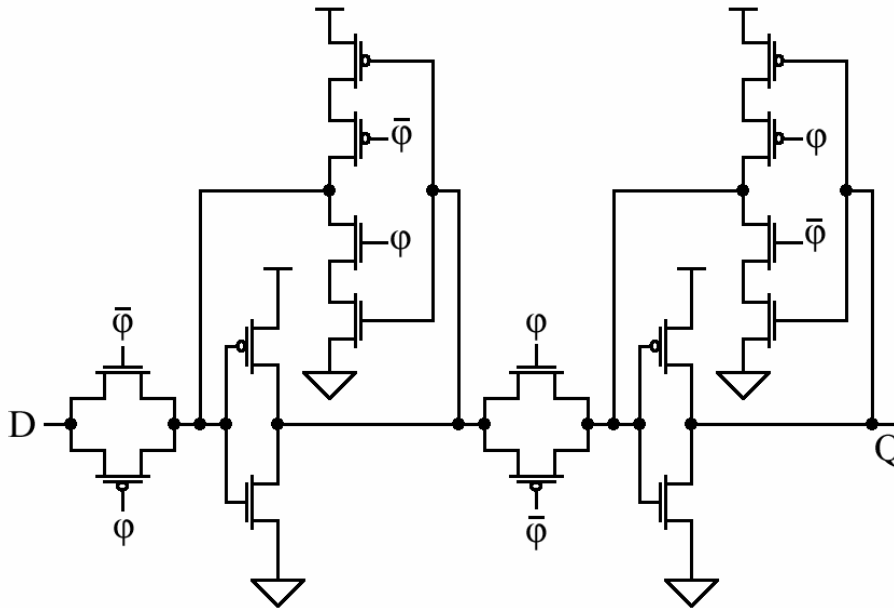
Figure 22 - PowerPC 603 flip-flop

2.4 9T TSPC flip-flop (TSPC)
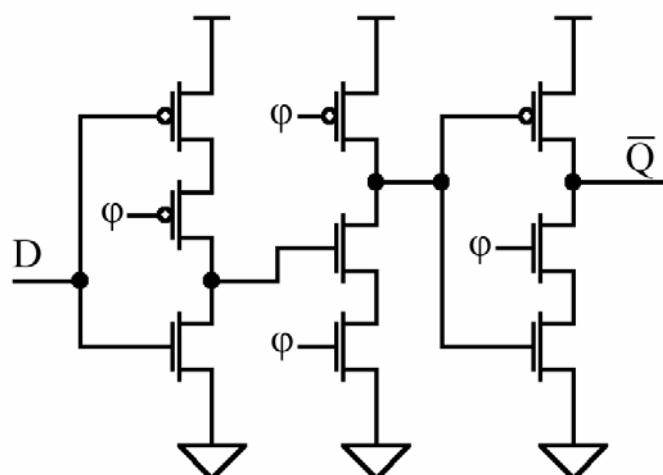
Figure 23 - 9T True single phase clock flip-flop (TSPC)

In order to overcome the problem of distributing several clock signals and avoid the serious problems caused by clock skew, a development of NORA-CMOS technique introduced True Single Phase Clock (TSPC) CMOS circuit technique[12], [14]. TSPC flip-flops (figure 23) have the advantage of single clock distribution, small area for clock lines, high speed and no clock skew. The basic TSPC latches can be obtained in many ways to implement all essential sequential components. Figure 24 show implementation of eight-transistor positive edge-triggered D flip-flop using split-output TSPC latches [12], [14], [4]. Although this structure seems to have smaller area than 9T TSPC flip-flop and less clocked transistors, it hasn't been used for simulations. The main reason is that there are some nodes in this structure which are not fully driven to VDD or GND.
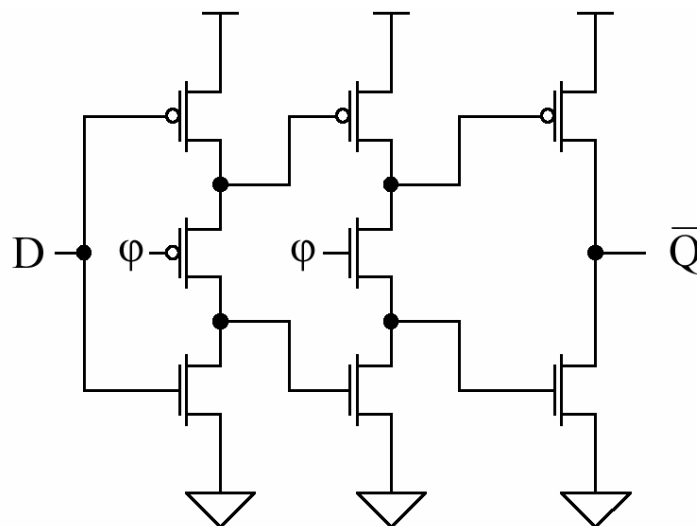
Figure 24 - 8T TSPC flip-flop

2.5 Hybrid latch flip-flop (HLFF)

This structure is basically a level sensitive latch which is clocked with an internally generated sharp pulse [10]. This sharp pulse is generated at the positive edge of the clock using clock and delayed version of clock. Transistor level implementation of this flip-flop is shown in figure 25.
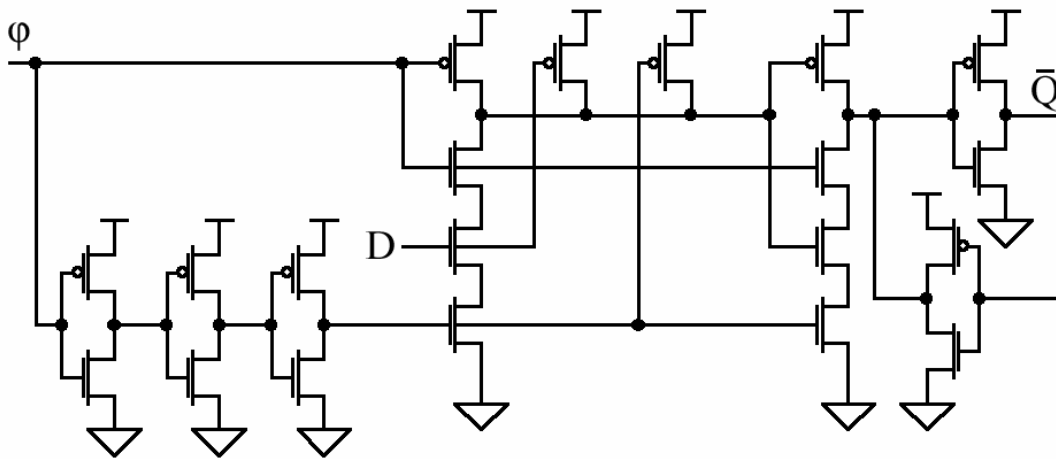
Figure 25 - Hybrid latch flip-flop (HLFF)

2.6 Semi-dynamic flip-flop (SDFF)

Similar to hybrid-latch flip-flop semi-dynamic flip-flop (figure 26) is also classified in the group of pulse-triggered flip-flops [11]. Two main building blocks are a level sensitive latch and a pulse generator. The latch is clocked with an internally generated sharp pulse, behaving like a flip-flop when the pulse width is very short.
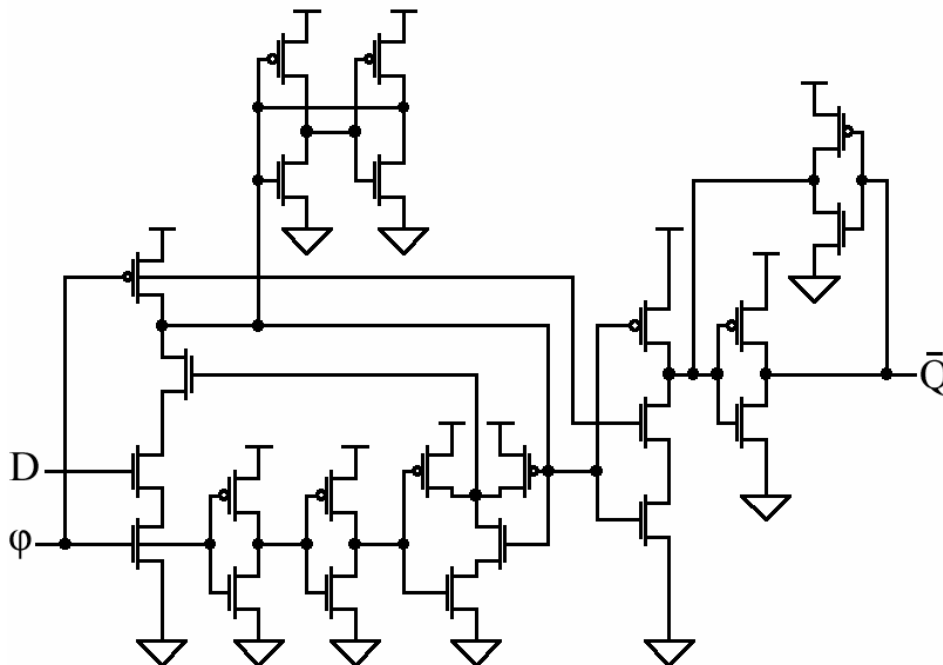
Figure 26 - Semi-dynamic flip-flop (SDFF)

2.7 NAND-NOR master-slave flip-flop (NANDNOR)
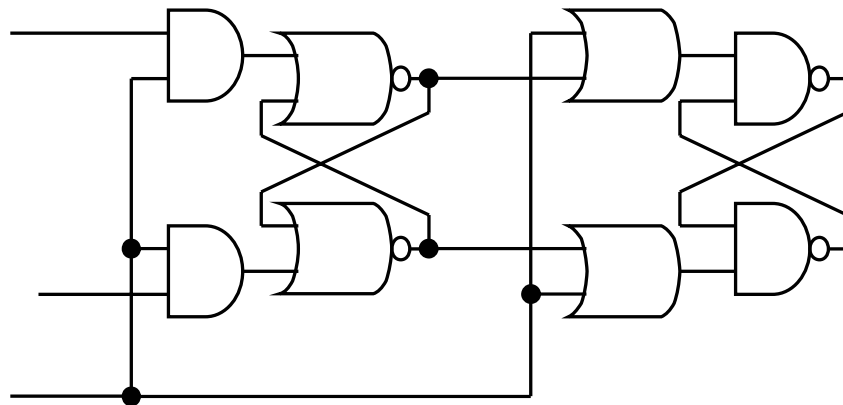
Figure 27 - NANDNOR flip-flop

This design uses only one clock phase and two gated RS latches (master and slave) [3], [6]. Gate level schematic of the flip-flop is shown in figure 27. Each of gated RS latches can be require 14 transistors. Transistor level schematic of this flip-flop is shown in figure 28.
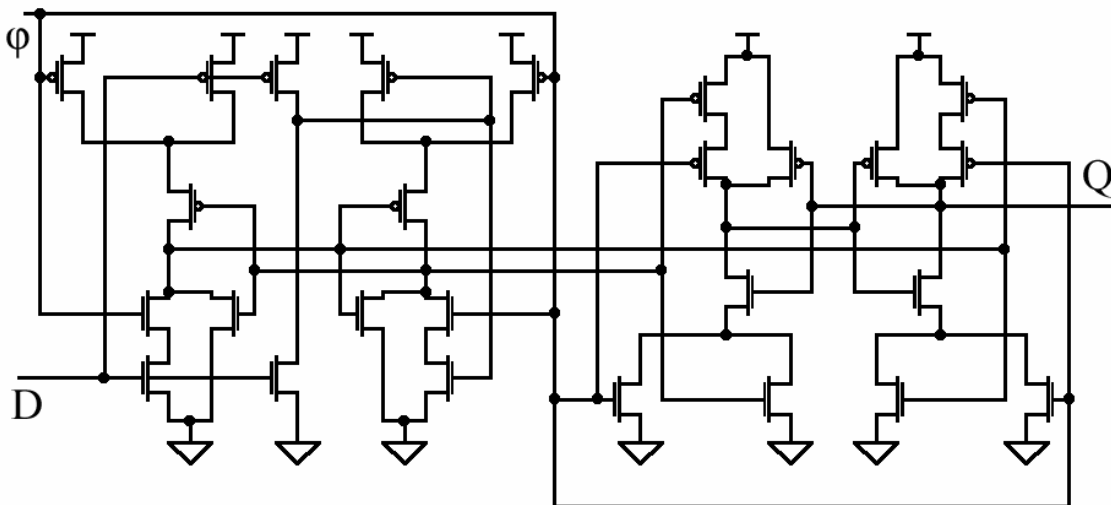
Figure 28 - NANDNOR flip-flop

Chapter 3

3. Simulation setup

All the circuits are designed and simulated in a standard 0.13μm technology. More detailed information about this technology is shown in table 1. The supply voltage used for simulations is 1.2V, and the operating temperature is 27ºC.

Technology	CMOS 0.12 (HCMOS9)
Gate length	0.13μ(drawn), 0.12μ(effective)
Power supply	1.2V
Specific process characteristics	• Triple well • Multiple Vt transistors (Ultra low leakage and high speed transistors) • 6 metal layer • Low k inter level dielectric
Threshold voltage (for different transistor types)	VTN=570/500/380mV VTP=590/480/390mV
Isat	TN@1.2V: 410/535/680μA/mic TP@1.2V: 170/240/320μA/mic

Table 1 - HCMOS9 technology overview

The simulation conditions are shown in figure 29. All of the flip-flops utilize identical and fixed input drivers (minimum sized inverters) and are loaded equally by the input capacitance of four minimum sized inverters. For delay and energy

consumption measurements the clock frequency is constant and equal to 1GHz for all flop-flops.
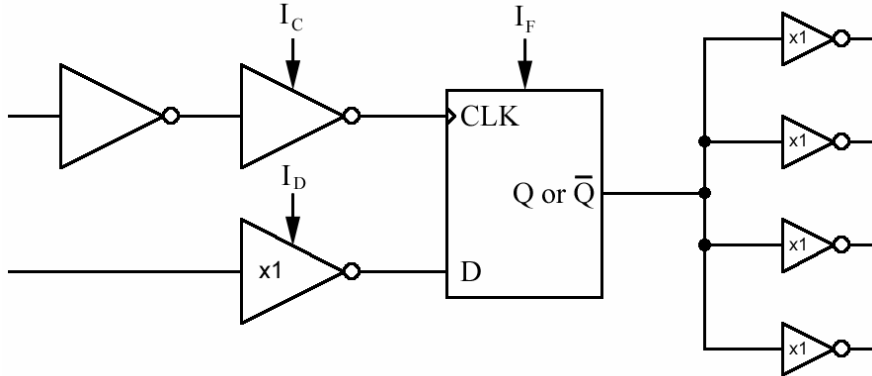
Figure 29 - The simulation test bench

For energy consumption calculations, the input drivers connected to the flip-flop are considered in addition to the flip-flop itself. Also, all the inversions are made inside flip-flop cell if needed. For instance if true and complementary data inputs or clock inputs are needed will be created in the flip-flop cell hence will be considered in power consumption measurements. So for the circuit shown in figure 29, the energy consumption will be equal to:

$$E = V_{DD} \int_{t_0}^{t_0+T} \left(i_C(\tau) + i_D(\tau) + i_F(\tau) \right) d\tau$$

Chapter 4

4. Simulation results

The raw measured data for TGMS flip-flop is shown in figure 30. The energy-delay space exploration is done by changing different parameters (e.g. transistor sizes) for this flip-flop. For simplicity, we have removed the points which are not efficient to use from energy and delay point of view. This process is illustrated in figure 30 for TGMS flip-flop. We only have shown the points that there is no other point with both less energy consumption and less delay in our simulation results. The star-shaped points in figure 30 are the points which can satisfy this condition. Other points that can not satisfy this property are omitted.
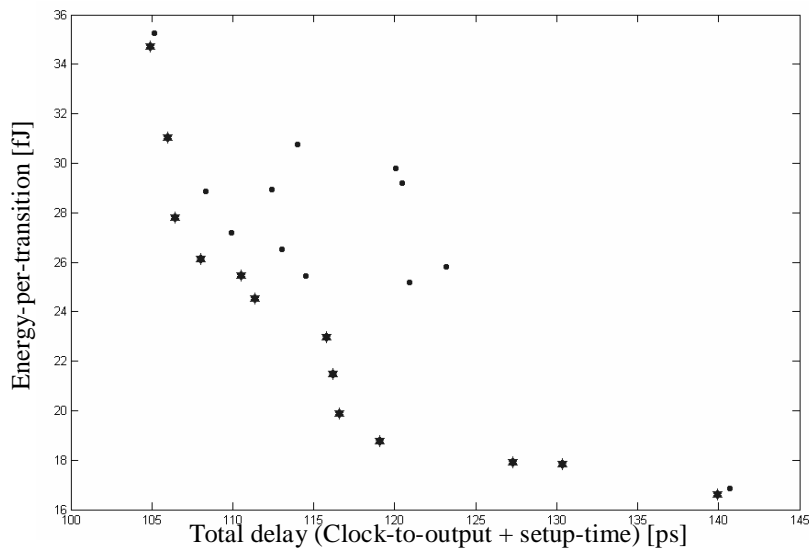
Figure 30 - Raw data for TGMS flip-flop and optimal points

Figures 31-38 show the measured data for each flip-flop. Each figure consists of four groups of points which correspond to clock-to-output delay vs. energy-per-transition, clock-to-output delay vs. clock-energy, total delay (clock-to-output + setup-time) vs. energy-per-transition and total delay vs. clock-energy.
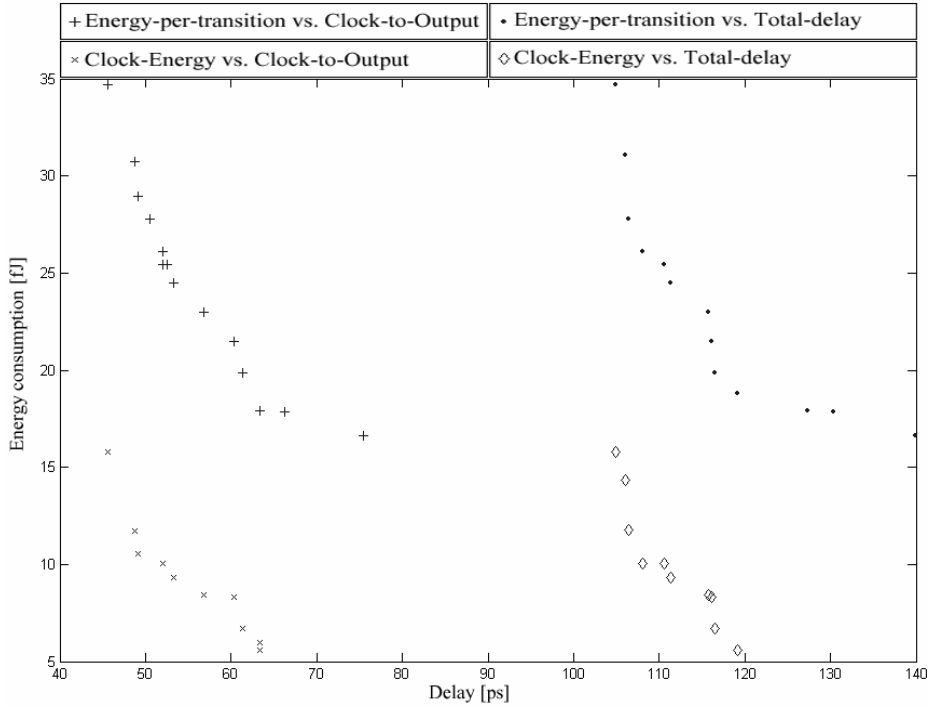
Figure 31 - Measured data for TGMS flip-flop
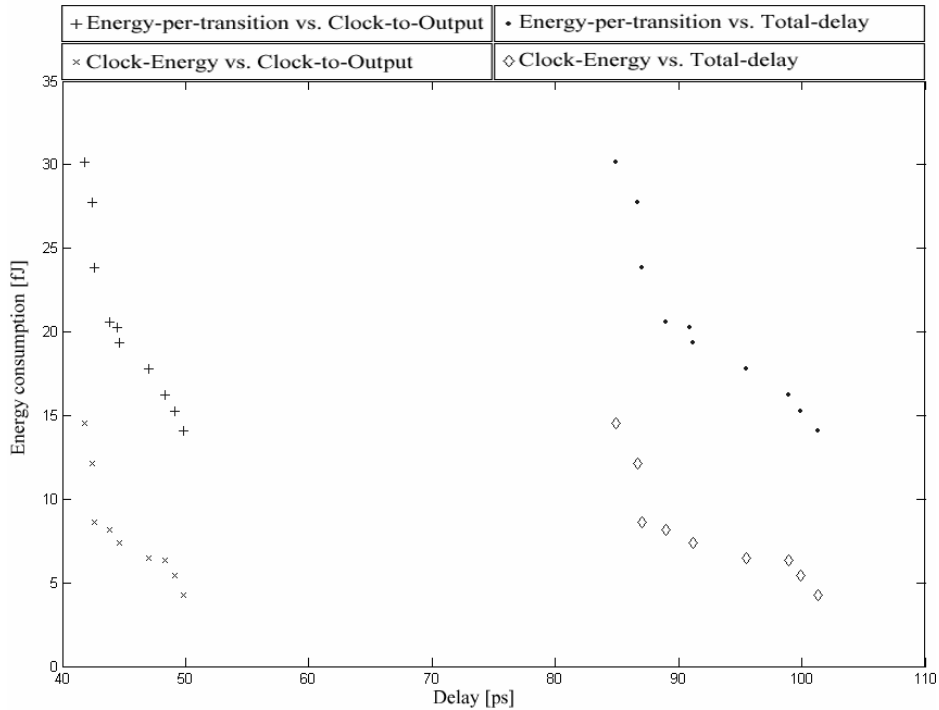
Figure 32 - Measured data for dynamic TGMS flip-flop
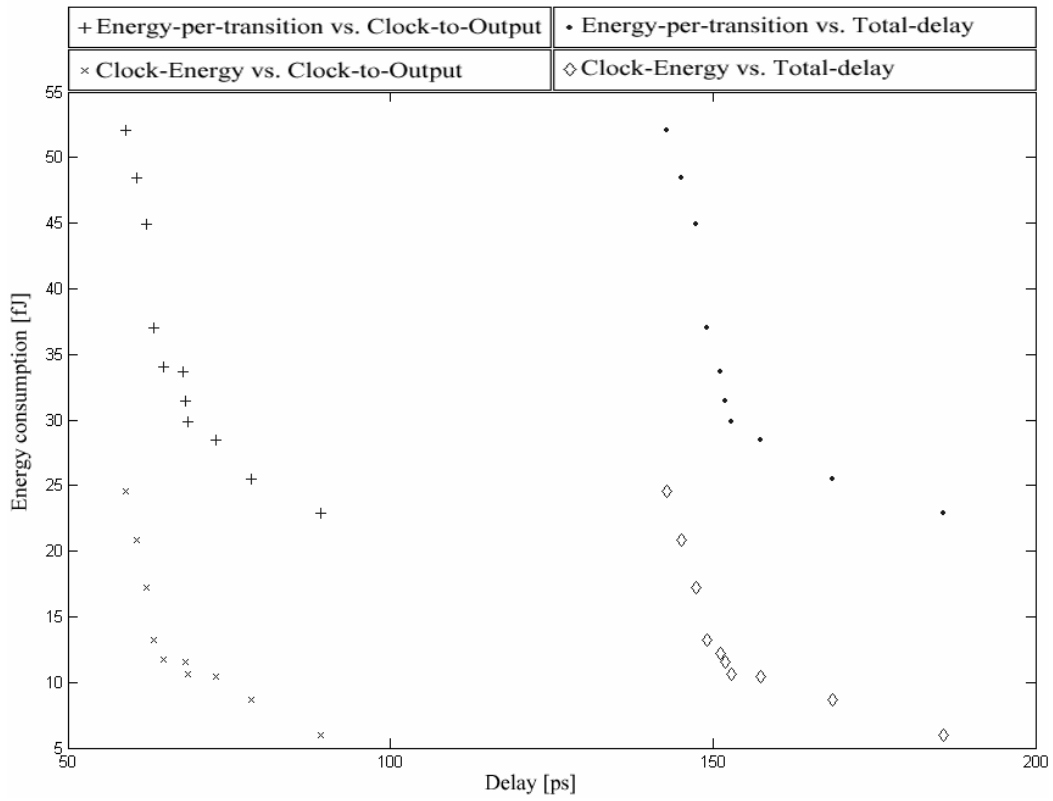
Figure 33 - Measured data for mC²MOS flip-flop
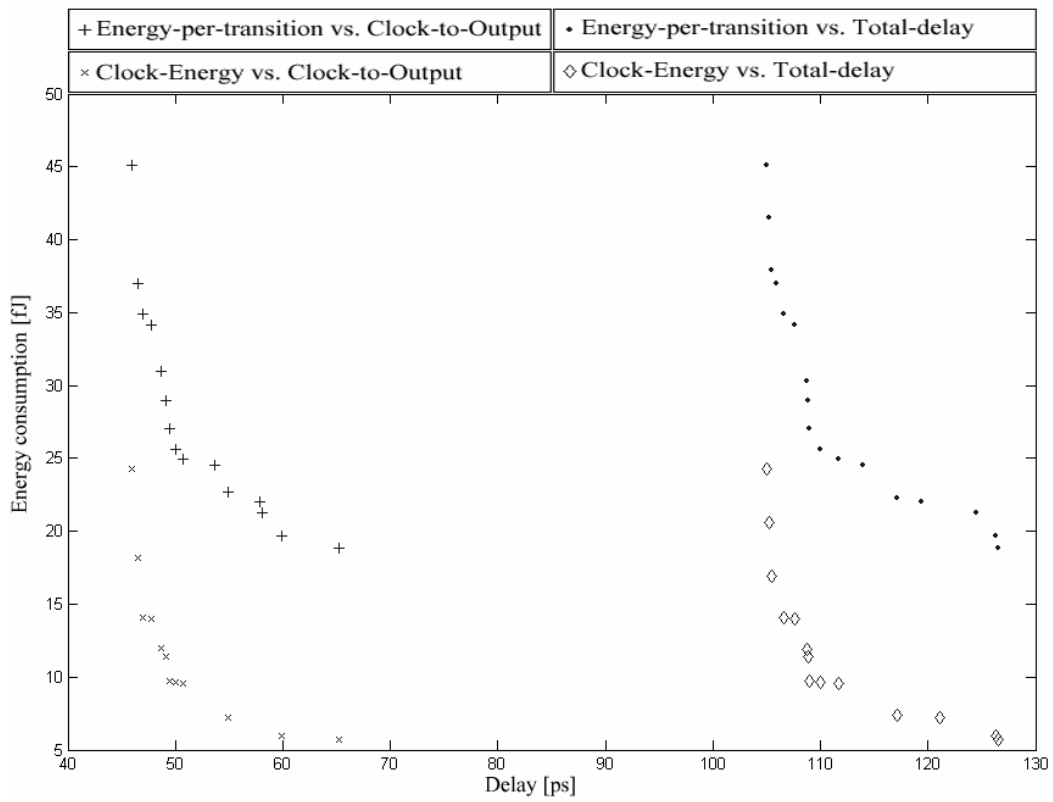
Figure 34 - Measured data for PowerPC 603 flip-flop
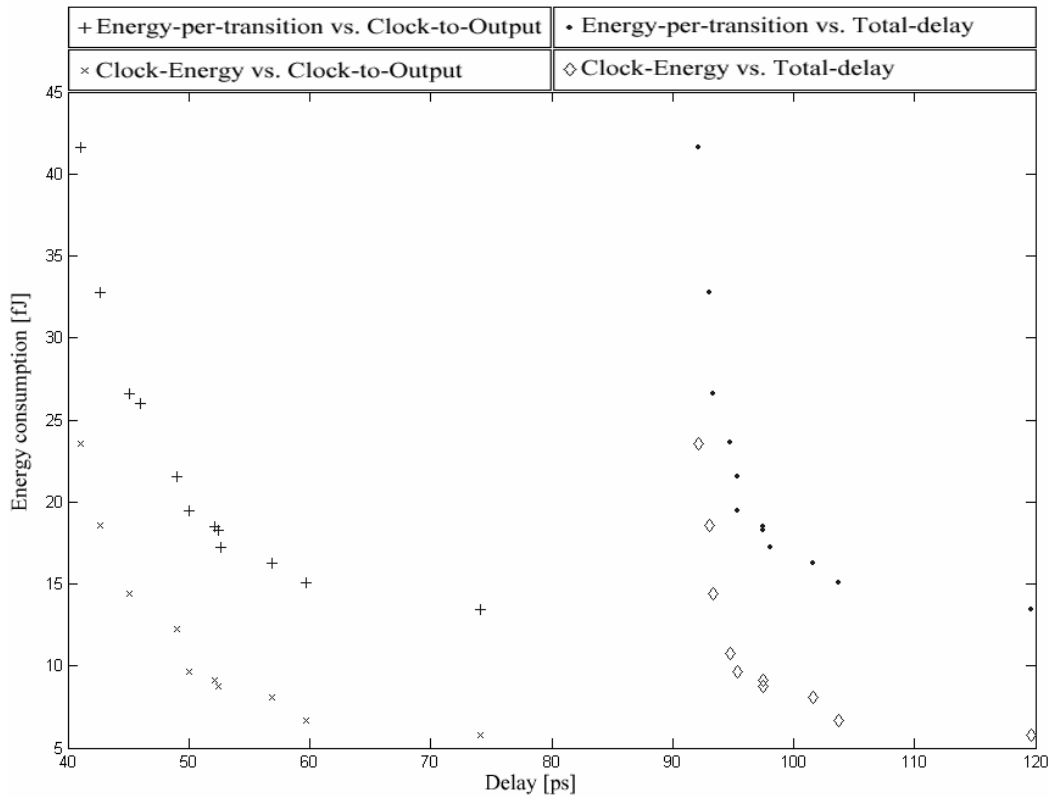
Figure 35 - Measured data for 9T TSPC flip-flop
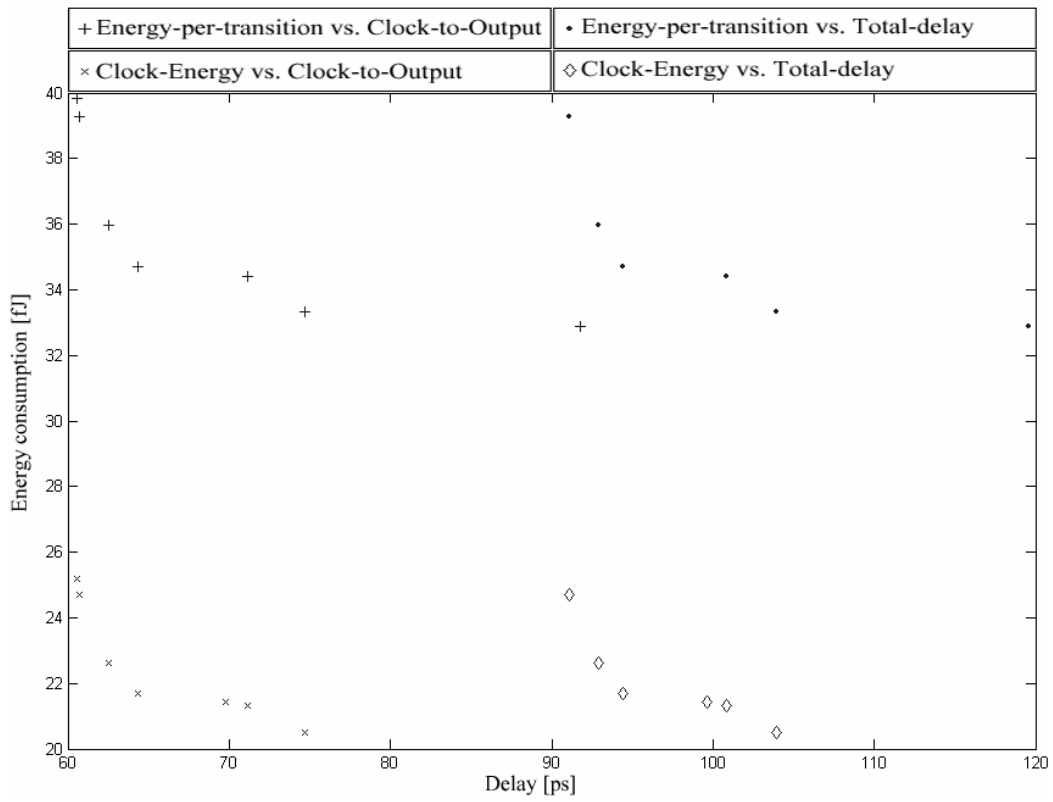
Figure 36 - Measured data for HLFF
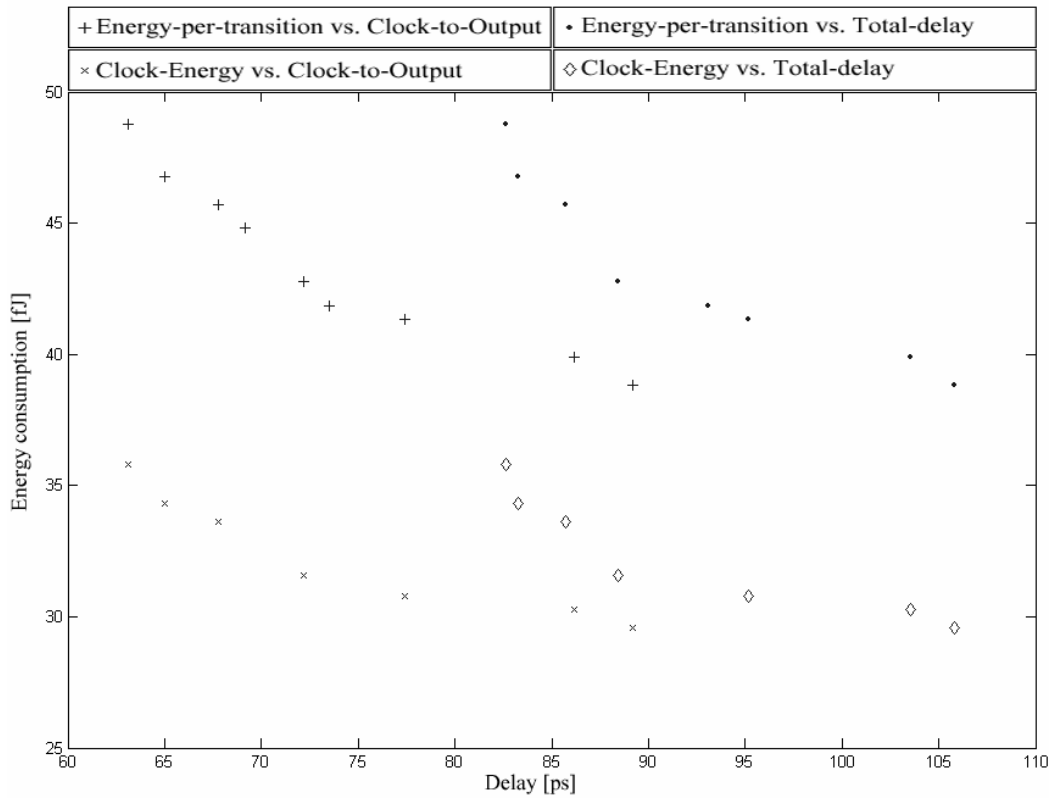
Figure 37 - Measured data for SDFF
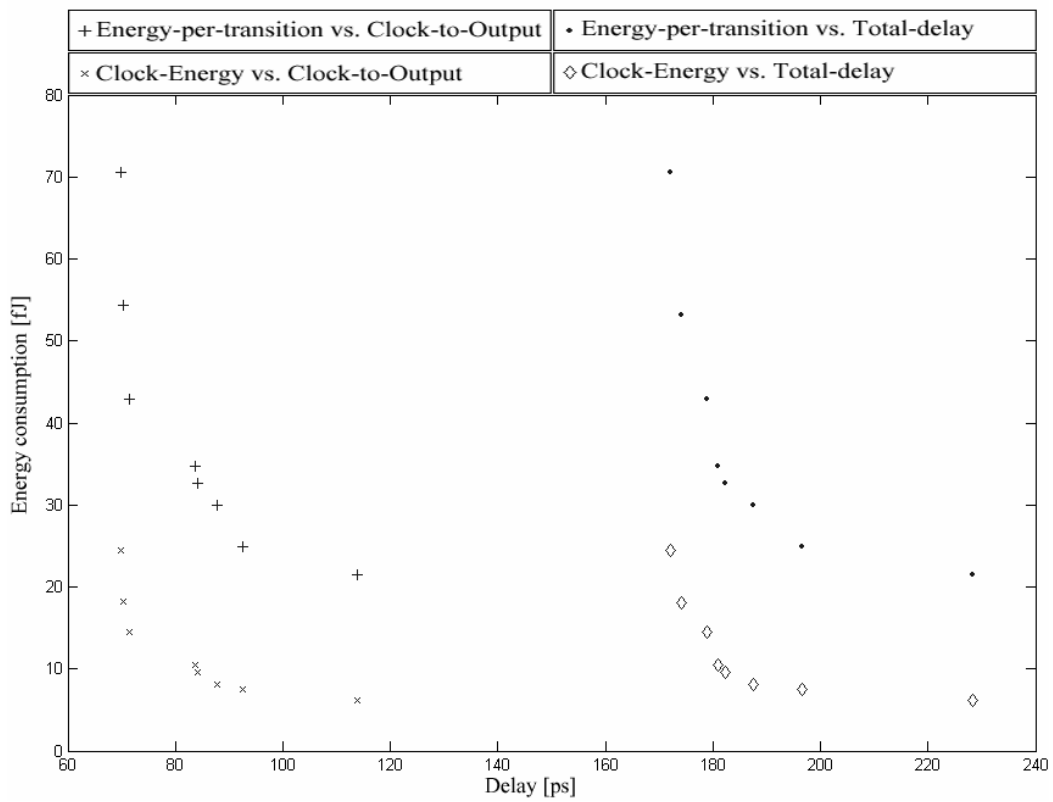
Figure 38 - Measured data for NANDNOR based flip-flop

Figures 39-46 show the energy-delay space of each flip-flop. Each figure includes two sub-graphs:

a) The upper sub-graph shows the flip-flop energy-per-transition versus the total delay time (clock-to-output + setup-time). The energy consumed by the clocked devices is shown with black color.

b) The lower sub-graph shows the total delay time (clock-to-output + setup-time) versus the total flip-flop energy per transition. The setup time and the clock-to-output delay are highlighted by white and black colors respectively.
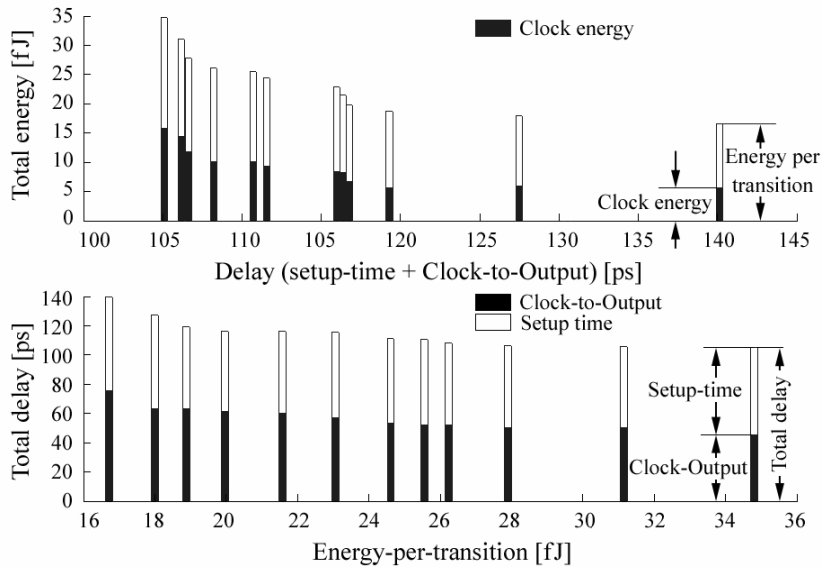
Figure 39 - Energy-Delay space for TGMS
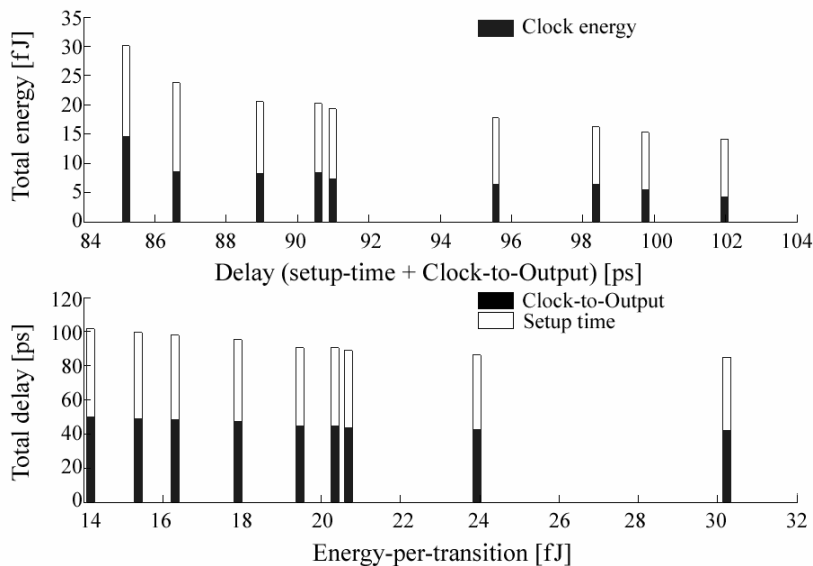
Figure 40 - Energy-Delay space for dynamic TGMS
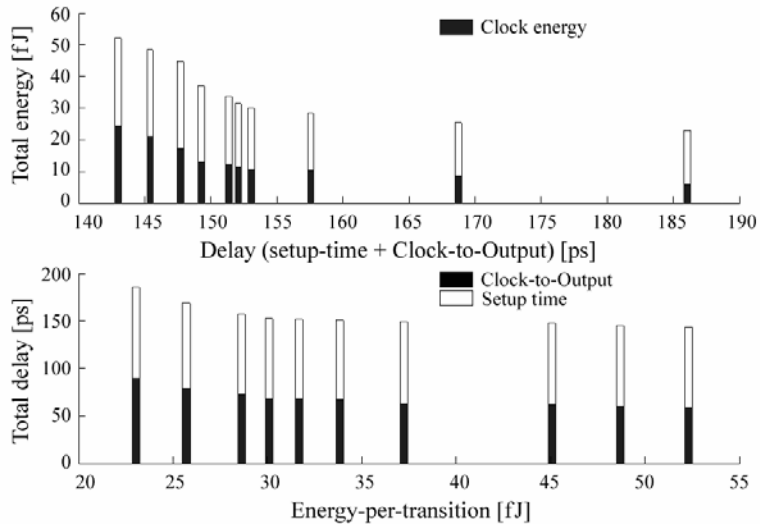
Figure 41 - Energy-Delay space for mC²MOS
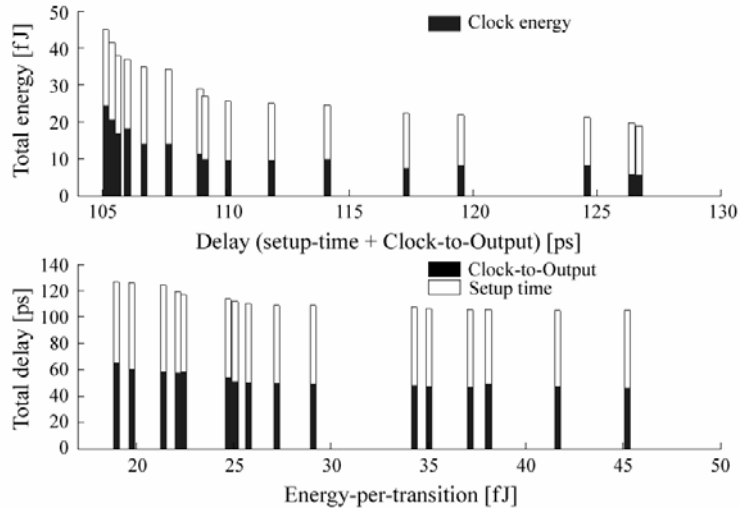
Figure 42 - Energy-Delay space for PowerPC 603
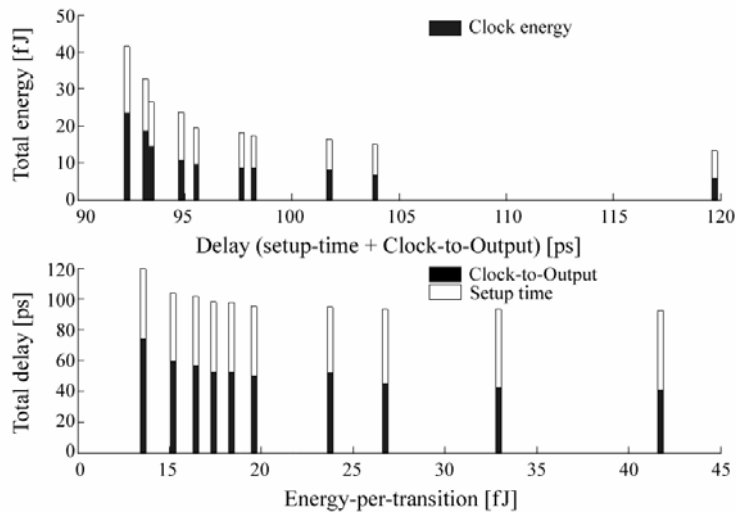
Figure 43 - Energy-Delay space for 9T TSPC flip-flop
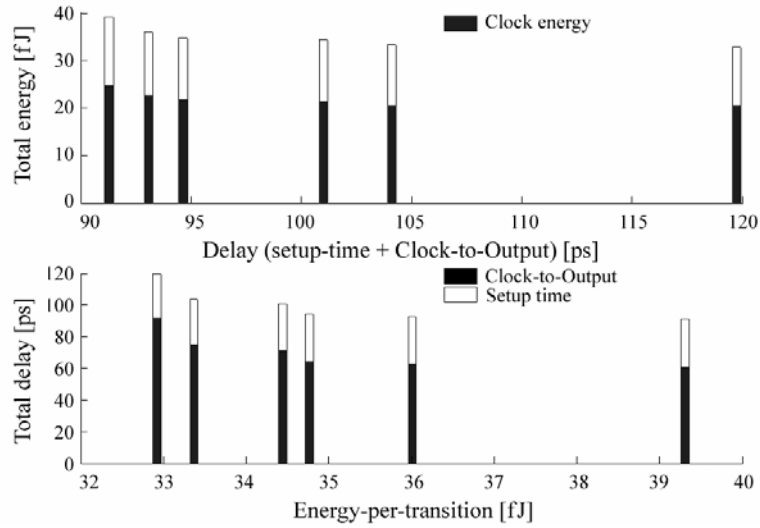
Figure 44 - Energy-Delay space for HLFF
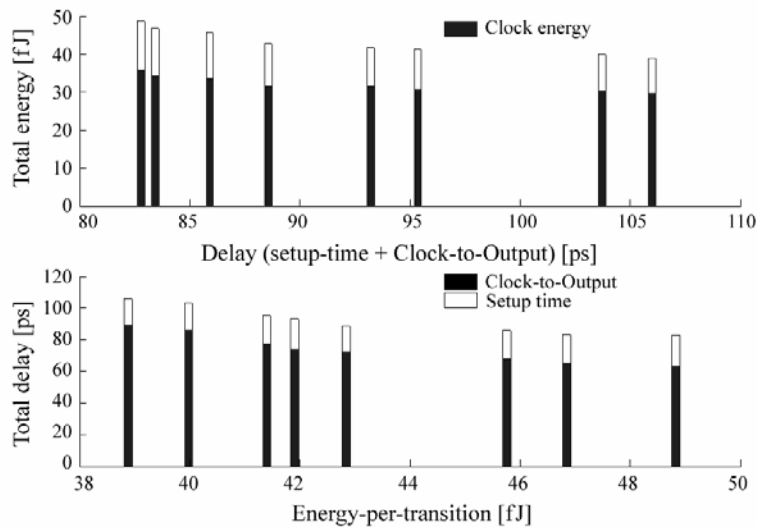
Figure 45 - Energy-Delay space for SDFF
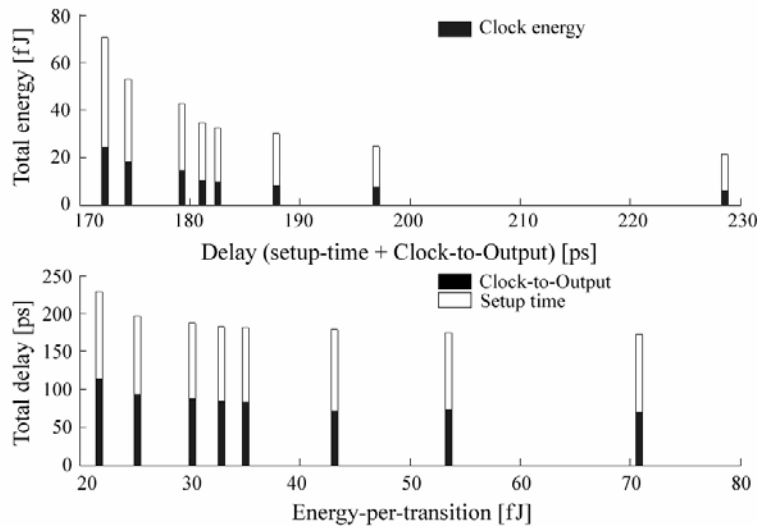
Figure 46 - Energy-Delay space for NANDNOR based flip-flop

Chapter 5

5. Comparisons and conclusions
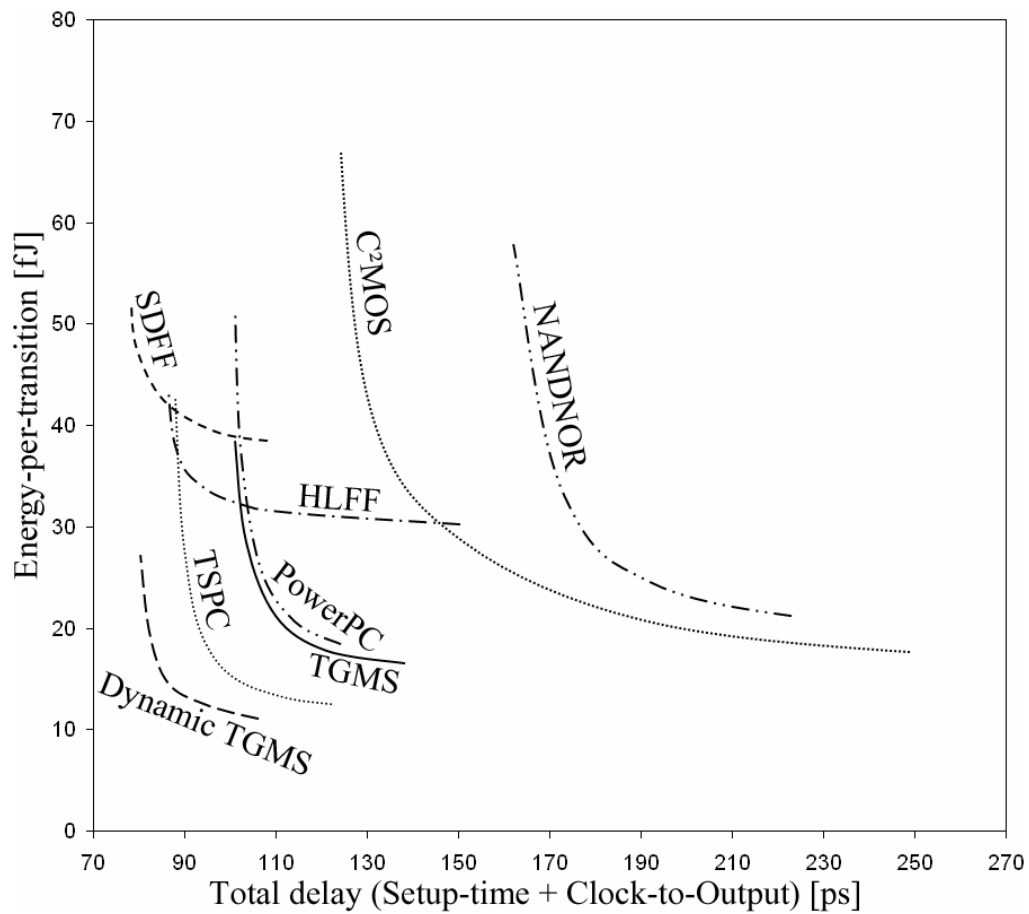
Figure 47 - Energy-per-transition vs. total delay

Figures 47-50 summarize the energy-delay space of all the flip-flops. As the figure 47 shows, transmission gates flip-flops TGMS and PowerPC 603 show the best power-performance trade-off among the fully static flip-flops. Further, they cover a relatively wide portion of the total energy-delay space. Pulse-triggered flip-flops HLFF and SDFF can support shorter delay targets. Figure 47 shows that pulse-triggered flip-flops HLFF and SDFF are faster mainly due to their shorter setup-time. Based on this figure the SDFF is the fastest flip-flop. However, the pulse-triggered flip-flops consume a considerably larger power (about 2x compared to TGMS flip-flops). The TSPC and the dynamic TG-based flip flops have a comparable performance while they consume up to 50% of the energy needed for SDFF. However, their internal floating nodes are sensitive to leakage currents and other sources of noise [13].
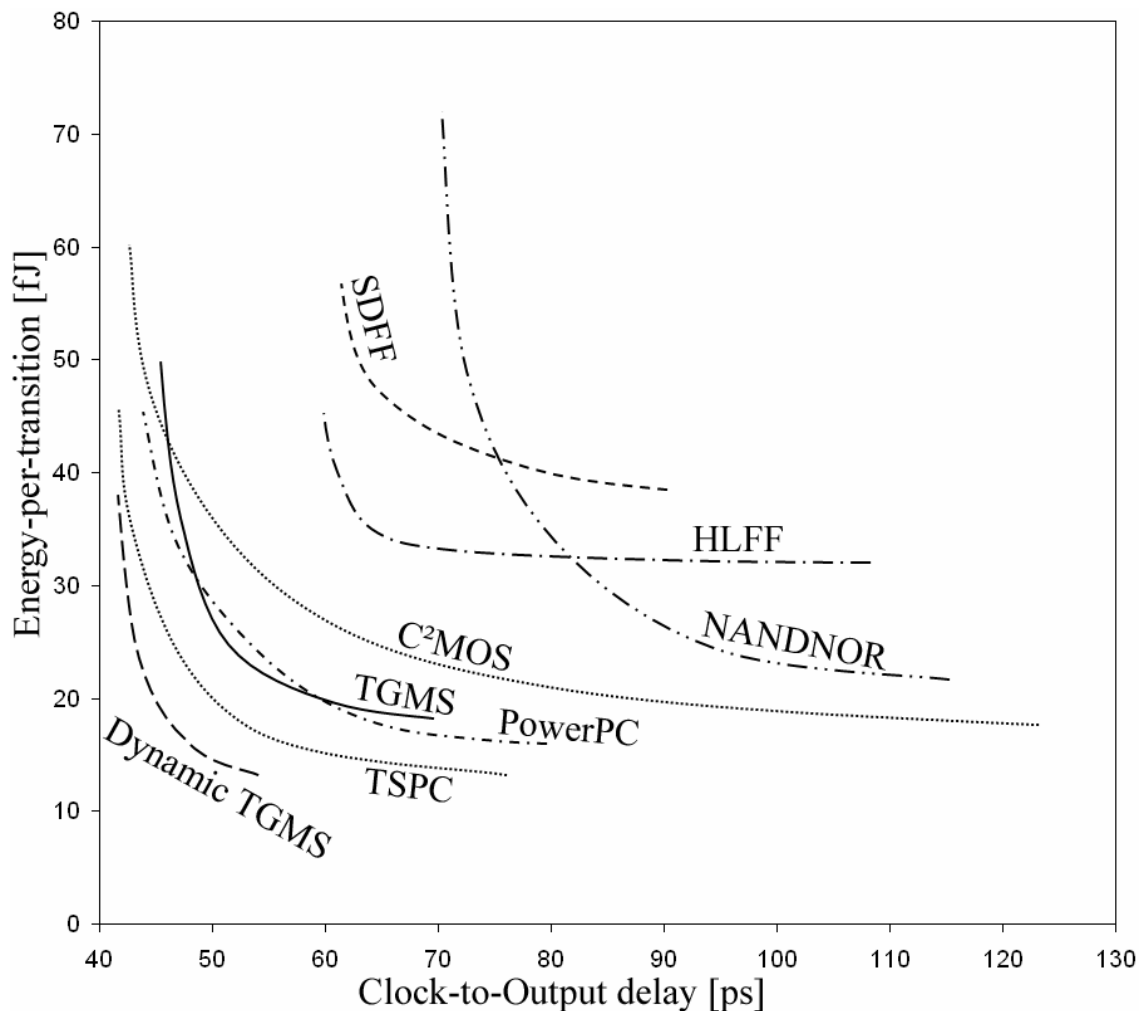
Figure 48 - Energy-per-transition vs. clock-to-output delay
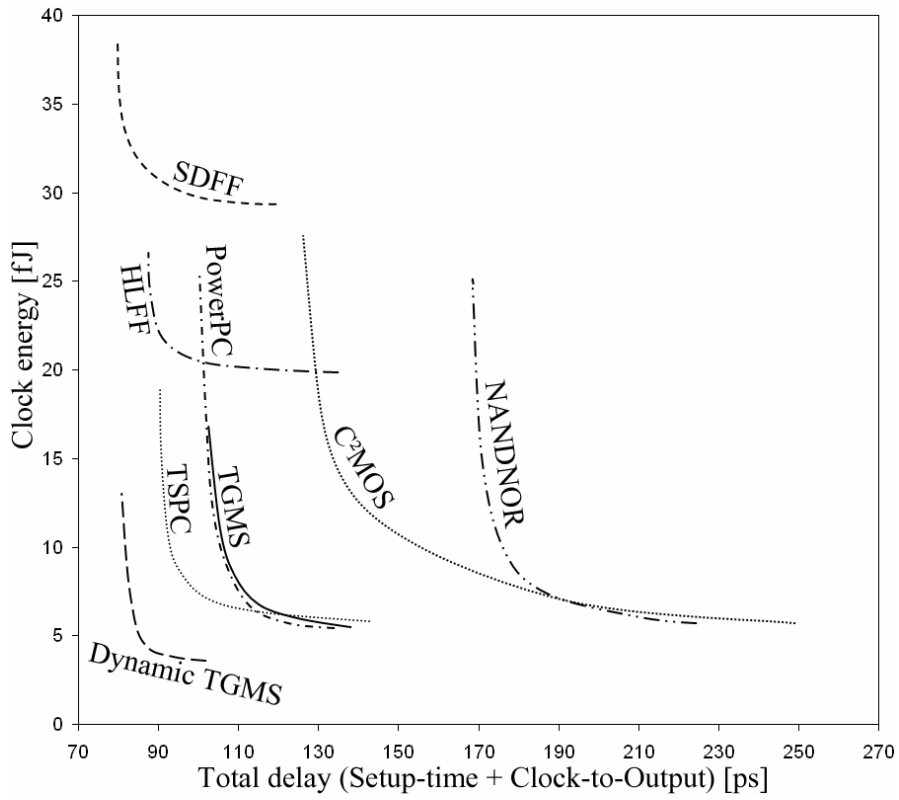
Figure 49 - Clock-energy vs. total delay
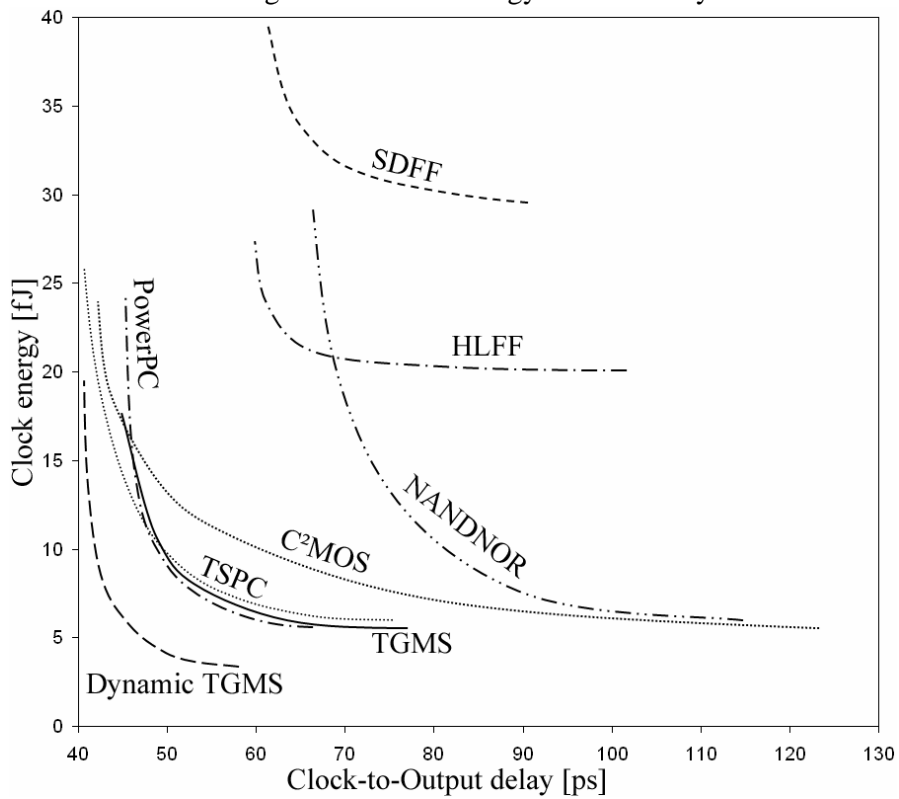
Figure 50 - Clock-energy vs. clock-to-output delay

Figures 47-50 can be used to identify the optimum flip-flop topology for different energy-delay targets. However, as an example, Table 2 compares the flip-flops at their minimum EPT$\times$delay^2 points in Fig. 47. This point is chosen as an example optimal point of operation for the flip-flops. Minimizing this weighted delay and energy consumption product, gives us a point among several measured points for each flip-flop.

	Overall delay [ps]	Clock-to-Output [ps]	Setup-time[ps]	Hold-time[ps]	Energy-per-transition [fJ]	Clock energy [fJ]
SDFF	83.6	65.1	15.0	18.8	46.8	34.4
HLFF	94.5	64.4	26.9	15.6	34.7	21.7
TGMS-dynamic	98.4	49.8	46.1	-6.4	15.8	4.4
TSPC	103.8	59.7	41.1	3.9	15.6	6.7
PowerPC	116.3	60.2	53.1	-17.4	18.9	5.7
TGMS	118.7	63.3	52.2	-17.8	18.8	5.6
mC^{2}MOS	152.8	68.6	80.8	-31.7	29.9	10.6
NANDNOR	197.5	94.9	97.9	-30.8	25.1	7.5

Table 2 -   Performance comparison at the minimum EPT$\times$Latency^2

In this thesis, we have explored the energy-delay space for eight of widely referred flip-flops to be included in a high performance flip-flop cell library covering a wide range of power-performance targets. All the eight flip-flops have been designed in a standard 0.13µm CMOS technology at 1.2V. Based on our simulation results, we have shown that transmission gate-based flip-flops (such as TGMS and PowerPC 603) exhibit the best power-performance trade-off with a total delay (clock-to-output + setup time) down to 105ps. For higher performance, the pulse-triggered semi-dynamic flip-flop SDFF (figure 26) is the fastest (80ps) alternative suitable to be included in a flip-flop cell library. However, pulse-triggered flip-flops consume significantly larger power (about 2.5x) compared to fully-dynamic flip-flops such as TSPC and dynamic TG-based flip-flops.

Appendix A

Detailed simulation results

This section includes detailed results of the simulations for different states of the flip-flops. A schematic of the flip-flops with transistor names follows by the transistors sizes for each state and the simulation results for those states. DATA_DRV, CLK_DRV1 and CLK_DRV2 are the relative size of the input driver, input clock driver and internal clock inverter with respect to minimum sized inverter (n=150n, p=400n).
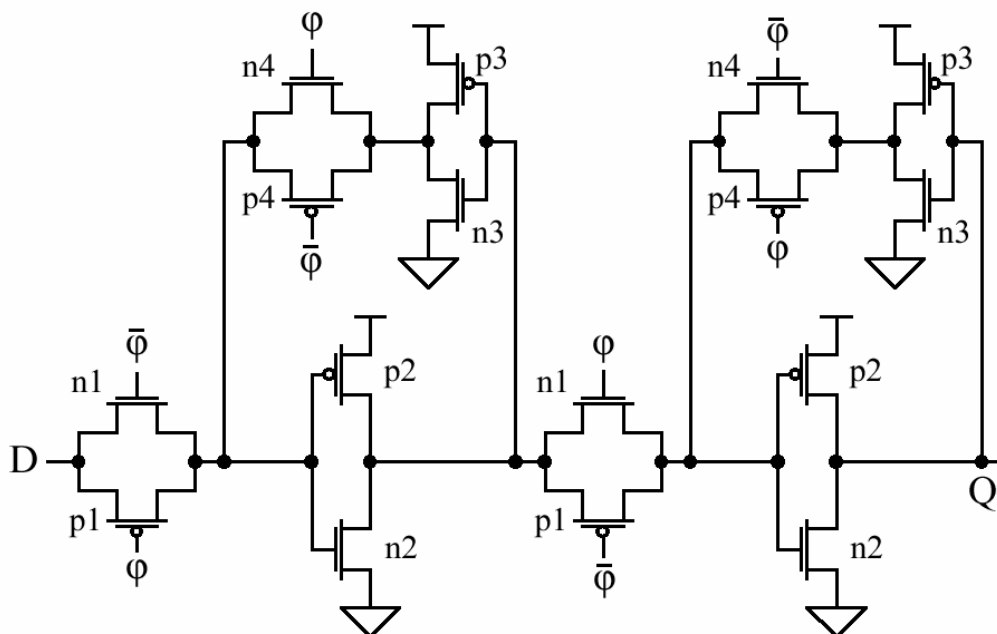
Figure 51 - Schematic and transistor names for TGMS flip-flop

	TGMS										
State	N1 (nm)	P1 (nm)	N2 (nm)	P2 (nm)	N3 (nm)	P3 (nm)	N4 (nm)	P4 (nm)	CLK DRV1	CLK DRV2	DATA DRV
1	350	595	350	595	150	255	150	255	4x	2x	2x
2	350	770	350	770	150	330	150	330	4x	2x	2x
3	350	525	350	525	150	225	150	225	4x	2x	2x
4	240	408	350	595	150	255	150	255	4x	2x	2x
5	525	892	350	595	150	255	150	255	4x	2x	2x
6	150	255	350	595	150	255	150	255	4x	2x	2x
7	350	595	525	892	150	255	150	255	4x	2x	2x
8	350	595	240	408	150	255	150	255	4x	2x	2x
9	150	255	240	408	150	255	150	255	4x	2x	2x
10	150	255	525	892	150	255	150	255	4x	2x	2x
11	350	595	350	595	150	255	150	255	4x	2x	1x
12	350	595	350	595	150	255	150	255	4x	2x	2.5x
13	150	255	240	408	150	255	150	255	3x	1.5x	2x
14	150	255	240	408	150	255	150	255	2x	1x	2x
15	350	595	350	595	150	255	150	255	6x	3x	2.5x
16	350	595	350	595	150	255	150	255	8x	4x	2.5x
17	350	525	350	525	150	225	150	225	4x	2x	2.5x
18	350	525	350	525	150	225	150	225	6x	3x	2.5x
19	450	765	525	892	150	255	150	255	4x	2x	2x
20	450	765	525	892	150	255	150	255	8x	4x	2x
21	450	765	525	892	150	255	150	255	6x	3x	2x
22	150	255	150	255	150	255	150	255	2x	1x	1x
23	150	255	240	408	150	255	150	255	2x	1x	1x
24	150	255	240	408	150	255	150	255	1x	1x	1x
25	150	255	150	255	150	255	150	255	1x	1x	1x

Table 3 - Detailed transistor sizes for TGMS flip-flop

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
1	10.39	17.93	26.52	52.62	57.8
2	11.32	19.67	29.18	54.30	63.5
3	10.03	17.25	25.45	52.03	55.9
4	9.31	16.42	24.52	53.31	55.4

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
5	12.12	20.36	29.76	53.68	63.7
6	8.43	15.23	22.97	56.82	56.1
7	10.57	19.15	28.94	49.18	60.8
8	10.30	17.26	25.18	59.26	58.7
9	8.32	14.47	21.49	60.28	52.9
10	8.62	16.65	25.81	56.88	63.5
11	10.31	17.38	25.43	52.59	74.3
12	10.43	18.26	27.18	52.64	54.7
13	6.70	12.85	19.88	61.29	52.2
14	5.56	11.74	18.78	63.33	52.6
15	12.16	19.97	28.86	50.91	54.9
16	14.36	22.16	31.05	50.00	55.7
17	10.07	17.58	26.13	52.03	53.4
18	11.79	19.27	27.80	50.49	53.4
19	11.75	20.70	30.74	48.80	62.8
20	15.81	24.73	34.72	45.62	65.0
21	16.31	25.25	35.25	46.74	63.1
22	5.59	10.80	16.62	75.45	60.7
23	5.97	11.61	17.91	63.32	60.8
24	5.90	11.54	17.85	66.23	60.8
25	5.82	11.03	16.85	78.10	58.7

Table 4 - Detailed data for TGMS flip-flop
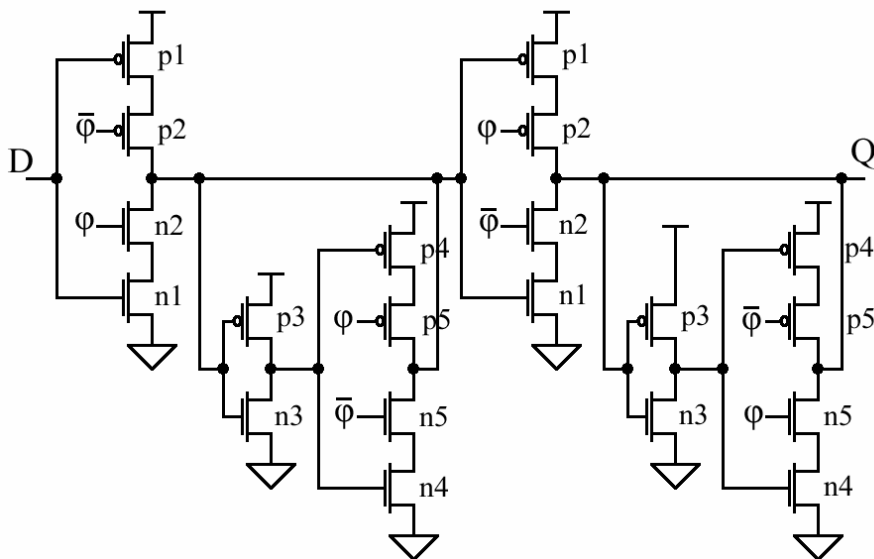
Figure 52 - Schematic and transistor names for mC²MOS flip-flop

mC²MOS									
State	N1 (nm)	P1 (nm)	N2 (nm)	P2 (nm)	N3,4,5 (nm)	P3,4,5 (nm)	CLK DRV1	CLK DRV2	DATA DRV
1	500	1000	450	900	150	300	4x	2x	2x
2	500	1250	450	1125	150	375	4x	2x	2x
3	500	1350	450	1215	150	405	4x	2x	2x
4	500	850	450	765	150	255	4x	2x	2x
5	500	1100	450	990	150	330	4x	2x	2x
6	700	1540	700	1540	150	330	4x	2x	2x
7	900	1980	900	1980	150	330	4x	2x	2x
8	1200	2640	1200	2640	150	330	4x	2x	2x
9	700	1890	700	1890	150	405	4x	2x	2x
10	700	1890	700	1890	150	405	6x	3x	2x
11	1200	3240	1200	3240	150	405	6x	3x	2x
12	900	2430	900	2430	150	405	6x	3x	2x
13	300	600	300	600	150	300	4x	2x	2x
14	300	510	300	510	150	255	2x	1x	1x
15	150	255	150	255	150	255	2x	1x	1x
16	300	510	300	510	150	255	4x	2x	2x

Table 5 - Detailed transistor sizes for mC²MOS flip-flop

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
2	13.02	22.98	33.99	50.57	89.2
3	13.46	23.82	35.28	49.67	87.7
4	11.24	19.64	28.96	57.63	97.8
5	12.36	21.73	32.10	52.38	93.0
6	15.32	26.65	39.20	50.64	88.2
7	17.74	30.89	45.42	51.24	88.1
8	21.38	37.30	54.88	53.58	92.5
9	16.88	29.49	43.44	49.51	84.8
10	19.22	31.85	45.77	43.58	87.2
11	26.22	44.13	63.90	45.62	90.0
12	22.02	36.72	52.96	43.91	86.7

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
13	10.20	17.76	26.12	65.53	97.3
14	7.22	13.74	20.97	79.21	111.5
15	5.72	11.41	17.67	123.30	125.6
16	9.70	16.54	24.71	71.99	107.2

Table 6 - Detailed data for mC²MOS flip-flop
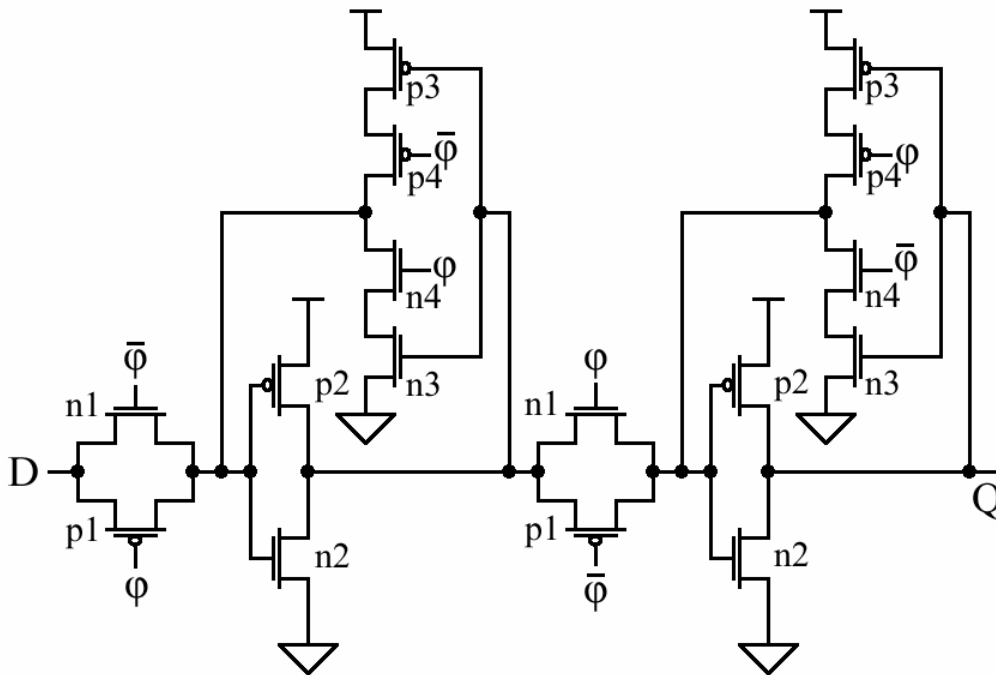
Figure 53 - Schematic and transistor names for PowerPC 603 flip-flop

PowerPC603											
State	N1 (nm)	P1 (nm)	N2 (nm)	P2 (nm)	N3 (nm)	P3 (nm)	N4 (nm)	P4 (nm)	CLK DRV1	CLK DRV2	DATA DRV
1	300	510	150	255	150	255	450	765	4x	2x	2x
2	300	660	150	330	150	330	450	990	4x	2x	2x
3	300	450	150	225	150	225	450	675	4x	2x	2x
4	300	750	150	375	150	375	450	1125	4x	2x	2x
5	500	850	150	255	150	255	450	765	4x	2x	2x
6	750	1275	150	255	150	255	450	765	4x	2x	2x
7	750	1275	150	255	150	255	500	850	4x	2x	2x
8	750	1275	150	255	150	255	350	595	4x	2x	2x

State	N1 (nm)	P1 (nm)	N2 (nm)	P2 (nm)	N3 (nm)	P3 (nm)	N4 (nm)	P4 (nm)	CLK DRV1	CLK DRV2	DATA DRV
PowerPC603 (Cont'd)											
9	500	850	150	255	150	255	500	850	4x	2x	2.5x
10	750	1275	150	255	150	255	500	850	6x	3x	2.5x
11	750	1275	150	255	150	255	500	850	6x	4.5x	2.5x
12	750	1275	150	255	150	255	500	850	8x	6x	2.5x
13	500	850	150	255	150	255	500	850	6x	4.5x	2.5x
14	150	255	150	255	150	255	350	595	4x	2x	2x
15	150	255	150	255	150	255	350	595	3x	1.5x	2x
16	150	255	150	255	150	255	350	595	2x	1x	1x
17	150	225	150	225	150	225	350	525	2x	1x	1x
18	500	850	150	255	150	255	500	850	4x	2x	2x
19	300	450	150	225	150	225	500	750	4x	2x	2x
20	300	450	150	225	150	225	600	900	4x	2x	2x
21	500	750	150	225	150	225	500	750	4x	2x	2x
22	150	225	150	225	150	225	350	525	3x	1.5x	2x
23	750	1275	150	255	150	255	350	595	2x	1x	1x
24	300	450	150	225	150	225	450	675	2x	2x	1x

Table 7 - Detailed transistor sizes for PowerPC 603 flip-flop

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
1	9.92	17.52	26.00	51.35	59.7
2	10.79	19.26	28.67	53.12	63.9
3	9.57	16.83	24.93	50.68	58.5
4	11.31	20.28	30.27	54.29	56.6
5	11.85	20.24	29.59	51.09	64.1
6	13.99	23.38	34.15	52.77	57.4
7	14.04	23.74	34.88	51.42	57.3
8	9.78	16.76	24.57	53.69	57.6
9	11.97	20.94	30.95	53.68	61.4
10	16.93	26.86	37.94	50.15	53.9
11	20.57	30.44	41.49	48.02	55.9
12	24.26	34.08	45.09	46.92	56.8
13	18.19	27.07	37.00	46.47	57.1

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
14	8.36	14.80	22.00	57.89	58.6
15	8.41	14.83	22.05	58.50	58.8
16	5.95	12.43	19.65	60.90	63.4
17	5.71	11.92	18.85	60.22	58.1
18	11.92	20.62	30.32	50.06	56.2
19	9.63	17.19	25.63	50.06	57.4
20	9.77	17.95	27.07	49.45	57.1
21	11.44	19.72	28.96	49.18	57.2
22	8.17	14.35	21.27	58.08	63.5
23	7.40	14.45	22.31	58.07	56.2
24	7.19	14.51	22.68	54.87	63.5

Table 8 - Detailed data for PowerPC 603 flip-flop
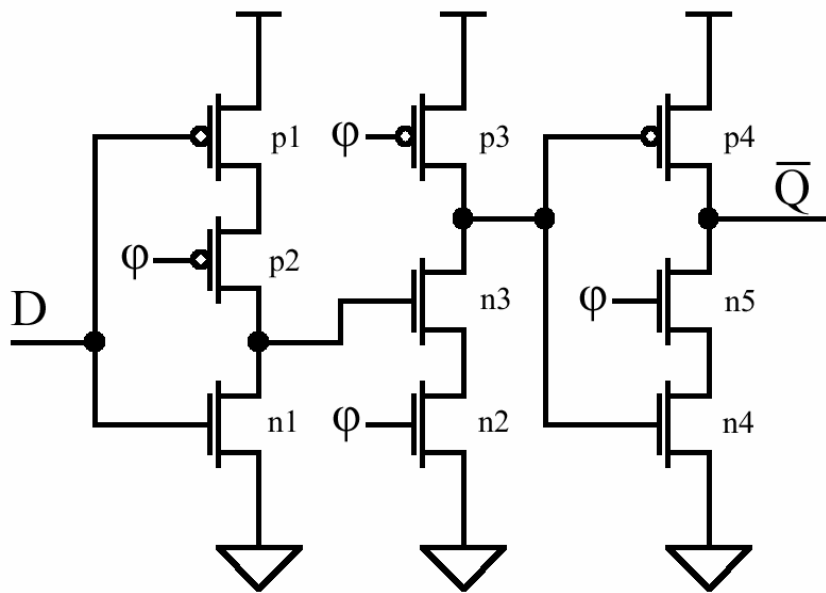
Figure 54 - Schematic and transistor names for 9T-TSPC flip-flop

9T-TSPC

State	N1 (nm)	P1,2 (nm)	N2 (nm)	N3 (nm)	P3 (nm)	N4 (nm)	N5 (nm)	P4 (nm)	CLK DRV1	DATA DRV
1	200	880	350	350	385	500	500	550	4x	2x
2	200	680	350	350	297	500	500	425	4x	2x
3	200	1000	350	350	437	500	500	625	4x	2x

9T-TSPC										
State	N1 (nm)	P1,2 (nm)	N2 (nm)	N3 (nm)	P3 (nm)	N4 (nm)	N5 (nm)	P4 (nm)	CLK DRV1	DATA DRV
4	200	600	350	350	262	500	500	375	4x	2x
5	400	1760	350	350	385	500	500	550	4x	2x
6	150	660	350	350	385	500	500	550	4x	2x
7	200	880	400	400	440	500	500	550	4x	2x
8	200	880	400	400	440	750	750	825	4x	2x
9	300	1320	600	600	660	800	800	880	4x	2x
10	300	1320	600	600	660	800	800	880	4x	2.5x
11	300	1320	600	600	660	800	800	880	6x	2.5x
12	300	1320	600	600	660	800	800	880	8x	2.5x
13	400	1760	800	800	880	1000	1000	1100	8x	2.5x
14	150	660	350	350	385	500	500	550	3x	2x
15	150	660	350	350	385	500	500	550	2x	2x
16	150	660	350	350	385	500	500	550	1x	2x
17	150	660	250	250	275	500	500	550	2x	2x
18	150	660	250	250	275	350	350	385	2x	2x
19	150	450	250	250	188	350	350	289	2x	2x
20	600	2640	1000	1000	1100	1200	1200	1200	8x	2.5x

Table 9 - Detailed transistor sizes for 9T-TSPC flip-flop

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
1	9.16	13.61	18.53	52.1	42.8
2	8.30	12.41	16.93	58.31	42.8
3	9.66	14.33	19.47	50.01	42.9
4	7.97	11.93	16.29	62.28	43.0
5	10.73	16.85	23.62	52.11	46.9
6	8.77	12.80	18.24	52.40	42.5
7	9.94	14.48	19.51	50.11	43.6
8	12.22	16.67	21.58	49.01	44.4
9	14.56	20.00	26.04	46.04	47.0
10	14.61	20.34	26.73	46.03	46.4
11	14.52	20.26	26.64	45.39	45.9
12	14.42	20.21	26.60	45.05	46.0

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
13	18.56	25.30	32.77	42.62	48.6
14	8.79	12.82	17.26	52.66	42.8
15	8.81	12.84	17.28	53.41	43.0
16	8.99	13.00	17.42	55.87	43.3
17	8.12	12.01	16.30	56.88	41.9
18	6.69	10.68	15.06	59.67	41.1
19	5.81	9.44	13.41	74.11	41.8
20	23.53	32.06	41.61	41.03	52.7

Table 10 - Detailed data for 9T-TSPC flip-flop
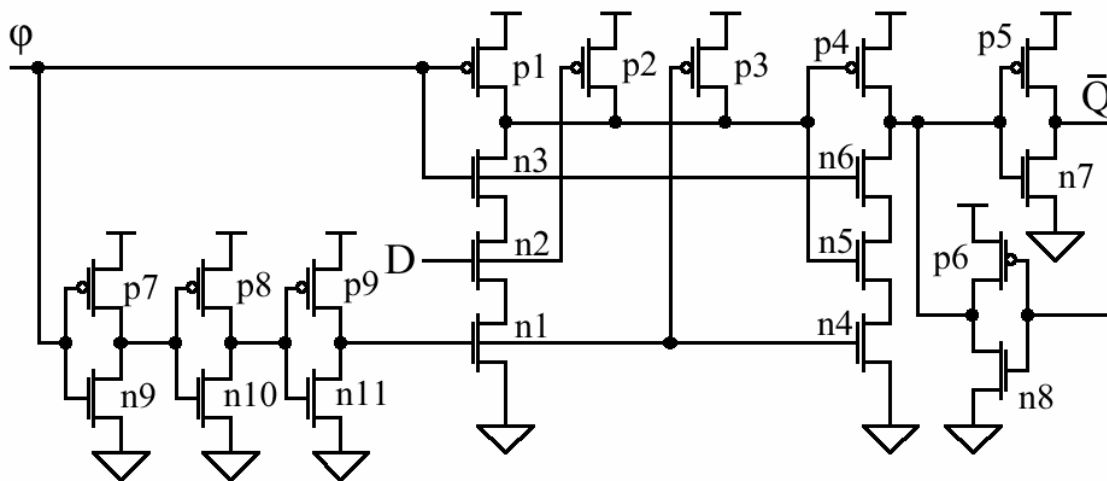
Figure 55 - Schematic and transistor names for HLFF

HLFF										
State	N1,2,3 (nm)	P1,2,3 (nm)	N4,5,6 (nm)	P4 (nm)	N7 (nm)	P5 (nm)	N8,9,10, 11 (nm)	P6,7,8,9 (nm)	CLK DRV1	DATA DRV
1	500	367	750	550	450	990	150	330	1x	2x
2	500	280	750	425	450	765	150	255	1x	2x
3	500	250	750	375	450	675	150	225	1x	2x
4	500	417	750	625	450	1125	150	375	1x	2x
5	600	440	750	550	450	990	150	330	1x	2x
6	750	550	750	550	450	990	150	330	1x	2x
7	1000	733	750	550	450	990	150	330	1x	2x

State	N1,2,3 (nm)	P1,2,3 (nm)	N4,5,6 (nm)	P4 (nm)	N7 (nm)	P5 (nm)	N8,9,10,11 (nm)	P6,7,8,9 (nm)	CLK DRV1	DATA DRV
8	1000	733	500	367	450	990	150	330	1x	2x
9	1000	733	500	367	300	660	150	330	1x	2x
10	1000	733	500	367	500	1100	150	330	1x	2x
11	1000	733	500	1320	500	1100	150	330	1x	2x
12	1000	733	500	1650	500	1100	150	330	1x	2x
13	1000	733	500	2200	500	1100	150	330	1x	2x
14	1000	733	600	440	450	990	150	330	1x	2x
15	1000	733	550	403	450	990	150	330	1x	2x
16	1000	733	600	1650	450	990	150	330	1x	2x
17	1000	733	600	1320	450	990	150	330	1x	2x
18	1000	567	500	283	300	510	150	255	1x	2x
19	1000	500	500	250	300	450	150	225	1x	2x
20	1000	567	600	1020	450	510	150	255	1x	2x
21	1000	567	500	283	450	765	150	255	1x	2x
22	1000	500	600	900	450	675	150	225	1x	2x
23	600	300	750	375	450	675	150	225	1x	2x

HLFF (Cont'd)

Table 11 - Detailed transistor sizes for HLFF flip-flop

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
1	22.76	29.07	35.78	87.42	26.9
2	20.87	26.82	33.18	94.08	26.2
3	20.11	26.02	32.35	100.40	28.9
4	23.89	30.50	37.50	86.10	26.9
5	23.28	29.72	36.56	81.23	24.6
6	24.18	30.81	37.86	76.19	25.0
7	25.86	32.72	40.04	71.31	27.0
8	23.42	30.76	38.57	67.68	27.4
9	23.28	30.14	37.45	70.23	27.2
10	23.47	31.02	39.06	68.19	27.3
11	23.84	31.43	39.49	71.88	28.3
12	24.37	32.12	40.31	76.54	28.7
13	25.08	33.29	41.94	91.04	29.4

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
14	24.36	31.43	38.96	67.82	27.2
15	23.89	31.06	38.70	66.65	27.1
16	25.19	32.30	39.85	60.58	27.5
17	24.72	31.76	39.26	60.75	27.3
18	21.34	27.64	34.39	71.15	26.1
19	20.50	26.70	33.32	74.68	25.5
20	22.61	29.07	35.96	62.55	27.2
21	21.44	28.10	35.21	69.82	26.3
22	21.71	28.01	34.72	64.34	26.9
23	20.58	26.52	32.88	91.77	23.2

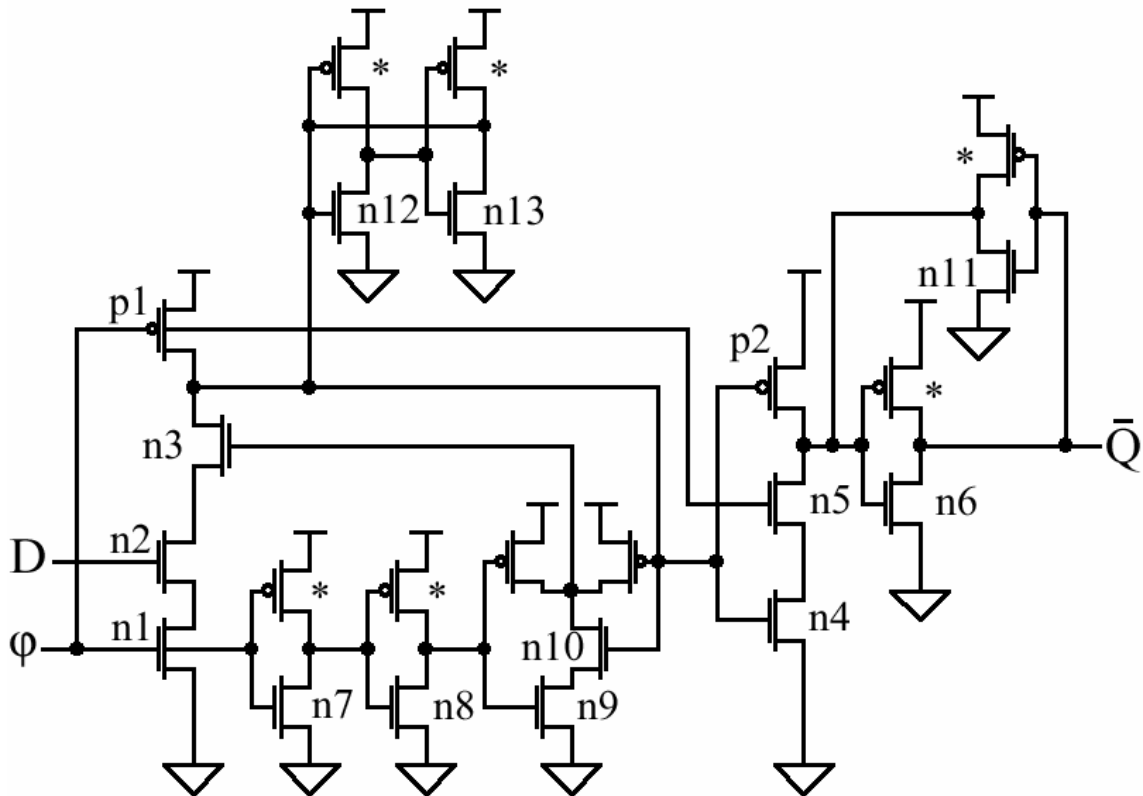Table 12 - Detailed data for HLFF flip-flop

Figure 56 - Schematic and transistor names for SDFF

The sizes of transistors marked with asterisk are PN_ratio times the corresponding n-transistor size.

SDFF State	N1,2,3 (nm)	P1 (nm)	N4,5 (nm)	P2 (nm)	N6 (nm)	N9,10 (nm)	N7,8,11, 12,13(nm)	PN ratio	CLK DRV1	DATA DRV
1	600	800	450	1000	700	300	150	1.7x	4x	1x
2	600	800	450	1500	700	300	150	1.7x	4x	1x
3	600	800	450	1500	700	300	150	2x	4x	1x
4	800	800	450	1500	700	300	150	1.7x	4x	1x
5	1000	800	450	1500	400	300	150	1.7x	4x	1x
6	1300	800	450	1500	400	300	150	1.7x	4x	1x
7	1300	800	450	1500	400	300	150	1.7x	6x	1x
8	1000	800	450	1500	400	300	150	1.7x	6x	1x
9	1800	800	450	1500	400	300	150	1.7x	6x	1x
10	1500	800	450	1500	400	300	150	1.7x	6x	1x
11	1500	800	450	2000	400	300	150	1.7x	6x	1x
12	1300	800	450	2000	400	300	150	1.7x	6x	1x

Table 13 - Detailed transistor sizes for SDFF flip-flop

State	Clock Energy [nJ]	Energy Consumption @ α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
1	29.59	34.10	38.82	89.18	12.2
2	30.27	34.99	39.91	86.16	13.1
3	31.44	36.31	41.42	86.96	12.3
4	30.80	35.93	41.33	77.42	13.9
5	31.71	36.63	41.83	73.49	15.9
6	33.74	39.09	44.81	69.14	19.2
7	33.63	39.46	45.68	67.76	14.6
8	31.59	37.01	42.77	72.21	12.6
9	37.49	43.81	50.68	64.03	18.2
10	35.12	41.18	47.73	65.95	16.0
11	35.81	42.03	48.76	63.09	16.4
12	34.33	40.33	46.77	65.03	15.0

Table 14 - Detailed data for SDFF flip-flop
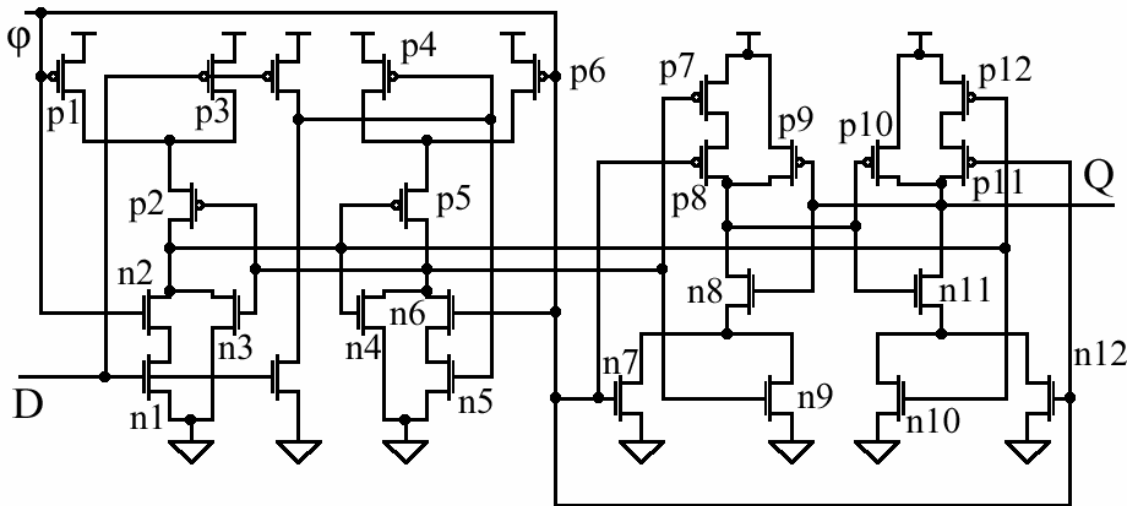
Figure 57 - Schematic and transistor names for NANDNOR flip-flop

NANDNOR									
State	N1,2,5,6 (nm)	N3,4 (nm)	P1-6 (nm)	N7-12 (nm)	P7,8,11,12 (nm)	P9,10 (nm)	CLK DRV1	DATA DRV
1	300	150	660	300	660	330	4	2
2	300	150	510	300	510	255	4	2
3	300	150	750	300	750	375	4	2
4	500	250	1250	500	1250	625	4	2
5	700	350	1750	700	1750	875	4	2
6	700	350	1750	300	750	375	4	2
7	300	150	660	300	660	330	4	1
8	300	150	450	300	450	225	2	1
9	300	150	450	300	450	225	1	1
10	300	150	300	300	300	150	1	1

Table 15 - Detailed transistor sizes for NANDNOR flip-flop

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
1	9.58	20.51	32.59	84.04	94
2	8.15	18.03	29.97	87.81	95.4
3	10.44	22.00	34.76	83.69	93
4	18.00	34.71	53.20	76.10	97.4
5	24.41	46.30	70.55	73.83	100.7
6	18.17	35.40	54.35	73.24	110.9

State	Clock Energy [nJ]	Energy Consumption @α=0.25	Energy per transition [nJ]	Clock to output [ps]	Setup time [ps]
7	16.52	31.47	47.83	71.52	118.9
8	7.48	15.81	24.98	92.64	99.4
9	7.63	15.98	25.17	94.97	97.9
10	6.20	13.46	21.47	113.90	108.7

Table 16 - Detailed data for NANDNOR flip-flop

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