1. Description

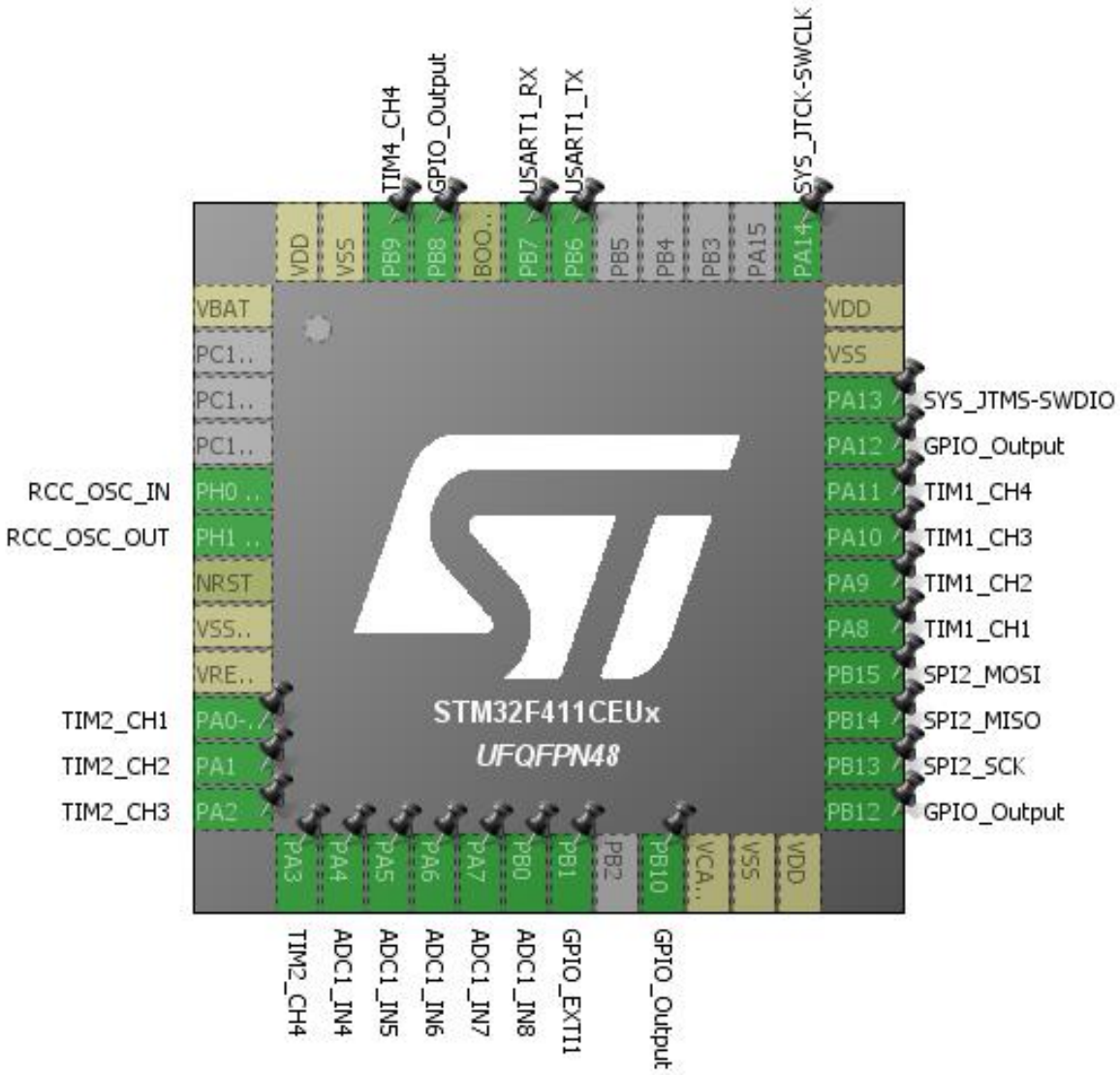
1.1. Project

Project Name	MicroQuadrotor
Board Name	MicroQuadrotor
Generated with:	STM32CubeMX 4.11.0
Date	11/14/2015

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411CEUx
MCU Package	UFQFPN48
MCU Pin number	48

2. Pinout Configuration



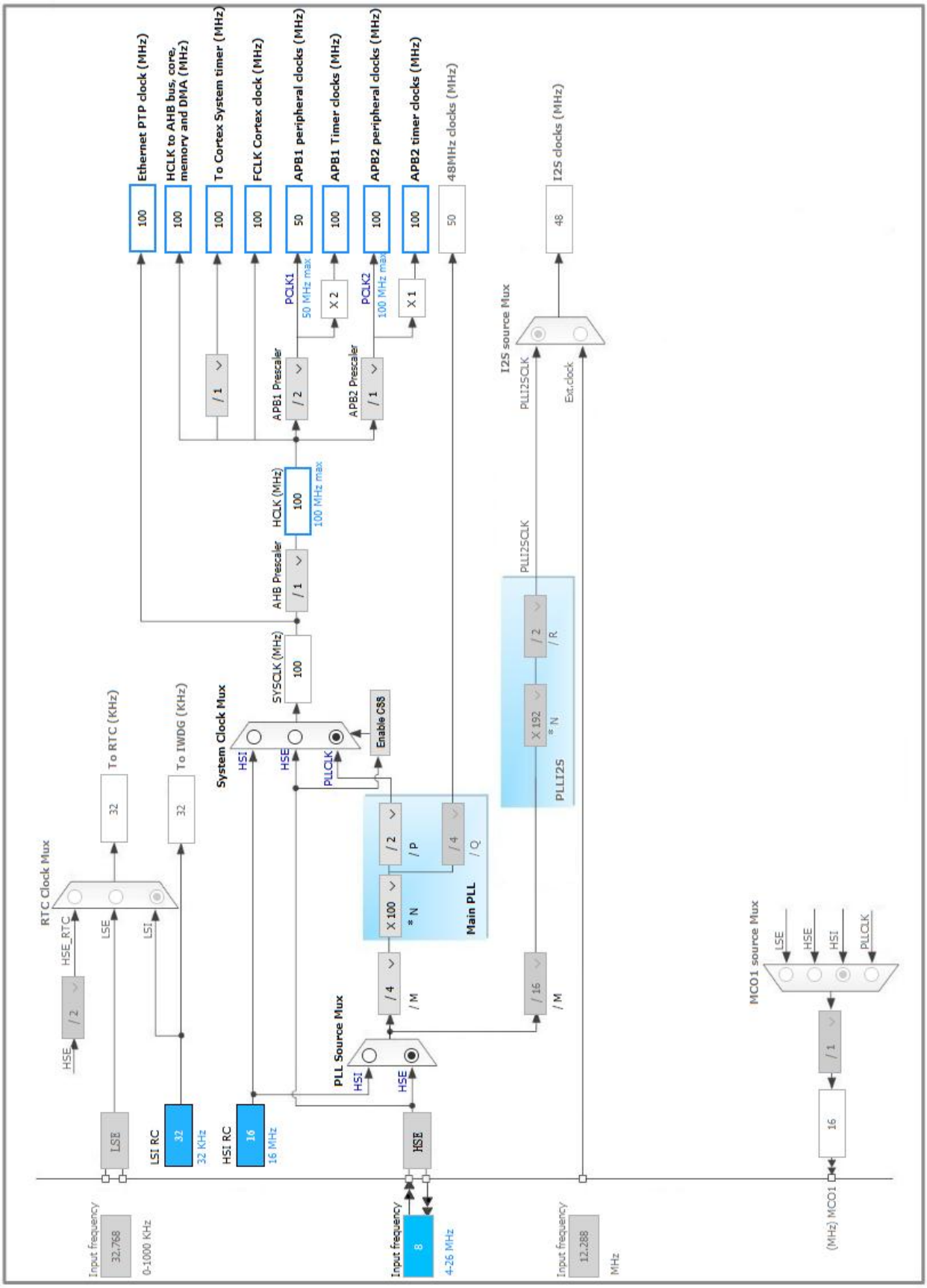
3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VREF+	Power		
10	PA0-WKUP	I/O	TIM2_CH1	
11	PA1	I/O	TIM2_CH2	
12	PA2	I/O	TIM2_CH3	
13	PA3	I/O	TIM2_CH4	
14	PA4	I/O	ADC1_IN4	
15	PA5	I/O	ADC1_IN5	
16	PA6	I/O	ADC1_IN6	
17	PA7	I/O	ADC1_IN7	
18	PB0	I/O	ADC1_IN8	
19	PB1	I/O	GPIO_EXTI1	
21	PB10 *	I/O	GPIO_Output	
22	VCAP1	Power		
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Output	
26	PB13	I/O	SPI2_SCK	
27	PB14	I/O	SPI2_MISO	
28	PB15	I/O	SPI2_MOSI	
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	TIM1_CH2	
31	PA10	I/O	TIM1_CH3	
32	PA11	I/O	TIM1_CH4	
33	PA12 *	I/O	GPIO_Output	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
42	PB6	I/O	USART1_TX	
43	PB7	I/O	USART1_RX	
44	BOOT0	Boot		

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
45	PB8 *	I/O	GPIO_Output	
46	PB9	I/O	TIM4_CH4	
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN4

mode: IN5

mode: IN6

mode: IN7

mode: IN8

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**5 ***
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	**28 Cycles ***
Rank	**2 ***
Channel	**Channel 5 ***
Sampling Time	**28 Cycles ***
Rank	**3 ***
Channel	**Channel 6 ***
Sampling Time	**28 Cycles ***
Rank	**4 ***
Channel	**Channel 7 ***
Sampling Time	**28 Cycles ***
Rank	**5 ***

Channel	**Channel 8 ***
Sampling Time	**28 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.3. SPI2

Mode: Full-Duplex Master

5.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**1.5625 MBits/s ***
Clock Polarity (CPOL)	

	High *
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.4. SYS

Debug: Serial Wire Debug (SWD)

5.5. TIM1

Clock Source : Internal Clock
Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**99 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1

Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.6. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**99 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**255 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.7. TIM4

Channel4: PWM Generation CH4

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**99 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**255 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0

Fast Mode	Disable
CH Polarity	High

5.8. USART1

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. FREERTOS

mode: Enabled

5.9.1. Config parameters:

Versions:

CMSIS-RTOS version	1.02
FreeRTOS version	8.2.1

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Enabled
USE_COUNTING_SEMAPHORES	Enabled

QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4
USE_ALTERNATIVE_API	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Disabled
USE_TICKLESS_IDLE	Disabled

Hook function related definitions:

USE_IDLE_HOOK	**Enabled ***
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	**Enabled ***
CHECK_FOR_STACK_OVERFLOW	**Option1 ***

Run time and task stats gathering related definitions:

USE_TRACE_FACILITY	Enabled
GENERATE_RUN_TIME_STATS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled
TIMER_TASK_PRIORITY	2
TIMER_QUEUE_LENGTH	10

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.9.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled

xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	**Enabled ***
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	**Pull-up ***	**High ***	
	PB14	SPI2_MISO	Alternate Function Push Pull	**Pull-up ***	**High ***	
	PB15	SPI2_MOSI	Alternate Function Push Pull	**Pull-up ***	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PB7	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	
GPIO	PB1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**High ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
EXTI line1 interrupt	true	5	0
USART1 global interrupt	true	7	0
DMA2 stream0 global interrupt	true	5	0
Non maskable interrupt	unused		
Memory management fault	unused		
Pre-fetch fault, memory access fault	unused		
Undefined instruction or illegal state	unused		
Debug monitor	unused		
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt	unused		
SPI2 global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411CEUx
Datasheet	026289_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	MicroQuadrotor
Project Folder	E:\Electronic
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.9.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No