



**SPECIFICATION
FOR
LCD Module
KD030FM-1**

MODULE:	KD030FM-1
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2015.04.10
1.1	SECOND ISSUE	2015.12.21

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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常备库存
Standing Stock

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range

Revision History

[illegible]



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	常 备 库 存 Standing Stock	长 期 供 货 Long Time supply	支持小量 NO MOQ	品 种 齐 全 In Full Range



General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.0'TFT-LCD contains 240x400 pixels, and can display up to 262K colors.

* Features

- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 65K/262K Colors
- Interface: 8/9/16/18Bit MCU Interface
- 3/4SPI+16/18Bit RGB Interface
- 3-line/4-line Serial Interface

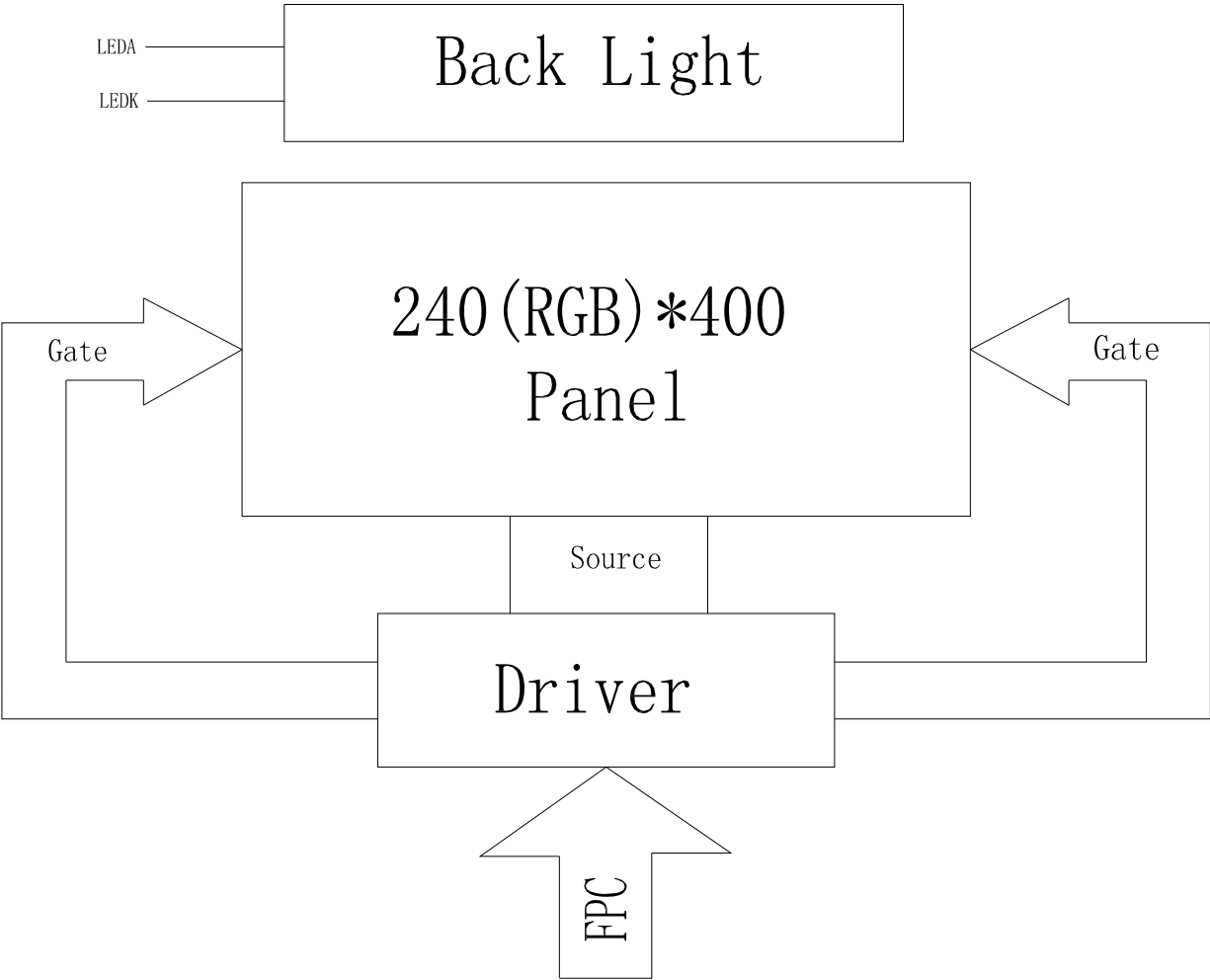
General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	39.24(H)*65.40(V) (3.0inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	240(RGB)*400	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1635(H)*0.1635(V)	mm	-
Viewing angle	ALL	o'clock	-
Controller IC	ILI9327	-	-
Display mode	Transmissive/ Normally Black	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		45.04		mm	-
	Vertical(V)		77.00		mm	-
	Depth(D)		2.60		mm	-
Weight			TBD		g	-



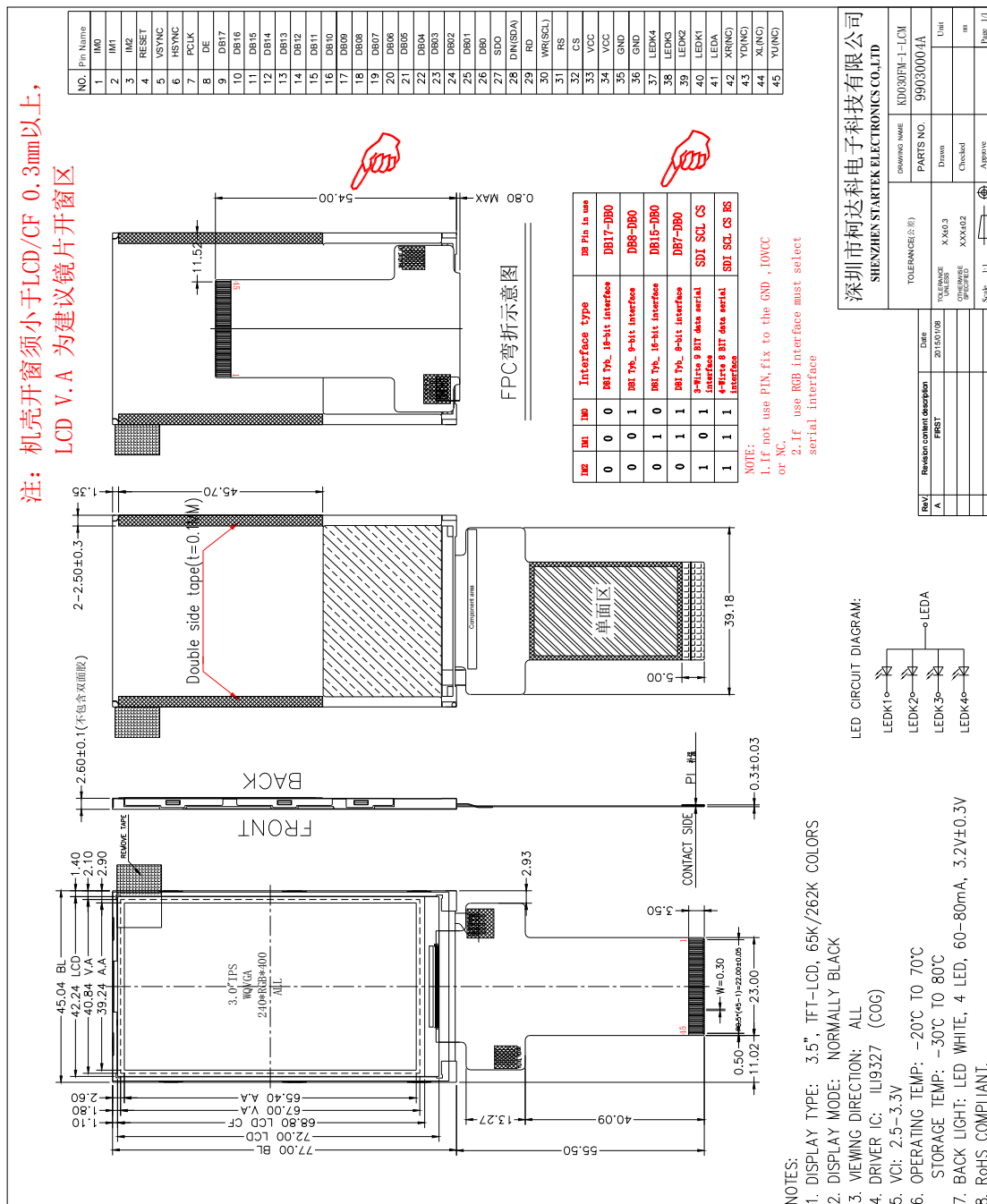
1. Block Diagram



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2. Outline dimension



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3. Input terminal Pin Assignment

NO.	SYMBOL	Description	
1	IM0	Interface selecting signal.	I
2	M1		I
3	IM2		I
4	RESET	This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active	I
5	VSYNC	Vertical sync. Signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_CS) In MDDI mode, this is an output pin, If it's not used; please let this pin as open. In other mode, this is an input pin, If it's not used; please fix this pin as GND.	I
6	HSYNC	Horizontal sync. signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_RS) In MDDI mode, this is an output pin, If it's not used; please let this pin as open. In other mode, this is an input pin, If it's not used; please fix this pin as GND.	I
7	PCLK	Pixel clock signal in DPI interface mode. If not used, please fix this pin at GND level.	I
8	DE	Data enable signal in DPI interface mode. In MDDI operation, VSYNC is assigned for the sub-display interface output (S_WR) In MDDI mode, this is an output pin, If it's not used; please let this pin as open. In other mode, this is an input pin, If it's not used; please fix this pin as GND.	I
9-26	DB17-DB0	These pins are data bus. In MDDI operation, DB[17:9]/S_DB[8:0] can be assigned for the sub-display interface output. In MDDI mode, these pins are output, If they are not used; please let these pins as open. In other mode, these pins are input, If they are not used; please fix these pins as GND.	I/O
27	SDO	Serial data output pin and used for the DBI type C mode.	O
28	DIN	Serial data input pin and used for the DBI type C mode. If not used, please connect this pin to ground.	I



29	RD	Read control pin for the DBI interface. If not used, please connect this pin to VCC.	I
30	WR(SCL)	Write control pin for the DBI interface. When the DBI type C is selected, this pin is used as serial clock pin. If not used, please connect this pin to VCC.	I
31	RS	Display data / Command selection pin D/CX='1': Display data. D/CX='0': Command data. If not used, please fix this pin at GND level.	I
32	CS	Chip select input pin ("Low" enable). When it is not used, please fix this pin at VCC.	I
33	VCC	Power supply voltage (VCI=2.5V-3.3V).	P
34	VCC		P
35	GND	Ground.	P
36	GND		P
37	LEDK4	LED Cathode 4.	P
38	LEDK3	LED Cathode 3.	P
39	LEDK2	LED Cathode 2.	P
40	LEDK1	LED Cathode 1.	P
41	LEDA	LED Anode.	P
42	XR(NC)	Touch panel Right Glass Terminal	A/D
43	YD(NC)	Touch panel Bottom Film Terminal	A/D
44	XL(NC)	Touch panel LIFT Glass Terminal	A/D
45	YU(NC)	Touch panel Top Film Terminal	A/D



4. LCD Optical Characteristics

4.1 Optical specification

Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
*1) Threshold Voltage	Vsat	3.7	3.8	3.9	V	Fig.2
	Vth	1.9	2.0	2.1	V	
*1) Transmittance	T(%)	3.86	4.40	-	%	Fig.1
*1) Contrast Ratio	C/R	400	500	-		
*1) Response Time	Tr+Tf	-	35	50	msec	Fig.3
*2) CIE Color Coordinate	Rx	0.640	0.660	0.680		
	Ry	0.297	0.317	0.337		
	Gx	0.240	0.260	0.280		
	Gy	0.555	0.575	0.595		
	Bx	0.121	0.141	0.161		
	By	0.055	0.075	0.095		
	Wx	0.275	0.295	0.315		
	Wy	0.297	0.317	0.337		
*1) Viewing Angle	Θl	-	80	-	Degree	C/R>10 Fig.4
	Θr	-	80	-		
	Θu	-	80	-		
	Θd	-	80	-		

4.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: 25±2℃
- 15min. warm-up time.



4.3 Measuring Equipment

■ FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

FIG. 1 Optical Characteristic Measurement Equipment and Method

Pritchard 880 System

[Test Equipment Set Up]

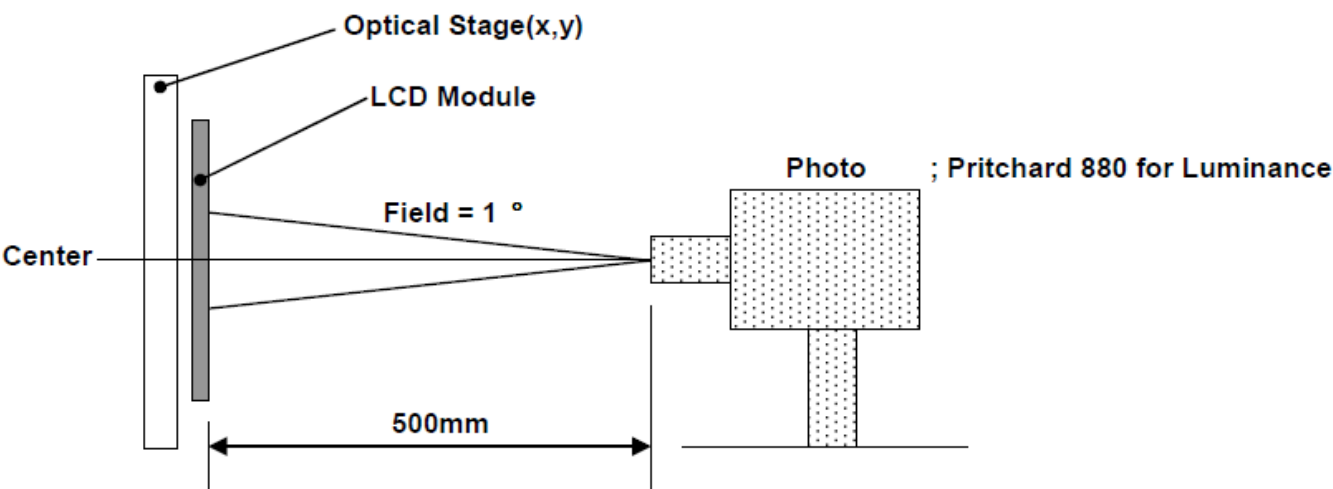
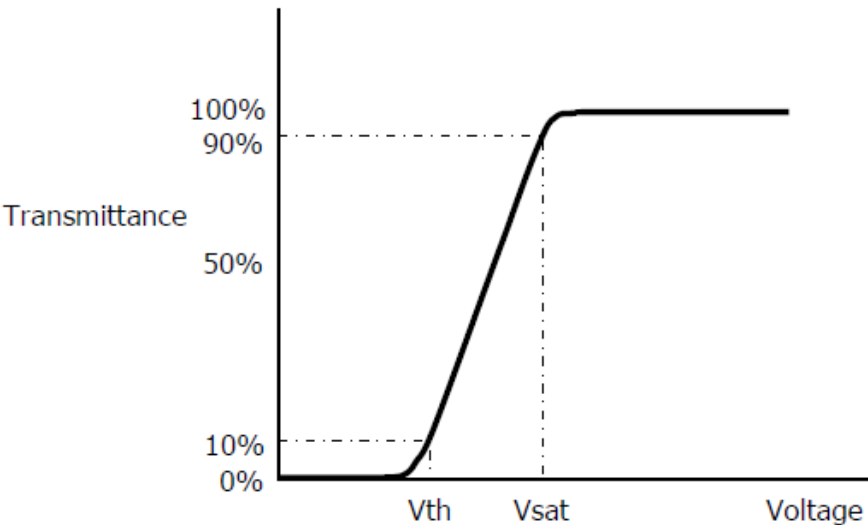


FIG. 2 The definition of Vth and Vsat



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FIG. 4 The definition of viewing angle

<dimension of viewing angle range>

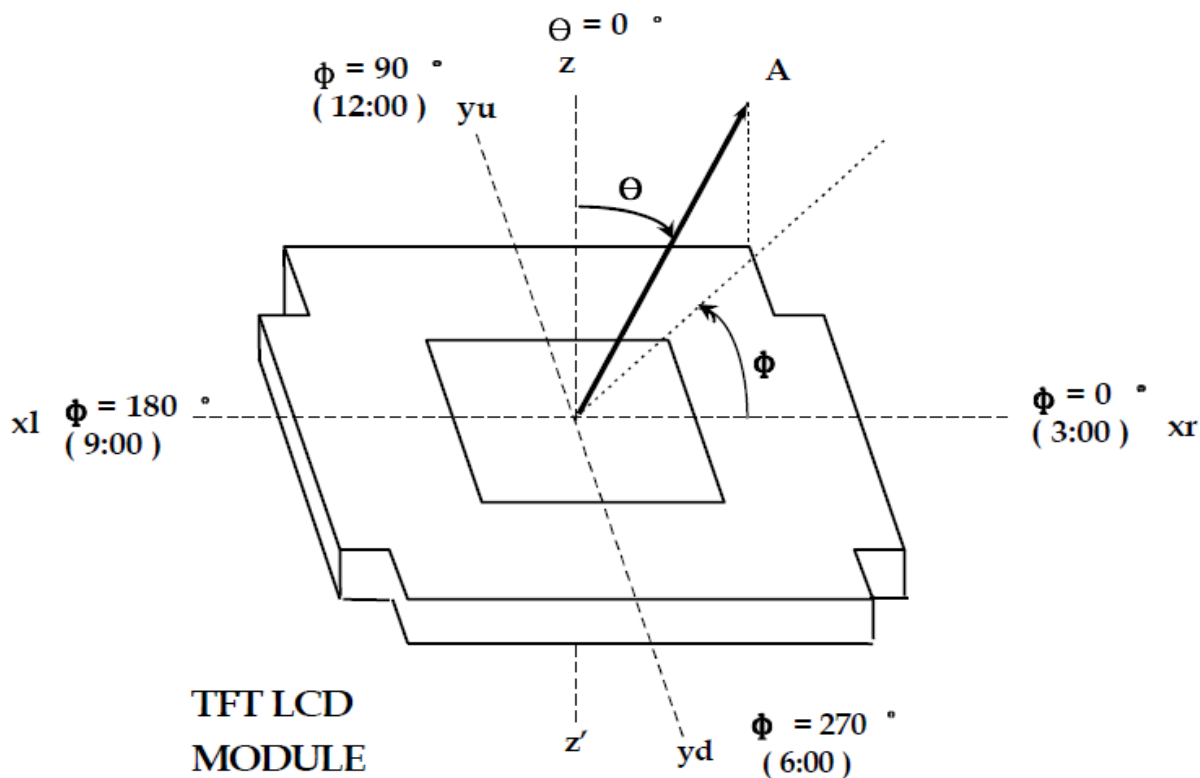
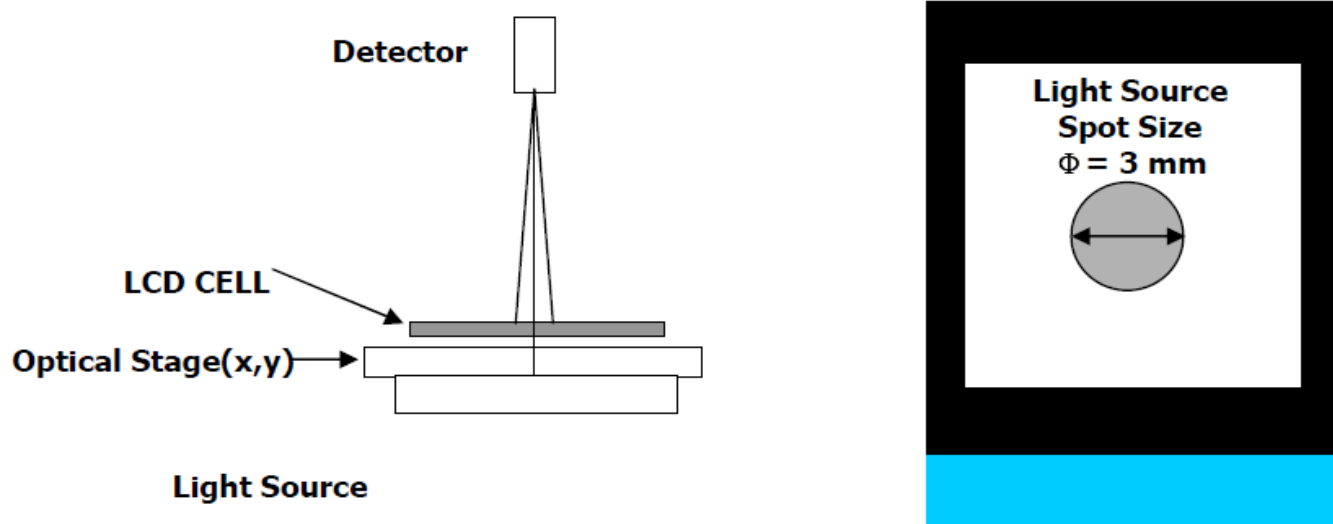


FIG. 5 Response Time Measurement Equipment and Method

DMS 803 System



<Transmissive Mode>

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5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Digital interface supply Voltage	VDDIO	-0.3	4.6	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.4	3..3	4.2	V	
Digital interface supply Voltage	VDDIO	1.65	3.3	4.2	V	
Normal mode Current consumption	IDD	--	8	--	mA	
Level input voltage	V _{IH}	0.7V _{DDIO}		VDDIO	V	
	V _{IL}	GND		0.3V _{DDIO}	V	
Level output voltage	V _{OH}	0.8VDDIO		VDDIO	V	
	V _{OL}	GND		0.2VDDIO	V	

5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 4 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I _F	60	80	--	mA	
Forward Voltage	V _F	--	3.2	--	V	
LCM Luminance	L _V	--	450	--	cd/m2	I _F =80mA

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LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	

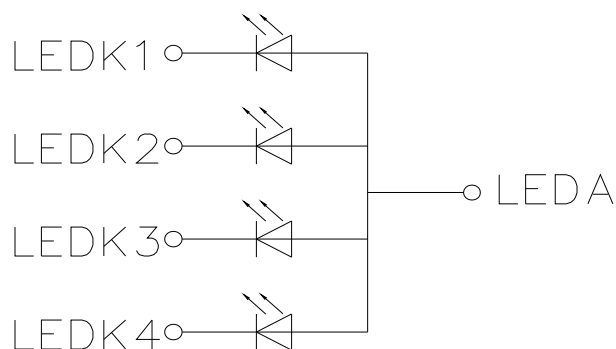
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at

Ta=25°C and IL=80mA. The LED lifetime could be decreased if operating IL is larger than 80mA. The

constant current driving method is suggested.



LED CIRCUIT DIAGRAM:

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常备库存
Standing Stock

长期供货
Long Time supply

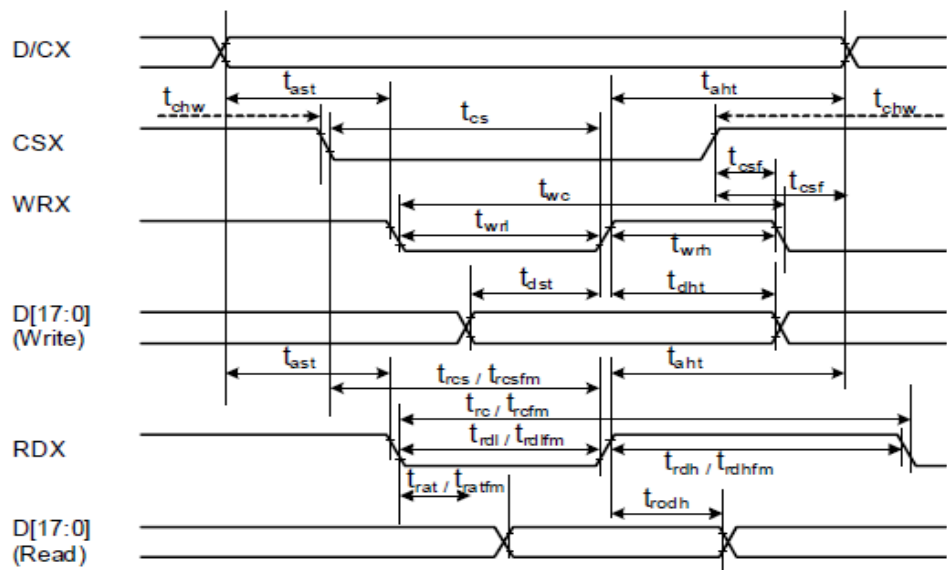
支持小量
NO MOQ

品种齐全
In Full Range



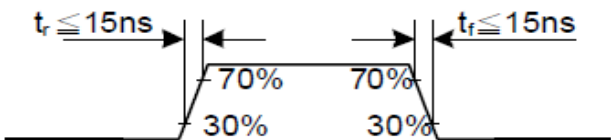
6. AC Characteristic

6.1. Display Parallel Interface Timing Characteristics: 18/16/9/8-bit bus



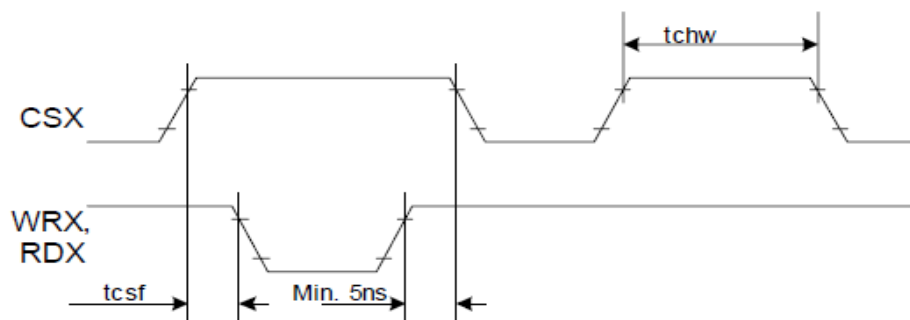
Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" Pulse Width	0	-	ns	
	tcs	Chip Select setup time (Write)	20	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	80	-	ns	
	twrh	Write Control pulse H duration	25	-	ns	
	twrl	Write Control pulse L duration	25	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration (ID)	90	-	ns	
	trdl	Read Control pulse L duration (ID)	45	-	ns	
RDX (FM)	trcfm	Read cycle (FM)	450	-	ns	
	trdhfm	Read Control pulse H duration (FM)	90	-	ns	
	trdlfm	Read Control pulse L duration (FM)	355	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	tdst	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Data hold time	10	-	ns	
	trat	Read access time (ID)	-	40	ns	
	tratfm	Read access time (FM)	-	340	ns	
	todh	Output disable time	20	-	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, DGND=0V



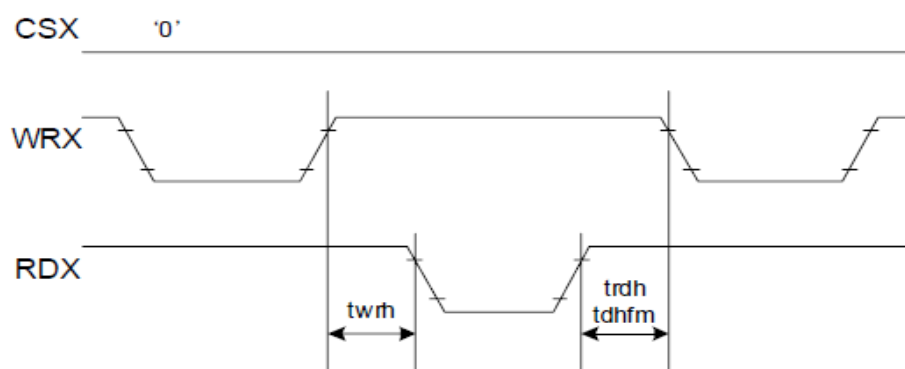
CSX timings:

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Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

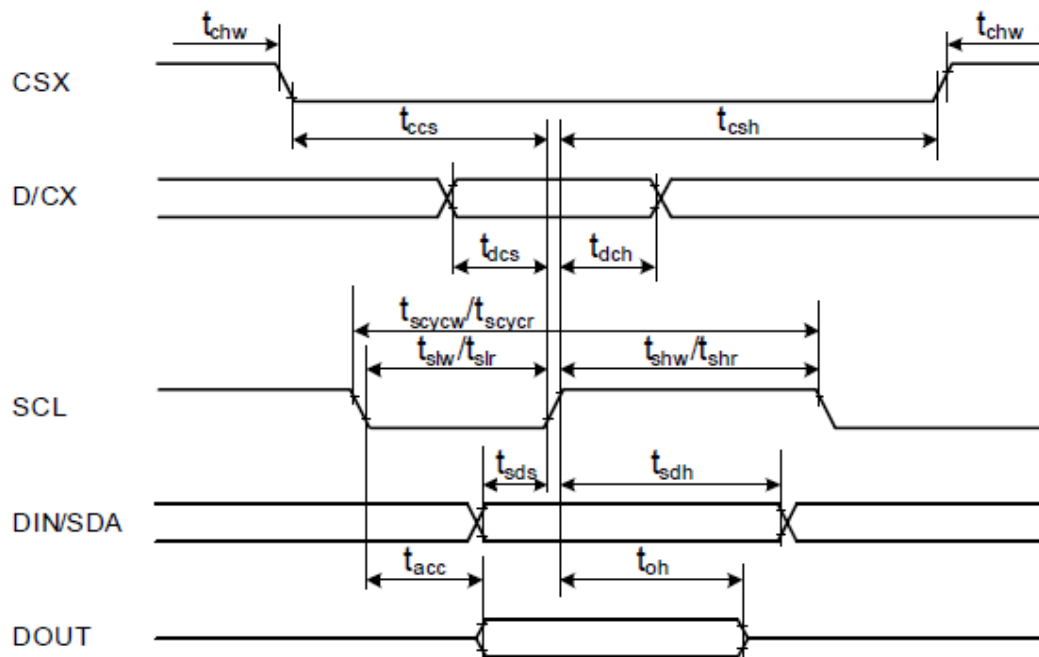


Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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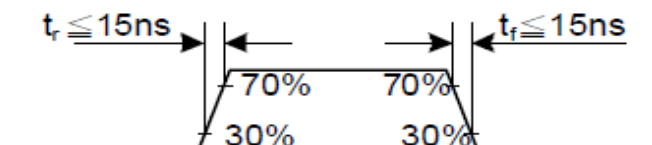


6.2 DBI Type C (SPI) Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcsw	CSX-SCL time (Write)	15	-	ns	
	tcsr	CSX-SCL time (Read)	15	-	ns	
	tcsw	CSX-SCL time (Write)	60	-	ns	
	tcsr	CSX-SCL time (Read)	60	-	ns	
	tchw	CSX "H" pulse time	40	-	ns	
SCL	tscycw	Serial clock cycle (Write)	60	-	ns	
	tshw	SCL "H" pulse width (Write)	15	-	ns	
	tslw	SCL "L" pulse width (Write)	15	-	ns	
	tscycr	Serial clock cycle (Read GRAM)	300	-	ns	
	tshr	SCL "H" pulse width (Read GRAM)	110	-	ns	
	tslr	SCL "L" pulse width (Read GRAM)	110	-	ns	
	tscycr	Serial clock cycle (Read ID)	150	-	ns	
	tshr	SCL "H" pulse width (Read GRAM)	54	-	ns	
D/CX	tdcs	D/CX setup time	7	-	ns	
	tdch	D/CX hold time	7	-	ns	
SDA (Input) (Output)	tacc	Access time	10	50	ns	For maximum CL=30pF
	toh	Output disable time	15	50	ns	For minimum CL=8pF
	tsds	Data setup time	7	-		
	tsdh	Data hold time	7	-		

Note: $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $V_{DDI}=1.65\text{V}$ to 3.3V , $V_{DD}=2.5\text{V}$ to 3.0V , $AGND=DGND=0\text{V}$



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常备库存
Standing Stock

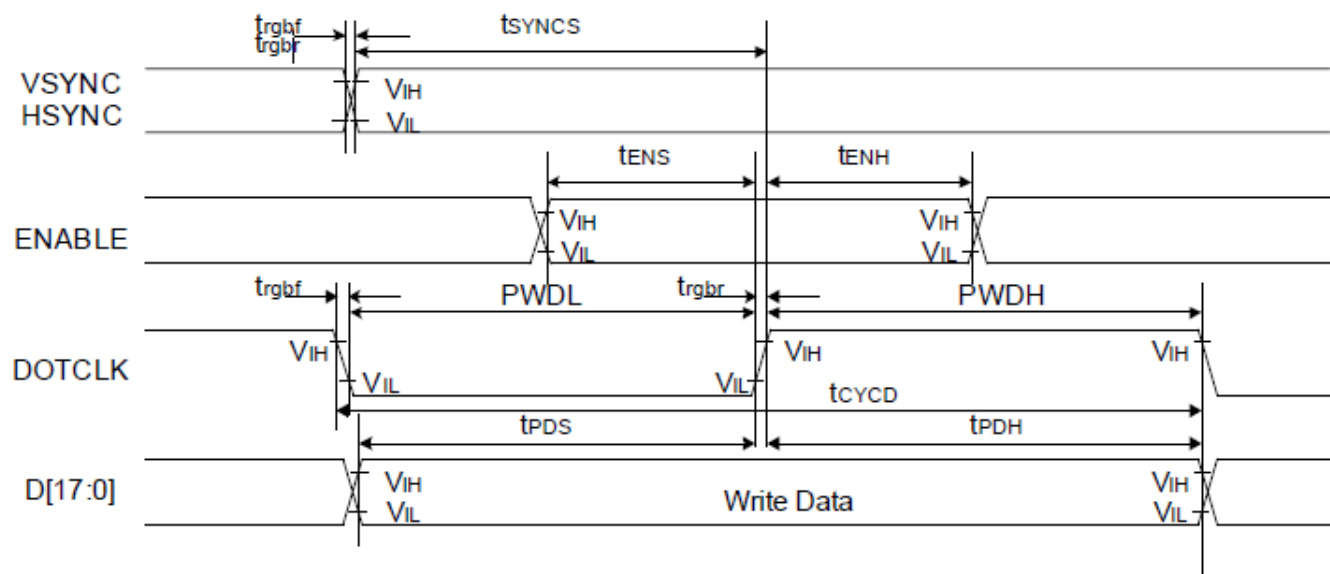
长期供货
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支持小量
NO MOQ

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In Full Range

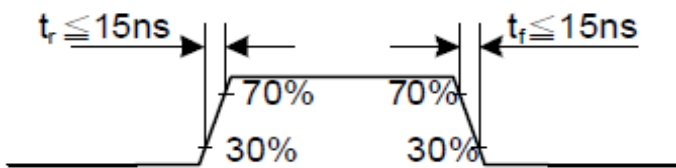


6.3 DPI Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	tENS	ENABLE setup time	15	-	ns	
	tENH	ENABLE hold time	15	-	ns	
D[17:0]	tPOS	Data setup time	15	-	ns	
	tPDH	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tCYCD	DOTCLK cycle time	100	-	ns	
	tRGBR, tRGBF	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	tSYNCS	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	tSYNCH	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	tENS	ENABLE setup time	15	-	ns	
	tENH	ENABLE hold time	15	-	ns	
D[17:0]	tPOS	Data setup time	15	-	ns	
	tPDH	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	tCYCD	DOTCLK cycle time	100	-	ns	
	tRGBR, tRGBF	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.0V, AGND=DGND=0V





6.4 Reset Timing Characteristics

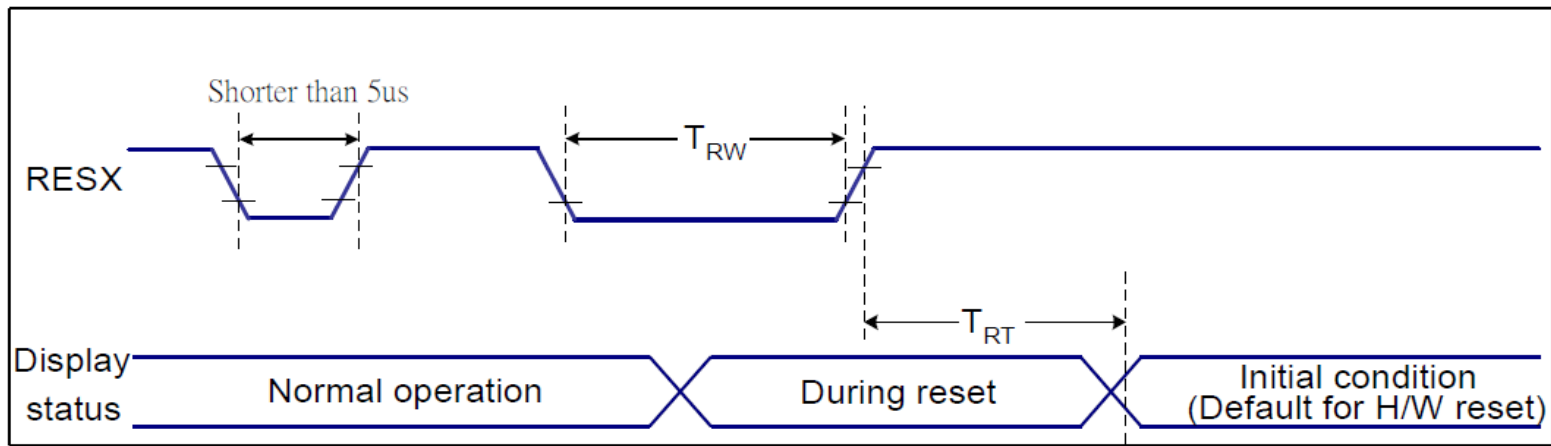


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 8 Reset Timing

Notes:

- 1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
- 2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

- 3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.
- 4. Spike Rejection also applies during a valid reset pulse as shown below:

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7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

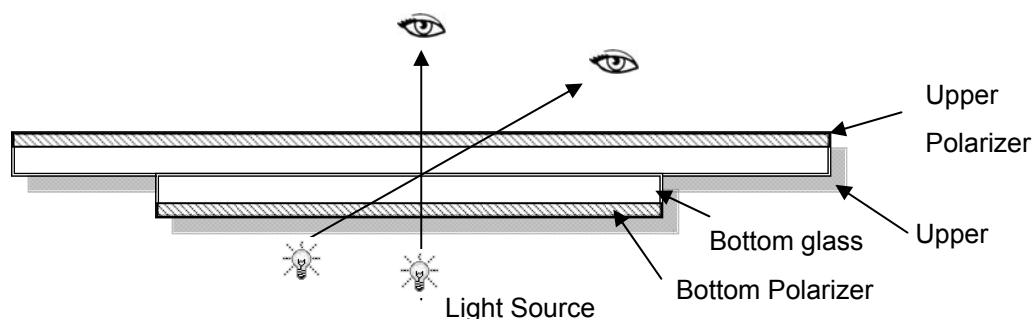
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

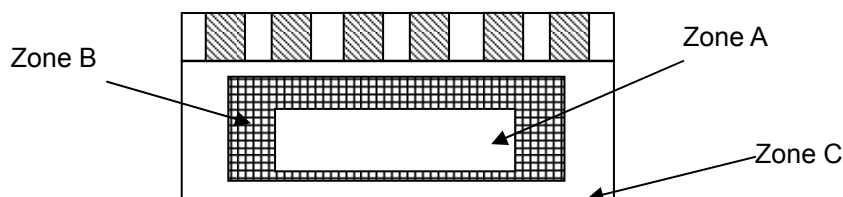
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

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7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

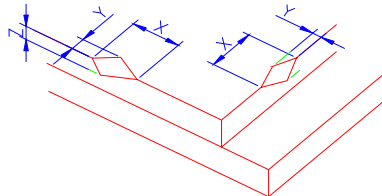
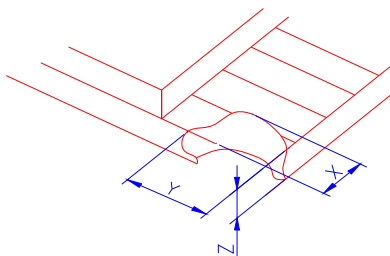
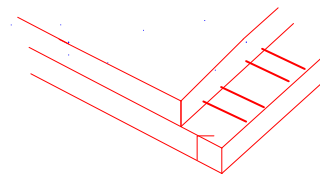
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

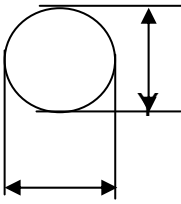
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	



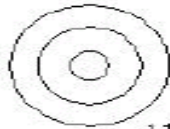


7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	<div></div> <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	<div></div> <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	<div></div> <div>Crack Not allowed</div>							

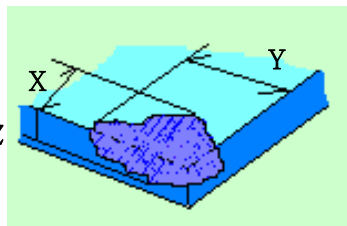
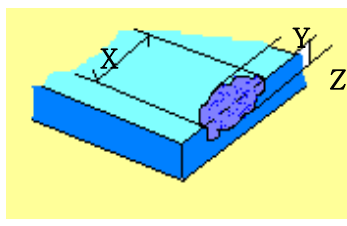


2.0	Spot defect	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)																													
	<div></div> <div>X</div> <div>Φ=(X+Y)/2</div>	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Accep able Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.10</td><td colspan="2">Ignore</td><td rowspan="4">Ignor</td></tr><tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance ≥ 10mm)</td></tr><tr><td>0.20<Φ≤0.25</td><td colspan="2">2</td></tr><tr><td>Φ > 0.25</td><td colspan="2">0</td></tr></table>					Zone Size (mm)	Accep able Qty			A	B	C	Φ≤0.10	Ignore		Ignor	0.10<Φ≤0.20	3(distance ≥ 10mm)		0.20<Φ≤0.25	2		Φ > 0.25	0						
	Zone Size (mm)	Accep able Qty																													
		A	B	C																											
	Φ≤0.10	Ignore		Ignor																											
	0.10<Φ≤0.20	3(distance ≥ 10mm)																													
	0.20<Φ≤0.25	2																													
	Φ > 0.25	0																													
	②Dim spot (LCD/TP/Polarizer dim dot, light leakage、dark spot)																														
	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.1</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>0.10<Φ≤0.20</td><td colspan="2">3(distance ≥ 10mm)</td></tr><tr><td>0.20<Φ≤0.30</td><td colspan="2">2</td></tr><tr><td>Φ > 0.30</td><td colspan="2">0</td></tr></table>						Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.1	Ignore		Ignore	0.10<Φ≤0.20	3(distance ≥ 10mm)		0.20<Φ≤0.30	2		Φ > 0.30	0						
	Zone Size (mm)	Acceptable Qty																													
		A	B	C																											
	Φ≤0.1	Ignore		Ignore																											
	0.10<Φ≤0.20	3(distance ≥ 10mm)																													
	0.20<Φ≤0.30	2																													
	Φ > 0.30	0																													
	③ Polarizer accidented spot																														
	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.2</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.3<Φ≤0.5</td><td colspan="2">2(distance ≥ 10mm)</td></tr><tr><td>Φ>0.5</td><td colspan="2">0</td></tr></table>						Zone Size (mm)	Acceptable Qty			A	B	C	Φ≤0.2	Ignore		Ignore	0.3<Φ≤0.5	2(distance ≥ 10mm)		Φ>0.5	0									
	Zone Size (mm)	Acceptable Qty																													
		A	B	C																											
	Φ≤0.2	Ignore		Ignore																											
	0.3<Φ≤0.5	2(distance ≥ 10mm)																													
	Φ>0.5	0																													
Line defect (LCD/TP /Polarizer black/white line, scratch, stain)	<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>Φ≤0.03</td><td>Igno e</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr><tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr><tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr></table>					Width(mm)	Length(mm)	Acceptable Qty			A	B	C	Φ≤0.03	Igno e	Ignore		Ignore	0.03<W≤0.05	L≤3.0	N≤2		0.05<W≤0.08	L≤2.0	N≤2		0.08<W	Define as spot defect			
Width(mm)	Length(mm)	Acceptable Qty																													
		A	B	C																											
Φ≤0.03	Igno e	Ignore		Ignore																											
0.03<W≤0.05	L≤3.0	N≤2																													
0.05<W≤0.08	L≤2.0	N≤2																													
0.08<W	Define as spot defect																														



3.0	Polarizer Bubble	<table><tr><th rowspan="2">Zone Size (mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.2$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.2 < \Phi \leq 0.4$</td><td colspan="2">3(distance ≥ 10 m)</td></tr><tr><td>$0.4 < \Phi \leq 0.6$</td><td colspan="2">2</td></tr><tr><td>$0.6 < \Phi$</td><td colspan="2">0</td></tr></table>	Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.2$	Ignore		Ignore	$0.2 < \Phi \leq 0.4$	3(distance ≥ 10 m)		$0.4 < \Phi \leq 0.6$	2		$0.6 < \Phi$	0			
Zone Size (mm)	Acceptable Qty																							
	A	B	C																					
$\Phi \leq 0.2$	Ignore		Ignore																					
$0.2 < \Phi \leq 0.4$	3(distance ≥ 10 m)																							
$0.4 < \Phi \leq 0.6$	2																							
$0.6 < \Phi$	0																							
4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.																						
5.0	TP Related	TP bubble/ accidented spot	<table><tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.1$</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>$0.1 < \Phi \leq 0.25$</td><td colspan="2">3 (distance \geq</td></tr><tr><td>$0.25 < \Phi \leq 0.3$</td><td colspan="2">2</td></tr><tr><td>$0.3 < \Phi$</td><td colspan="2">0</td></tr></table>	Size Φ (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore		Ignore	$0.1 < \Phi \leq 0.25$	3 (distance \geq		$0.25 < \Phi \leq 0.3$	2		$0.3 < \Phi$	0		
			Size Φ (mm)		Acceptable Qty																			
				A	B	C																		
			$\Phi \leq 0.1$	Ignore		Ignore																		
			$0.1 < \Phi \leq 0.25$	3 (distance \geq																				
$0.25 < \Phi \leq 0.3$	2																							
$0.3 < \Phi$	0																							
Assembly deflection	beyond the edge of backlight $\leq 0.15\text{mm}$																							
Newton Ring	Newton Ring area $>1/3$ TP area NG Newton Ring area $\leq 1/3$ TP area OK	 1 规律性  2 非规律性  似牛顿环																						



		<div>TP corner broken</div> <div>X : length</div> <div>Y : width</div> <div>Z : height</div>	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>$X \leq 3.0\text{mm}$</td><td>$Y \leq 3.0\text{mm}$</td><td>$Z < \text{LCD thickness}$</td></tr></table> <div>*</div> <div>Circuitry broken is not allowed.</div>	X	Y	Z	$X \leq 3.0\text{mm}$	$Y \leq 3.0\text{mm}$	$Z < \text{LCD thickness}$	
X	Y	Z								
$X \leq 3.0\text{mm}$	$Y \leq 3.0\text{mm}$	$Z < \text{LCD thickness}$								
		<div>TP edge broken</div> <div>X : length</div> <div>Y : width</div> <div>Z : height</div>	<table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>$X \leq 6.0\text{mm}$</td><td>$Y \leq 2.0\text{mm}$</td><td>$Z < \text{LCD thickness}$</td></tr></table> <div>* Circuitry broken is not allowed.</div>	X	Y	Z	$X \leq 6.0\text{mm}$	$Y \leq 2.0\text{mm}$	$Z < \text{LCD thickness}$	
X	Y	Z								
$X \leq 6.0\text{mm}$	$Y \leq 2.0\text{mm}$	$Z < \text{LCD thickness}$								

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed



8. Reliability Test Result

8.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20℃, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70℃90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20℃ ↔ 70℃, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80℃, 96HR	3ea	pass	-
Low Temperature Storage test	- 30℃, 96HR	3ea	pass	-
ESD test	150pF, 330Ω , ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds

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常备库存
Standing Stock

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range



9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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	常备库存 Standing Stock	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range



10. Packing

----TBD-----

Part. No	KD030FM-1	REV	V1.1	Page 27 of 27
	常 备 库 存 Standing Stock	长 期 供 货 Long Time supply	支持小量 NO MOQ	品 种 齐 全 In Full Range