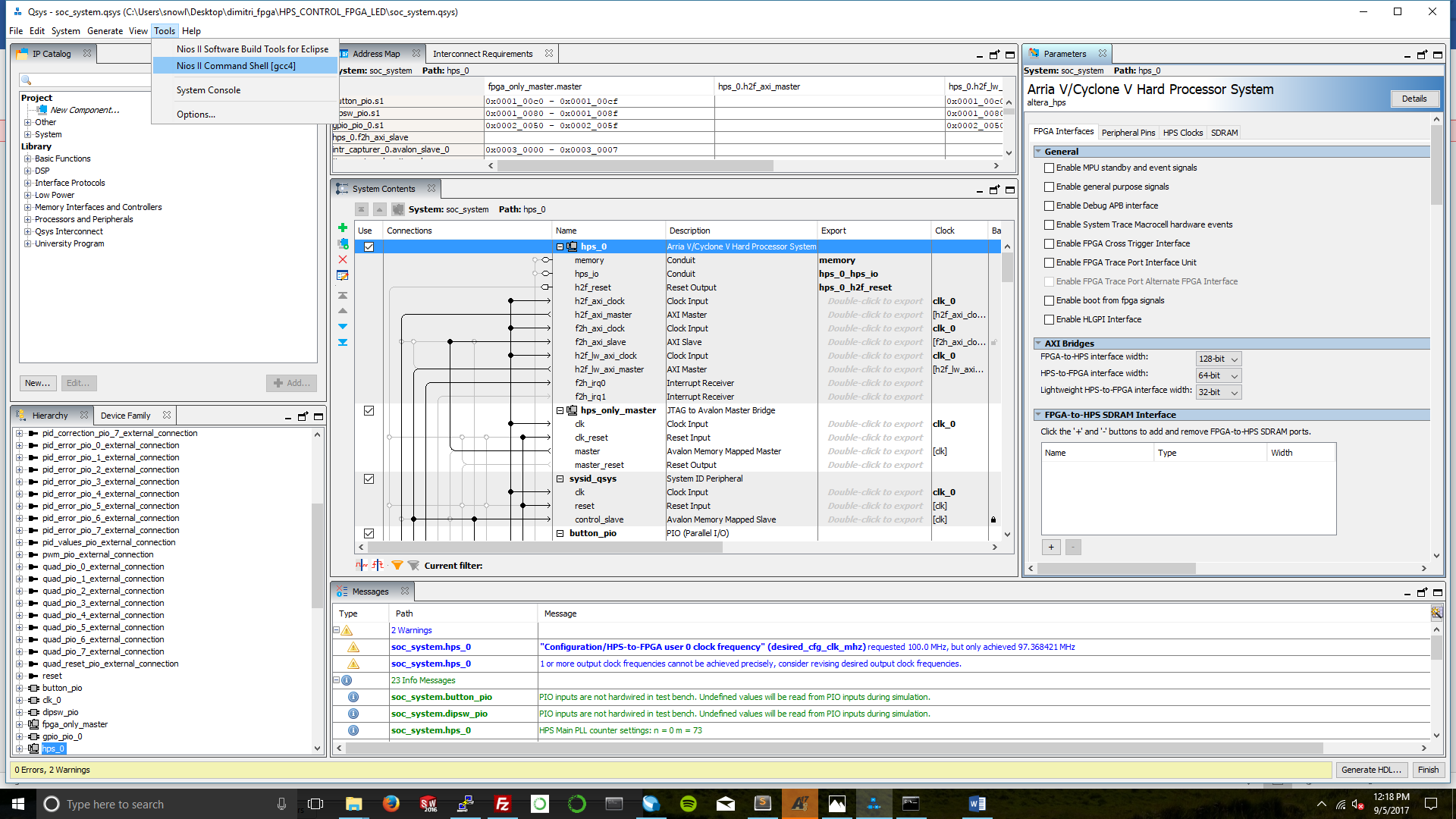
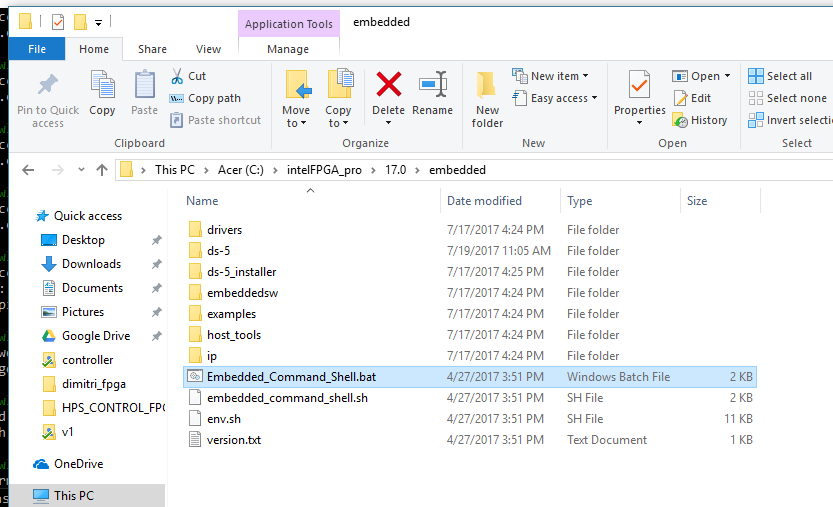
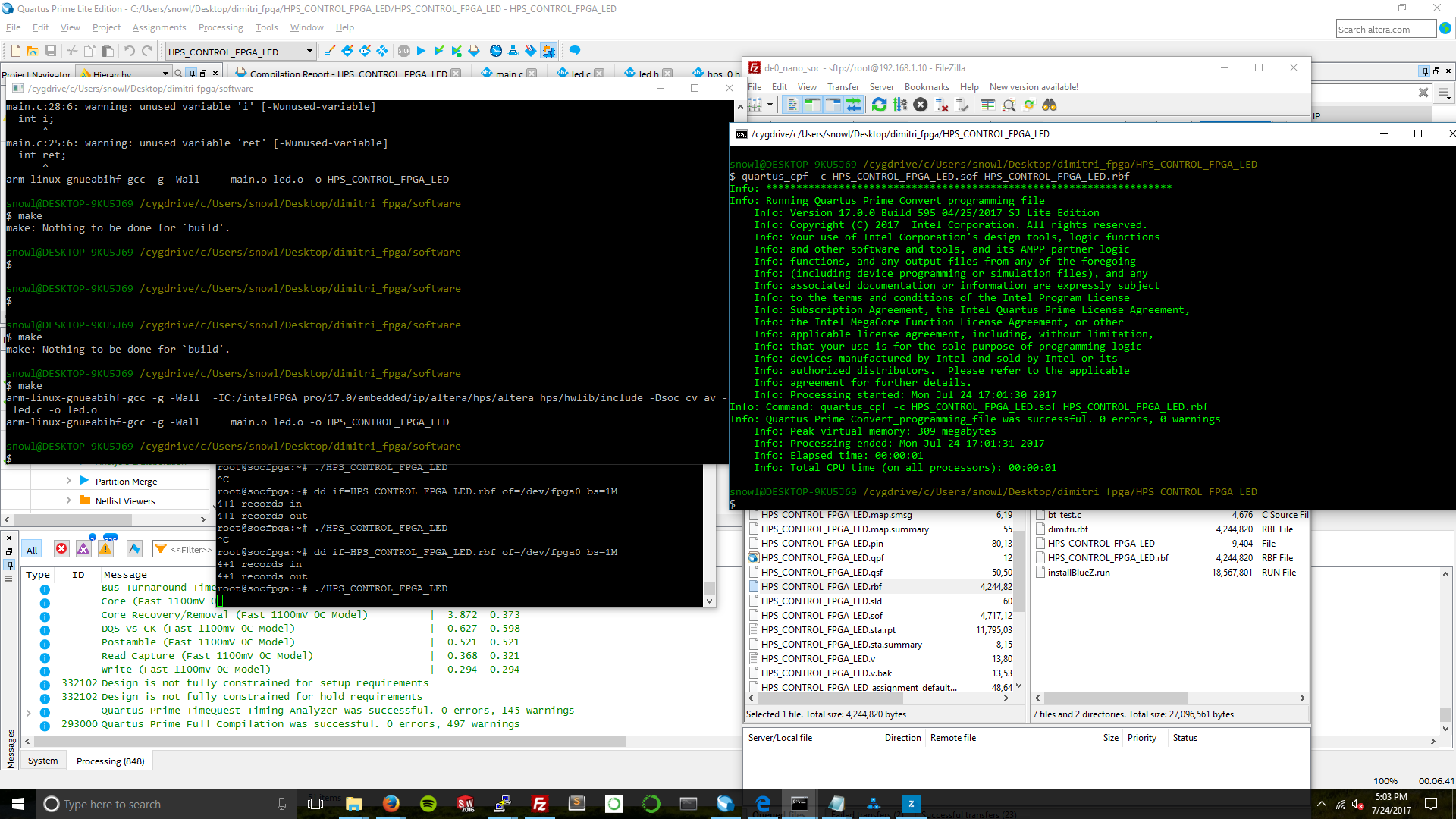
FPGA IP: 192.168.1.10

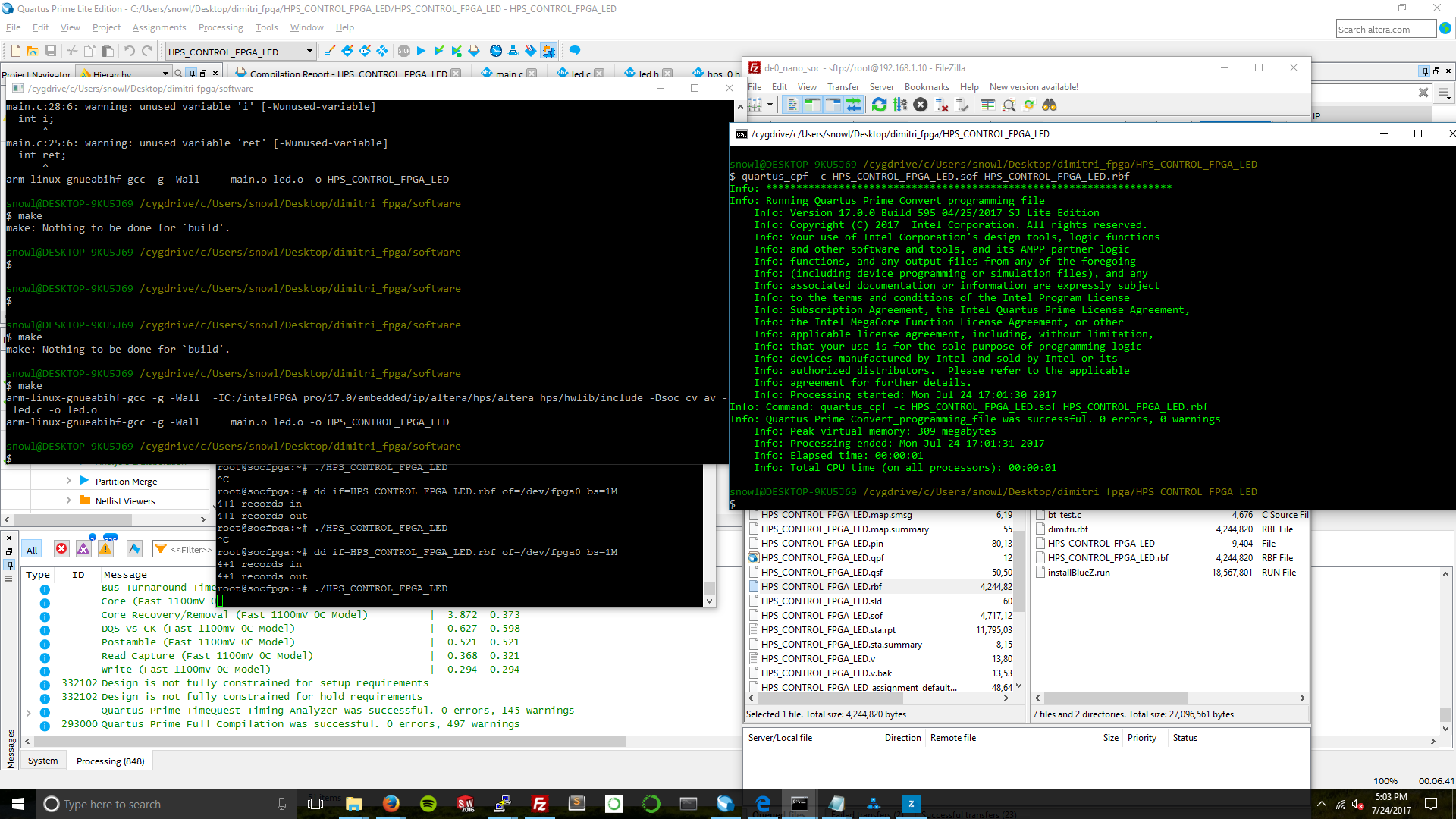
To start CYGWIN shell:



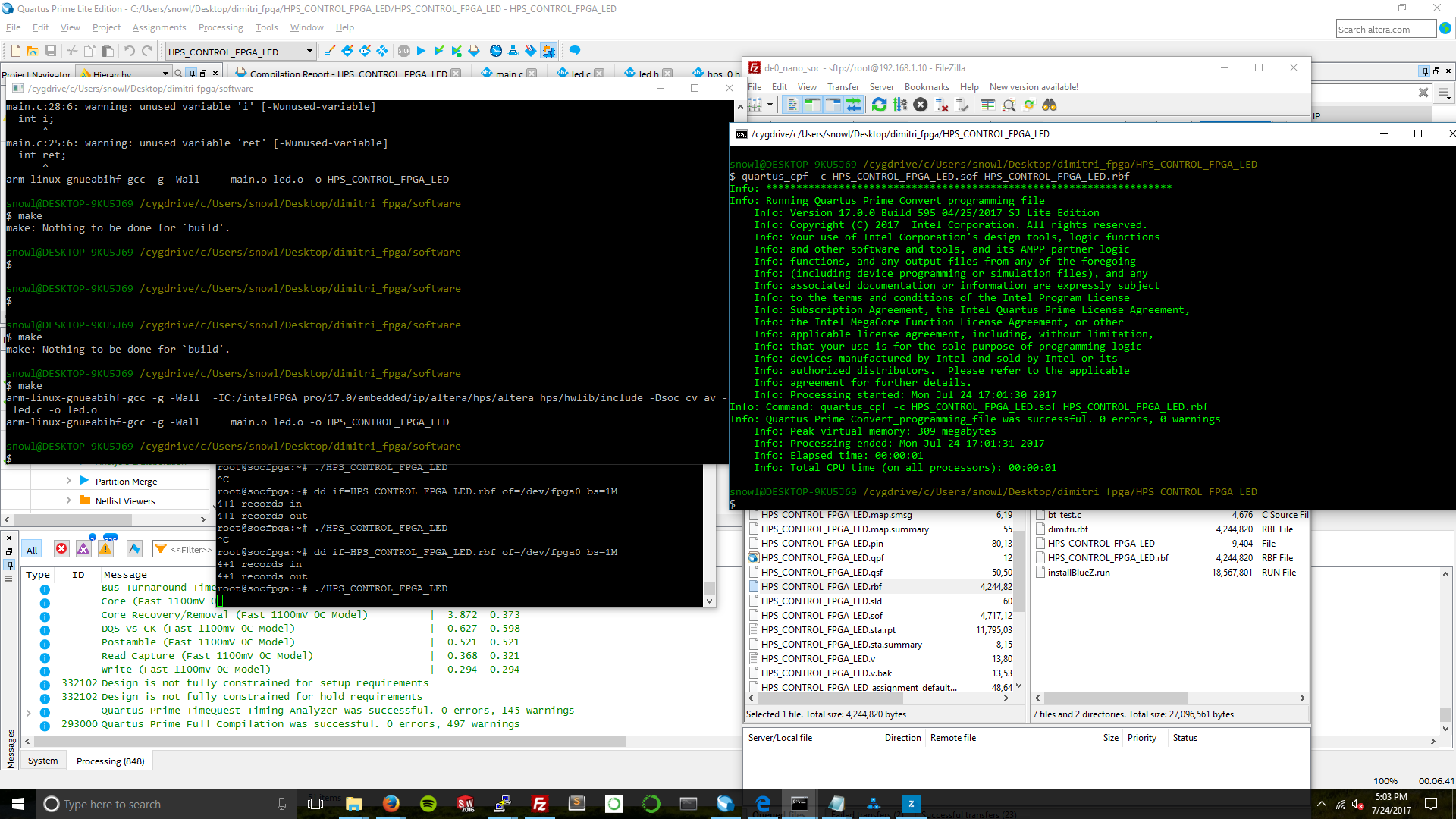
To compile update FPGA fabric code and run controller:



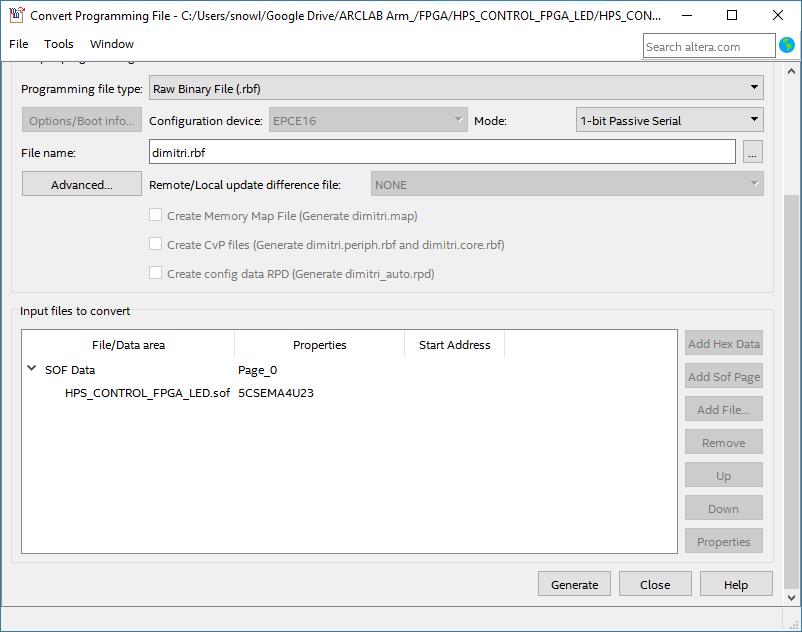




To generate FPGA programming file, first compile in Quartus Prime:



To generate to FPGA flashing files with GUI:



Use QSYS to remap peripherials, add new modules.

To regenerate header files after QSYS generation, copy over to software directory after command:

