



# N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	$r_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A)	
30	0.057 @ V <sub>GS</sub> = 10 V	3.5	
	0.094 @ V <sub>GS</sub> = 4.5 V	2.8	

#### **FEATURES**

- TrenchFET® Power MOSFET
- 100% R<sub>q</sub> Tested

TO-236 (SOT-23) G 1 S 2 Top View Si2306DS (A6)\* \*Marking Code

Ordering Information: Si2306DS-T1

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage		V <sub>DS</sub>	30	,,		
Gate-Source Voltage		V <sub>GS</sub>	±20			
Continuous Drain Current (T <sub>.I</sub> = 150°C) <sup>a, b</sup>	T <sub>A</sub> = 25°C	1-	3.5			
Continuous Diam Current (1) = 150 C)-5-	T <sub>A</sub> = 70°C	ID	2.8	A		
Pulsed Drain Current		I <sub>DM</sub>	16			
Continuous Source Current (Diode Conduction)a, b		I <sub>S</sub>	1.25			
Manifester Device Dissipations h	T <sub>A</sub> = 25°C	Б	1.25	14/		
Maximum Power Dissipation <sup>a, b</sup>	T <sub>A</sub> = 70°C	P <sub>D</sub>	0.80	W		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Na. drawar karaka ka Anaki anta	t ≤ 5 sec	0		100	°C/W
Maximum Junction-to-Ambient <sup>a</sup>	Steady State	$R_{thJA}$	130		

#### Notes

a. Surface Mounted on FR4 Board.

 $b. \quad t \leq 5 \text{ sec.}$ 

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Parameter	Symbol	<b>Test Condition</b>	Min	Тур	Max	Unit	
Static	l l		l	I	I	l	
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{DS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1			v	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS}$ = 0 V, $V_{GS}$ = $\pm 20$ V			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			0.5	0.5 10 μA	
		$V_{DS}$ = 30 V, $V_{GS}$ = 0 V, $T_{J}$ = 55°C			10		
On-State Drain Current <sup>a</sup>		$V_{DS} \ge 4.5 \text{ V}, V_{GS} = 10 \text{ V}$	6				
	I <sub>D(on)</sub>	$V_{DS} \geq$ 4.5 V, $V_{GS}$ = 4.5 V	4			A	
Drain-Source On-State Resistance <sup>a</sup>		$V_{GS} = 10 \text{ V}, I_D = 3.5 \text{ A}$		0.046	0.057	Ω	
	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.8 A		0.070	0.094		
Forward Transconductancea	9fs	$V_{DS} = 4.5 \text{ V}, I_D = 3.5 \text{ A}$		6.9		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.25 A, V <sub>GS</sub> = 0 V		0.8	1.2	V	
Dynamic <sup>b</sup>							
Gate Charge	Qg	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 3.5 A		4.2	7		
Total Gate Charge	Q <sub>gt</sub>			8.5	20	nC	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, \ V_{GS} = 10 \text{ V}, \ I_D = 3.5 \text{ A}$		1.9			
Gate-Drain Charge	$Q_{gd}$			1.35			
Gate Resistance	$R_g$		0.5		2.4	Ω	
Input Capacitance	C <sub>iss</sub>			555			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		120		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			60		1	
Switching							
Turn-On Delay Time	t <sub>d(on)</sub>			9	20		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$		7.5	18	1	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		17	35	ns	
Fall Time	t <sub>f</sub>			5.2	12	1	

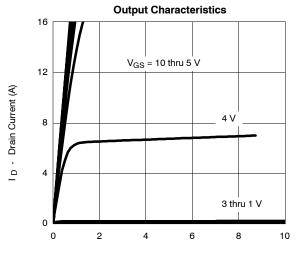
 $<sup>\</sup>begin{tabular}{ll} Notes \\ a. & Guaranteed by design, not subject to production testing. \\ b. & Pulse test; pulse width $\leq 300~\mu s$, duty cycle $\leq 2\%$. \\ \end{tabular}$ 



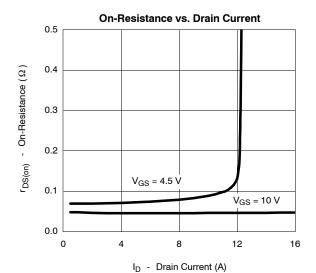


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## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

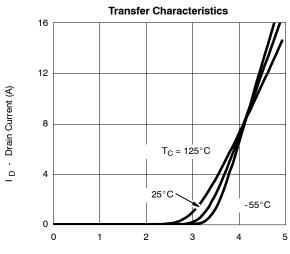


 $V_{\mbox{\footnotesize DS}}\,$  -  $\,$  Drain-to-Source Voltage (V)

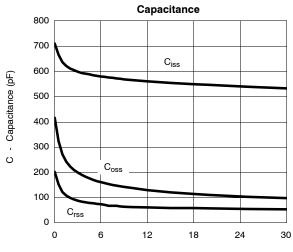


10 V<sub>DS</sub> = 15V I<sub>D</sub> = 3.5 A V<sub>DS</sub> = 15V A V<sub></sub>

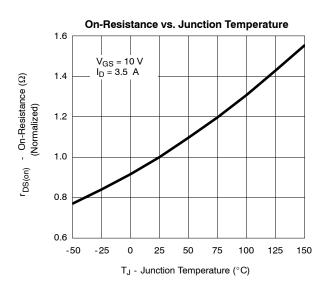
**Gate Charge** 



V<sub>GS</sub> - Gate-to-Source Voltage (V)



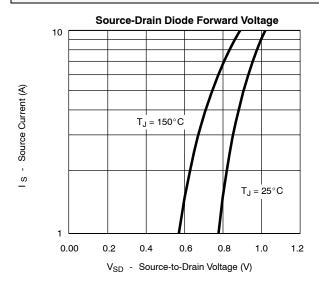
V<sub>DS</sub> - Drain-to-Source Voltage (V)

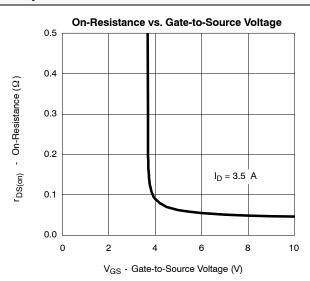


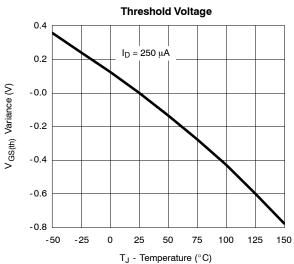
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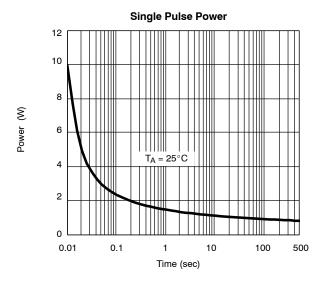


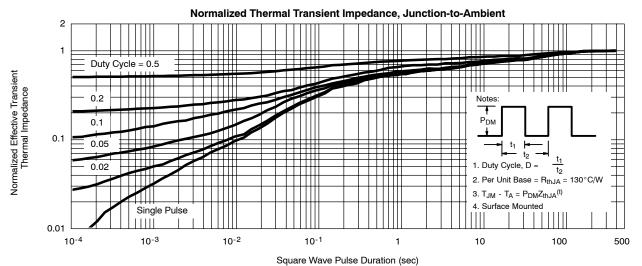
## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)













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