Yi Sun

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Education

South China University of Technology 2023.09 - Present
School of Microelectronics *Guangzhou, China*

- **GPA:** 3.96/4.00 (Ranking 2/96)
- **Relevant Courses:** Verilog and FPGA Design - 99, Microcomputer System and Interfacing Technology - 95, Fundamentals of C++ programming - 98, Calculus - 100, Signals and Systems - 98, Linear Algebra - 95

University of California, Berkeley 2026.01 - 2026.05
School of Electrical Engineering and Computer Science (Visiting Student) *Berkeley, USA*

Publication

◆ T-Trans DPD: TCN-Enhanced Transformer for Wideband Digital Predistortion of Power Amplifiers *(First Author)*

[ICTA2025 Supervised by Prof. Xiang Yi and Prof. Enyi Yao]

Research Experience

❂ High-Performance Heterogeneous ASIC Accelerator for Transformer Models 2025.10 - Present
Supervised by Prof. Tim CHENG and Prof. Chi-Ying TSUI

- Develop an ASIC accelerator featuring a heterogeneous multi-core architecture to boost the performance of Transformer models
- Implement a high-performance hardware solution for Transformers, leveraging heterogeneous cores to balance computation and memory access

❂ Generation and Optimization of Spatial Accelerators for Tensor Workloads 2025.09 - 2025.12
Supervised by Prof. Jieru Zhao

- Implement an Output Stationary (OS) Systolic Array using Verilog for high-performance computing
- Run and reproduce the Gemmini project to explore hardware-software co-design for accelerating matrix multiplication and deep learning workloads
- Investigate mapping strategy and optimized dataflow, resulting in improved data reuse and high hardware utilization

❂ TCN-Enhanced Transformer for Wideband Digital Predistortion of Power Amplifiers 2025.03 - 2025.09
Supervised by Prof. Xiang Yi and Prof. Enyi Yao

- Propose a novel neural network algorithm based on temporal convolutional networks and transformers for digital predistortion, specifically designed to be applicable to both digital power amplifiers (DPA) and analog power amplifiers (APA)
- Use the OpenDPD training framework to complete the digital pre-distortion algorithm and the training effects exceed the baseline models

❂ Millimeter Wave Reconfigurable Low Noise Amplifier Design on 65nm CMOS Process 2024.11 - 2025.10
Supervised by Prof. Li Gao

- Design of a millimeter-wave low-noise amplifier with band reconfigurable functions and good S-parameters, low power and low noise factor in TSMC 65nm CMOS process
- Explore novel reconfigurable inter-stage matching network and output matching network with low Q loss when making reconfigurable functions
- Design and simulation of tri-coupled transformer in matching networks

❂ Analog Front End Design for High-speed Serial Interface Receiver 2025.03 - 2025.08
Supervised by Prof. Guangyin Feng

- Designe a 100Gb/s PAM-4 Analog Front End (AFE) in TSMC 65nm technology, integrating a first-stage CTLE and a two-stage VGA
- Demonstrate 3-12dB peaking at the Nyquist frequency through post-layout simulation, ensuring signal integrity for high-speed transmission

- Extend system bandwidth by utilizing a transformer load in the first-stage VGA to introduce a new pole, achieving a low power envelope of 11mW

❂ Receiver Design Based on Kramers-Kronig Relation 2024.09 - 2024.11
Supervised by Prof. Guangyin Feng

- Conduct system-level modeling of a Kramers-Kronig receiver in MATLAB, reproducing the architecture of a synthesizer-free coherent receiver (Ref: ISSCC2024 12.2)
- Investigate mixed-signal phase reconstruction techniques and developed a compensation algorithm to mitigate phase signal distortion

Awards and Honors

‡Scholarships:

National Scholarship 2023-2024, 2024-2025
10000 CNY/year (Awarded for Two Consecutive Years)

First-Class Scholarship 2023-2024, 2024-2025
30000 CNY/year (Awarded for Two Consecutive Years)

Outstanding Student Scholarship 2024-2025
30000 CNY/year

Holedfound Enterprise Scholarship 2024-2025
8000 CNY/year

Xiao Noodle Enterprise Scholarship 2023-2024
1000 CNY/year

‡Contest Awards:

9th National Integrated Circuit Innovation and Entrepreneurship Competition National Final 2025
Third Prize

9th National Integrated Circuit Innovation and Entrepreneurship Competition South China Regional 2025
First Prize

16th National Undergraduate Mathematics Competition 2024
First Prize

Mathematical Contest in Modeling (MCM) 2024
Honorable Mention

14th APMCM Asia-Pacific Mathematical Contest in Modeling 2024
Third Prize

National Undergraduate Mathematical Modeling Competition Guangdong Division 2024
Winning Prize

Skills

◆ Solid self-learning skills and motivation for continuous improvement:

-Additional Courses (online):

- MIT: 6.S191 Introduction to Deep Learning
  6.5940 TinyML and Efficient Deep Learning Computing
- UC Berkeley: CS 61C Great Ideas in Computer Architecture (Machine Structures)
  EECS 290 Hardware for Machine Learning
- Stanford: CS 217 Hardware Accelerators for Machine Learning
- ISSCC, CICC, ESSERC: Tutorials (Slides & Video)

◆Programming: Verilog, SystemVerilog, C/C++ Programming, Python, MATLAB

◆Framework: PyTorch, Tensorflow

◆IC and FPGA tools: Cadence Virtuoso, Cadence Innovus, Design Compiler, ModelSim, Vivado

◆Others: Visio, OriginPro, PowerPoint, LaTeX, Zotero

◆English (Fluent): TOEFL: 101 (Reading: 28, Listening: 26, Speaking: 23, Writing: 24), CET-6: 688