ELC 2137 Lab 07: Binary Coded Decimal

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Summary

In the last lab, we implemented a 7-segment display. We input numbers in binary, and it outputs in hex. When you get used to it, hex is fine to read, but its not as easy as decimal, particularly for multi-digit numbers. In this lab, you will make a cheat button that will turn the display to decimal and then back to hex.

Q&A

There is no question in lab7.

Results

Firgure 1 is the simulation waveform and ERT of the Add3.

Time (ns):	0	10	20	30	40	50	60	70	80	90	100	110	120	130
num	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101
out	0000	0001	0010	0011	0100	1000	1001	1010	1011	1100	1101	1110	1111	0000

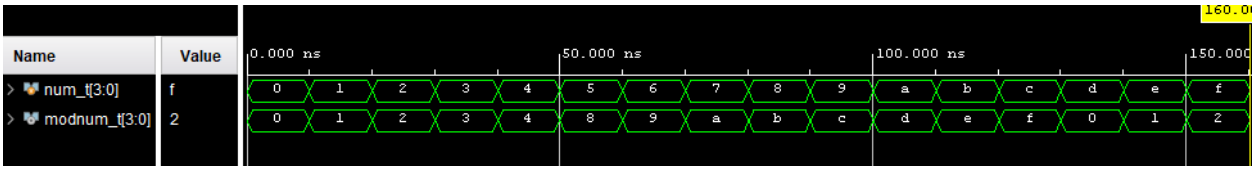

Figure 1: the simulation waveform and ERT of the 4-bit Multiplexer

Firgure 2 is the simulation waveform and ERT of the 6-bit BCD.

Firgure 1 is the simulation waveform and ERT of the Add3.

Code

File Inclusion

Time (ns): 140	0 150	10	20	30	120	130
num	0000	0001	0010	1101	1110	1111
out 0010	0000	0001	0010	1111	0000	0001

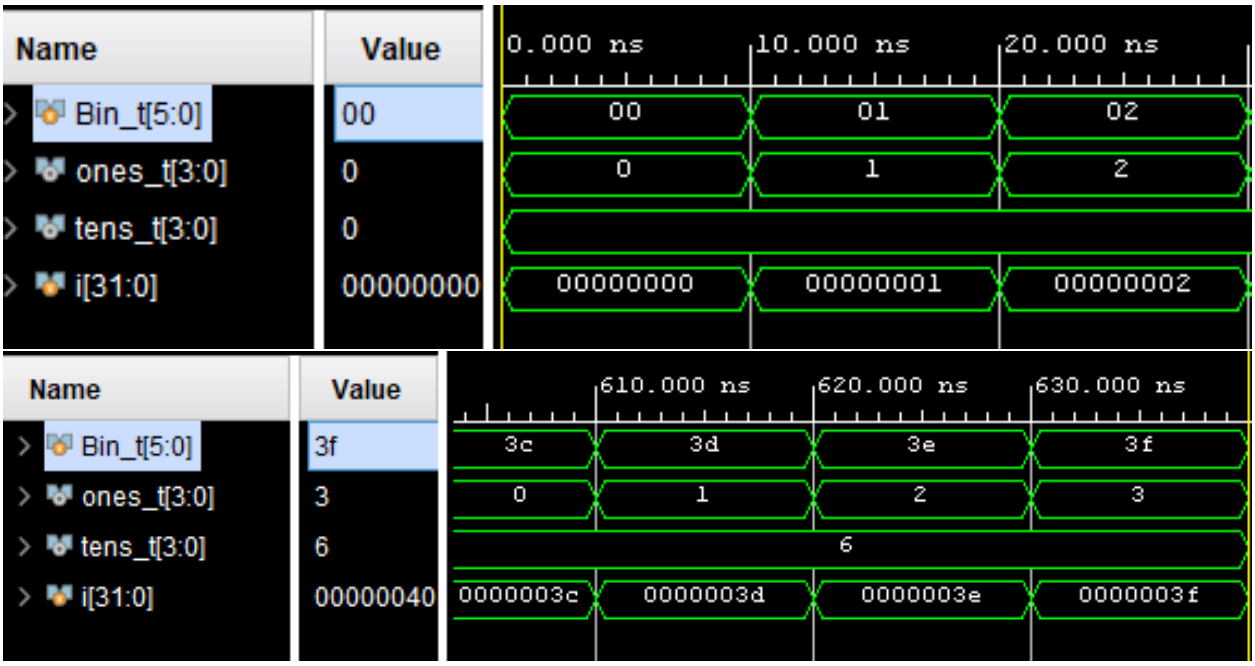

Figure 2: the simulation waveform and ERT of the 4-bit Multiplexer

Listing 1: Add3 Verilog code

```
‘timescale 1ns / 1ps
//
    //////////////////////////////////////////////////////////////////////////////////

// Company: ELC 2137
// Engineer: Yiting Wang
// Create Date: 10/08/2020
//
    //////////////////////////////////////////////////////////////////////////////////



module add3(
    input [3:0] num,
    output reg [3:0] mod
    );

    always @*
        if (num > 4’h4)
            mod = num + 4’h3;
        else
```

Time (ns):	0	10	20	30	40	50	60	70	80	90	100	110	120	130
num	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101
out	0000	0001	0010	0011	0100	1000	1001	1010	1011	1100	1101	1110	1111	0000

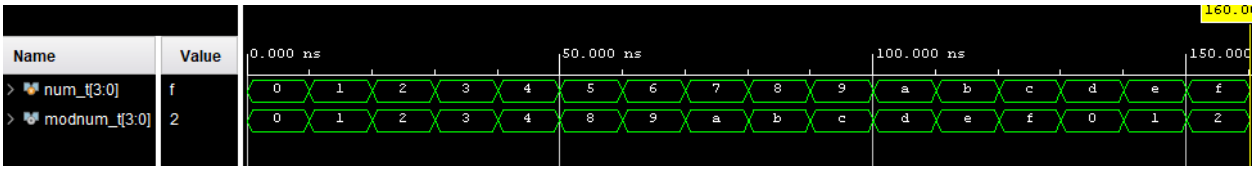

Figure 3: the simulation waveform and ERT of the 4-bit Multiplexer

```
            mod = num;

endmodule
```

File Inclusion

Listing 2: Add3 Multiplexer Test Benches Verilog code

```
‘timescale 1ns / 1ps
//
    //////////////////////////////////////////////////////////////////////////////////

// Company: ELC 2137
// Engineer: Yiting Wang
// Create Date: 10/08/2020
//
    //////////////////////////////////////////////////////////////////////////////////



module add3_test();

    reg [3:0] num_t;
    wire [3:0] mod_t;

    add3 dut(
        .num(num_t),
        .mod(mod_t)
    );


    integer i;

    initial begin
        for (i=4’h0; i<=4’hf; i=i+1) begin
            num_t = i; #10;
        end
        $finish;
    end
```

```
endmodule
```