

# ELC 2137 Lab 04: Subtractor

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September 24, 2020

## Summary

In this lab, it is to compare various implementations of a two-bit adder/subtractor. This is a relatively simple circuit that has sufficient complexity to highlight some important aspects of digital circuit design. After completing this lab, I can describe the operation of a two-bit adder/subtractor, and develop a moderately complex circuit on a breadboard using standard electrical parts, develop my own test procedure and verify operation of the circuit, also I may recognize that digital circuits quickly become complex and difficult to implement in hardware.

## Q&A

1. Why did we use two full adders instead of a half adder and a full adder?

The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry designated as CIN. In here, we use two full adders instead of a half adder and a full adder, cause we need a third input to represent the signed number.

2. How many input combinations would it take to exhaustively test the adder/subtractor?

16.

3. Why were the combinations given in the truth table chosen?

Cause we can use 3 for add and 3 for subtract to figure out the rule for how the two-bit adder/subtractor works

4. Do the results from your adder/subtractor match what you would expect from theory? Explain any discrepancies.

The results are close to, but don't exactly agree with the theory behind it. The MSB is different from what I expected. When the result should be a positive signed number, it shows negative; when the result should be a negative signed number, it shows positive.

## Results

Figure 1 is the picture of my two bit adder/subtractor circuit, I built it based on the two bit adder/subtractor schematic.

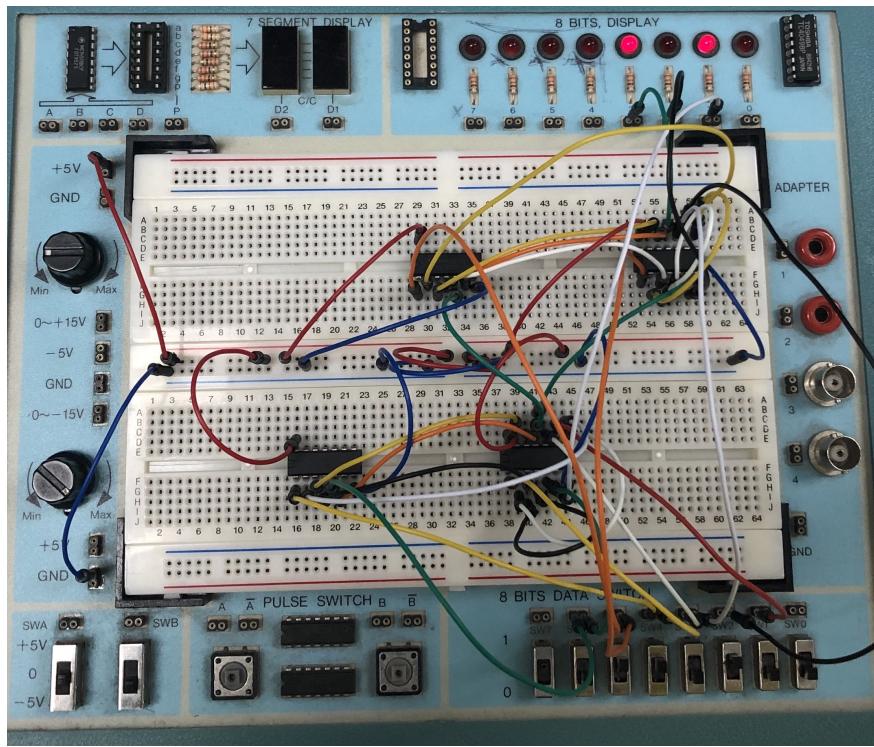


Figure 1: The two bit adder/subtractor Circuit

Figure 2 is the picture of my two-bit adder/subtractor schematic.

Figure 3 is the circuit demonstration page. It has the ERT and instructor signature.

## Code

There is no code required in this lab.

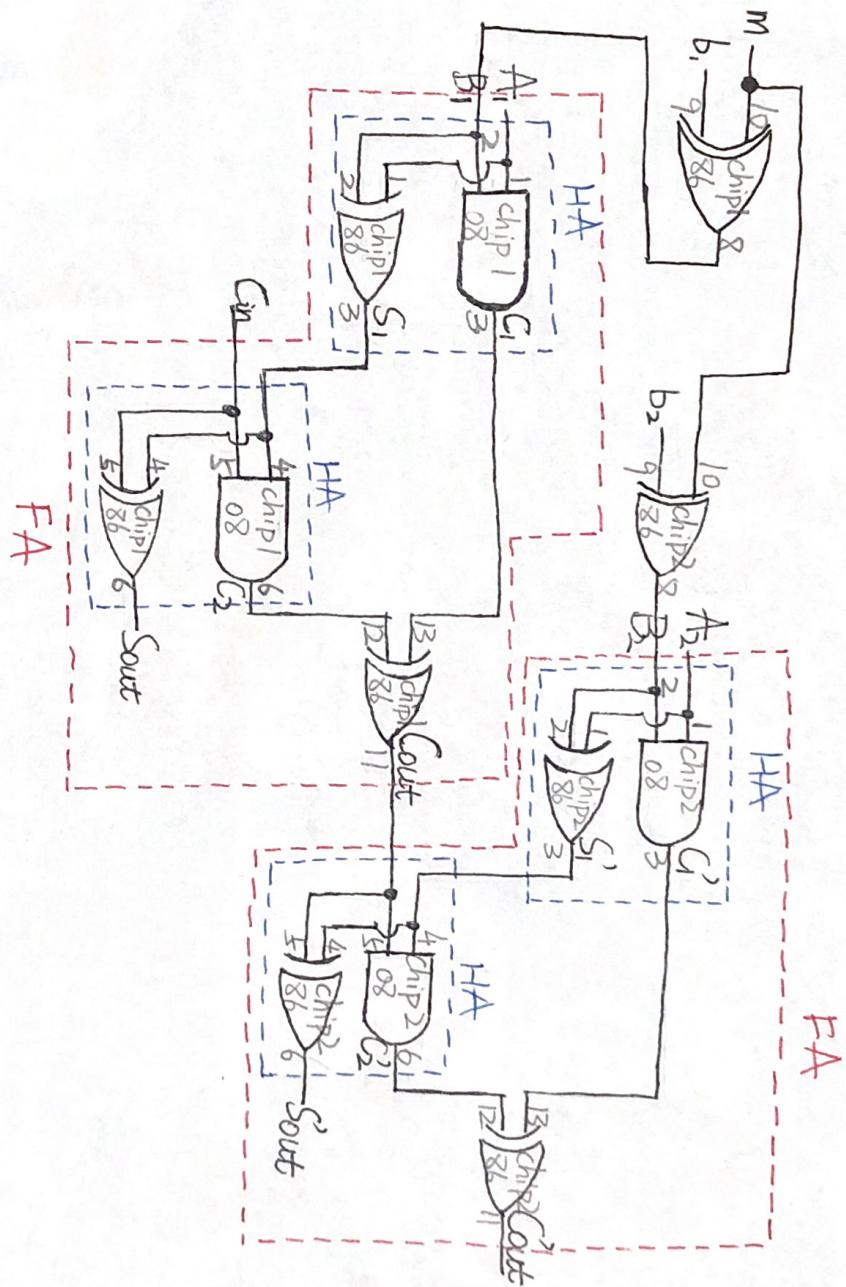


Figure 2: The two-bit adder/subtractor schematic

## Circuit Demonstration Page

Student names:

Y.Ting Wang

### Instructor Signatures

Separate Full Adders

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Two-Bit Adder

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Adder/Subtractor

AKS

Inputs		Expected Results			Actual Results	
A	B	B 2's comp	Sub	Dec	Sub	
00	01	111	111	-1	011	
00	10	110	110	-2	010	
00	11	101	101	-3	001	
01	01	111	000	0	100	
10	01	111	001	1	101	
10	00	000	010	2	110	

Figure 3: The cricuit domonstration page