

# ELC 2137 Lab 03: Adders

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## Summary

Logic circuits began as discrete components, which were then packaged into integrated circuits (ICs or chips) that might contain several individual gates or more complicated circuits. The goals of this Lab are to be able to design logical circuits that implement a desired function, and introduces a family of logic chips (integrated circuits or ICs) that can be used to design simple logic circuits.

## Q&A

1. Which gates could we use for combining the carry bits? Which one should we use and why?  
We should use XOR gate. When there are two 1s as inputs, we need to cut off 1 bit; and when there are 0's and 1s as inputs, we need to keep that. An XOR gate will give you a 0 with two 1s as inputs, and a 1 with one 1's as input.

## Results

Figure 1 is the circuit demonstration page. It has the HA and FA schematics and wiring diagrams, and three instructor signatures.

Figure 2 is the picture of my Half Adder circuit, I built it based on the Half Adder wiring diagrams I draw on the circuit demonstration page.

Figure 3 is the picture of my Full Adder circuit, I built it based on the Full Adder wiring diagrams I draw on the circuit demonstration page.

Figure 4 is the picture of my 2-bit Adder circuit, I built it based on the 2-bit Adder instruction. I built 2 working Full Adders, I connected the carry output of one adder to the carry input of the other adder (instead of a switch).

Table 1 is the Full Adder's expanded truth table. I did this table based on these:  $c_1 = A$  and  $B$ ;  $s_1 = A \text{ xor } B$ ;  $c_2 = s_1 \text{ and } \text{Cin}$ ;  $S = s_2 = s_1 \text{ xor } \text{Cin}$ ;  $\text{Cout} = c_1 \text{ xor } c_2$ . This table also proves that the carry outputs of the first and second stage HAs cannot both be high at the same time.

Table 1: FA expanded truth table

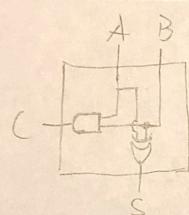
Cin	A	B	c1	s1	c2	s2	Cout	S
0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0	1
0	1	0	0	1	0	1	0	1
0	1	1	1	0	0	0	1	0
1	0	0	0	0	0	1	0	1
1	0	1	0	1	1	0	1	0
1	1	0	0	1	1	0	1	0
1	1	1	1	0	0	1	1	1

## Code

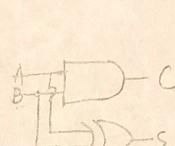
There is no code require in this lab.

## Circuit Demonstration Page

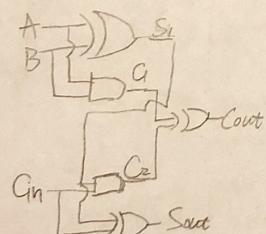
Half adder schematic



Half adder wiring diagram

Half adder: 78

Full adder schematic



Full adder wiring diagram

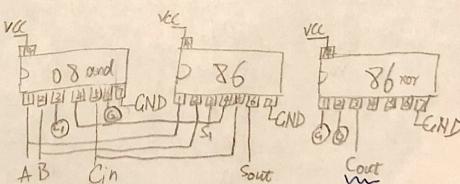
Full adder: 1582-bit adder: 162

Figure 1: The Circuit Demonstration Page

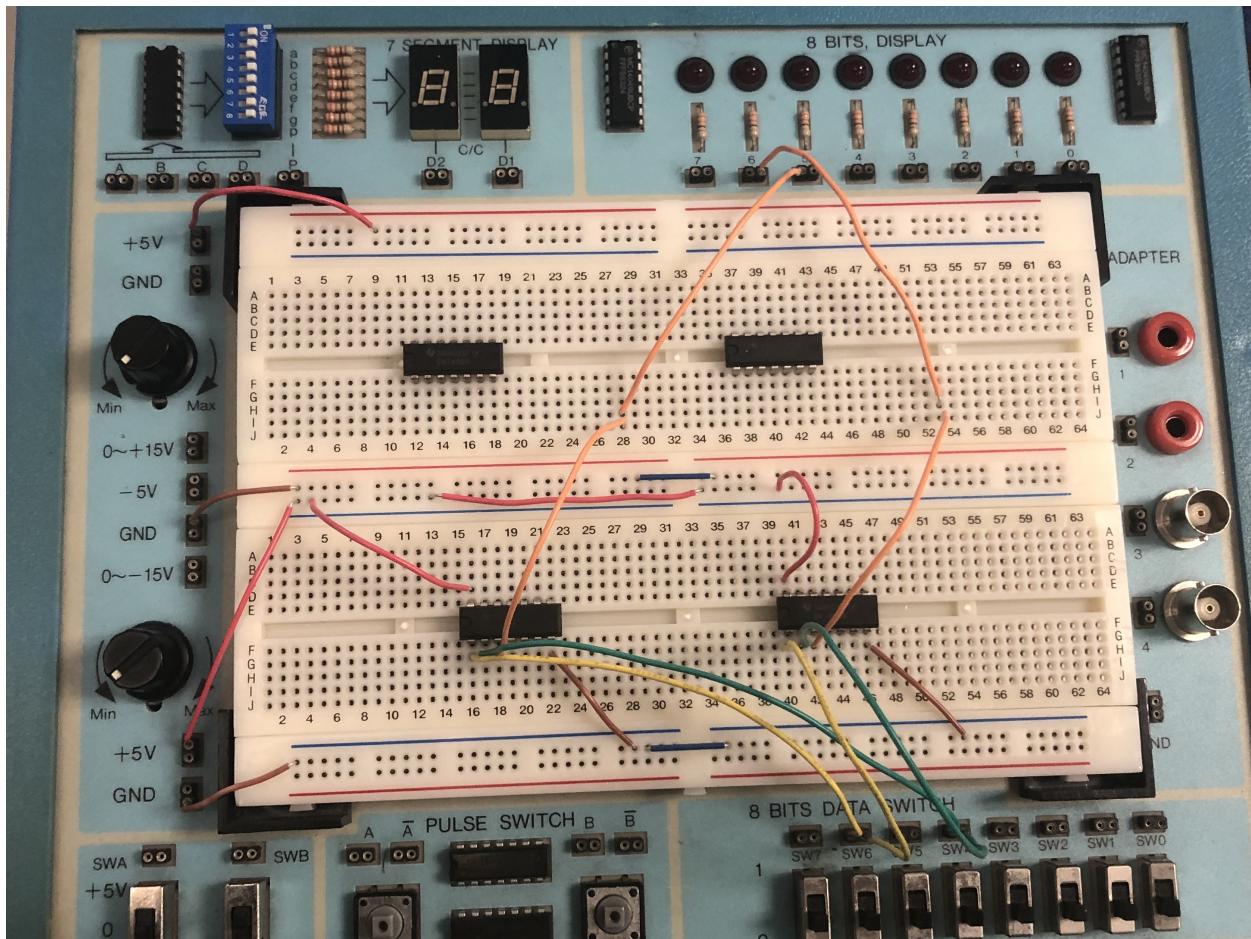


Figure 2: The Half Adder Circuit

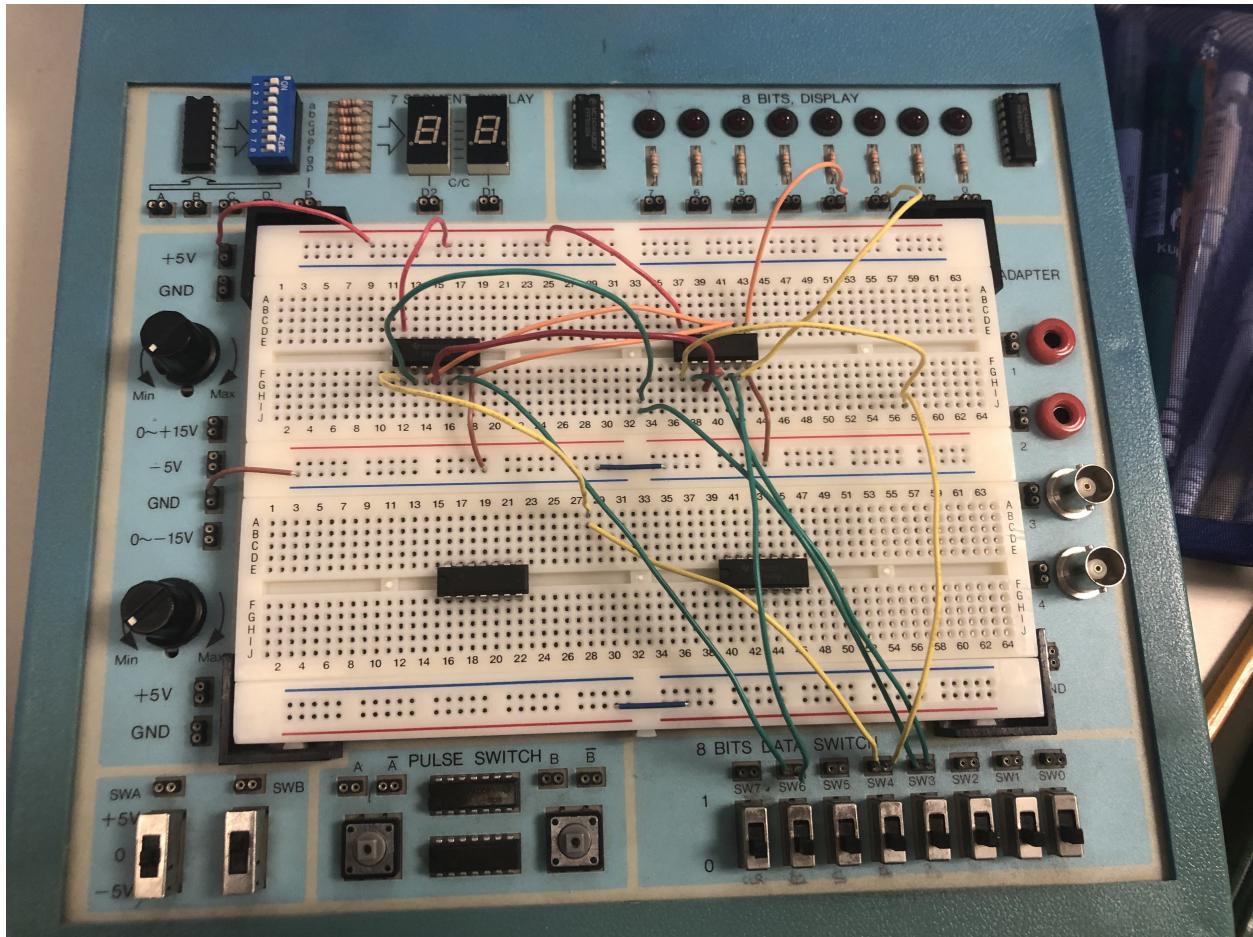


Figure 3: The Full Adder Circuit

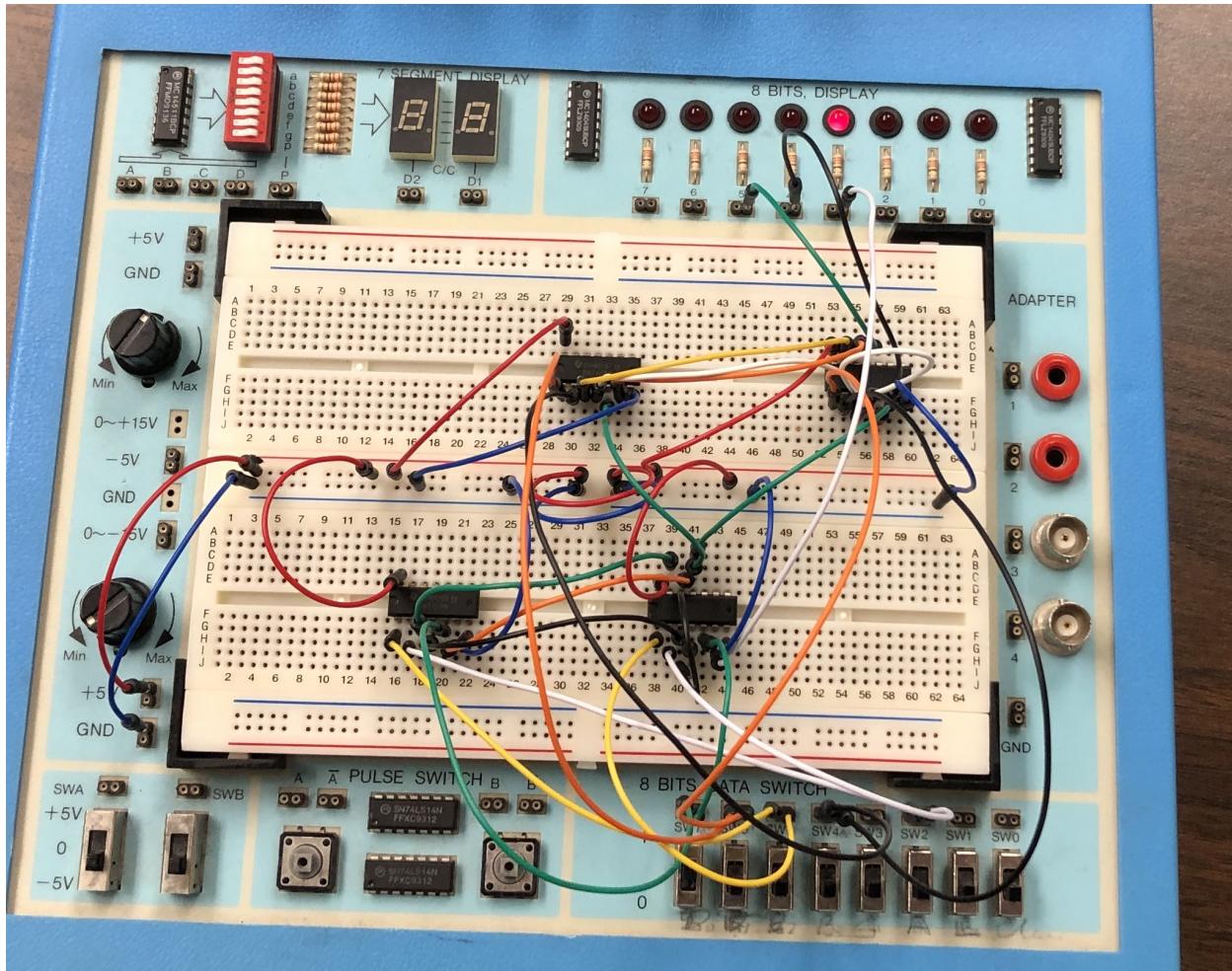


Figure 4: The 2-bit Adder Circuit