

Paging and Large Address Spaces

Dr Andrew Scott
a.scott@lancaster.ac.uk

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Problem: Page Table size

- 4K Pages, 32 bit addresses
 - 12 bits for offset (i.e. 4K byte range)

Process n
Page Table

32 bits = 20 bits | 12 bits

Page | Offset

2²⁰ gives 1M entries, each holding 32 bit/ 4 byte frame address

32 bits

So, 4MB Page Table!
...per process!!!!
Few processes will use all addresses

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Hierarchical/ Multi-level Paging

Process n
Page Directory

Page Directory

Page Table

Physical Address

Page 1 | Page 2 | Offset

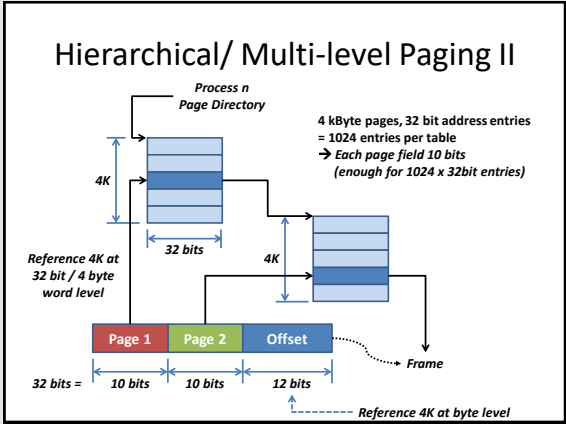
Outer | Inner

Frame | Offset

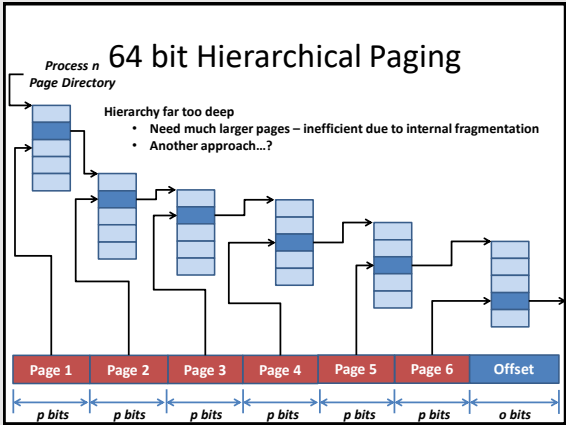
Notice as we increase depth of hierarchy we increase number of memory accesses
-- *Reduces speed of every memory reference*

We call top level table the *Page Directory*

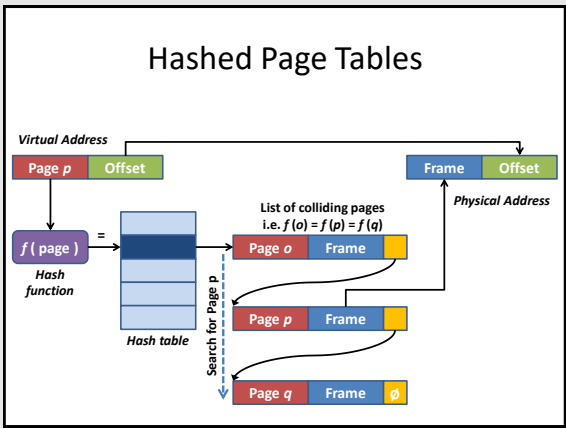
3



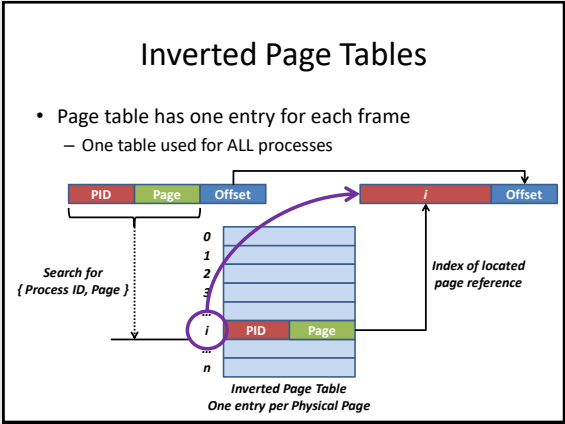
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