Paging: Translation Lookaside Buffer (TLB)

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Page Table in Registers vs. Memory

- Register based page tables
  - Fast but limited capacity
- Memory based page tables
  - Capacity only limited by memory
  - Slow access time... ***Remember these also translated via table!***
- 'Hybrid': maintain cache of *Page* to *Frame* translations
  - ***Translation Look-aside Buffer*** (TLB)
  - Beware as each entry only valid for one process
    - Often *pin* or *wire-down* kernel entries to prevent these being flushed
      -- *Assumes kernel always visible*
    - Generally have to flush entries when changing process

On x86: `invlpg virtAddr`

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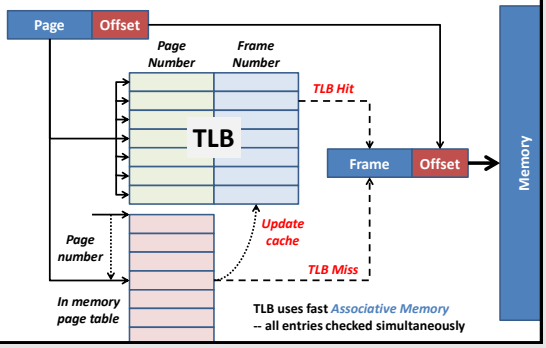
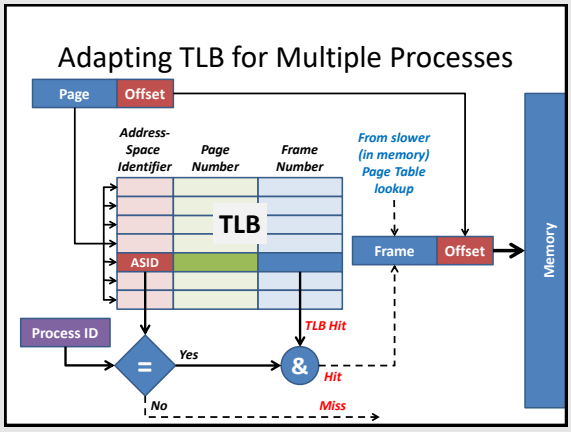
Translation Look-aside Buffer (TLB)



3


Adapting TLB for Multiple Processes
Page
Offset
Address-Space Identifier
Page Number
Frame Number
From slower (in memory) Page Table lookup
TLB
ASID
Frame
Offset
Memory
Process ID
=
Yes
&
TLB Hit
Hit
No
Miss

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