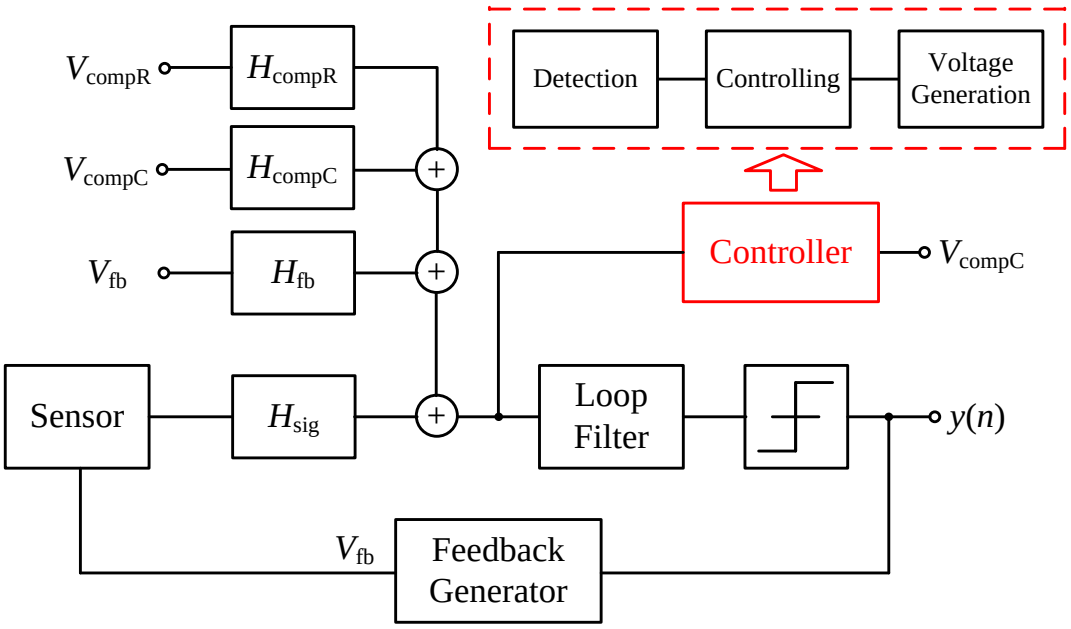
IMTEK

Master's Thesis

Design of an Automatic Compensation Controller for a Continous Time Collocated Force Feedback



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Title page The picture shows the block diagram of the $\Delta\Sigma$-modulator with the automatic compensation controller.

Declaration

according to the Examination Regulations:

I hereby confirm to have written the following thesis on my own, not having used any other sources or resources than those listed. All passages taken over literally or correspondingly from published sources have been marked accordingly. Additionally, this thesis has not been prepared or submitted for another examination, neither partially nor completely.

Freiburg, April 18, 2017

Jing Jiang

Abstract

Microelectromechanical(MEM)-gyroscopes are used for the detection of the angular rate of a body. This inertial sensor is established in automotive as well as consumer applications, e.g. for the electronic stability control or image stabilization, respectively. It is beneficial to integrate the gyroscope in an electromechanical ΔΣ-modulator readout loop featuring an improved sensitivity, linearity as well as an inherent analog-digital conversion. In this closed loop system, electrostatic feedback forces are applied to hold the sense mass in its idle position. This is achieved by a collocated feedback (CCFB), which makes use of the sense electrodes to detect the proof mass deflection and to apply the feedback forces simultaneously. Therefore, a special continuous time front end is used, which requires the balancing of the feedback and a compensation voltage, otherwise a disturbance signal emerges, which increases the in-band noise (IBN) or even saturates the ΔΣ-modulator readout loop.

This thesis focuses on the development of three implementation approaches on the automatic compensation controller, which achieves the balanced condition of the front end. In order to not deteriorate the IBN of the electromechanical ΔΣ-loop, the target is to achieve an accuracy of the required compensation voltage of 1% of the value for ideal balancing. The parameters in the controller are optimized for the best performance. In addition, techniques are introduced to further improve the performance of the control loop. Finally, the stability of the controller and of the overlaying ΔΣ-modulator is analyzed. All implementations of the controller are simulated in the system level by MATLAB® Simulink® as well as Cadence® Virtuoso® using a transistor level implementation of the CCFB front end, therefore the controller is realized in Verilog-A.

The ΔΣ-modulator equipped with the compensation controller is verified with a constant angular rate of 1 °/s and a sampling frequency of 80 kHz. In the system-level simulations the best performing controller achieves an IBN equal to -116 dBFS with a control error of 0.2% and a settling time of 2 ms. The transistor-level simulation including thermal noise results in an IBN of -92 dBFS, which is compared to the ideally balanced condition, achieving -91 dBFS, not deteriorating the overall performance.

Keywords: MEM-gyroscope, ΔΣ-modulator, charge integrator, collocated feedback, compensation

Zusammenfassung

Mikroelektromechanische (MEM)-Drehratensensoren werden verwendet um die Rotationsgeschwindigkeit einer Körpers zu messen. Dieser Intertialsensor hat sich in den Bereichen der Automobilindustrie und der Unterhaltungselektronik etabliert, wo diese beispielsweise für das elektronische Stabilitätsprogramm oder die Bildstabilisierung eingesetzt werden.

Es ist vorteilhaft den Drehratensensor in einem elektromechanischen $\Delta\Sigma$-Modulator einzubinden, da so die Sensitivität sowie die Linearität gesteigert werden können und eine inhärente Analog-Digital-Wandlung erreicht wird. In dieser geschlossenen Regelschleife wird eine elektrostatische Kraft aufgebracht, welche die Detektionsmasse in ihrer Ruhelage hält. Dies wird durch eine Sensorausleseschaltung mit integrierter Kraftrückkopplung erreicht, welche die Detektionselektroden zeitglich zur Detektion und zu Kraftrückkopplung verwendet. Zum Betrieb dieser Sensorausleseschaltung muss der Abgleich zwischen der Rückkoppelspannung und einer Kompensationsspannung erzielt werden. Bei einem Fehlabgleich entsteht ein Störsignal, welches das Rauschen im Signalband (IBN) erhöht oder sogar zur Sättigung der $\Delta\Sigma$-Schleife führen kann.

In dieser Masterarbeit werden drei verschieden Konzepte einer Regelschleife zum automatischen Abgleich der Sensorausleseschaltung untersucht. Um das Rauschen im Signalband nicht zu verschlechtern ist das Ziel ein Abgleichgenauigkeit von 1% der idealen Kompensationsspannung zu erreichen. Hierfür werden die Regelparameter optimiert und Techniken vorgestellt, welche die Gesamtleistung der Regelung verbessern. Abschließend wird die Stabilität der Regelung sowie die Auswirkung auf die Stabilität des $\Delta\Sigma$-Modulators betrachtet. Die verschiedenen Konzepte der Regelung werden auf Systemeben in MATLAB® Simulink® sowie in Cadence® Virtuoso® mit einer auf Transistorebene implementierten Sensorausleseschaltung untersucht, wobei bei letzterem die Regelung in Verilog-A realisiert wird.

Der $\Delta\Sigma$-Modulator inklusive Regelung für den automatischen Abgleich wird bei einer konstanten Rotationsgeschwindigkeit von 1 °/s und einer Abtastrate von 80 kHz verifiziert. Die Simulationen auf Systemebene mit der leistungsfähigsten Regelung erreichen ein IBN von -116 dBFS, wobei ein Regelfehler von 0.2% und eine Einschwingzeit von 2 ms erreicht wird. Die Simulationen auf Transistorebene mit thermischen Rauschen zeigen ein IBN von -92 dBFS, welches im Vergleich zum dem idealen abgeglichenen Zustand mit -91 dBFS die Gesamtleistung nicht verschlechtert.

Contents

Nomenclature

Abbreviation

Abbreviation	Denotation
AAF	Anti Aliasing Filter
ADC	Analog Digital Converter
A/D	Analog-Digital
ASIC	Application Specific Integrated Circuit
CCFB	Collocated Feedback
CI	Charge Integrator
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous Time
DAC	Digital Analog Convertor
DC	Direct Current
DCR	Duty Cycle Resistor
DCF	Duty Cycle Filter
DDA	Differential Difference Amplifier
DSP	Digital Signal Processing
ESD	Electrostatic Discharge
FS	Full Scale
IBN	In Band Noise
ICM	Input Common Mode
LPF	Low Pass Filter
LSB	Least Significant Bit
MEM	Microelectromechanical
MEMS	Microelectromechanical System
NOFT	Noise Observation Frequency Tuning
NTF	Noise Transfer Function
opamp	Operational Amplifier
OSR	Oversampling Ratio
NOFT	Noise Observation Frequency Tuning
PDF	Probability Density Function
PSD	Power Spectral Density
RC	Resistor-Capacitor
S/H	Sample-Hold
SC	Switched Capacitor
SNR	Signal Noise Ratio

Abbreviation	**Denotation**
SQNR	Signal Quantization Noise Ratio
STF	Signal Transfer Function

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1 Introduction

Microelectromechanical Systems (MEMS) are one of the most advanced technologies, which developed from the microelectronics with interdisciplinarity, involving electronics, mechanics, material science, physics, chemistry, biology and medicine. The MEMS are now under expansive prospect on application such as medical treatment, automotive, movement tracking and consumer products (e.g. smartphone and digital camera). The MEM-sensor is a modern type of sensor produced with this advanced technology, providing prominent characteristics such as small size and weight, low cost and power consumption, high reliability and robustness, batch manufacturing and integration. Nowadays MEM-sensors are realized in versatile forms, in which the MEM-accelerometer and MEM-gyroscope are two of the most common implementations. The MEM-accelerometer is designed to detect the linear acceleration, while the MEM-gyroscope detects the angular rate. In this thesis, the MEM-gyroscope and its readout concept are introduced. Based on this, a control loop to guarantee proper functionality of the readout system is presented.

大背景，都有哪些应用，现在发展如何。本论文研究的是什么

In order to process the signal generated by the sensor element, a readout system is required, which can built as an open or closed loop system. In an open loop system, the sensor signal can be directly read at the output node. In a closed loop system, a feedback signal is superimposed to the sensor signal at the input node and thus they have the similar magnitude in order to cancel each other. The $\Delta\Sigma$-modulator is a form of analog-digital converter (ADC) as an interface between the analog environments of the sensor to the digital signal processing (DSP). A design of electromechanical-modulator includes the gyroscope in a closed loop readout system. Therefore, a feedback path to the sensor element is necessary to apply restoring forces at the sensor in order to keep the proof mass at the idle position. A strategy called collocated feedback (CCFB) is employed, which uses the same electrode as the readout input of the charge integrator (CI), which is designed for converting the variance in charge to voltage, to detect the deflection of the proof mass and thus apply a feedback voltage to generate a proper electrostatic force. The concept of continuous time (CT) CCFB requires the balancing of a set of voltages, which would otherwise result in an imbalance saturating the electromechanical $\Delta\Sigma$-modulator. As a result, a compensation network is proposed in order to eliminate the disturbance as well as to increase the signal-noise ratio (SNR) of the readout system. A straightforward implementation is manual adjustment on the compensation voltage introduced in [2]. One disadvantage of this strategy is that the time for compensation is quite long, because each chip must be adjusted manually. This method cannot guarantee a unified accuracy of the compensation throughout all the chips.

针对什么问题，怎么解决的， 有什么缺点，又是也怎么解决的

In this thesis, a design of an automatic compensation controller is under study with different possible implementation approaches. The target of the design is that the compensation voltage can be automatically generated after the startup of the $\Delta\Sigma$-modulator and achieve an accuracy of 1% deviation from the value required for ideal balancing. Parameters of the controller and optimization strategies are analyzed which may influence the stability of the readout system as well as the performance in SNR. For an implementation with digital blocks, the accuracy of the compensation magnitude depends on the number of bits of the digital-analog convertor (DAC), which is utilized to generate the analog compensation voltage.

The following five chapters of this thesis are structured as follows:

论文结构

Chapter 2: MEM-sensor readout. This chapter begins with the introduction of the fundamentals about the signal processing theories as the preparation knowledge for the MEM-sensor readout system. Accelerometer and gyroscope are two types of widely used MEM-sensors and share similar mechanical structure. The sensor is embedded in an electromechanical $\Delta\Sigma$-modulator featuring inherent analog-digital (A/D) conversion, in which the collocated feedback strategy is implemented.

Chapter 3: Compensation tuning loop. Feedback and compensation paths are necessary to keep the $\Delta\Sigma$-modulator in stability and low in-band noise (IBN). The balanced condition of the CI is achieved by properly adjusting the value of the compensation voltage. A manual calibration of the capacitive compensation and its disadvantage are introduced. An automatic compensation controller is then proposed.

Chapter 4: Automatic compensation controller. In this chapter different implementations of the automatic compensation controller are introduced. The introduction begins with the principle and structure including specific transfer characteristics. The performance of the controller is analyzed by the comparison with the $\Delta\Sigma$-modulator loop with 1% imbalance and thus reveals the benefit as well as impact of the controller to the operation of the $\Delta\Sigma$-modulator. Stability is critical to the close loop controlling system, therefore several conditions which might occur at practical application are discussed and their influence to the stability of the $\Delta\Sigma$-modulator with the controller is described. All simulations are done in the system level by MATLAB® Simulink®.

Chapter 5: Verilog-A implementation. Besides the system level simulation, the concept of an automatic compensation controller is implemented in Verilog-A in order to simulate the controller in combination with the transistor-level implementation of the CCFB CI in Cadence®. Simulation with transistor-level CI offers the opportunity to gain more realistic specifications for the transistor-level implementation of the controller.

Chapter 6: Conclusion and outlook. The conclusion chapter summarizes all the introduced implementations of the automatic compensation controller in term of SNR and the corresponding condition to achieve the best performance. Noise analysis can be studied in the future in order to acquire more realistic behavior of the controller. The perspective of memorizing blocks to be integrated into analog structures is mentioned.

2 MEM-gyroscope Readout System

2.1 Analog-digital Conversion Fundamentals

It is common in application field of electrical and communication technology with post-processing and storage of data in digital domain. For example, a sensor system receives the information from analog environment and converts it to the digital form which is easy for devices to memorize. Digital system can only process discrete values of the original signal, both in time and amplitude. Therefore, analog-to-digital conversion has to be performed by the methods of sampling and quantization, which are implemented for the discretion in time and amplitude, respectively. One can distinguish between the Nyquist-rate ADC and the oversampled ADC, especially $\Delta\Sigma$-converter, which make use of oversampling and noise-shaping in order to increase the SNR.

2.1.1 Sampling

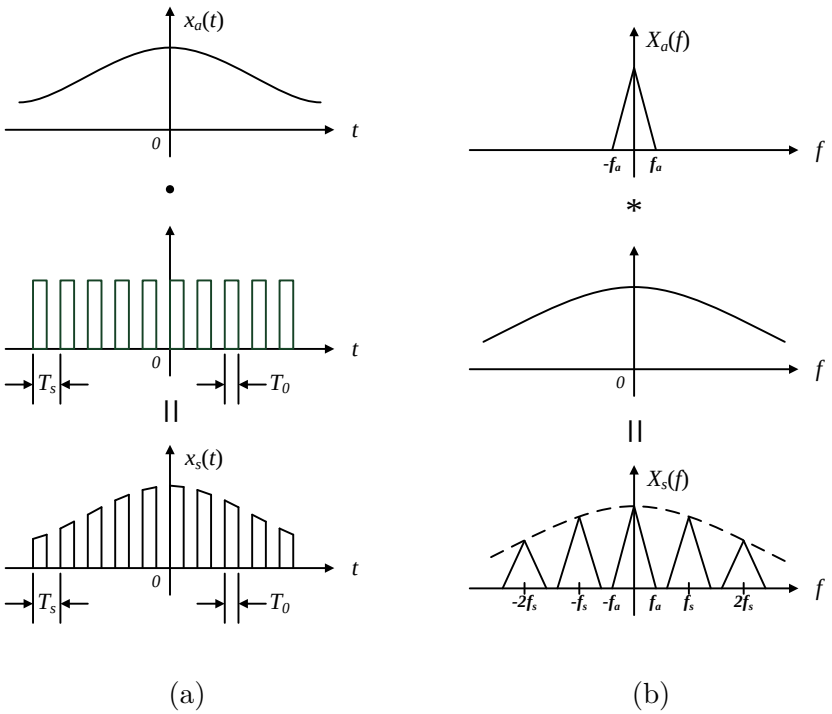
During the sampling process, a continuous-time signal is transformed into a discrete-time signal by measuring the amplitude at uniform intervals of time. A discrete-time sequence is generated by periodically sampling a continuous-time signal at uniform intervals of time. The spacing between two consecutive samples, as known as sampling period T_s, determines the resolution of the sequence in the time domain.

The ideal sampling process is defined mathematically as the multiplication in the time domain of the input signal $x_a(t)$ and the Dirac comb $\mathrm{III}(t/T_s)$, or in the form

$$x_s(t) = x_a(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{2.1}$$

with $x_s(t)$ the sampled signal in the time domain and T_s the uniform interval of time called sampling period. The result is a sequence of pulse with infinite narrow time window but includes the information of magnitude of $x_a(t)$ at the time n/T_s. In frequency domain, the result is described as the convolution $X(f) * \mathrm{III}(fT_s)$, with $X(f)$ and $\mathrm{III}(fT_s)$ the Fourier transformation of the input signal and Dirac comb, respectively. The replicas of $X(f)$ can be observed with the interval $1/T_s$.

Since it is impossible to achieve infinite narrow time window in the real world, practical sampling can only be implemented instead of ideal method. Normally



(a) (b)

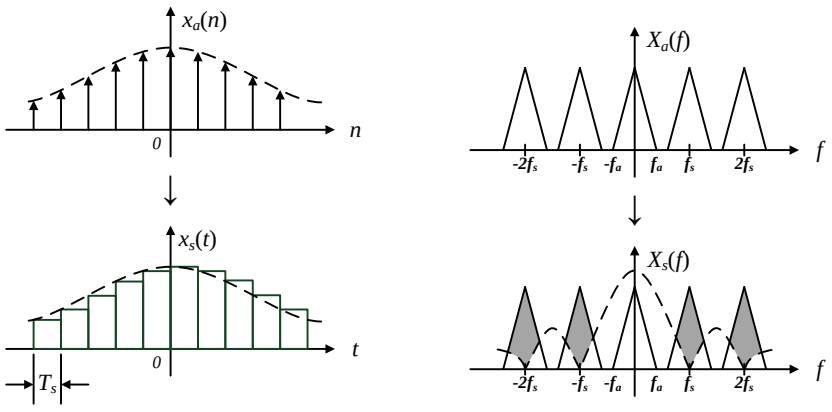
Figure 2.1: An illustration of sampling process by the multiplication with rectangular pulses in time domain (a) and frequency domain (b).

there are two methods to perform practical sampling in an application. One way is to activate the signal path for a time span T_0 in one single period and then disable the path by switch, as depicted in Figure 2.1a. This type of sampling is equivalent to the multiplication between signal and pulse series with unity gain, as expressed in the following equation:

$$x_s(t) = x_a(t) \cdot \sum_{n=-\infty}^{\infty} \text{rect}\left(\frac{t - nT_s}{T_0}\right) \tag{2.2}$$

As a result of sampling in the frequency domain, the base band is duplicated at multiples of the sampling frequency $1/T_s$ and the group magnitude is modulated by the envelop $T_0 \text{sinc}(T_0 f_s)$. As a result, attenuation occurs on the power spectrum of the sampled signal throughout the frequency band, which is illustrated in Figure 2.1b. The residual energy of the sampled signal comparing to the original signal is proportional to T_0.

Another way called sample-hold (S/H) is to measure the value at the beginning of one single period and maintain it for a specified minimum time span. Figure 2.2a shows principle in time domain, in which the result of sample-hold process can be modeled as the reconstruction of ideally sampled signal. It is equivalent to the convolution between ideally sampled signal and rectangular pulses. The S/H process



(a) (b)

Figure 2.2: An illustration of sample-hold process in time domain (a) and frequency domain (b).

in the time domain can be described by the following expression

$$x_s(t) = \sum_{n=-\infty}^{\infty} x_a(n) \cdot \text{rect}\left(\frac{t - nT_s}{T_s}\right) \tag{2.3}$$

Figure 2.2b illustrates the spectrum of the sampled signal. The duplicates of the base band are located at the multiple frequencies of n/T_s and thus suppressed. The original signal band, however, suffers the sinc-function distortion by the multiplication with the sinc function. This can be equalized with an inverse sinc-filter. The function of S/H is normally realized by switched capacitor in the circuit level. The S/H module works in two phases. Firstly the capacitor is switched to the analog signal and charged or discharged due to the voltage difference in between. After the capacitor is fully charged, it is switched to the input of following component. Normally, this is a buffer or operational amplifier (opamp) with high input resistance so that the voltage remains almost constant until the period finishes and the capacitor is switched again to the analog signal path.

There is possibility that the neighboring replicas violate each other. As illustrated in Figure 2.3, if the sampling frequency isn't higher than the Nyquist rate, overlap will occur between the spectrums of neighboring duplicates, which is known as aliasing. The reconstruction of base band signal without distortion is now impossible. In order to avoid aliasing during the sampling, the Nyquist theorem must be achieved. The frequency of the sampling signal is higher than twice the highest frequency component of the sampled signal, which is expressed by

$$f_s > 2f_a \tag{2.4}$$

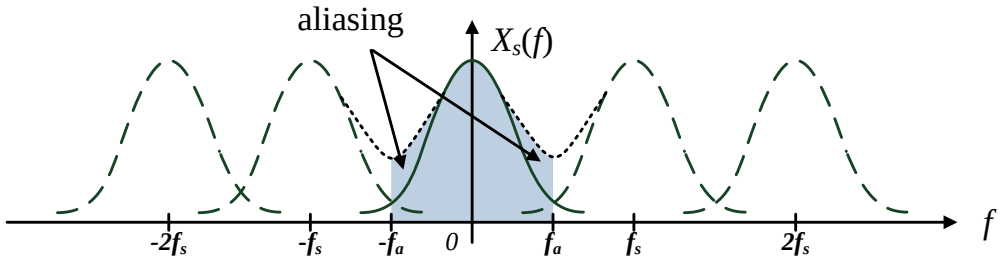


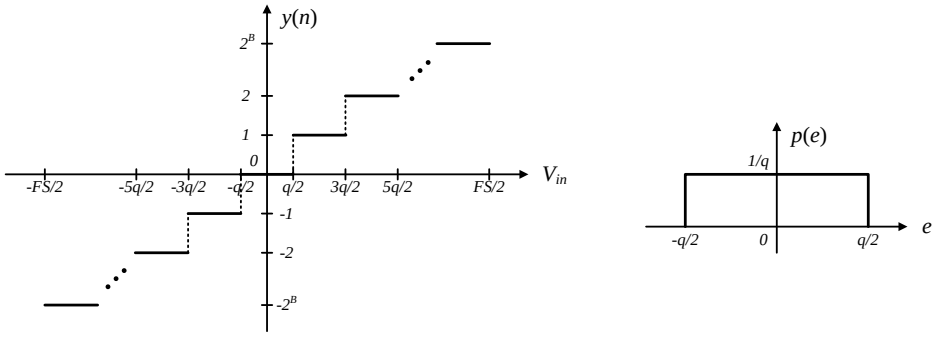
Figure 2.3: An illustration of aliasing when the Nyquist theorem is violated. The overlap between neighboring duplication of original signal causes distortion in base band.

with f_a the frequency of sampled signal. In most cases, the bandwidth of the sampled signal is not strictly limited. Therefore, it is necessary to limit the signal bandwidth by an additional anti-aliasing filter (AAF), which is normally realized by a low pass filter (LPF), before sampling takes place in order to fulfill the Nyquist rate.

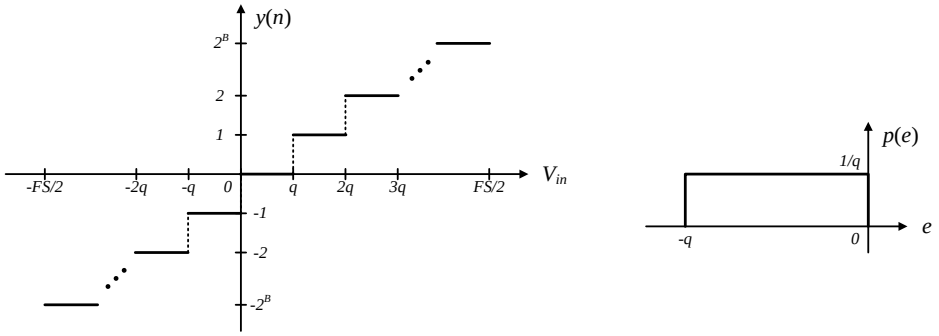
2.1.2 Quantization

Quantization describes the procedure of approximating the magnitude of an analog signal by limited number of levels. The required number of levels is determined by the resolution, which refers to the step width q between the neighboring digital values and full scale (FS) range defined by the valid maximum magnitude of the input signal. The distinguishable number of levels determines the resolution of quantizer. The binary representation of the quantized signal is the most common type in electrical system. Therefore, the maximum number of levels equals 2^B, where B refers to the number of bits.

The quantization is a process which maps the analog signal with infinite amplitude levels to finite amount of discrete levels. Since the output values have finite quantity, each digital data corresponds to an interval of the original analog signal. Obviously difference occurs when the analog signal is quantized, which is known as the quantization error. Figure 2.4 depicts the differences between truncation and rounding, both of which are typical methods of quantization. During the truncation process, all residuals are neglected. The mean and deviation of the quantization error are $m_{e,t} = -q/2$ and $\sigma^2_{e,t} = q^2/12$. During the rounding process, residuals less than $q/2$ are neglected while those more than $q/2$ are considered as q. The mean and deviation of the quantization error are $m_{e,r} = 0$ and $\sigma^2_{e,r} = q^2/12$.[4] Typically, the rounding process is implemented since the quantization error shows the characteristic closer to white noise because of the zero mean value and thus it is easy for modeling.



(a)



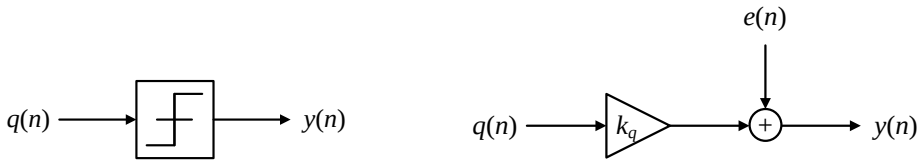
(b)

Figure 2.4: An illustration of the transfer curves of rounding (a) and truncation (b) quantization and the corresponding probability density function (PDF).

Figure 2.5 shows the block diagram of a quantizer with the linear modeling of quantization noise. The original signal and noise can be analyzed and calculated independently, especially in terms of transfer characteristics. One can calculate the signal-to-quantization noise ratio (SQNR) of power as showed below:

$$\mathrm{SQNR} = 10\log\left(\frac{P_{\mathrm{sig}}}{P_{\mathrm{noise}}}\right) = 10\log\left[\frac{\frac{1}{2}\left(\frac{\mathrm{FS}}{2}\right)^2}{\frac{q^2}{12}}\right] = 6.02\,\mathrm{dB} \times B + 1.76\,\mathrm{dB} \qquad (2.5)$$

with P_{sig} and P_{noise} the signal power and quantization noise power.[3] The SQNR increases about 6 dB by each additional bit provided by the quantizer. In order to achieve a quantizer with high number of bits, even more effort is introduced into the design of quantizer hardware due to the consequent requirement on complexity



(a) (b)

Figure 2.5: A block diagram of quantizer (a) and linearized model with scale factor k_q and quantization noise $e\,(n)$ (b).

and linearity.

2.1.3 Oversampling

Given the FS, the SQNR can be improved by decreasing P_{noise}. The most straightforward method to reduce the quantization error is to introduce smaller step. However, the additional bit count means considerable amount of hardware cost and increasing effort on linearity and offset control. One solution to increase the resolution without increasing the number of bits is oversampling. In this situation, the sample frequency f_s is chosen higher than Nyquist rate. The spectrum of quantization noise spreads further and thus P_{noise} in the signal band is scaled down by increasing $f_s/2f_a$, which is known as oversampling ratio (OSR). Figure 2.6 depicts the spectrum of the signal with and without oversampling, as well as the corresponding power spectral density (PSD) of the quantization noise. The part of noise power inside is call in-band noise (IBN) and it contributes to the SQNR. Therefore we don't care about the noise power outside the signal band. The SQNR is calculated as[3]

$$\begin{aligned}\text{SQNR}_{\text{OSR}} = 10\log\left(\frac{P_{\text{sig}}}{P_{\text{noise,IBN}}}\right) &= 10\log\left[\frac{\frac{1}{2}\left(\frac{\text{FS}}{2}\right)^2}{\frac{q^2}{12}\frac{1}{\text{OSR}}}\right] \\ &= 6.02\,\text{dB} \times B + 1.76\,\text{dB} + 10\log\left(\text{OSR}\right)\end{aligned} \tag{2.6}$$

The SQNR increases 3 dB by each doubling of OSR, equivalent to half of a bit contributed to the resolution of quantizer. Nevertheless, high OSR requires high speed sampling clock and thus increases the power consumption.[5] The trade-off is the speed of quantizer because higher sampling frequency of is required to achieve the specific OSR.

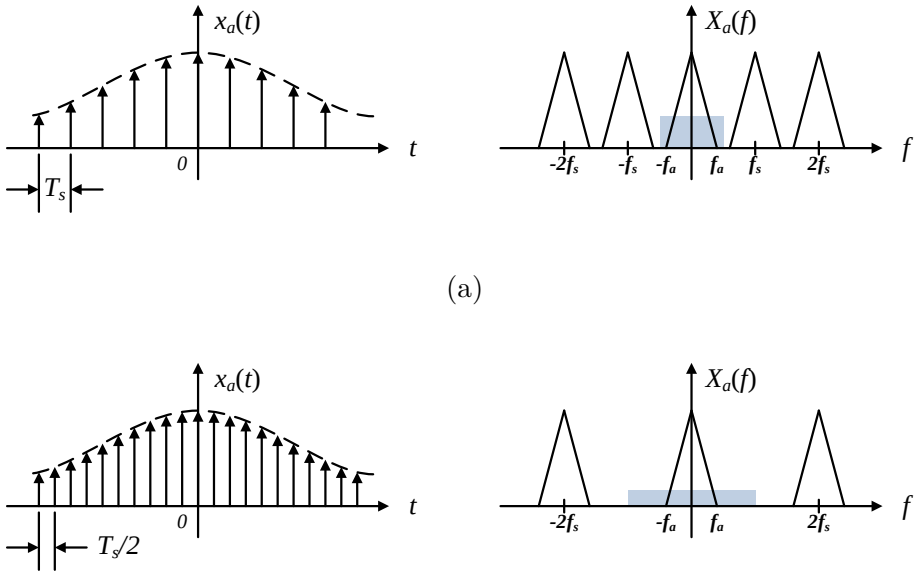
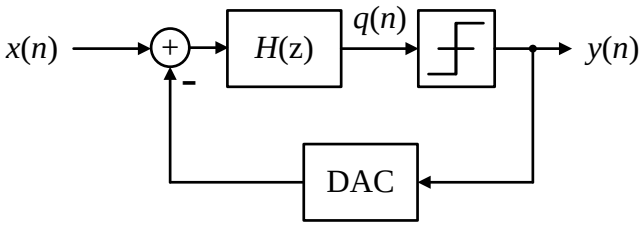


Figure 2.6: An illustration of the oversampling effect. The signal in time domain is either originally sampled (a) or 2-times oversampled (b). The PSD of quantization noise with (OSR = 2) and without oversampling (OSR = 1) distinguishes the residual power within the filter band.

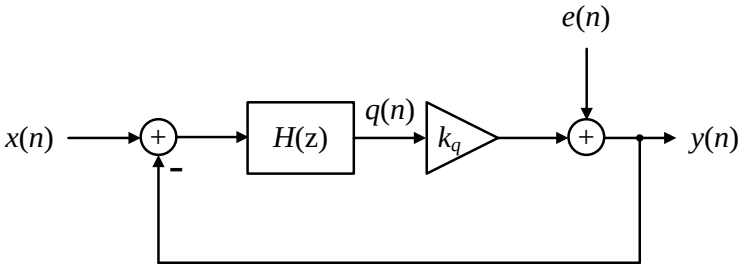
Another advantage of oversampling is the relaxed specification of AAF, which must provide necessarily sharp cutoff edge to ensure the limited bandwidth under $f_s/2$ in the most critical case.

2.1.4 Noise Shaping

Besides the contribution of oversampling, the SQNR can be further more improved by the concept of noise shaping in order to achieve an ADC with high resolution and low power. This concept is normally introduced in the $\Delta\Sigma$-modulator, of which the block diagram can be seen in Figure 2.7a. A typical $\Delta\Sigma$-modulator is a closed-loop system, which consists of a loop filter (LP), quantizer and a DAC for analog feedback. Due to the linear model in Figure 2.7b, the signal paths of signal and quantization noise are separated. The LP in forward path is utilized to suppress the quantization noise. Since the modulator processes discrete sampled signal, it is more straightforward to express the transfer characteristics in Z-domain. The transmission paths of original signal and quantization error contribute different attenuation scales. They are known as signal transfer function (STF) and noise transfer function (NTF), which are respectively calculated as:



(a)



(b)

Figure 2.7: A block diagram of 1st-order $\Delta\Sigma$-modulator (a) and the equivalent linear model (b) with sampled signal $x\,(n)$ and quantization noise $e\,(n)$.

$$\mathrm{STF} = \frac{H_{\mathrm{LF}}\,(z)}{1 + H_{\mathrm{LF}}\,(z)} \tag{2.7}$$

$$\mathrm{NTF} = \frac{1}{1 + H_{\mathrm{LF}}\,(z)} \tag{2.8}$$

with $H_{\mathrm{LF}}\,(z)$ the transfer function of LP in Z-domain.[3] Due to the high gain of the LPF in the base band, the magnitude of the STF keeps close to unity in the base band, while the magnitude of the NTF is quite low. As the frequency increases, the magnitude of NTF also increases outside the base band. This high-pass characteristic can significantly suppress the noise power in the base band and thus improve the performance of SQNR. Figure 2.8 shows the PSD of quantization noise of an oversampled signal after noise shaping.

In the case of a $\Delta\Sigma$-modulator with 1st-order LP, the IBN and SQNR can be calculated as:[3]

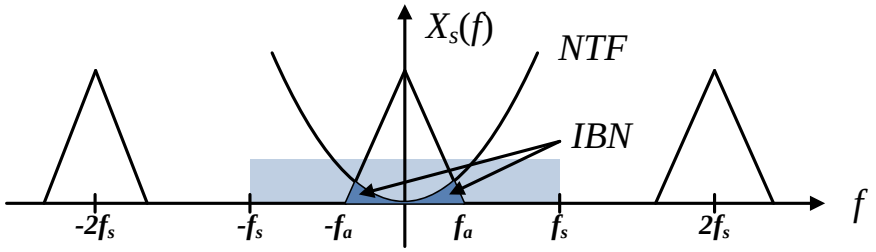


Figure 2.8: An illustration of noise shaping. Strong attenuation on the quantization noise occurs in the signal base band.

$$\mathrm{IBN}_{1\mathrm{st-order}\ \Delta\Sigma} = \frac{q^2}{12}\frac{\pi^2}{3}\frac{1}{\mathrm{OSR}^3} \tag{2.9}$$

$$\mathrm{SQNR}_{1\mathrm{st-order}\ \Delta\Sigma} = 10\log\left(\frac{P_{\mathrm{sig}}}{\mathrm{IBN}_{1\mathrm{st-order}\ \Delta\Sigma}}\right) \tag{2.10}$$

$$= 6.02\,\mathrm{dB} \times B + 1.76\,\mathrm{dB} - 5.2\,\mathrm{dB} + 30\log\left(\mathrm{OSR}\right) \tag{2.11}$$

The SQNR increases by 9 dB for each doubling of the OSR, equivalent to one and half bits contributed to the resolution of a Nyquist-rate quantizer. A much better efficiency in the improvement of ADC is showed comparing to the pure oversampling. The trade-off brought by the $\Delta\Sigma$-modulator is higher complexity, additional loop design and stability consideration.

2.2 Capacitive MEM-sensor Fundamentals

The application of sensor nowadays requires not only the accuracy and linearity for the measurement of analog signal as well as data processing, but also power efficiency and noise control for specific implementation. For example, the power supply for applications on the human body is supported using energy harvesters that convert body heat and the kinetic energy available during walking into usable electrical energy. The sensor information is prepared using data fusion algorithms for specific application scenarios from the fields of pedestrian navigation, medical orthotics and gesture recognition.[6] MEM-accelerometer and MEM-gyroscopes are two types of widely used electromechanical sensor for versatile implementation in automotive, navigation, industrial robotics etc. They share common part of capacitive interface in the form of comb electrodes for peripheral readout system.

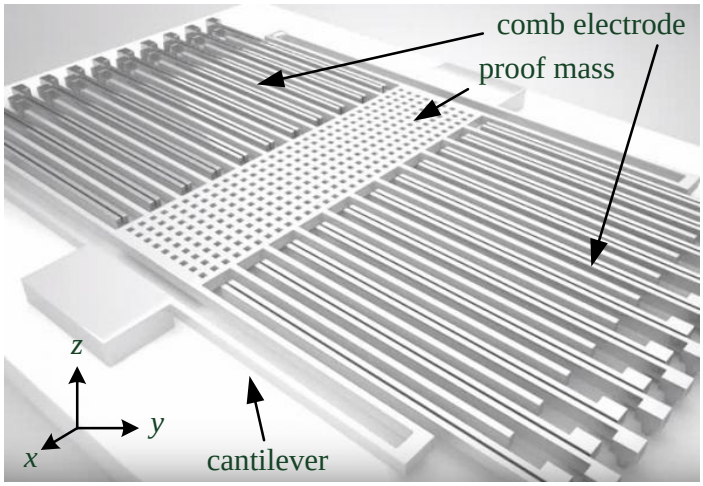


Figure 2.9: An illustration of MEM-accelerometer with highlights for proof mass, comb electrodes and cantilever.[1]

2.2.1 MEM-accelerometer

Figure 2.9 illustrates the common structure of the MEM-accelerometer. Basically the accelerometer consists of the proof mass suspended by cantilevers and comb electrode fixed on the substrate. The proof mass also has combs and overlap to the fixed combs. The neighboring fingers of combs are independent in voltage potentials. Due to the suspension structure, the proof mass is forced to move along x-axis, known as the sensitive axis. When the acceleration occurs on the sensor element and thus causes the inertial force, the capacitance between the electrode fingers changes due to the displacement of proof mass.

One method is the modulation of the voltage across the comb electrode. This can be achieved by changing the polarization voltage on the fixed combs. Another method is the modulation of the inertial force. This normally requires more effort and it is not a straightforward solution in every situations. For example, one can rotate the sensor element in z-axis and thus the inertial force (e.g. gravity force) along the sensitive axis is modulated by the angular speed Ω_m. However this implementation requires complicated control system of the mechanical rotation platform.

2.2.2 MEM-gyroscope

The Coriolis force, which is described as an inertial effect, can be observed on objects with movement relative to a rotating reference frame. The magnitude of the force is proportional to the mass m and the relative velocity $\overrightarrow{v}$ of the object as well as

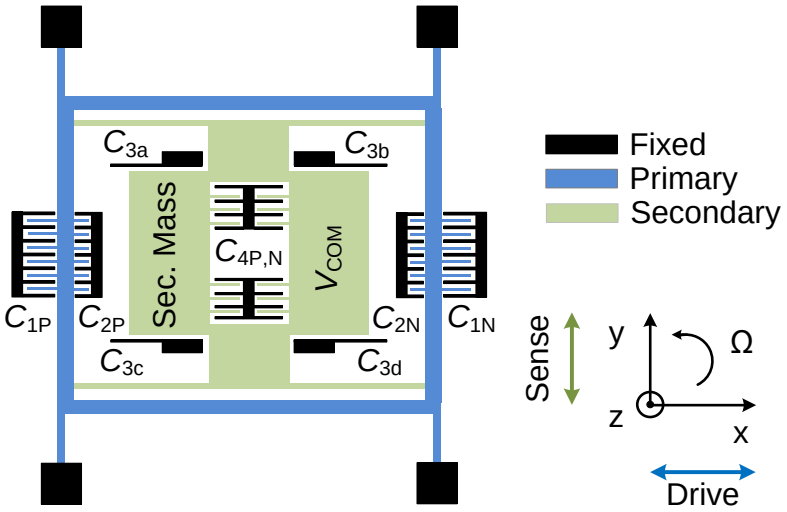


Figure 2.10: An illustration of MEM-gyroscope with highlights for primary mass, secondary mass and fixed parts. The primary mass is driving along x-axis. The Coriolis force acts on the secondary mass causing deflection along y-axis.[2]

the angular rate $\overrightarrow{\Omega}$ of the reference frame, as written in the following expression:

$$\overrightarrow{F_c} = -2m\left(\overrightarrow{\Omega} \times \overrightarrow{v}\right)\sin\alpha \tag{2.12}$$

The magnitude of Coriolis force also changes due to the angle α between the rotary speed and velocity vectors. It achieves the maximum when the vectors are perpendicular to each other. Therefore in the MEM-gyroscope, the mechanical structure has the best sensitivity at the corresponding direction, which means the output signal achieves maximum with the constant magnitude of angular rate of the device.

Figure 2.10 illustrates the common structure of the MEM-gyroscope. The mechanical structure composes of coupled orthogonal resonators, known as the primary (drive) and secondary (sense) resonator. The primary mass is actuated by electrostatic interface of the drive loop, which ensures the oscillation in the resonance frequency with constant velocity amplitude. The secondary mass vibrates together with the primary mass due to the suspension. Applying angular rate across the sensitive axis results in so called Coriolis force and contributes to the oscillation along y-axis. The resonance at the primary mass guarantees the maximum $\overrightarrow{v}$ and thus the maximum $\overrightarrow{F_c}$ to achieve high dynamic range of the sensor output. The displacement of the secondary mass results the change of gap between sense electrodes and consequently the variance of capacitance. The input signal of gyroscope representing the angular rate depends on the transient velocity of the primary mass, which includes the driving frequency component. Therefore, the frequency of the

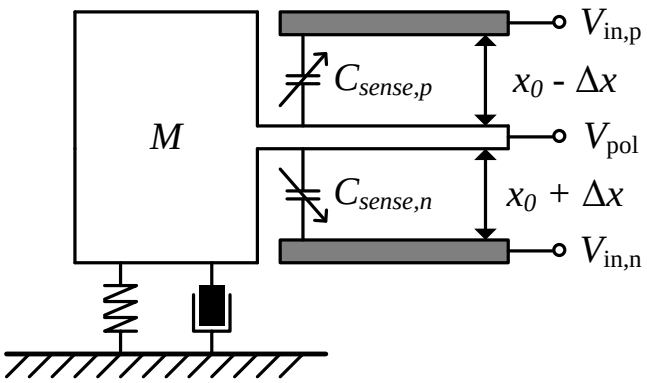


Figure 2.11: Concept of differentially configured capacitive comb electrodes.

angular rate is modulated on the driving frequency.

The MEM-gyroscope sensor used here is provided by Hahn-Schickard of Type 423, a 1D-gyro sensor. It is equipped with feedback electrodes at the primary and secondary mass for external control, such as quadrature cancellation and spring softening. The resonant frequency of the secondary mass is about 10 kHz. The gyroscope has symmetric mechanical structure. Two halves are coupled between primary masses and transiently move in the opposite direction during the operation, which is compatible to the differential readout module. It is beneficial to the suppression on offset signals by linear acceleration.

2.2.3 Capacitive Interface

The sense electrode detects the displacement of the secondary mass through the variance of the sense capacitance C_{sense} due to the change of the gap distance between the electrodes. This capacitive interface ensures the independency of common mode level. Since the polarization voltage of the sensor is quite high (7.5 V for Type 423), the readout circuit, which includes active components such as amplifier, won't be designed to operate at such high bias voltage due to the consideration on power consumption. Besides, it is not necessary on the generation of multiple voltages in order to match the polarization voltage of sensor which causes extra hardware cost.

Figure 2.11 illustrates the conceptive structure of the comb electrode. Suppose that the relative displacement of the secondary mass Δx is small, the change of the capacitance can be considered as linearly proportional to the displacement as described in the following expression:

$$\Delta C = \frac{\partial C_{\text{sense}}(x)}{\partial x}\Delta x \approx -\frac{C_0}{x_0}\Delta x \tag{2.13}$$

with C_0 and x_0 respectively the capacitance and gap at steady state, when the secondary mass has zero deflection. This variance of capacitance changes the differentially configured capacitors $C_{\text{sense,p}}$ and $C_{\text{sense,n}}$ by

$$C_{\text{sense,p}} = C_0 + \Delta C \tag{2.14}$$
$$C_{\text{sense,n}} = C_0 - \Delta C \tag{2.15}$$

2.3 Electrical Readout Interface

In order to recognize the signal of angular rate from the gyroscope, an electrical system with satisfying accuracy and speed is mandatory. The charge offered by the capacitive interface of the gyroscope must be firstly transduced to voltage and then converted to digital format for the following DSP stage.

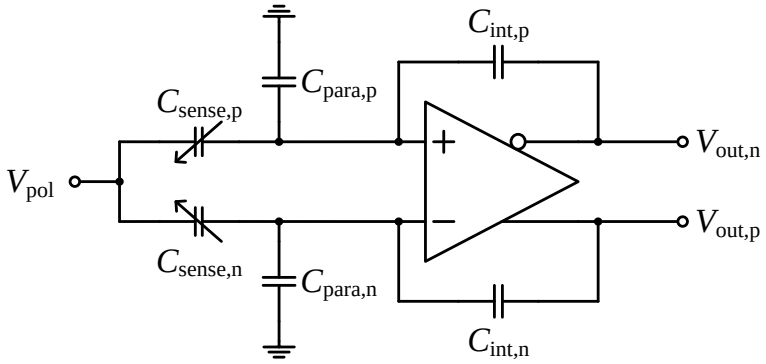
2.3.1 Charge Integrator

The charge integrator (CI) acts as a transducer between the sensor element and signal processing circuit, converting the change of capacitance of the sense comb to the output voltage. As depicted in Figure 2.12a, the conceptive structure consists of an operational amplifier with integration capacitor C_{int}. The capacitor of the sense comb C_{sense} directly connects to the input of amplifier. The proof mass is polarized by a fixed voltage V_{pol}. The other node of the sense capacitor is determined by the input common mode voltage V_{cm} of the CI. As long as the capacitance at the input node changes, extra charges will be transported to C_{fb} and cause the change of voltage at the output node. The output voltage can be derived by charge conservation $Q_{\text{sense}} = Q_{\text{int}}$:

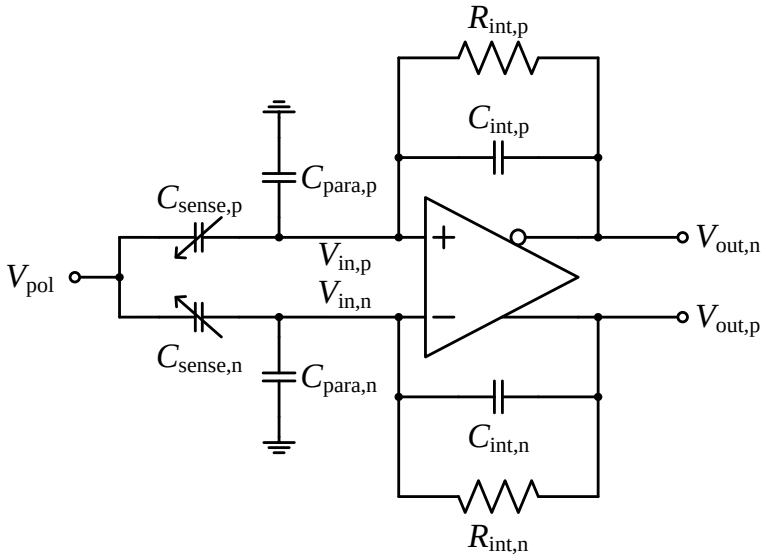
$$Q_{\text{sense}} = \Delta C_{\text{sense}}(V_{\text{pol}} - V_{\text{cm}}) \tag{2.16}$$
$$Q_{\text{int}} = C_{\text{int}}(V_{\text{cm}} - V_{\text{out}}) \tag{2.17}$$

For the fully differential structure of the CI, this results in:

$$V_{\text{out,p}} = V_{\text{cm}} - \frac{\Delta C_{\text{sense}}}{C_{\text{int}}}(V_{\text{pol}} - V_{\text{cm}}) \tag{2.18}$$
$$V_{\text{out,n}} = V_{\text{cm}} + \frac{\Delta C_{\text{sense}}}{C_{\text{int}}}(V_{\text{pol}} - V_{\text{cm}}) \tag{2.19}$$
$$V_{\text{out}} = V_{\text{out,p}} - V_{\text{out,n}} = -2\frac{\Delta C_{\text{sense}}}{C_{\text{int}}}(V_{\text{pol}} - V_{\text{cm}}) \tag{2.20}$$



(a)



(b)

Figure 2.12: A schematic of a fully-differential CI (a) and the version with feedback resistors (b).

with V_{out} the differential mode output voltage of the CI, $V_{\text{out,p}}$ and $V_{\text{out,n}}$ respectively the output of the CI at the positive and negative node. The input common mode (ICM) is fixed and thus V_{cm} is constant.Therefore, from the expression above, the variance of V_{out} is due to the change of either capacitance in the sensor or the voltage difference over the interface. Since there exists no resistive feedback path from input to output in the original CI block, the direct current (DC) component of the operational amplifier is floating. Any offset introduced by the amplifier will be

significantly amplified by its open-loop gain and cause its saturation. As a result, a feedback resister is introduced in order to define the ICM and reduce the offset amplification. Figure 2.12b shows the modified version of CI with feedback resistor R_{int}. The output voltage is now calculated as

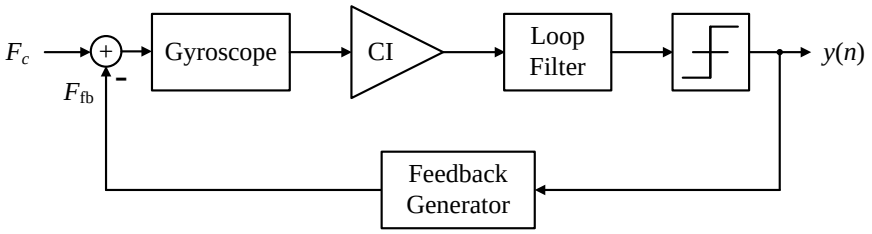
$$V_{\text{out,feedback}} = -2\frac{\Delta C_{\text{sense}}}{C_{\text{int}}}\frac{sR_{\text{int}}C_{\text{int}}}{1+sR_{\text{int}}C_{\text{int}}}\left(V_{\text{pol}} - V_{\text{cm}}\right) \tag{2.21}$$

Obviously the additional resistive path contributes high-pass characteristics to the CI. If the frequency of the input signal f_a is lower than the corner frequency $f_{c,\text{CI}} = 1/\left(2\pi R_{\text{int}}C_{\text{int}}\right)$, the magnitude of input signal will be attenuated. This might be an issue to the circuit design, since $f_{c,\text{CI}}$ must be at least one decade lower than f_a to avoid distortion. For the provided gyroscope, the driving frequency $f_d \approx 10\,\text{kHz}$ and $f_a \approx f_d$ due to the modulation of angular rate. C_{int} is normally under pico-Farad level due to the small gain of the CI. In consequence, R_{int} must be extremely high in order to meet the required corner frequency. For example, by using a typical value of 100 fF for C_{int}, it requires a resistance around $10\,\text{G}\Omega$ for R_{int}. This implemented resistor makes the design not straightforward because of the extraordinary area consumption for a chip. Some feasible solutions to implement such high resistance are back-to-back complementary metal-oxide-semiconductor (CMOS) structures[7] and T-network[8], which can achieve giga-ohm resistance.

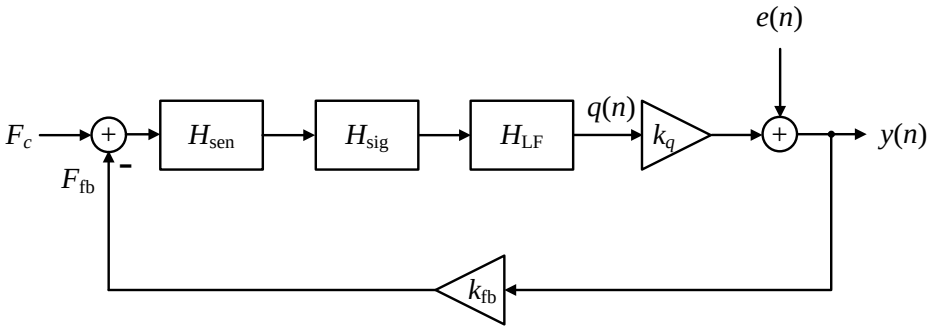
2.3.2 Electromechanical ΔΣ-modulator

The ΔΣ-converter is a type of analog-digital converter which is ideal for wide range of frequency of input analog signal, from DC to several mega-hertz. The mechanical sensor element and ΔΣ-convertor together constitute the so called MEM-gyroscope electromechanical system. There are two structural types of the electromechanical ΔΣ-modulator depending on the position where the sensor element is located. One can utilize the readout block and the ΔΣ-converter after the sensor element in the open loop configuration, which is straightforward in design and easy to achieve the stability of the system. Another type, which is used in this thesis, includes the sensor element in the feedback path and thus forms a close loop system. Figure 2.13a depicts the block diagram of the ΔΣ-modulator in the gyroscope control system illustrating both options mentioned above.

In principle, the electromechanical ΔΣ-modulator composes of a loop filter followed by an oversampling quantizer in order to generate bitstream, which represents the digital information of the analog signal. The bitstream is converted to the analog feedback signal, which controls the proof mass in the idle position. Hence, the modulator is built as a 1-bit sampling system, which simplifies the design of feedback path in terms of linearity. As a close loop structure for the electromechanical ΔΣ-modulator, technical advantages are straightforward: better linearity, extended bandwidth and dynamic range, stable temperature characteristics as well as less dependence on variance of components during the fabrication of MEMS. Nevertheless,



(a)



(b)

Figure 2.13: A block diagram of electromechanical $\Delta\Sigma$-modulator (a) and its equivalent linear model (b).

it requires extra design effort on the system.

As a part of the signal loop, the transfer function of the secondary mass $H_{\text{sen}}(s)$ contributes to the loop behavior by introducing additional orders and thus improves the performance in terms of noise shaping. The provided gyroscope owns the spring-mass-dumping system which has the transfer function of 2^{nd}-order, $f_{c,\text{sense}} \approx 10\,\text{kHz}$ as the resonance frequency and $Q_{\text{sense}} \approx 750$ as the quality factor of the proof mass. By applying spring softening[3] on the secondary stage, $f_{c,\text{sense}}$ can be reduce to the value, which exactly equals to $f_{c,\text{drive}}$ as the resonance frequency of the primary mass in order to achieve the matched mode between the primary and secondary stage and thus obtain a higher sensitivity. On the other hand, additional double poles are introduced by $H_{\text{sen}}(s)$ and thus decrease the phase margin of the signal loop by 180°, causing instability in the $\Delta\Sigma$-modulator. Hence, a lead filter is applied to cancel the poles by introducing additional phase leads. In this design of the $\Delta\Sigma$-modulator, the lead filter is integrated to the loop filter $\text{LF}(s)$.

The role of the loop filter is to suppress the frequency components beyond the expected bandwidth and thus avoid aliasing during the sampling procedure in the

quantizer. The specification of the filter can be more relaxed due to higher OSR. The order of filter also affects the performance of the converter in term of NTF and hence SQNR:[3]

$$\mathrm{IBN}_{\mathrm{Lth-order}\ \Delta\Sigma} = \frac{q^2}{12}\frac{\pi^{2L}}{2L+1}\frac{1}{\mathrm{OSR}^{2L+1}} \tag{2.22}$$

$$\mathrm{SQNR}_{\mathrm{Lth-order}\ \Delta\Sigma} = 6.02\,\mathrm{dB} \times B + 10\log\left[\frac{3}{2\pi^{2L}}(2L+1)\right] \tag{2.23}$$

$$+ (2L+1) \times 10\log(\mathrm{OSR}) \tag{2.24}$$

The lead filter, however, has relatively low magnitude in the low frequency band. Therefore it doesn't contribute much to the noise shaping and thus the SQNR.

2.3.3 Collocated and Non-collocated Feedback

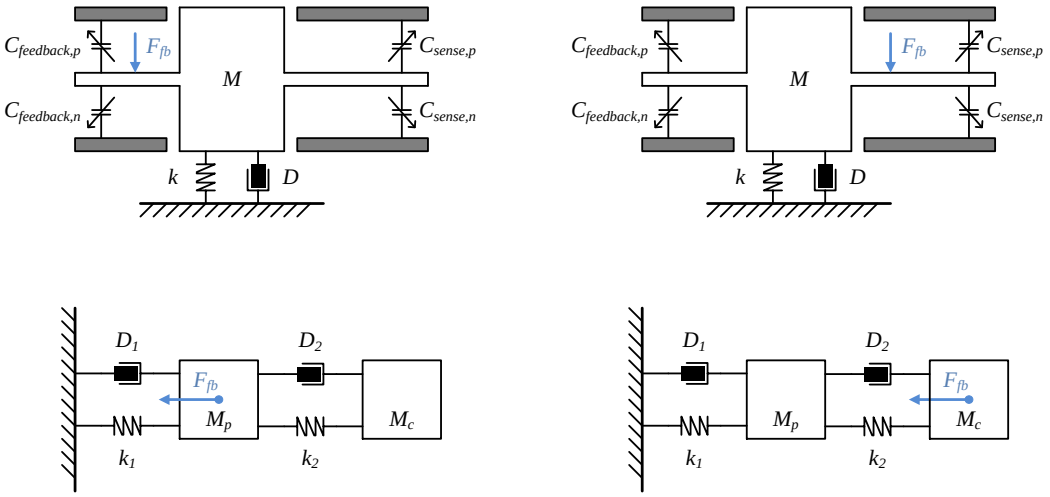
The MEMS-gyroscope equipped with $\Delta\Sigma$-modulator requires a feedback signal path. Generally, there exist two methods to generate the required electrostatic feedback force. In one case, the sense electrodes are utilized to generate the electrostatic feedback force, which is known as the collocated feedback. Another case is called non-collocated feedback, which means separate electrodes equipped on the proof mass are utilized.

There are two possibilities to apply external force on the secondary mass based on the structure illustrated in Figure 2.14. Here, the mechanical force F_{es} is generated by the electrostatic field between the comb electrodes, following the relationship with displacement y in the expression

$$F_{es} = \frac{\partial E_c}{\partial y} = \frac{1}{2}\frac{\partial C}{\partial y}U^2 = -\frac{\varepsilon_{\mathrm{eff}} A}{(y_0+y)^2}U^2 \tag{2.25}$$

where E_c is the energy stored in the comb capacitance C, $\varepsilon_{\mathrm{eff}}$ is the effective permittivity, A is the overlap area, y_0 is the initial position, U is the applied voltage across the electrode.

The complex shape of the secondary mass determines its mechanical characteristic which differs in resonance frequencies and oscillation modes between collocated and non-collocated configuration. At the resonance frequency of the lumped proof mass which is relatively lower, the sense fingers move together. The higher oscillation mode arises due to the Eigen-oscillation of the movable electrode fingers. In addition, this higher resonance frequency is identical for both the non-collocated and the collocated feedback. This phenomenon is analyzed as depicted in Figure 2.15, in which the secondary mass is modeled as a mechanical system with coupled oscillators. M_1 refers to the proof mass while M_2 refers to the electrode cantilever.



(a) (b)

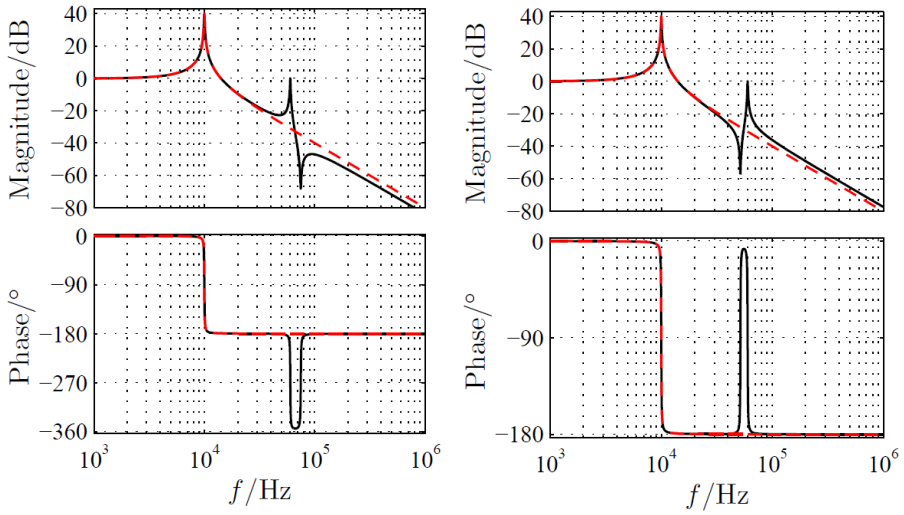
Figure 2.14: The model of the damped spring-mass system in the case of a non-collocated (a) and a collocated (b) force-feedback. The two concepts differ in the point at which the feedback force F_{fb} is applied. Additionally, the sense electrodes are modeled as flexible beams to include their eigen-oscillation.An illustration of dynamic system of proof mass with electrode. M_1 represents the proof mass while M_2 represents the electrode cantilever.

Based on the hypothesis of small displacement and deformation of the cantilever, the correlation between M_1 and M_2 can be described by spring constant k_{cp}. The situation is described by the coupled ordinary differential equations considering two harmonic oscillators coupled together and with one oscillator driven by oscillating external force F_{ex}:

$$\ddot{x}_1 + 2\zeta_1\omega_{\mathrm{res},1}\dot{x}_1 - \frac{k_{cp}}{m_1}x_2 + \omega_{\mathrm{res},1}^2 x_1 = 2F_{ex}\cos\omega t \tag{2.26}$$

$$\ddot{x}_2 + 2\zeta_2\omega_{\mathrm{res},2}\dot{x}_2 - \frac{k_{cp}}{m_2}x_1 + \omega_{\mathrm{res},2}^2 x_2 = 0 \tag{2.27}$$

The solution of the equations is[9, pp.173]



(a) (b)

Figure 2.15: An example bode plot of the secondary mass transfer function, including one higher resonance mode, in the case of a non-collocated (a) and a collocated (b) force-feedback.[3]

$$X_1 = \frac{F_0}{k_{1x}} \frac{1 - \left(\frac{\omega}{\omega_{2x}}\right)^2 + j\omega\frac{c_{2x}}{k_{2x}}}{\left[1 + \frac{k_{2x}}{k_{1x}} - \left(\frac{\omega}{\omega_{1x}}\right)^2 + j\omega\frac{c_{1x}}{k_{1x}}\right]\left[1 - \left(\frac{\omega}{\omega_{2x}}\right)^2 + j\omega\frac{c_{2x}}{k_{2x}}\right] - \frac{k_{2x}}{k_{1x}}} \tag{2.28}$$

$$X_2 = \frac{F_0}{k_{1x}} \frac{1}{\left[1 + \frac{k_{2x}}{k_{1x}} - \left(\frac{\omega}{\omega_{1x}}\right)^2 + j\omega\frac{c_{1x}}{k_{1x}}\right]\left[1 - \left(\frac{\omega}{\omega_{2x}}\right)^2 + j\omega\frac{c_{2x}}{k_{2x}}\right] - \frac{k_{2x}}{k_{1x}}} \tag{2.29}$$

The displacement of the comb electrode relative to the substrate along x-axis $X = X_1 + X_2$. The Bode plot of the transfer function $H(s) = X(s)/F_0(s)$ is depicted in Figure 2.15. In the case of non-collocated feedback, an additional negative 180° phase shift is observed and the resonant frequency ω_{2x}. This could cause problem in stability by decreasing the phase margin when the sensor is integrated into the control loop of the $\Delta\Sigma$-modulator. The collocated feedback, however, introduces a positive 180° phase shift. This advantage can be benefitial for the stability of the close loop system.

2.3.4 State-of-the-art Collocated Feedback

Readout method of switched capacitor (SC) is quite popular in many analog circuit blocks in previous designs.[10, 11] The SC structure works in the way of time-multiplexing: the feedback force is applied to the sense electrode in the first time

interval, while the capacitance variance of the sense electrode is measured in the second time interval.[12–14] One of the disadvantages of the SC collocated feedback is the reduction of energy transmitted from the sensor and thus the equivalent amplification of the CI decreases in comparison with a continuous time (CT) type. Another drawback comes from the noise folding effect, which introduces the frequency component located on multiples of Nyquist frequency into the signal band. Some specialized sampling methods, such as boxar sampling, can suppress the noise folding effet and thus the SNR by one order of magnitude in comparison to the normal SC integrators.[12] In addition, the SC circuit itself introduces kT/C noise and flicker noise. These two types of noises are related to the temperature and frequency but frozen in time. Therefore the low varying noise can be attenuated by using correlated double sampling (CDS) with the extra cost of doubling the thermal noise component.[12]

Due to the unsatisfying characteristics of the SC strategy, a solution CT collocated feedback is promising for an implementation of high gain and low noise for the gyroscope. A novel concept of continuous time collocated feedback is available in [3]. The magnitude of feedback voltage is generated from the bandgap reference "abgpc0" delivered by X-FAB®, which provides two DC-voltages $V_{\mathrm{BG,H}} = 2.12\,\mathrm{V}$ and $V_{\mathrm{BG,L}} = 1.25\,\mathrm{V}$ respectively. The bandgap reference block is already on chip for global usage, thus the division of voltage is necessary for a lower value of feedback magnitude, normally about several hundred millivolts. Modulated by the bitstream, the pulses with the amplitude of ΔV_{fb} are applied to the positive input of the charge integrator. Due to the virtual short effect of operational amplifier, the feedback signal can be also observed at the negative input which is connected to the sense comb of the gyroscope.

3 Compensation Tuning Loop

The implementation of collocated feedback introduces benefits on stability and hardware complexity to the $\Delta\Sigma$-modulator loop. Nevertheless, the feedback signal causes side effect due to the electrical structure which introduces the disturbance to the main path of the $\Delta\Sigma$-modulator in case of an unbalanced condition. As a result, we need extra signal path to compensate the disturbance to avoid the deterioration of SNR and even the saturation of the CI which terminates the functionality of the $\Delta\Sigma$-modulator.

3.1 Feedback and Compensation

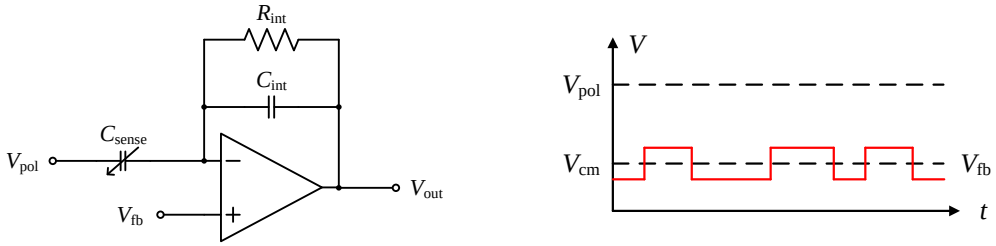
Based on the collocated feedback strategy, the sense comb of secondary mass is used for the measurement of Coriolis force as well as the actuation of electrostatic feedback force. Figure 3.1a depicts the schematic of proposed CI with collocated feedback. The feedback voltage V_{fb} is generated from the bandgap voltage as a stable reference which is already available on chip.[2] The collocated feedback is realized by applying V_{fb} to the positive input of the charge integrator. Due to the virtual short at the output of opamp, the varying signal can be also observed at the negative input which is connected to the sense comb of the gyroscopeas showed in Figure 3.1b. In this chapter, methods of compensation for this disturbance are introduced.

3.1.1 Resistive Compensation

Figure 3.2 illustrates the schematic of the resistive feedback path. Due to the fact that the feedback voltage is modulated onto the ICM, there exists a voltage drop ΔV_{fb} across the integration resistor R_{int}, generating a current I_{fb}. This current discharges all capacitors connected to the negative input, especially the integration capacitor C_{int} of the CI, and thus must be compensated by the resistive compensation. In [3] the resistive compensation voltage V_{compR} for the disruption on V_{out} due to the collocated feedback is given by the following equation:

$$V_{\mathrm{compR}} = V_{\mathrm{cm}} + 2\Delta V_{\mathrm{fb}} \tag{3.1}$$

with the assumption of $R_{\mathrm{comp}} = R_{\mathrm{int}}$. This means the amplitude of the compensation voltage for a balanced resistive compensation must be twice the feedback voltage.



(a) (b)

Figure 3.1: An illustration of the top-level schematic of the CI with collocated feedback (a). The feedback voltage is modulated onto the input common mode of the CI as visualised in (b).

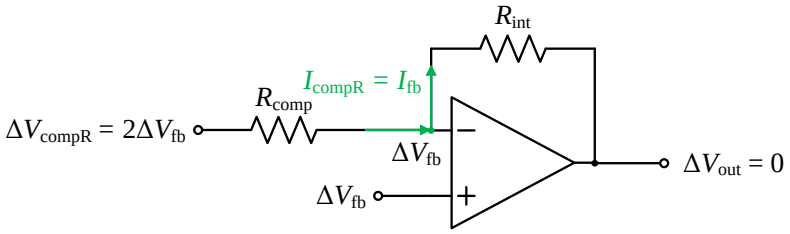


Figure 3.2: A schematic of the resistive compensation network.

This constant voltage can be achieved by a straightforward implementation. In [3] the bandgap voltage is doubled with a fully differential amplifier with a fixed gain to generate V_{compR}.

3.1.2 Capacitive Compensation

Another reason of imbalance comes from the discharge of C_{int} when V_{fb} changes due to the finite input resistance of real opamp. Therefore, the capacitive compensation is required to deliver charges to charge all the capacitors connected to the negative input. However, the amount of charge cannot be precisely calculated, especially considering the parasitic capacitances on the node. The parasitic capacitance is normally introduced by the local wiring, bond wire, ESD pads and those from the sensor chip. The fabrication of the MEM-gyroscope can only guarantee a range of reasonable parasitic components based on the predefined specification instead of accurate values. C_{para} refers to the equivalent total parasitic capacitors on the input node of CI. Due to the limited gain of opamp, the charge delivered by the sense comb C_{sense} will partly flow to C_{para}. Therefore, C_{int} will not be fully charged and

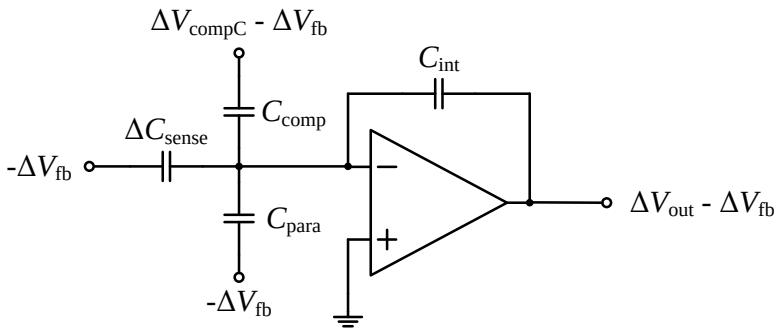


Figure 3.3: A small-signal schematic of the CI with feedback voltage applied in the collocated mode. The influence of parasitic capacitance is illustrated.

thus V_{out} is violated. For the provided gyroscope, the typical value of the parasitic capacitance on the output node is around 3 pF and the total parasitic capacitance is around 8 pF including wiring and ESD pads, much larger than C_{sense} and C_{int} which are normally in the range of fF. In this case, V_{out} is derived through the charge conservation $Q_{\text{sense}} = Q_{\text{int}} + Q_{\text{para}}$. Since the CI readout loop theoretically guarantees that the proof mass keeps at the idle position and thus $\Delta C_{\text{sense}} \approx 0$, the output voltage of the CI can be calculated as below with approximation:

$$\begin{aligned} V_{\text{out}} &= V_{\text{sense}} + V_{\text{disturbance}} \\ &= V_{\text{cm}} - \frac{\Delta C_{\text{sense}} + C_{\text{para}}}{C_{\text{int}}} \left(V_{\text{pol}} - V_{\text{cm}}\right) \\ &\approx V_{\text{cm}} - \frac{C_{\text{para}}}{C_{\text{int}}} \left(V_{\text{pol}} - V_{\text{cm}}\right) \end{aligned} \tag{3.2}$$

where V_{sense} represents the voltage from the sensor and $V_{\text{disturbance}}$ the voltage caused by residual charges. The ratio $C_{\text{para}}/C_{\text{int}}$ is typically in the order of 10^1 and in consequence causes saturation of the CI. This means that V_{out} shows relatively high sensitivity on the variance of C_{para}. The capacitive compensation is implemented to cancel the deterioration introduced by C_{para}. Figure 3.3 shows the small-signal schematic which is specified for the analysis, when the voltages change. The condition of balanced compensation when $\Delta V_{\text{out}} = 0$ is given by

$$\Delta V_{\text{out}} - \Delta V_{\text{fb}} = -\frac{C_{\text{comp}}}{C_{\text{int}}} \left(\Delta V_{\text{compC}} - \Delta V_{\text{fb}}\right) + \frac{\Delta C_{\text{sense}}}{C_{\text{int}}} \Delta V_{\text{fb}} + \frac{C_{\text{para}}}{C_{\text{int}}} \Delta V_{\text{fb}} \tag{3.3}$$

Supposing $\Delta V_{\text{compC}} = k_C \Delta V_{\text{fb}}$, we have

$$C_{\text{comp}} = \frac{C_{\text{int}} + \Delta C_{\text{sense}} + C_{\text{para}}}{k_C - 1} \tag{3.4}$$

in order to satisfy the condition of $\Delta V_{\text{out}} = 0$. Therefore, the required ΔV_{compC} is calculated from the expression

$$k_C = \frac{C_{\text{int}} + \Delta C_{\text{sense}} + C_{\text{para}} + C_{\text{comp}}}{C_{\text{comp}}} \tag{3.5}$$

3.1.3 Condition of Balanced Compensation

The approaches of resistive and capacitive compensation have to be applied due to the corresponding reasons of the imbalance, as mentioned in subsection 3.1.2 . A CCFB CI with compensation network as part of the $\Delta\Sigma$-convertor is illustrated in Figure 3.4a. The compensation voltages are separated in capacitive and resistive path, respectively named as V_{compC} and V_{compR}. V_{compC} is applied to the compensation capacitor C_{comp} and V_{compR} is applied to the compensation resistor R_{comp}. As analyzed in the subsection 3.1.1 and subsection 3.1.2, the current flow through R_{comp} has to compensate the the current flow through R_{int}, while charges are delivered by C_{comp} to the input node of the CI.

The concept of the collocated $\Delta\Sigma$-modulator with the linear model of the CI is shown in Figure 3.4b. The advantage of the equivalent schematic with separate transfer paths for feedback and compensation compared to an implementation in the circuit level is that the error node is accessible and observable. A better understanding of the imbalance in term of system analysis is also achieved. Therefore, the condition of the balanced CI is expressed by

$$H_{\text{fb}}(s)\, V_{\text{fb}} + H_{\text{compC}}(s)\, V_{\text{compC}} + H_{\text{compR}}(s)\, V_{\text{compR}} \cong V_{\text{err}} = 0 \tag{3.6}$$

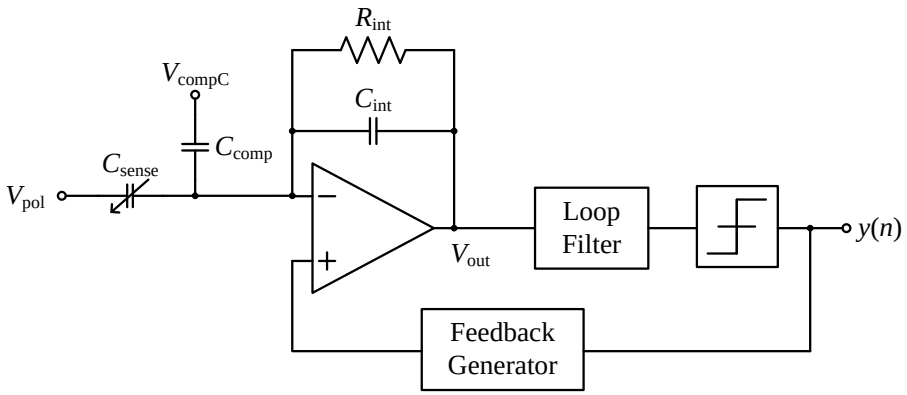
with $H_{\text{fb}}(s)$, $H_{\text{compC}}(s)$ and $H_{\text{compR}}(s)$ the transfer function of feedback, capacitive compensation and resistive compensation path, respectively. The error is expressed by the superposition of feedback and compensation transfer functions. The expression of these transfer functions are derived as shown below:

$$H_{\text{fb}}(s) = \frac{1}{R_{\text{comp}}} \cdot \frac{R_{\text{comp}} + R_{\text{int}} + s\,(C_{\text{comp}} + C_{\text{int}} + C_{\text{para}})\, R_{\text{comp}} R_{\text{int}}}{1 + sC_{\text{int}} R_{\text{int}}} \tag{3.7}$$

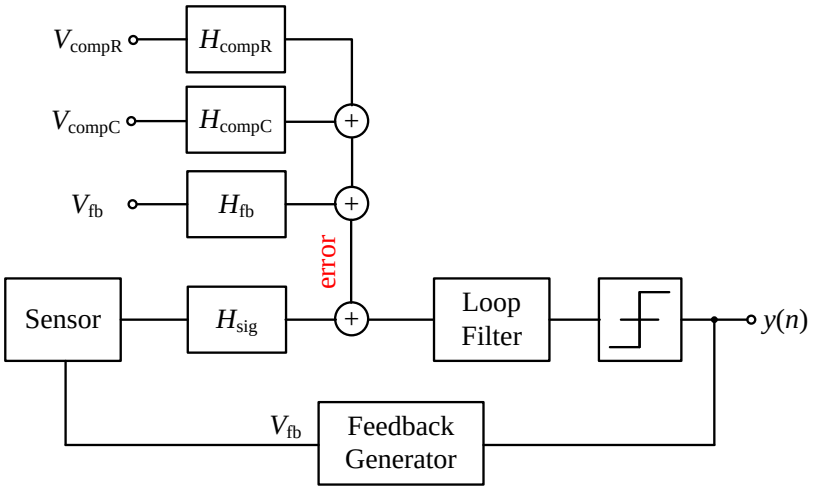
$$H_{\text{compC}}(s) = -\frac{sC_{\text{comp}} R_{\text{int}}}{1 + sC_{\text{int}} R_{\text{int}}} \tag{3.8}$$

$$H_{\text{compR}}(s) = -\frac{R_{\text{int}}}{R_{\text{comp}}} \cdot \frac{1}{1 + sC_{\text{int}} R_{\text{int}}} \tag{3.9}$$

$H_{\text{compC}}(s)$ shows the high-pass behavior. The high-frequency gain of $H_{\text{compC}}(s)$ equals $C_{\text{comp}}/C_{\text{int}}$. $H_{\text{compR}}(s)$ shows the low-pass behavior. The DC gain of $H_{\text{compR}}(s)$ is $R_{\text{int}}/R_{\text{comp}}$. $H_{\text{fb}}(s)$, $H_{\text{compC}}(s)$ and $H_{\text{compR}}(s)$ have the same pole frequency of $1/C_{\text{int}} R_{\text{int}}$.



(a)



(b)

Figure 3.4: A schematic of the electromechanical ΔΣ-modulator with collocated feedback and compensation paths (a) and the corresponding block diagram with the linear CI (b). Feedback and compensation signals are shaped by the CI in terms of corresponding transfer functions.

Supposing that the resistive compensation is already achieved due to Equation 3.1, the imbalance is considered only in terms of the capacitive path. When a deviation of V_{compC} to its ideal value occurs, the residual of the sum of feedback and compensation voltages emerges as the disturbance. The disturbance is superimposed to the original CI output signal and thus contributes to the IBN in the ΔΣ-modulator system.

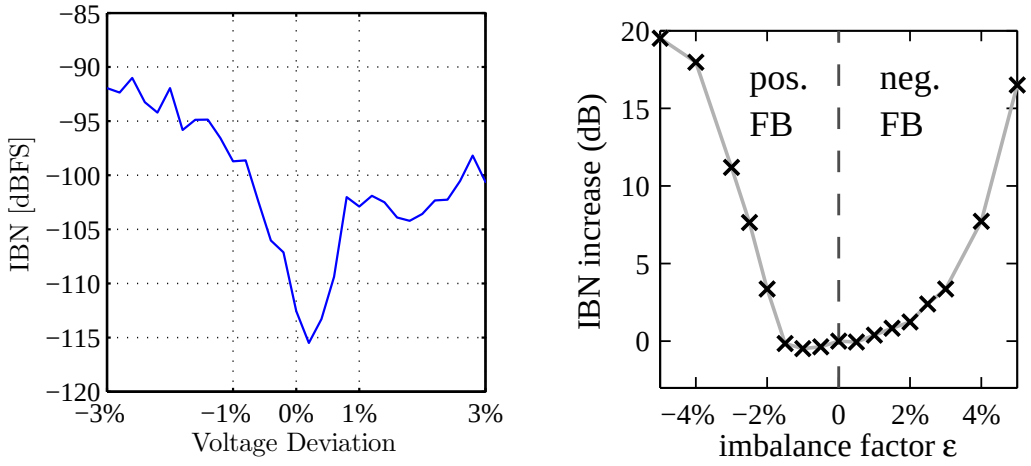
An ideal compensation is achievable only for theoretical analysis. In practical uti-

lization, it is more reasonable to set an acceptable range of imbalance in order to judge the required accuracy of the compensation voltage. Given $C_{\text{int}} = 125\,\text{fF}$, $C_{\text{comp}} = 1\,\text{pF}$, $C_{\text{para}} = 8\,\text{pF}$ and in the condition of balance $\Delta C_{\text{sense}} \approx 0$, one can calculate $k_C = 9.125$ from Equation 3.5. In this thesis the feedback voltage is set as $V_{\text{fb}} = 120\,\text{mV}$. Figure 3.5a plots the simulation result based on ±5% the deviation of V_{compC}. The simulation includes only the quantization noise while excludes the thermal noise from the mechanical part of the sensor element and the electrical noise in the ΔΣ-modulator. It can be observed that the IBN reaches minimum at V_{compC} of perfect balancing while quickly rises when V_{compC} deviates. This phenomenon comes from the high quality factor of the proof mass. However, it is so far difficult to achieve in the provided sensor element due to the extra damping factor caused by the low vacuum degree in the package. The measurement of IBN in lab under the change of imbalance factor is depicted in Figure 3.5b. One can observe a flatter notch of IBN around the balancing V_{compC}. Therefore one can define a range of 1% V_{compC} deviating from the ideal value, which is considered as the acceptable imbalance. Table 3.1 lists the IBN under the situation of balanced compensation and ±1% deviation of V_{compC}.Besides, the thermal and electrical noises are considered into the IBN in Figure 3.5b. The equivalent noise floor measured is about $4 \times 10^{-5}\,\text{V}/\sqrt{\text{Hz}}$. One can also discover that the IBN deteriorates relatively less when V_{compC} deviates positively than negatively. Since the capacitive compensation is applied at the inverse input of the CI, a positive deviation means negative feedback due to the overcompensation and vice versa. The further the deviation, the more difficult it gets to guarantee a stable closed loop behavior of the ΔΣ-modulator.[3]

Table 3.1: IBN of balanced compensation and ±1% deviation of V_{compC}.

Deviation of V_{compC}	IBN [dBFS]
0%	-109.04
1%	-94.78
-1%	-96.70

Fatal problem occurs when the imbalance in the readout system of the gyroscope is too high, because the IBN increases and thus the output of CI is not proportional to the angular rate Ω_a as the input signal of the gyroscope. Only noise is detected. If the CI turns into saturation, it is impossible to detect Ω_a. Figure 3.6 shows the waveform of the CI output in the condition of balance and imbalance, respectively. The imbalance is due to 1% V_{compC} over the ideal value but the resistive compensation is fulfilled. One can notice that the error signal is totally dominant in the unbalanced condition and thus the SNR is significantly decreased. Simulation data is acquired given that $\Omega_a = 1\,^\circ/\text{s}$ and $C_{\text{para}} = 8\,\text{pF}$. The balanced CI gives the output voltage in the range of $\pm 0.05\,\text{V}$ and the error is around $10^{-14}\,\text{V}$ due to the simulation tolerance. The proof mass is controlled to stay around the idle position



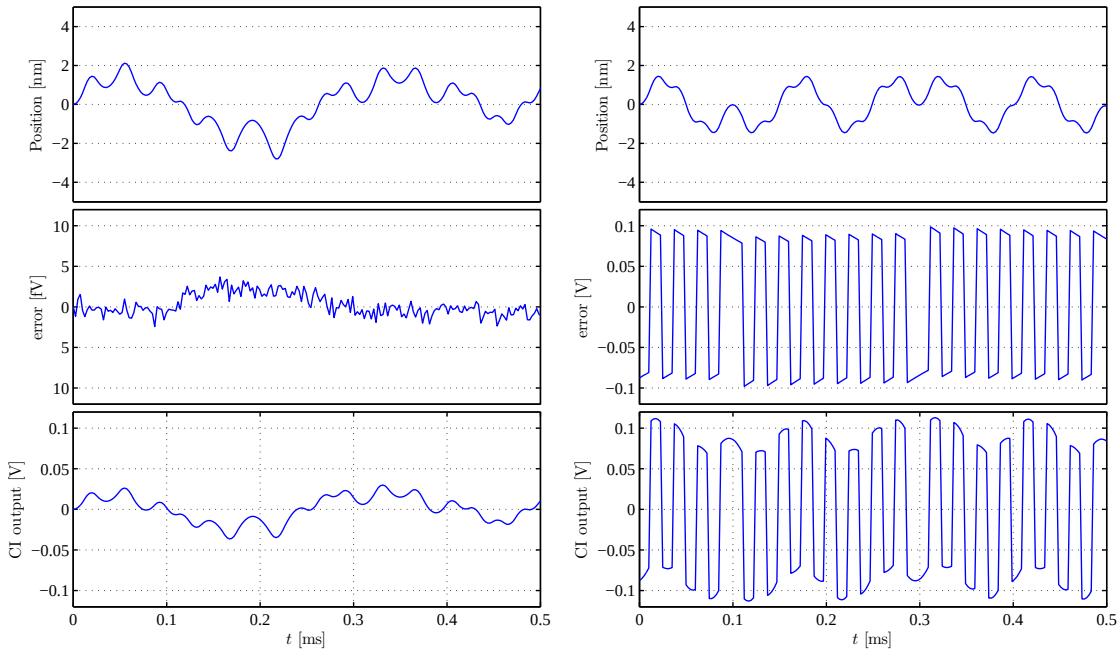
(a) (b)

Figure 3.5: Plots of IBN of the ΔΣ-modulator from (a) the simulation under the deviation of V_{compC} and (b) the measurement in the lab under the deviation of imbalance factor.

and the displacement range is about 2×10^{-9} m. The output of the unbalanced CI, however, reaches the rail and thus saturates the CI. The proof mass oscillates at the resonance frequency and shows offset to the idle position, because the modulator in saturation is not stable any more.

3.2 State-of-the-art Capacitive Compensation

The value of the parasitic capacitance can only be predicted in a reasonable range. The specification of the provided gyroscope gives the intrinsic parasitic capacitance of about 3 pF. Due to the layout of application-specific integrated circuit (ASIC), the total parasitic capacitance might reach up to 8 pF due to wiring and electrostatic discharge (ESD) pads. Equation 3.5 shows that the balanced condition can be satisfied by adjusting either C_{comp} or k_C in order to match the unknown C_{para}. An implementation called capacitor array is posted in [2]. In this structure, the equivalent compensation capacitor C_{comp} consists of three unit capacitors, which are configured in a 3-bit binary weighted array and thus only coarse selection of capacitance is achievable. The array is controlled by external logic blocks, such as data bus or register. Given the smallest value of 125 fF for the integration capacitors, the maximum value of C_{comp} can achieve 875 fF. A requirement of large C_{comp} can be realized by either larger integration capacitors or more binary levels, but more area on chip is occupied and less accuracy of matching to C_{para} is provided. Large C_{comp} also causes the increasing of noise and decreasing of bandwidth of the CI. Besides, the accuracy of compensation is determined by the least significant bit (LSB) of the



(a) (b)

Figure 3.6: The transient simulation results of the CI involving the position of proof mass, the error voltage and the CI output in the balanced (a) and unbalanced (b) condition. The imbalance is caused by 1% V_{compC} over the ideal value. The resistive compensation is already achieved.

capacitor array, which is limited by the manufacturing process adapted by the design. Another approach is setting the right V_{compC} in order to achieve the factor k_C for balancing. A typical solution of DAC can generate a range of voltages given the dynamic range and resolution. The necessary resolution of the compensation voltage is acquired according to the minimum acceptable amount of unbalance. Here, 1% deviation of V_{compC} is given as the standard, which is about 10 mV as mentioned in the subsection 3.1.3. Therefore a DAC at least with 10 bits is required given the dynamic range of 3.3 V. This brings a considerable challenge to the design in terms of linearity and offset. Actual implementation combines these two approaches, which means the utilization of 3-bit capacitor array for coarse tuning and adjustable V_{compC} for fine tuning.

The approach of configurable capacitor array implicitly makes it more difficult to achieve an accurate compensation. Instead, a fully analog implementation generates the compensation voltage with infinite levels and thus is theoretically capable to achieve perfect balance. Besides, a manual compensation requires additional time-costly calibration step. As a result, the automatic voltage compensation is significantly benefited for the situation that the parasitic parameters are variable due to the fabrication process. The chip runs the calibration program after the startup

of the system and the balanced compensation is automatically achieved in a small time span. By the equipment of data storage blocks, the compensation value can be memorized digitally and directly used as the initial value for the compensation at the next calibration. This saves the time of the compensation process even more.

4 Automatic Compensation Controller

In previous work a continuous-time collocated feedback (CCFB) readout loop was developed. This concept makes it possible to detect the deflection of the proof mass of a capacitive sensor such as a gyroscope or an accelerometer, while simultaneously applying a feedback force using the same electrodes. This restoring force is required for a closed loop operation by the electromechanical $\Delta\Sigma$-modulator. For the stable operation of the CCFB, precise trimming of the capacitive compensation voltage V_{compC} is required. Figure 4.1 shows the conceptual schematic of the $\Delta\Sigma$-modulator with feedback and compensation paths, in which the automatic compensation controller is implemented to control V_{compC}.

In this chapter, a detailed analysis of the automatic compensation controller is presented. Firstly, the theoretical mechanism of an automatic controlling system and related functional blocks are introduced. Then several implementation approaches are described in terms of principle, performance and its stability analysis. Mechanical and electrical noises deteriorate the SNR in the $\Delta\Sigma$-modulator. The influence of the controller to the SNR is studied accordingly. In the end, a concept of preset offset is introduced in order to reduce the settling time of the compensation procedure and relax the requirement on dynamic range of the control loop.

All simulations and analyses in this chapter are processed in a MATLAB® Simulink® environment. Simulink is a graphical programming environment for modeling, simulating and analyzing multi-domain dynamic systems and offers tight integration with the MATLAB environment and can either drive MATLAB or be scripted from it.

4.1 Theory and Structure

The automatic compensation controller consists of three stages, respectively named as detection, controlling and voltage generation, which are illustrated in Figure 4.2. The detection stage measures the disturbance at the CI output; the controlling stage determines the required magnitude of compensation; the voltage generation stage generates the analog compensation voltage.

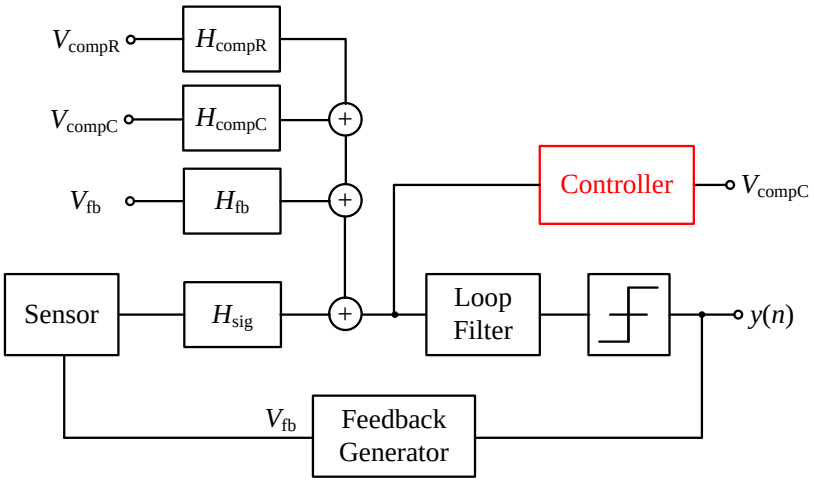


Figure 4.1: A conceptual schematic of the ΔΣ-modulator including the automatically controlled capacitive compensation path.

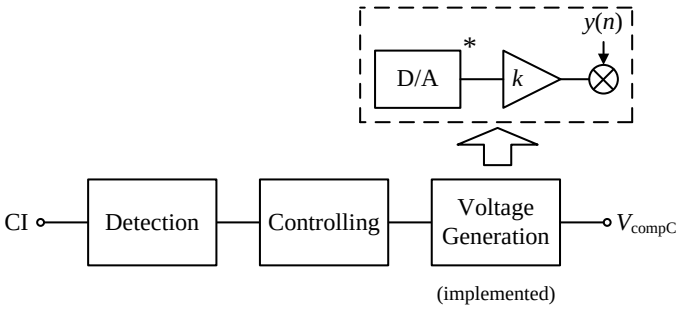


Figure 4.2: A block diagram of the automatic compensation controller. An implementation of the voltage generation is already available.

- Detection. The magnitude of imbalance can be extracted from the amplitude of the disturbance and can be processed in two methods. In order to detect the low frequency component, the disturbance signal can be either demodulated with the bitstream or integrated by a LPF. In order to detect the high frequency component, the slew rate of the disturbance signal can be detected by differentiation of the CI output signal. Both proposals are investigated and introduced in detail throughout the following chapter.

- Controlling. The detection result is observed by the controlling stage. In general, the controlling stage separates the useful information from the result and calculates the magnitude of the required compensation. Since the controller is configured as a closed loop structure in the top-level system, the output

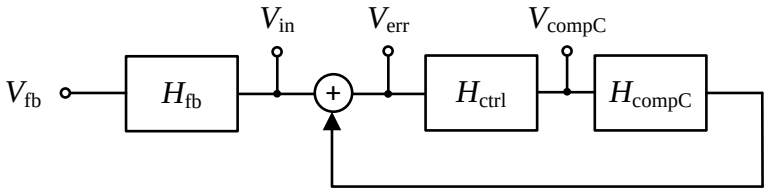


Figure 4.3: A conceptual schematic of the control loop. The control error is suppressed by the open loop gain $|H_{\text{ctrl}}H_{\text{compC}}|$.

of the controlling stage gradually approximates the accurate value for perfect compensation. Nevertheless, there always exists error in the magnitude of compensation in the practical case and thus a perfect compensation can never be achieved.

- Voltage generation. Based on the specific implementation of the controlling stage, the structure of voltage generation stage can vary accordingly. For an analog implementation, the analog voltage generated by the controlling stage is directly modulated on the bitstream. For mixed-signal implementation with digital output, the digital value must be firstly converted by a DAC.

Figure 4.3 shows the conceptual schematic of the control loop involving the simplified and rearranged feedback and compensation paths. It is under the assumption of balanced resistive compensation and neglected transmission path of the sensor signal. Thus, the input signal V_{in}, which refers to the voltage on the feedback path, is converted to the control error V_{err} due to the closed loop function as expressed by

$$V_{\text{err}} = H_{\text{err}} V_{\text{in}} \tag{4.1}$$

where

$$H_{\text{err}}(s) = \frac{1}{1 - H_{\text{ol}}(s)} = \frac{1}{1 - H_{\text{ctrl}}(s) H_{\text{compC}}(s)} \tag{4.2}$$

A large gain of H_{ol} is required to achieve a small magnitude of H_{err}. Since H_{compC} is already fixed by the CI circuit, the open loop gain is basically controlled by H_{ctrl}. The transmission characteristic of $H_{\text{ol}}(s)$ determines the magnitude of suppression throughout different frequency components. Due to the limited bandwidth, a controller configured by opamp normally deteriorates on the gain in the high frequency range. Thus, a better compensation is achieved by shifting more frequency components of the input signal to low frequency range or even DC.

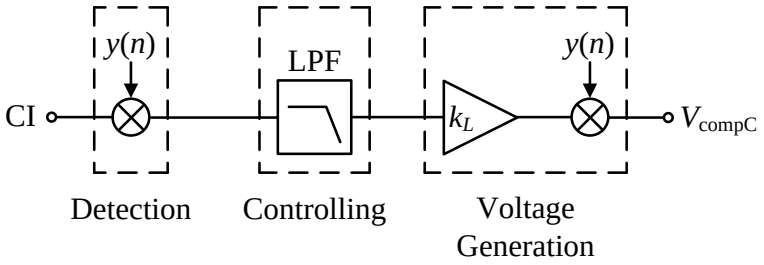


Figure 4.4: A block diagram of the demodulation-type compensation controller. The functional stages of detection, controlling and voltage generation are highlighted.

4.2 Demodulation

The imbalance of the CCFB comes from the residual sum of the feedback and compensation signal correlated to the bitstream. The amplitude refers to the magnitude of disturbance. By the method of demodulation, the disturbance is shifted into the baseband and thus DC signal is measured while high frequency components are suppressed.

4.2.1 Principle

The illustration of the compensation controller with demodulation structure is shown in Figure 4.4. $y\,(n)$ represents the bitstream generated by the quantizer, which can be simplified as fixed sinusoidal signal for straightforward analysis. Firstly, the output of CI including the disturbance is demodulated by the bitstream. Next, The LPF eliminates the high frequency components while the offset remains, which is relevant to the magnitude of disturbance. Finally the output of LPF is scaled to proper amplitude by k_L and modulated on the bitstream, generating the compensation voltage V_{compC}.

Figure 4.5 shows the conceptual schematic of the controller including the modulation and demodulation stages. H_{LPF} represents the LPF in the control loop. $V_{\text{err,dem}}$ represents the control error as the residual of the disturbance. Figure 4.6 shows the part of the control loop including H_{compC} as well as the modulation and demodulation block before and after. The bitstream includes the baseband frequency ω_m and corresponding harmonics, which requires the analysis by nonlinear method. Therefore, the bitstream is written as $\sin(\omega_m t)$ for the simplified calculation, with ω_m the angular frequency of modulation. One can calculate the expression of the output signal $U_{\text{out}}\,(s)$ by following the steps shown below. $u\,(t)$, $u_1\,(t)$, $u_2\,(t)$ and $u_{\text{out}}\,(t)$

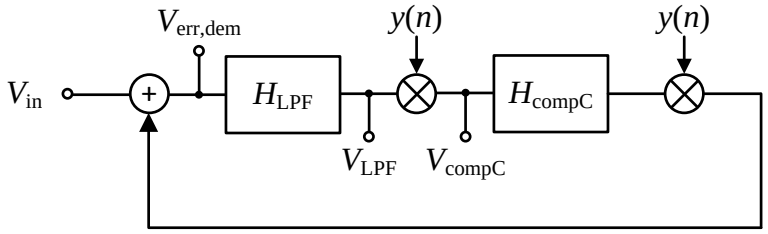


Figure 4.5: A conceptual schematic of the closed loop demodulation type compensation controller.

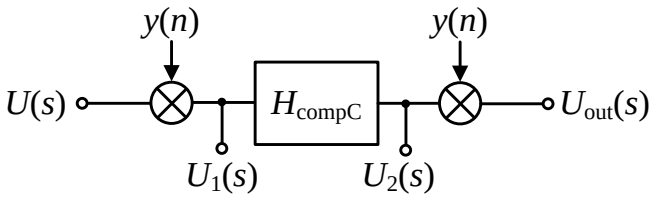


Figure 4.6: A conceptual schematic of the modulated transfer function for the capacitive compensation.

represent to the signal in time domain at corresponding nodes shown in Figure 4.6.

Step 1:

$$\begin{aligned} u_1(t) &= u(t) \cdot \sin\omega_m t \;\Rightarrow \\ U_1(s) &= U(s) * \frac{\delta(s - j\omega_m) - \delta(s + j\omega_m)}{2j} \\ &= \frac{U(s - j\omega_m) - U(s + j\omega_m)}{2j} \end{aligned} \tag{4.3}$$

Step 2:

$$\begin{aligned} u_2(t) &= u_1(t) * H_{\text{compC}}(t) \Rightarrow \\ U_2(s) &= U_1(s) \cdot H_{\text{compC}}(s) \\ &= \frac{U(s - j\omega_m) H_{\text{compC}}(s) - U(s + j\omega_m) H_{\text{compC}}(s)}{2j} \end{aligned} \tag{4.4}$$

Step 3:

$$
\begin{aligned}
& u_{\text{out}}(t) = u_2(t) \cdot \sin\omega_m t \;\Rightarrow \\
& U_{\text{out}}(s) = U_2(s) * \frac{\delta(s-j\omega_m) - \delta(s+j\omega_m)}{2j} \\
& = \frac{U(s-j\omega_m) H_{\text{compC}}(s) - U(s+j\omega_m) H_{\text{compC}}(s)}{2j} * \frac{\delta(s-j\omega_m) - \delta(s+j\omega_m)}{2j} \\
& = \frac{1}{2j} \cdot \frac{1}{2j} \cdot [U(s-2j\omega_m) H_{\text{compC}}(s-j\omega_m) - U(s) H_{\text{compC}}(s-j\omega_m) \\
& \quad + U(s+2j\omega_m) H_{\text{compC}}(s+j\omega_m) - U(s) H_{\text{compC}}(s+j\omega_m)] \\
& \approx \frac{1}{2j} \cdot \frac{1}{2j} \cdot [-U(s) H_{\text{compC}}(s-j\omega_m) - U(s) H_{\text{compC}}(s+j\omega_m)] \\
& = U(s) \cdot \frac{H_{\text{compC}}(s-j\omega_m) + H_{\text{compC}}(s+j\omega_m)}{4}
\end{aligned}
\tag{4.5}
$$

Here, higher frequency terms $U(s-2j\omega_m)$ and $U(s+2j\omega_m)$ are neglected because one expects the suppression of these terms by the LPF. A low cutoff frequency, especially in the range of several Hz, is necessary in this case but difficult to achieve for a common passive LPF because it requires large resistance and capacitance, which is impractical in the ASIC design. In [15, 16] the solution of gm-C filter structure can overcome this problem. This type of active LPF is capable to achieve the cutoff frequency in the range of sub-Hz. In addition, the power consumption of the gm-C filter is very low.

The expression of the output voltage now can be written in the form of:

$$
\begin{aligned}
& U_{\text{out}}(s) = U(s) \cdot \left[\frac{H_{\text{compC}}(s)}{2} * \frac{\delta(s-j\omega_m) + \delta(s+j\omega_m)}{2} \right] \\
& \Rightarrow u_{\text{out}}(t) = u(t) * \frac{1}{2} \left[H_{\text{compC}}(t) \cdot \cos\omega_m t \, \right] \cong u(t) * H_{\text{modC,dem}}(t)
\end{aligned}
\tag{4.6}
$$

Equation 4.6 can be also written as

$$
U_{\text{out}}(s) = U(s) H_{\text{modC,dem}}(s) \tag{4.7}
$$

where

$$
H_{\text{modC,dem}}(s) = \frac{H_{\text{compC}}(s-j\omega_m) + H_{\text{compC}}(s+j\omega_m)}{4} \tag{4.8}
$$

The transfer characteristics can be written as a multiplication of H_{compC} and a cosine signal with the modulation frequency ω_m, which is called the modulated transfer function $H_{\text{modC,dem}}$. In the frequency domain, the modulated transfer function is the sum of two replicas of original spectrums, which is shifted by ω_m to higher or lower frequency, respectively. Since H_{compC} has a high-pass behavior, the magnitude

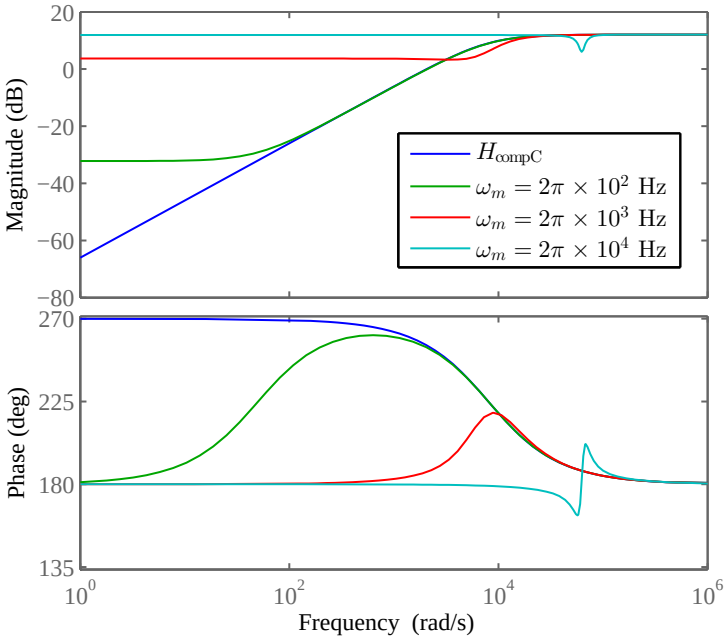


Figure 4.7: A Bode plot of cosinus-modulated transfer functions $H_{\text{modC,d}}(s)$ depending on different modulation frequencies ω_m. The magnitude and phase gradually turn to constant as ω_m increases.

reaches maximum when $f > f_{c,\text{HcompC}}$, with $f_{c,\text{HcompC}}$ the corner frequency of H_{compC}. Thus, the sum is dominated by the replica at higher frequency when ω_m is large. In this case, the modulated transfer function can be approximated to the high frequency part of H_{compC} and thus considered as constant magnitude as expressed below:

$$H_{\text{modC,dem}}(s) \approx \frac{1}{2} H_{\text{compC}}(s)|_{f\to\infty} = -\frac{1}{2}\frac{C_{\text{comp}}}{C_{\text{fb}}} \cong k_{\text{mod,dem}} \tag{4.9}$$

Figure 4.7 illustrates the dependency of the transfer characteristics of $H_{\text{modC,dem}}(s)$ on the modulation frequency ω_m. As ω_m increases, the difference in magnitude and phase between the frequency range $f < f_{c,\text{HcompC}}$ and $f > f_{c,\text{HcompC}}$ becomes smaller until the transfer characteristic is considered constant throughout the frequency domain. The open loop transfer function of the demodulation structure $H_{\text{ol,dem}}$ can be accordingly simplified to

$$H_{\text{ol,dem}}(s) = H_{\text{LPF}}(s)\, H_{\text{modC,dem}}(s) \cong k_{\text{mod,dem}} H_{\text{LPF}}(s) \tag{4.10}$$

H_{LPF} can be written as

$$H_{\text{LPF}}(s) = \frac{k_L}{1 + \dfrac{s}{2\pi f_c}} \tag{4.11}$$

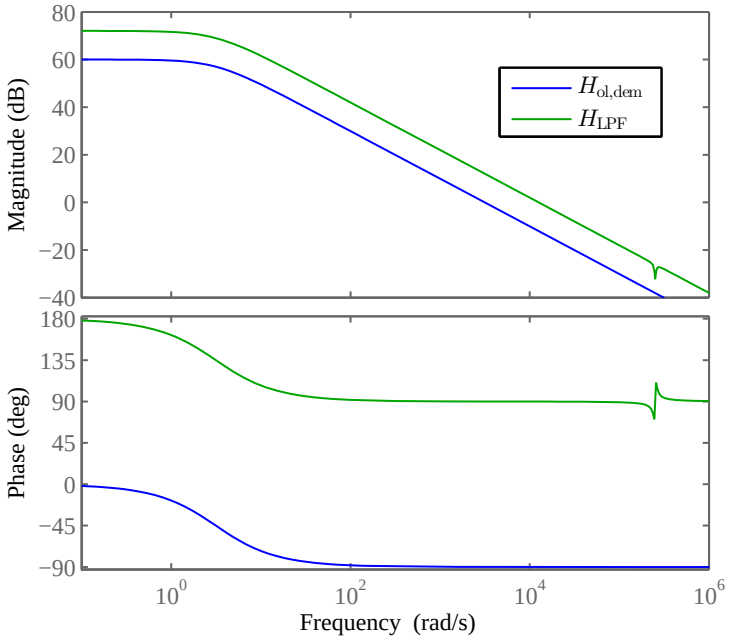


Figure 4.8: A Bode plot for the comparison between the LPF H_{LPF} and open loop transfer function $H_{\mathrm{ol,dem}}$.

with k_L involved as the DC gain and f_c the corner frequency of the LPF. In consequence, $H_{\mathrm{ol,dem}}(s)$ also shows the low-pass behavior as $H_{\mathrm{LPF}}(s)$ with additional gain as shown in the Bode plot from Figure 4.8.According to Equation 4.2, the residual of disturbance is calculated by

$$H_{\mathrm{err,dem}}(s) = \frac{1}{1 - H_{\mathrm{ol,dem}}(s)} = \frac{1}{1 - k_{\mathrm{mod,dem}} H_{\mathrm{LPF}}(s)} \tag{4.12}$$

The compensation controller is a closed loop system, of which the stability can be investigated by the open loop transfer function $H_{\mathrm{ol,dem}}(s) = H_{\mathrm{LPF}}(s) H_{\mathrm{modC,dem}}(s)$. Since $H_{\mathrm{modC,dem}}$ can be approximated as a pure gain factor in a wide range of frequency, in first order the control loop can be described as a one-pole system and thus is guaranteed stable. Figure 4.9 illustrates the waveform during the compensation process. One can notice that less fluctuation exists in the output of LPF in the case of $f_c = 0.5\,\mathrm{Hz}$ than $f_c = 5\,\mathrm{Hz}$ because more high frequency components are suppressed.

4.2.2 Stability of the ΔΣ-modulator with the control loop

As described in subsection 2.3.2, the stability of the ΔΣ-modulator is guaranteed by the lead filter. However, the compensation controller can also be involved in the transfer characteristics of the modulator. Not only the disturbance but also

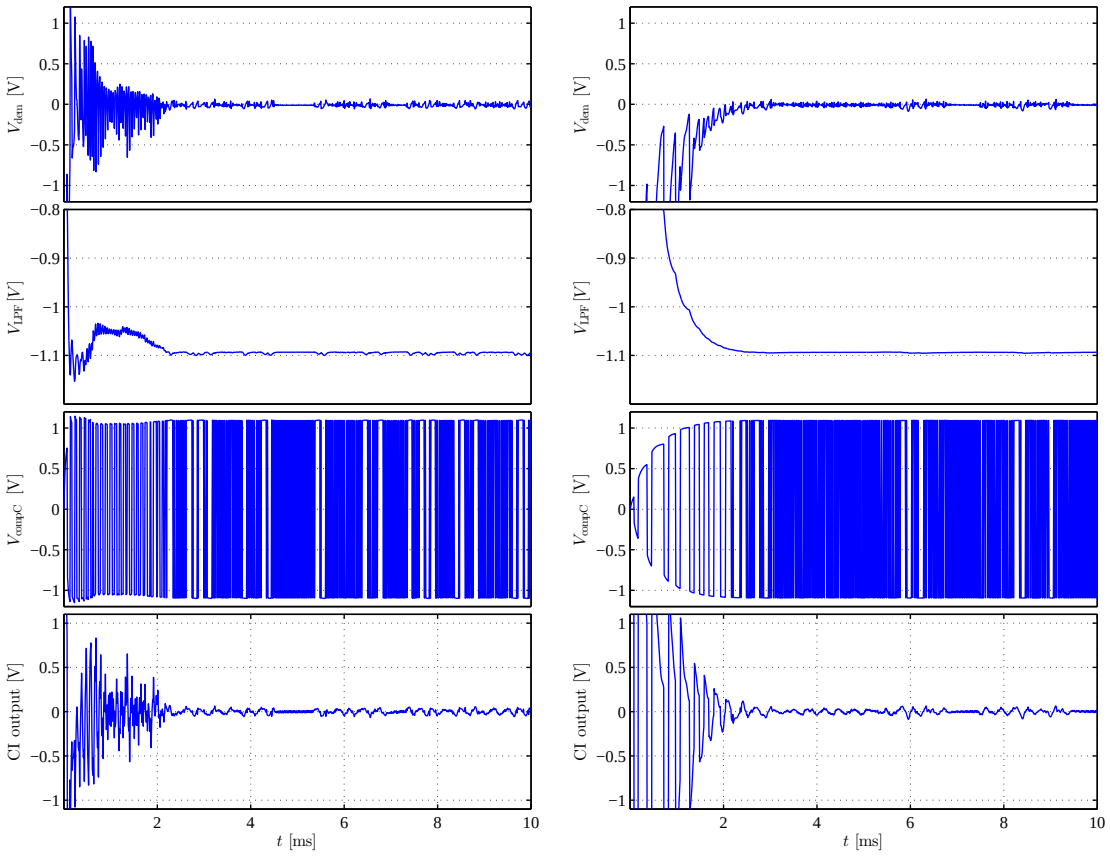
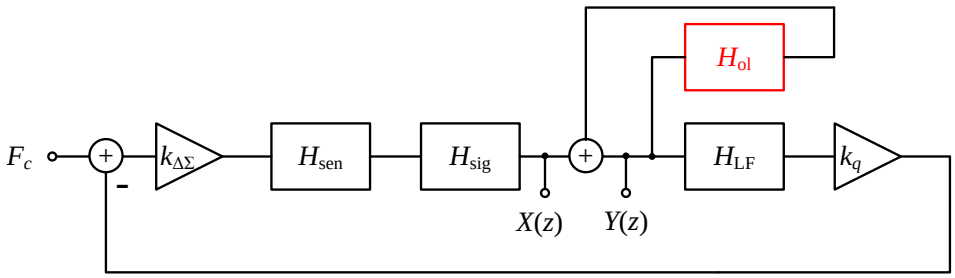


Figure 4.9: The transient simulation results of the compensation process in the case of $f_c = 5\,\mathrm{Hz}$ (a) and $f_c = 0.5\,\mathrm{Hz}$ (b). $k_L = 100$ for both cases. V_{dem} refers to the demodulated input of controller.

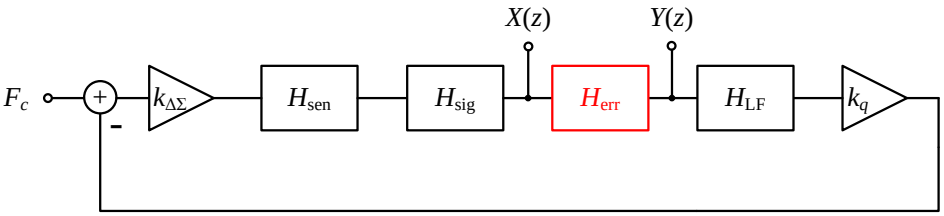
the sensor output signal is shaped by the controller during the operation of the $\Delta\Sigma$-modulator. As depicted in Figure 4.10a, $X(z)$ represents the output of H_{sig} while $Y(z)$ the control error which couples back into the $\Delta\Sigma$-modulator loop. The equivalent $\Delta\Sigma$-modulator schematic shows the integrated transmission block $H_{\mathrm{err,dem}}$ as depicted in Figure 4.10b, of which the open loop transfer function is expressed with

$$H_{\Delta\Sigma,\mathrm{err,dem}}(z) = k_{\Delta\Sigma} k_q H_{\mathrm{sen}}(z) H_{\mathrm{sig}}(z) H_{\mathrm{err,dem}}(z) H_{\mathrm{LF}}(z) \tag{4.13}$$

with k_q the equivalent gain of the quantizer and $k_{\Delta\Sigma}$ the rest of gain factors in total. Its stability can be analyzed by the root locus and the results are shown in Figure 4.11. The unity circle represents the region of convergence (ROC). For a 1-bit quantizer, the gain can range from zero to infinity by an arbitrary signal input. It is still variable though the practical system limits both of the extremes.[17] As k_q increases, some roots move closer to the unity circle. The intersections are highlighted in Figure 4.11a, which represents the root locus of the original $\Delta\Sigma$-

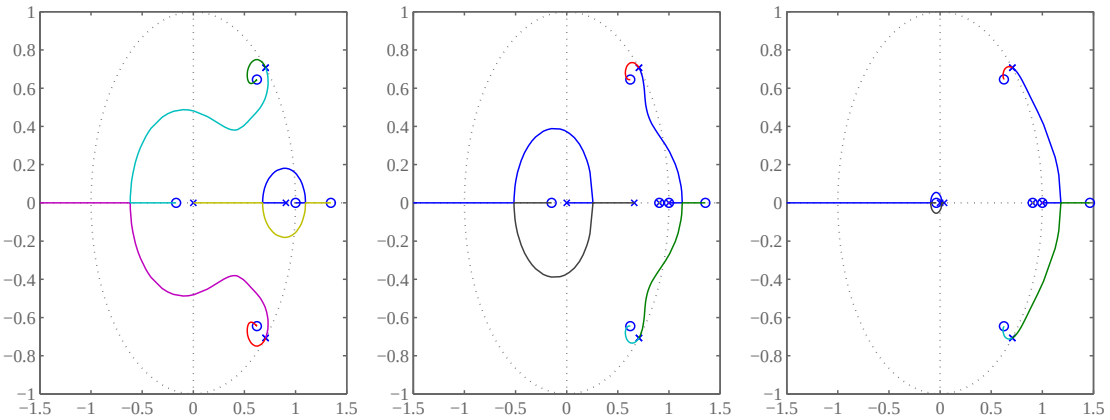


(a)



(b)

Figure 4.10: A schematic of the $\Delta\Sigma$-modulator loop with the compensation controller (a). The transfer functions are expressed in the Z-domain. $X(z)$ is the output of the CI and $Y(z)$ is the control error. The equivalent schematic with $H_{\mathrm{err,dem}}$ integrated in the loop is shown in (b).



(a) (b) (c)

Figure 4.11: A root locus plot for the $\Delta\Sigma$-modulator loop (a) and with the compensation controller in the case of $k_L = 10^3$ (b) and $k_L = 10^4$ (c). $f_c = 5\,\mathrm{Hz}$ in both cases.

modulator. k_q must be less than the minimum gain among which are correlated to these intersections so that all roots are located in the unity circle. In the case of $k_L = 10^3$ and $f_c = 5\,\text{Hz}$ as shown in Figure 4.11b, two intersections has lower corresponding gain in comparison to Figure 4.11a, which means that k_q is limited in a smaller range. In the case of $k_L = 10^4$ and $f_c = 5\,\text{Hz}$ as shown in Figure 4.11c,two locus don't across the unit circle. The corresponding roots are always located outside the unity circle and thus the instability of the $\Delta\Sigma$-modulator cannot be avoided.

4.2.3 Ringing on the disturbance

When the stability of the control loop is guaranteed, more transient specifications can be analyzed on H_{err}. Regarding to the pole zero map, H_{err} introduces one pair of conjugated pole, one pair of conjugated zero, one real pole and one real zero as listed in Table 4.1. Figure 4.12 illustrates the movement of poles and zeros due to the variance of k_L as well as the corresponding plots of the step response. While increasing k_L, the zero pair stands still while the pole pair moves on the plane. The real part of the moving conjugated pole determines the damping factor of H_{err}, which can be observed in the step response plot. The arrows indicate the direction of the movement in the pole zero map and the corresponding change of waveforms in step response plots. When k_L is low ($k_L = 10^2$), the moving pole pair is very close to the zero pair and thus they approximately cancel each other. Its step response becomes similar to PT1 behavior. As k_L increases further, the pole pair gradually moves away from the zero pair and the ringing starts to appear in the step response. Its amplitude increases as the pole pair continues moving away from the zero. The frequency of the ringing is determined by the imaginary part of the pole. Then the distance in the imaginary axis between pole and zero decreases as k_L keeps increasing. Thus, the amplitude of ringing starts to decrease. The ringing component contributes noise to the $\Delta\Sigma$-modulator, which is folded to the baseband by the quantizer. Thus, it increases the IBN and deteriorates the SNR.

Table 4.1: The poles and zeros of H_{err} when $k_L = 10^2$ and $f_c = 0.5\,\text{Hz}$.

Pole	Zero
$-7.996 \times 10^3 \pm 2.519e \times 10^5 i$	$-8.000 \times 10^3 \pm 2.521e \times 10^5 i$
-1.261×10^4	-31.416

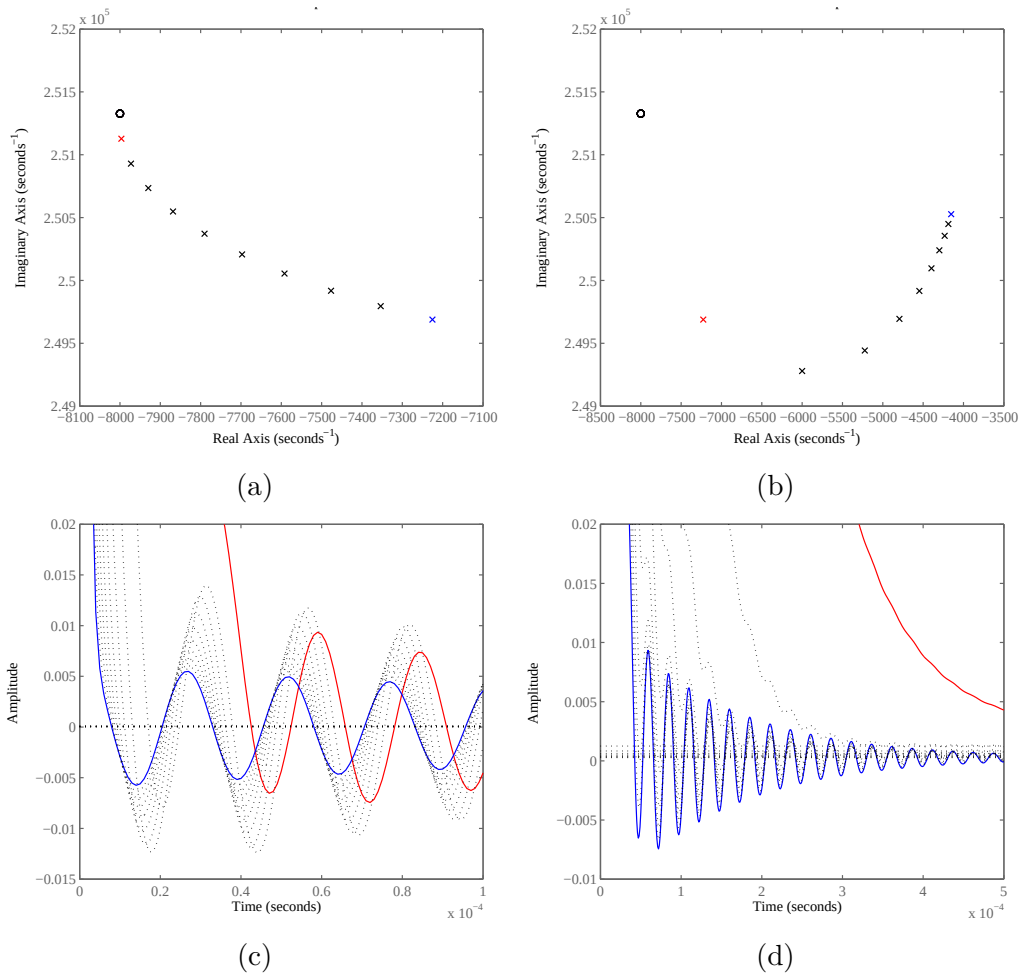


Figure 4.12: The analysis of transient characteristics of the control loop by the illustration of pole zero map and step response of $H_{\text{err,dem}}$. The position of the poles "x" and the zeros "o" are marked. Only poles and zeros above the real axis are visible because of the symmetry of conjugation. Plots of the movement of the pole are depicted in the case of $k_L = 10^2 \sim 10^3$ (a) and $k_L = 10^3 \sim 10^4$ (b). The initial pole is colored in red and ends at the blue one. The step response in the case of $k_L = 10^2 \sim 10^3$ (c) and $k_L = 10^3 \sim 10^4$ (d) are depicted. The curve changes from the red one to the blue one accordingly. All simulations are performed with $f_c = 0.5\,\text{Hz}$.

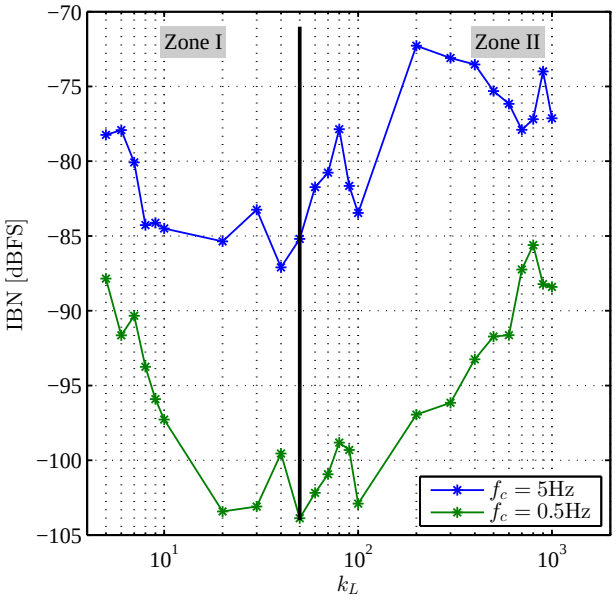
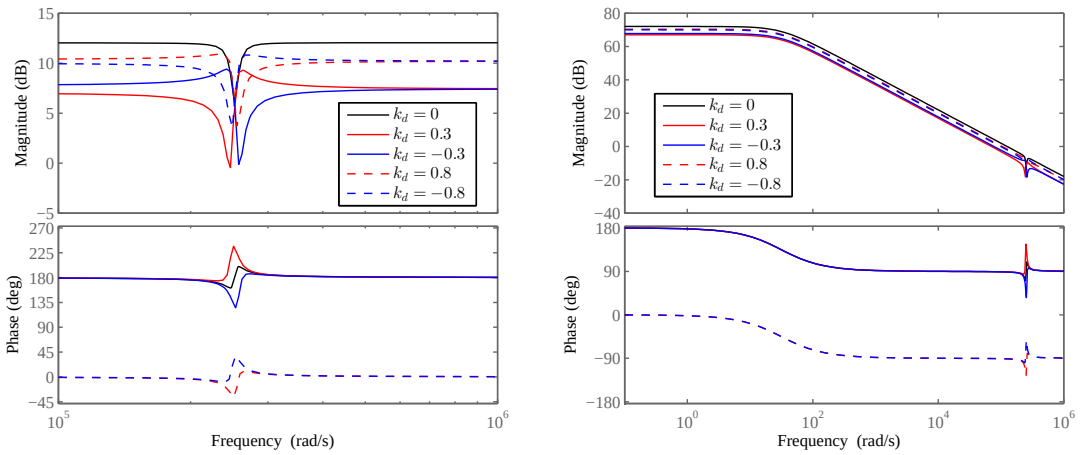


Figure 4.13: A plot of the IBN with k_L sweeping from 5 to 10^3 when $f_c = 5\,\text{Hz}$ and 5 to 10^4 when $f_c = 0.5\,\text{Hz}$.

Figure 4.13 shows the IBN by sweeping k_L in the case of $f_c = 5\,\text{Hz}$ and $f_c = 0.5\,\text{Hz}$. The IBN achieves the minimum value when k_L is in the range of $10^1 \sim 10^2$. For $f_c = 5\,\text{Hz}$, the minimum IBN is around -87 dBFS when $k_L = 40$; For $f_c = 0.5\,\text{Hz}$, the minimum IBN is around -104 dBFS when $k_L = 50$. One can separate the plot of changing IBN in two zones due to the dominant factor respectively. In Zone I the IBN is mostly contributed by the disturbance, on which the suppression increases with k_L. In Zone II the ringing effect starts to overcome the disturbance as k_L increases. In order to satisfy the specification of a maximum deviation of $\pm 1\%$ V_{compC} from its ideal value, $f_c = 0.5\,\text{Hz}$ is chosen and k_L should be in the corresponding range.

4.2.4 Transmission delays in the compensation network

In the practical ASIC design, the influence on the performance of the $\Delta\Sigma$-modulator, which is introduced by the transmission delay of the signals, cannot be neglected. We consider two cases of misalignment of the signals correlated to the bitstream. In one case, V_{compC} and V_{fb} are temporally aligned, while the misalignment exists between the bitstream paths of modulation and demodulation block in the controller. This means that bitstream for demodulation is ahead or after the quantizer output. In the other case, the bitstream paths of modulation and demodulation block in the controller are aligned, while the misalignment exists between V_{compC} and V_{fb}. This means that bitstream for the modulation of feedback voltage is ahead or after the quantizer output.



(a) (b)

Figure 4.14: A Bode plot of $H_{\text{modC,dem}}$ (a) and $H_{\text{ol,dem}}$ (b) in the consideration of delay at the demodulation controller.

In the first case, the delay at the demodulation block is expressed by

$$T_d = \frac{k_d}{f_s} \tag{4.14}$$

with k_d named as the delay factor. A positive k_d means that the bitstream arrives later than expected while a negative k_d means earlier. Based on the default case introduced in subsection 4.2.1, the output signal with delay at the demodulation block is derived from

$$\begin{aligned} U_{\text{out}}(s) &\cong U_2(s) * \left[\frac{\delta(s - j\omega_m) - \delta(s + j\omega_m)}{2j} \cdot e^{-T_d s}\right] \\ &= U(s) \cdot \frac{H_{\text{compC}}(s - j\omega_m) \cdot e^{T_d j\omega_m} + H_{\text{compC}}(s + j\omega_m) \cdot e^{-T_d j\omega_m}}{4} \end{aligned} \tag{4.15}$$

By this we have the expression of $H_{\text{modC,dem}}$ and $H_{\text{ol,dem}}$ in the case of delay. Figure 4.14 shows the Bode plot of $H_{\text{modC,dem}}$ and $H_{\text{ol,dem}}$ in the consideration of delay at the demodulation block. The magnitude of $H_{\text{modC,dem}}$ decreases to the minimum near zero and then increases back to the initial value as $|k_d|$ increases from 0 to 1. Besides, the phase shifts by -180° when $0.5 < |k_d| < 1$. This causes the proportional change in the magnitude and phase of $H_{\text{ol,dem}}$. When $0 < |k_d| < 0.5$, the influence of delay on the $\Delta\Sigma$-modulator is equivalent to nothing but the controller with smaller open loop gain. When $0.5 < |k_d| < 1$, the additional phase shift changes the polarization of the feedback and thus the closed loop controller is unstable.

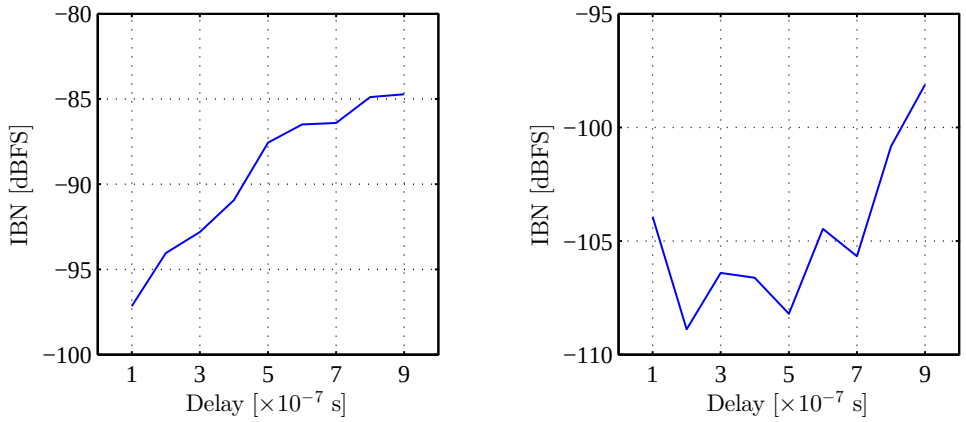


Figure 4.15: A plot of IBN based on the delay in the feedback path (a) and the capacitive compensation path (b). The setting of the LPF is $k_L = 10^2$ and $f_c = 0.5\,\text{Hz}$.

In the second case, the balanced CI requires the alignment in time domain between feedback and compensation signals, which are all synchronized to the bitstream. Due to the linear model shown in Figure 4.1, a temporal mismatch causes spikes due to the high slew rate of the feedback and compensation signals. These spikes could be dominant in the signal path and may serious influence the performance of $\Delta\Sigma$-modulator. Supposing the resistive compensation path intrinsically synchronizes to the feedback path due to its generation, we only analyze the misalignment of the capacitive compensation path caused by the controller. We consider both situations of mismatch due to the capacitive compensation signal has either positive or negative phase shift in comparison to the feedback signal. This phase shift is realized by delaying the bitstream signal used for the modulation of the compensation voltage from the LPF. Figure 4.15 shows the IBN when the delay varies from 100 ns to 900 ns for both cases. The IBN monotonously increases to around -84 dBFS as the delay in the feedback path increases, while the IBN achieves minimum when the compensation path has delay of maximum 500 ns and then increases. Therefore, more tolerance of the transmission delay is available in the capacitive compensation path for the transistor-level design. A good layout can limit the group delay under a few nano-seconds, by which the impact of the misalignment between the feedback and compensation signals is very small. Instead, different slew rates between V_{fb} and V_{compC} due to the corresponding amplifiers will more likely cause spikes.

4.2.5 Option: Duty-cycle LPF

As described in subsection 4.2.2, the corner frequency f_c of the LPF influences the IBN regardless of the DC gain k_L. A sub-Hz frequency of f_c is quite a challenge to

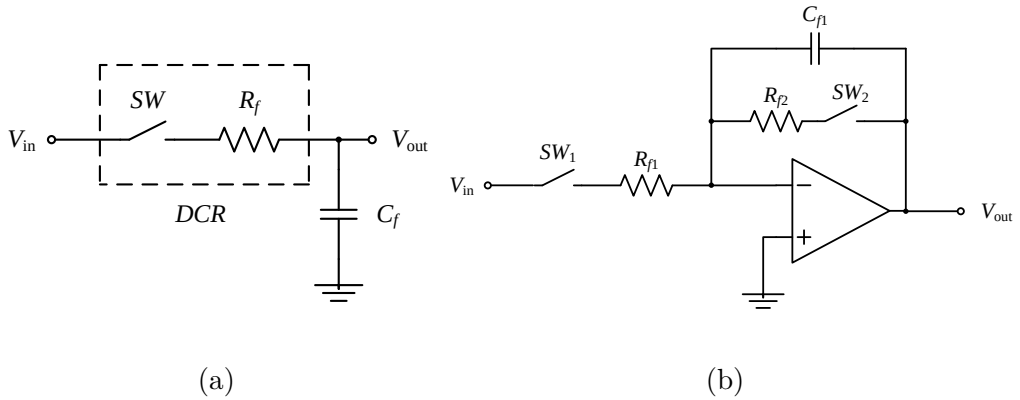


Figure 4.16: A conceptual schematic in which the duty-cycle resistor (DCR) is equipped in a passive LPF (a) and an active LPF (b).

the circuit design, because high resistances and capacitances are not feasible due to its large area occupation on chip. There are several alternatives to achieve a LPF with very low corner freqency. Normally they are specified for either generating an enlarged equivalent capacitance like capacitance multiplier, or enlarged equivalent resistance like gm-C filter[15, 16] and pseudo resistor[18]. Nevertheless, they requires much effort during the system design and can be sensitive to the variation on the component value over the manufacuring process and temperature. In [19, 20] the concept of a duty-cycle resistor (DCR) is introduced with relatively simple implementation. This method can be categoried to the resistance enhancement as mentioned before. Figure 4.16a illustrates a schematic of a passive LPF, in which the resistor R_f is configure as a DCR by a switch. When the switch is closed, the input signal is connected to R_f and thus is filtered. When the switch is open, the output voltage maintains stable because the capacitor C_f doesn't discharge. The switch is controlled by a trigger signal with the duty cycle of D and period of T_{sw}, which reduces the average current flowing through R_f. As a result, the equivalent resistance is R_f/D and the equivalent corner frequency of the LPF decreases to $D/C_f R_f$. This strategy can also be applied to an active LPF as shown in Figure 4.16b. Here, two switches are used for disconnecting the resistor R_{f1} and R_{f2} from the circuit. In the first time interval of DT_{sw}, both switches are closed and the filter works as normal. In the second time interval of $(1-D)\,T_{sw}$, both switches are open and thus the potential of capacitor C_{f1} is maintained by the opamp. Here, a filter implemented with DCR is called duty-cycle filter (DCF).

A functional structure of the demodulation compensation controller with the duty-cycle LPF is illustrated in Figure 4.17. Here, switches are realized by multipliers with trigger signals V_{sw1} and V_{sw2}. The second switch, however, is settled on the feedback path over the LPF. There are two reasons for this different structure. On one hand, the LPF for the system level simulation is built by the transfer function,

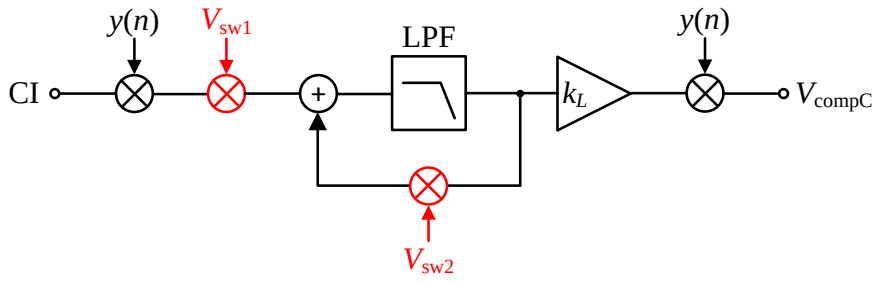


Figure 4.17: A block diagram of the demodulation compensation controller with the option of duty-cycle LPF.

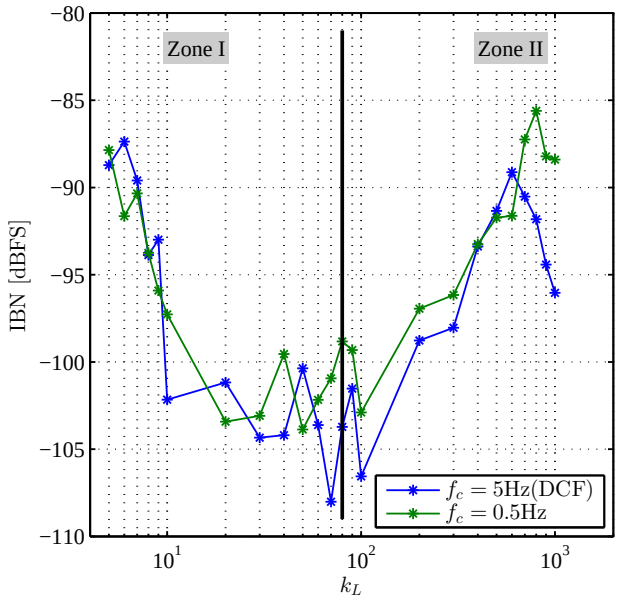


Figure 4.18: A plot of the IBN with k_L sweeping from 5 to 10^3 when $f_c = 5\,\mathrm{Hz}$ with the DCF option in comparison to the case of $f_c = 0.5\,\mathrm{Hz}$ in the original demodulation controller.

which can only be utilized as a whole. On the other hand, it is not possible to perform a floating input node in the simulation. Instead, it will be connected to the zero potential by default, which causes the discharge behavior of a LPF. In order to avoid instability, the DC gain of the LPF must not be more than one. k_L is used for the adjustment on the loop gain of the controller. Another difference is that the trigger signals for these switches have now the opposite polarity, which means that the duty cycle is D for V_{sw1} and $(1 - D)$ for V_{sw2}. During the simulation, the setting of trigger signal is $T_{sw} = T_s$ and $D = 0.1$. Figure 4.18 shows the IBN by sweeping k_L in the condition of $f_c = 5\,\mathrm{Hz}$ in comparison to the data from $f_c = 0.5\,\mathrm{Hz}$ in

the original demodulation structure. The best result achieved is -108 dBFS when $k_L = 70$. A good match is observed from the plot and thus the duty-cycle LPF is a prospective approach for a sub-Hz LPF implemented in the controller.

A possible drawback of the duty-cycle LPF is the noise folding effect due to the sample-hold behavior. The minimum pulse width of the trigger signal equals to the system clock frequency. Thus, a higher duty cycle can be achieved only by decreasing the frequency of the trigger signal, by which the noise folding effect is enhanced. This results in a reasonable range of the equivalent corner frequency of the duty-cycle LPF.

4.3 Differential

The sensor signal is superimposed on the residual of bitstream due to the unbalanced compensation paths. The center frequency of the sensor signal is around 10 kHz due to the tuning of the proof mass. The spectrum of the bitstream has the main frequency of around 80 kHz as well as high order harmonics, because the quantizer performs the sampling in zero-order hold mode and thus the output is formatted to a series of square pulses. However, attenuation occurs on the harmonics because the bandwidth of the CI is limited. Therefore, the slew rate of the disturbance cannot be infinite high. High frequency components of the disturbance due to the slope of edges are detected by the differential structure compensation controller. This distinguishes in principle from the demodulation structure, in which the disturbance is processed in the baseband.

4.3.1 Principle

The illustration of the compensation controller with differential structure is shown in Figure 4.19. Two differentiation paths are built as the inputs of the controller. The output of CI is processed in one path and thus the edge of the disturbance is detected. Due to the high slew rate of the bitstream, an additional is necessary in order to avoid the saturation at the following blocks. The bitstream is processed exactly the same way in another path and then two paths are multiplied. Since the disturbance is temporally correlated with the bitstream, the multiplication keeps the differential edge of the disturbance and results the strong attenuation in rest of time interval. The multiplication result is averaged by the LPF as the magnitude of the compensation.

Consider the case of an ideal differentiator applied in the controller. The open loop transfer function of the controller can be derived in the similar way as for the demodulation structure from the conceptual schematic shown in Figure 4.20:

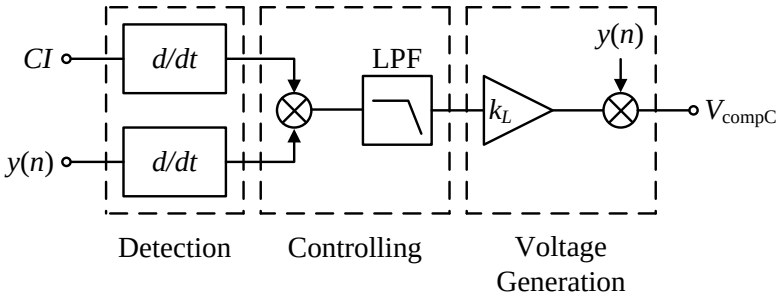


Figure 4.19: A block diagram of the differential-type compensation controller. Functional stages of detection, controlling and voltage generation are marked out.

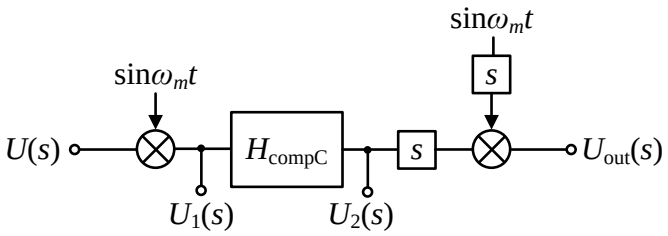
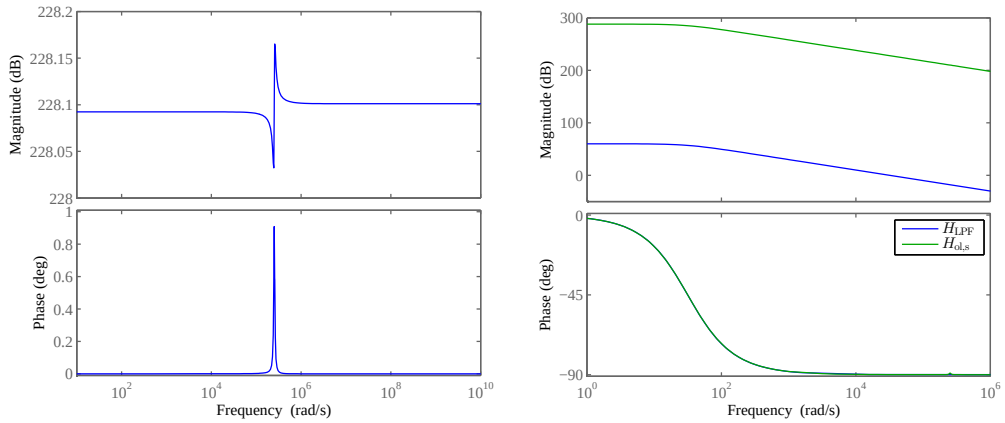


Figure 4.20: A conceptual schematic of the modulated transfer function in the differential structure for the capacitive compensation.

$$
\begin{aligned}
u_{\text{out}}(t) &\cong \frac{d}{dt}u_2(t) \cdot \frac{d}{dt}\sin\omega_m t \;\Rightarrow \\
U_{\text{out}}(s) &\cong sU_2(s) * s\frac{\delta(s-j\omega_m)-\delta(s+j\omega_m)}{2j} \\
&= sU_2(s) * \frac{j\omega_m\delta(s-j\omega_m)+j\omega_m\delta(s+j\omega_m)}{2j} \\
&= \frac{1}{2j}\cdot\frac{j\omega_m}{2j}\cdot[(s-j\omega_m)U(s-2j\omega_m)H_{\text{compC}}(s-j\omega_m) \\
&\quad -(s-j\omega_m)U(s)H_{\text{compC}}(s-j\omega_m) \\
&\quad -(s+j\omega_m)U(s+2j\omega_m)H_{\text{compC}}(s+j\omega_m) \\
&\quad +(s+j\omega_m)U(s)H_{\text{compC}}(s+j\omega_m)] \\
&\approx \frac{1}{2j}\cdot\frac{j\omega_m}{2j}\cdot[-(s-j\omega_m)U(s)H_{\text{compC}}(s-j\omega_m)+(s+j\omega_m)U(s)H_{\text{compC}}(s+j\omega_m)] \\
&= \omega_m U(s)\cdot\frac{-(s-j\omega_m)H_{\text{compC}}(s-j\omega_m)+(s+j\omega_m)H_{\text{compC}}(s+j\omega_m)}{4j}
\end{aligned}
\tag{4.16}
$$



(a) (b)

Figure 4.21: A bode plot of the modulated transfer function with the ideal differentiator $H_{\mathrm{modC,s}}(s)$ (a) and the corresponding open loop transfer function $H_{\mathrm{modC,s}}(s)$ (b).

Here, higher frequency terms $U(s-2j\omega_m)$ and $U(s+2j\omega_m)$ are neglected due to the low corner frequency f_c of the LPF. The expression of the output voltage now can be written in the form of

$$\begin{aligned} U_{\mathrm{out}}(s) &= U(s)\cdot\left[-\omega_m\frac{sH_{\mathrm{compC}}(s)}{2} * \frac{\delta(s-j\omega_m)-\delta(s+j\omega_m)}{2j}\right] \\ &\Rightarrow u(t) * \left(-\frac{\omega_m}{2}\right)\left[\frac{d}{dt}H_{\mathrm{compC}}(t)\cdot \sin\omega_m t\right] \cong u(t) * H_{\mathrm{modC,s}}(t) \end{aligned} \tag{4.17}$$

Equation 4.17 can be also written as

$$U_{\mathrm{out}}(s) \cong U(s)\, H_{\mathrm{modC,s}}(s) \tag{4.18}$$

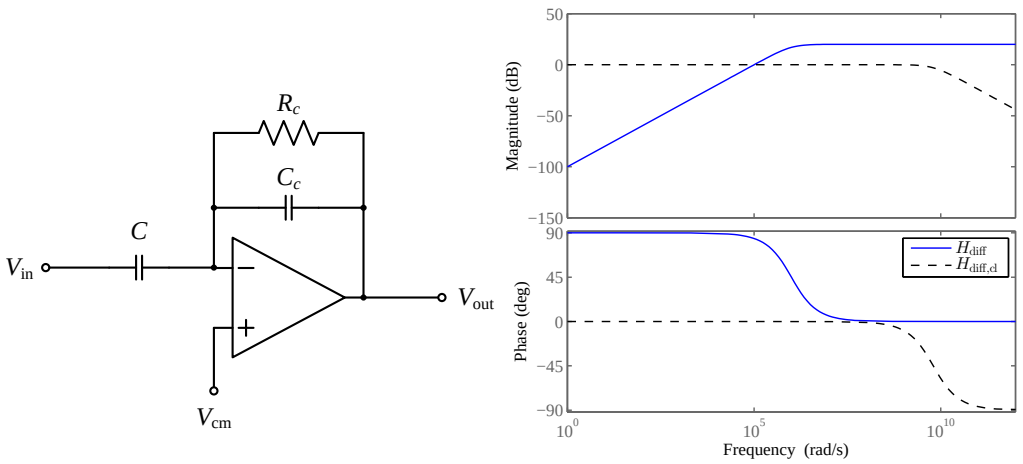
where

$$H_{\mathrm{modC,s}}(s) = j\omega_m \frac{(s-j\omega_m)\, H_{\mathrm{compC}}(s-j\omega_m) - (s+j\omega_m)\, H_{\mathrm{compC}}(s+j\omega_m)}{4} \tag{4.19}$$

as the modulated transfer function in the differential structure controller. The open loop transfer function $H_{\mathrm{ol,s}}$ is written as

$$H_{\mathrm{ol,s}}(s) = H_{\mathrm{LPF}}(s)\, H_{\mathrm{modC,s}}(s) \tag{4.20}$$

The transfer characteristics of $H_{\mathrm{modC,s}}(s)$ and $H_{\mathrm{ol,s}}(s)$ are depicted in Figure 4.21. Similar to $H_{\mathrm{modC,dem}}(s)$, the magnitude and phase of $H_{\mathrm{modC,s}}(s)$ can also be approximated to a constant. Thus, $H_{\mathrm{ol,diff}}(s)$ can be approximated to 1^{st}-order behavior



(a) (b)

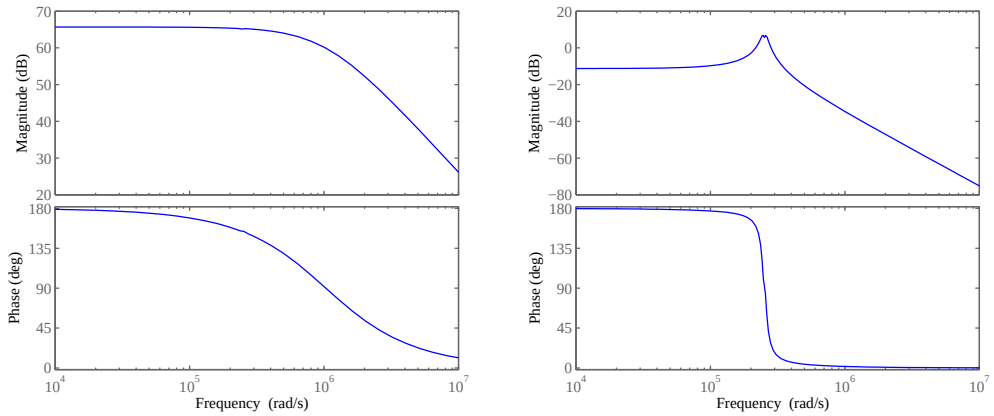
Figure 4.22: A schematic of the practical active differentiator (a) and its frequency response (b). The parameters are set as $R_c = 1\,\mathrm{M\Omega}$, $C = 10 \times 10^2\,\mathrm{pF}$, $C_c = 1\,\mathrm{pF}$.

and the controller is guaranteed stable in the closed loop configuration.

Consider a typical active differentiation stage as depicted in Figure 4.22, which is expressed by

$$H_{\mathrm{diff}}(s) = \frac{sR_cC}{sR_cC_c + 1} H_{\mathrm{diff,cl}}(s) \tag{4.21}$$

with $H_{\mathrm{diff,cl}}(s)$ the closed loop transfer function of the opamp in the differential stage. The practical differentiator introduces two additional poles. One is located at the corner frequency $f_{c,\mathrm{diff}} = 1/R_cC_c$ due to the RC network. When $\omega < 1/R_cC_c$, $H_{\mathrm{diff}}(s)$ can be considered as an ideal differentiator; When $\omega > 1/R_cC_c$, $H_{\mathrm{diff}}(s)$ can be considered as constant with the magnitude of C/C_c. Here, $C/C_c = 10^2$. R_c is necessary for stabilizing the bias voltage of the opamp. Higher $f_{c,\mathrm{diff}}$ causes the characteristic of $H_{\mathrm{diff}}(s)$ closer to an ideal differentiator in the base band of the input signal. The location of another pole is determined by $H_{\mathrm{diff,cl}}$ due to the limited bandwidth of opamp. Normally this corner frequency is much larger than the intrinsic pole of the opamp due to the feedback network. The corner frequency of the closed loop configuration $f_{c,\mathrm{cl}} = f_{c,\mathrm{ol}}(1 + A_L)$, where $f_{c,OL}$ is the corner frequency in the open loop condition and A_L is the loop gain. Thus, this pole is neglected in order to simplify the analysis. Similar to the case of ideal differentiator mentioned above, $U_{\mathrm{out}}(s)$ is derived as



(a) (b)

Figure 4.23: A Bode plot of the modulated transfer function $H_{\text{modC,diff}}$ in the case of $f_{c,\text{diff}} = 10\,\text{kHz}$ (a) and $f_{c,\text{diff}} = 100\,\text{Hz}$ (b).

$$\begin{aligned} U_{\text{out}}(s) &= H_{\text{diff}}(s)\, U_2(s) * H_{\text{diff}}(s)\, \frac{\delta(s - j\omega_m) - \delta(s + j\omega_m)}{2j} \\ &\approx H_{\text{diff}}(s)\, U_2(s) * H_{\text{diff}}(j\omega_m)\, \frac{\delta(s - j\omega_m) - \delta(s + j\omega_m)}{2j} \\ &= U(s) \cdot \left[H_{\text{diff}}(j\omega_m)\, \frac{H_{\text{diff}}(s)\, H_{\text{compC}}(s)}{2} \right. \\ &\quad \left. * \frac{\delta(s - j\omega_m) - \delta(s + j\omega_m)}{2j} \right] \\ &\cong U(s)\, H_{\text{modC,diff}}(s) \end{aligned} \tag{4.22}$$

Since $\omega_m > f_{c,\text{diff}}$, we have the approximation of $H_{\text{diff}}(j\omega_m) \approx C/C_c$. $H_{\text{modC,diff}}(s)$ refers to the modulated transfer function similar to the case of demodulation structure. The open loop transfer function is accordingly written as

$$H_{\text{ol,diff}} = H_{\text{modC,diff}}(s)\, H_{\text{LPF}}(s) \tag{4.23}$$

The bode plot of the modulated transfer function is depicted in Figure 4.23. $|H_{\text{modC,diff}}(s)|$ is approximately constant when $\omega < \omega_m$ and decreases by $40\,\text{dB/dec}$ when $\omega > \omega_m$. As $f_{c,\text{diff}}$ decreases, $|H_{\text{modC,diff}}(s)|$ shows an overshoot at ω_m and the overshoot increases as $f_{c,\text{diff}}$ becomes smaller. The phase decreases by $-90\,°/\text{dec}$ at ω_m. Hence, $H_{\text{modC,diff}}(s)$ behaves like a 2^{nd}-order LPF. Thus, an additional phase shift of 180° appears in $H_{\text{ol,diff}}(s)$ and thus might cause instability in the closed loop configuration. Therefore, the DC gain of $H_{\text{ol,diff}}(s)$ must be set properly in order to guarantee enough phase margin. With the parameter settings of $R_c = 1\,\text{M}\Omega$, $C = 1 \times 10^2\,\text{pF}$, $C_c = 1\,\text{pF}$, $k_L = 10$ and $f_c = 0.5\,\text{Hz}$, the phase margin of $H_{\text{ol,diff}}(s)$ reaches 83.4°.

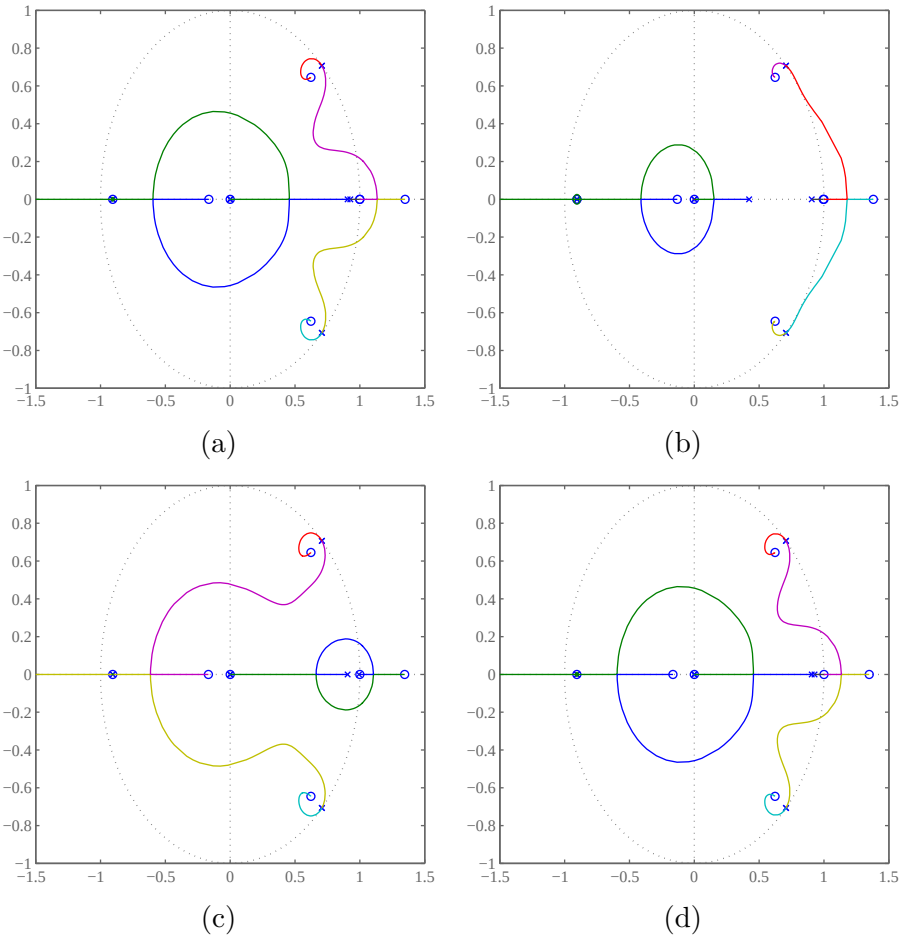


Figure 4.24: A root locus plot for the ΔΣ-modulator loop with the compensation controller in the case of $f_c = 5\,\text{Hz}$ with $k_L = 10$ (a) and $k_L = 100$ (b) as well as in the case of $f_c = 0.5\,\text{Hz}$ with $k_L = 10$ (c) and $k_L = 100$ (d).

4.3.2 Stability of the ΔΣ-modulator with the control loop

Similar to the demodulation structure, the compensation controller of the differential structure affects the stability of the ΔΣ-modulator. Figure 4.24 illustrates the root locus of the ΔΣ-modulator loop transfer function with $H_{\Delta\Sigma,\text{err,diff}}(z)$ with the expression

$$H_{\Delta\Sigma,\text{err,diff}}(z) = k_{\Delta\Sigma} k_q H_{\text{sen}}(z) H_{\text{sig}}(z) H_{\text{err,diff}}(z) H_{\text{LF}}(z) \tag{4.24}$$

Figure 4.24a shows the case of $k_L = 10$ and $f_c = 5\,\text{Hz}$. The system becomes unstable if k_L increases to 100 since the root locus exceed the unity circle as shown in Figure 4.24b. In the case of $f_c = 0.5\,\text{Hz}$, the system stays stable when $k_L = 10$ and $k_L = 100$ as shown in Figure 4.24c and Figure 4.24d. In conclusion, when f_c is fixed, the ΔΣ-modulator is closer to the instability as k_L increases; when k_L is fixed, a low value of f_c can dramatically decreases the chance of instability.

4.3.3 Ringing on the disturbance

The ringing effect on $H_{\text{err,diff}}$ can also be observed as k_L changes when f_c and $f_{c,\text{diff}}$ are fixed. Regarding to the pole zero map, $H_{\text{err,diff}}$ introduces two pairs of conjugated pole, two pairs of conjugated zero, one real pole and one real zero as listed in Table 4.2. Figure 4.25 illustrates the movement of poles and zeros as well as the corresponding plots of the step response. When k_L is low ($k_L = 1$), both pole pairs are very close to the corresponding zero pairs and thus they approximately cancel each other with only one pole and zero left, similar to PT1 behavior. One of the pole pairs moves away as k_L increases and reaches the real axis ($k_L = 10$), at which the pole pair splits into two independent poles P_1 and P_2. P_1 moves towards the negative direction along the real axis, while P_2 moves in the opposite direction until it meets P_3 and forms a new conjugated pair. This new pole pair is located much closer to the imaginary axis. In this case, the ringing suffers less damping and thus the magnitude of ringing becomes larger.

Table 4.2: The poles and zeros of $H_{\text{err,diff}}$ when $k_L = 10^0$ and $f_c = 0.5\,\text{Hz}$.

Pole	Zero
$-9.969 \times 10^5 \pm 2.397e \times 10^5 i$	$-1.000 \times 10^6 \pm 2.521e \times 10^5 i$
$-8.003 \times 10^3 \pm 2.521e \times 10^5 i$	$-8.000 \times 10^3 \pm 2.521e \times 10^5 i$
-6.111×10^3	-3.142

Figure 4.26 shows the IBN by sweeping k_L in the case of $f_c = 5\,\text{Hz}$ and $f_c = 0.5\,\text{Hz}$. The IBN achieves the minimum value when k_L is in the range of $10^0 \sim 10^1$. One can discover that the results don't distinguish much between two setting s of f_c, which means that the design requirement of the LPF can be relaxed. Similar to the case of the demodulation structure, the curve can be separated in two zones and a minimum value is achievable. For $f_c = 5\,\text{Hz}$, the minimum IBN is around -116 dBFS when $k_L = 0.3$; For $f_c = 0.5\,\text{Hz}$, the minimum IBN is around -112 dBFS when k_L.

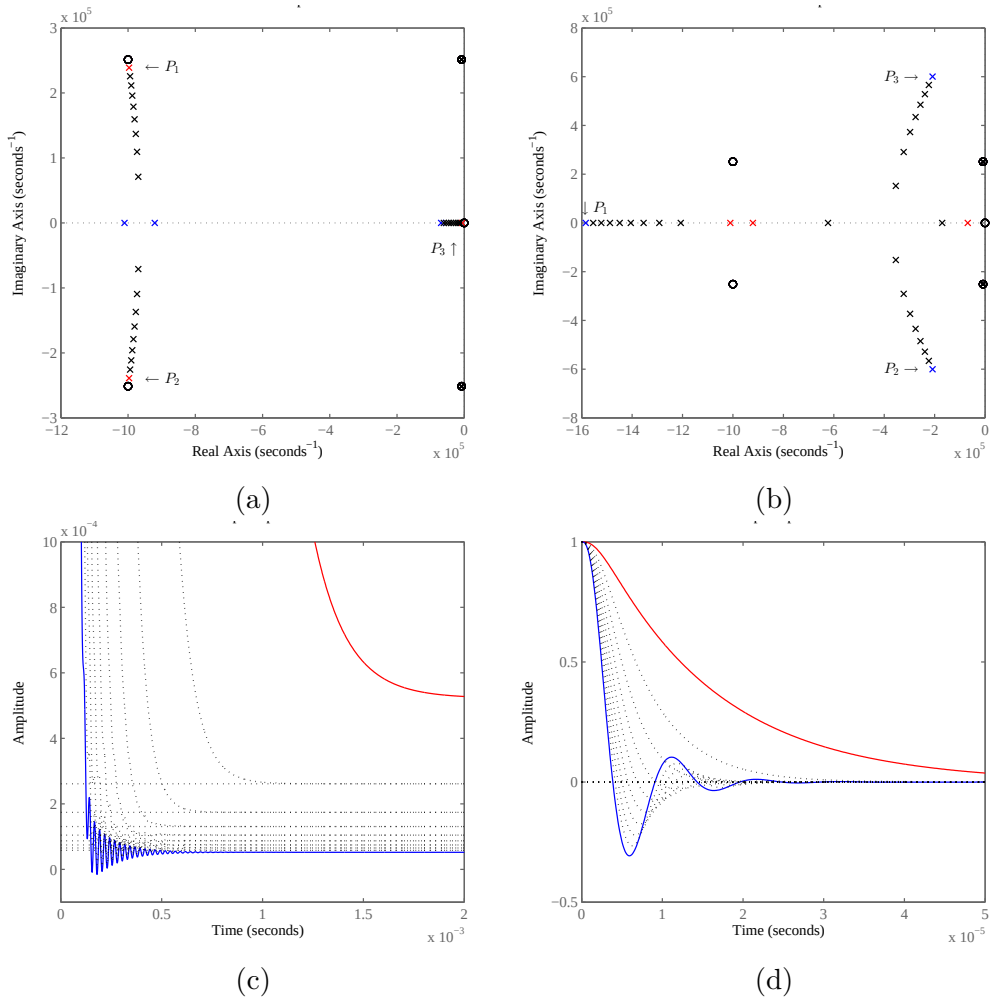


Figure 4.25: The analysis of transient characteristics of the control loop by the illustration of pole zero map and step response of $H_{\text{err,diff}}$. The position of the poles "x" and the zeros "o" are marked. Only poles and zeros above the real axis are visible because of the symmetry of conjugation. Plots of the movement of the pole are depicted in the case of $k_L = 10^0 \sim 10^1$ (a) and $k_L = 10^1 \sim 10^2$ (b). The initial pole is colored in red and ends at the blue one. The step response in the case of $k_L = 10^0 \sim 10^1$ (c) and $k_L = 10^1 \sim 10^2$ (d) are depicted. The curve changes from the red one to the blue one accordingly. All simulations are performed with $f_c = 0.5\,\text{Hz}$.

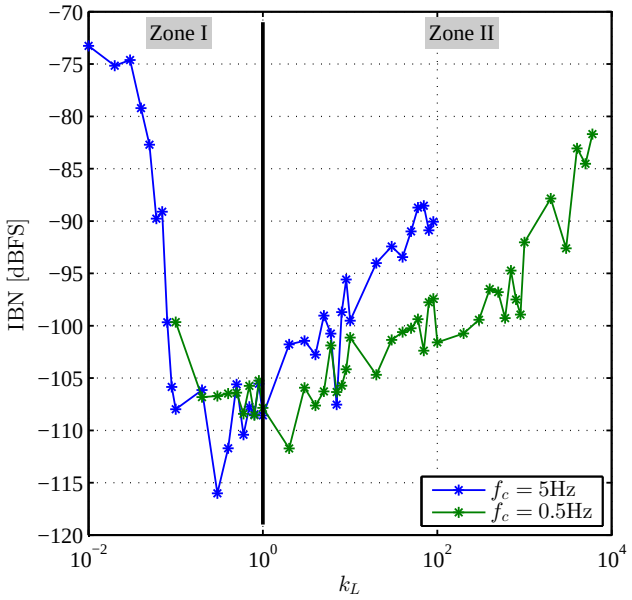
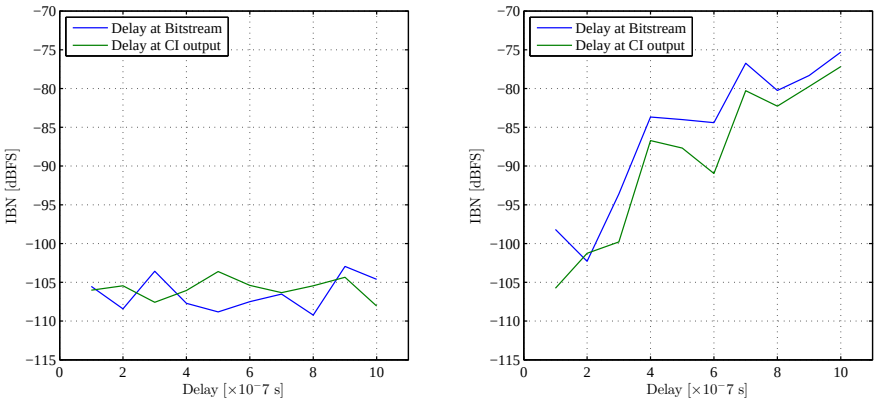


Figure 4.26: A plot of the IBN with k_L sweeping from 10^{-1} to 10^3 when $f_c = 0.5\,\text{Hz}$ and 10^{-2} to 10^1 when $f_c = 5\,\text{Hz}$.

4.3.4 Transmission delays in the compensation network

One factor, which is specialized in the differential structure and might deteriorate the performance, is that the two differentiation paths must be temporally synchronized in order to align the flipping edges between the output of CI and the bitstream. One can expect a symmetric layout of the differentiation stage in the transistor level design. However, the group delay of the differential channels might not be equal because the channel length to the readout system must also be considered. In the simulation, the pulse width generated by the differentiator is about 1 µs. Hence, the delay unit is set as 0.1 µs and thus the overlap of pulse from these two differentiators is changing. When the overlap decreases as the delay in one path occurs, the equivalent loop gain of the controller decreases and thus the IBN changes as in Figure 4.26. As long as the k_L is set aroung the value achieving the minimum IBN, the deviation of IBN along with k_L is also the smallest. Figure 4.27 depicts the variance of IBN based on the delay at either the CI output or the bitstream as the input of the controller. One can notice that in the case of $k_L = 1$ the simulation result shows stabler IBN deviation than that of $k_L = 0.1$.

In the case of delay at the bitstream for the modulation block, spikes on the CI output occur as described in subsection 4.2.4, because the feedback and compensation signals are not aligned. Nevertheless, the difference among channels can be controlled under a few nano-seconds. Therefore it is less critical on the temporal alignment among feedback and compensation paths in the common situation.



(a) (b)

Figure 4.27: A plot of IBN based on the differentiation channels: delay in the CI output and the bitstream path in the case of $k_L = 1$ (a) and $k_L = 0.1$ (b). $f_c = 5\,\text{Hz}$ for both cases.

4.4 Integrate-Dump

The previous two implementations for the compensation controller are totally analog. The advantages of an analog structure are the high accuracy and speed, simple circuit realization as long as the system is stable. Nevertheless, the sensor signal in the $\Delta\Sigma$-modulator is inevitably processed together with the disturbance by the controller and couples back to the readout loop, which might violate the loop function and even causes instability of the $\Delta\Sigma$-modulator. Besides, a good compensation requires high DC gain and ultra-low corner frequency of the LPF in the controller, which is only possible to be implemented by advanced technologies such as gm-C LPF. The integrate-dump strategy features on its dual-value detection and the discrete compensation voltage. The combination of analog and digital functional blocks enhances the compatibility and robust of the compensation controller. In addition, a digital value is easy to be stored and loaded at each startup of the $\Delta\Sigma$-modulator. It is unnecessary to activate the control loop as long as the balanced compensation voltage is achieved. Nevertheless, an additional DAC is required to generator the compensation voltage.

4.4.1 Principle

The illustration of compensation controller with integrate-dump structure is shown in Figure 4.28. The integrate-dump structure consists of an integrator, a window comparator and an up/down digital counter, which means that it is a mixed-signal system. The integrator includes a reset access, which is used for dumping the integration result by the window comparator if the upper or lower threshold is reached. The functional procedure is illustrated in Figure 4.29. Firstly the output of the CI

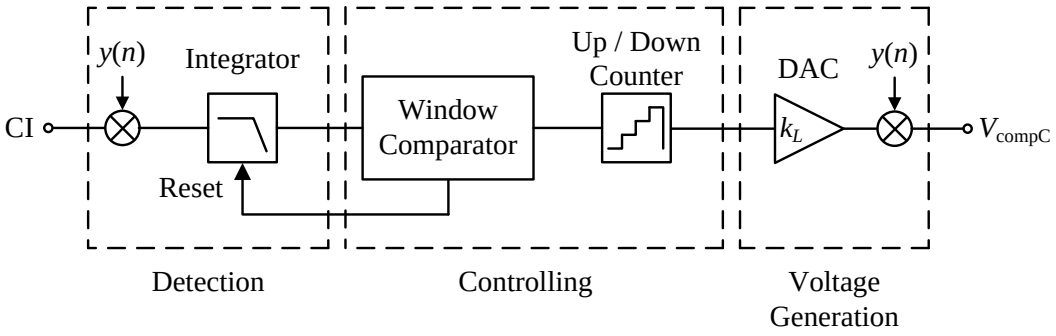


Figure 4.28: A block diagram of the integrate-dump compensation controller. Functional stages of detection, controlling and voltage generation are highlighted.

is demodulated by the bitstream. Hence, the DC and high-frequency components are separated. The integrator accumulates the DC component while high-frequency components are suppressed. In the window comparator block, two thresholds are predefined which respectively define the upper and lower boundary of the integration voltage. Here, the upper and lower boundary have the same potential difference to V_{cm}. As long as the integration result reaches either threshold, a trigger signal will be transmitted to the counter and thus the number stored in the counter is updated. This number represents the amplitude of the compensation voltage. When the voltage exceeds the upper boundary, a positive trigger signal is transmitted which makes the counter step up by one unit. On the contrary, when the integrated voltage exceeds the lower boundary, a negative trigger signal is transmitted which makes the counter step down by one unit. The number stored in the counter is converted to the analog compensation voltage by the scale factor k_L, which is implemented by a DAC, and then modulated on the bitstream in order to generate the compensation signal. As long as the counter changes its value, a reset signal is transmitted to the integrator and thus the integration result returns to zero. A new integration cycle starts.

4.4.2 Settling time and resolution

The speed of compensation by the integrate-dump structure is determined by several factors. The necessary time required for the balanced compensation is calculated by the steps as shown below.

Step 1: the demodulated input signal.

$$\begin{aligned} V_{\mathrm{dem}}(t) &= V_e(\cos\omega_e t\ ) \times V_m \cos(\omega_m t) \\ &= \frac{1}{2} V_e V_m \left[\cos(\omega_e + \omega_m)\, t\ + \cos(\omega_e - \omega_m)\, t\ \right] \cong V_1 \end{aligned} \tag{4.25}$$

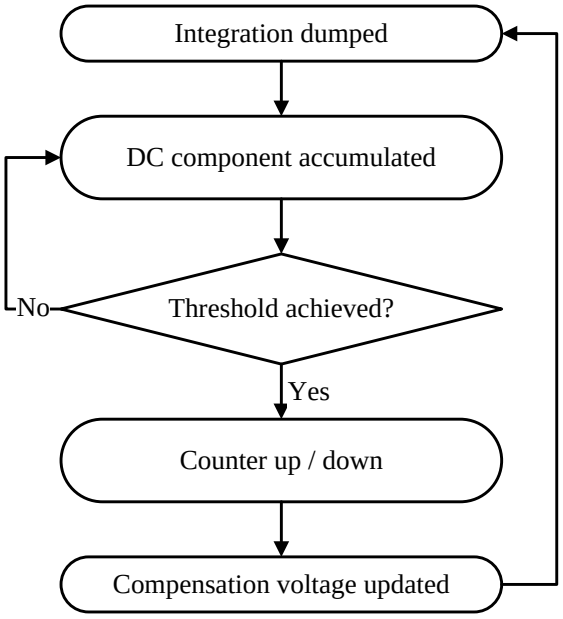


Figure 4.29: A flow chart describing the functional procedure of the integrate-dump compensation controller.

assuming that the input signal and demodulation signal both have cosinuous form. V_e and ω_e are the magnitude and frequency of the input signal. V_m and ω_m are the magnitude and frequency of the demodulation signal. In order to simplify the calculation in the following steps, the demodulated signal $V_{\text{dem}}(t)$ is approximated to a constant voltage V_1.

Step 2: the output signal $V_2(t)$ of the integrator $h_{int}(t)$.

$$V_2(t) = V_1 \cdot h_{\text{int}}(t) = AV_1\left(1 - e^{-\frac{t}{\tau}}\right) \tag{4.26}$$

with A and τ the gain and time constant of the integrator.

Step 3: the integration cycle ends when the voltage reaches the threshold.

$$t_T = -\tau \ln\left(1 - \frac{V_2}{AV_1}\right)\Big|_{V_2=V_{\text{th}}} = -\tau \ln\left(1 - \frac{V_{\text{th}}}{AV_1}\right) \tag{4.27}$$

with V_{th} the threshold voltage and t_T the cycle period. V_{th} has the same polarity as V_1.

Step 4: the sum of integration cycles to achieve balanced compensation.

$$\sum_{n=1}^{N} t_{T,n} = \sum_{n=1}^{N}\left[-\tau \ln\left(1 - \frac{V_{\text{th}}}{AV_{1,n}}\right)\right] \tag{4.28}$$

with $V_{1,n}$ and $t_{T,n}$ the demodulation voltage and cycle period at the n^{th} integration cycle, N the necessary cycles to achieve the balance. The sum is called the settling time. Larger amount of unbalance causes longer time of compensation. Since $V_{1,n}$ is changing during the compensation process, $t_{T,n}$ is also not constant. $V_{1,n}$ depends on the real-time disturbance and decreases as the compensation proceeds. Therefore $t_{T,n}$ becomes larger as n steps up and thus $|V_{\text{compC}}|$ increases slower accordingly. This phenomenon shows analogically PT1 behavior.

Since the accumulation of V_{compC} is linear, the cycle number N is calculated from the balancing compensation voltage $V_{\text{compC,0}}$ and the resolution, which is represented by the scale factor k_L:

$$N = \frac{V_{\text{compC,0}}}{k_L} = \frac{k_{C,0}\Delta V_{\text{fb}}}{k_L} \tag{4.29}$$

with $k_{C,0}$ the corresponding amplification factor of the compensation. From Equation 3.5 we have $k_{C,0} = 9.125$. Therefore a step size k_L, of which $k_{C,0}$ is the integer multiple, can theoretically eliminate the disturbance and achieve the balance state. However, due to the limited accuracy and non-linearity of the DAC as well as the tolerance of electrical parameters, an exact integer multiple can never be achieved. Obviously, the maximum error of the stabilized compensation voltage to $V_{\text{compC,0}}$ equals to $2k_L$. In order to fulfill the requirement of practical compensation, the maximum of k_L is calculated as $k_{L,max} = 2\%\ V_{\text{compC,0}} = 21.9\,\text{mV}$. Therefore V_{compC} can be guaranteed in the range of $\pm 1\%\ V_{\text{compC,0}}$.

In the simulation, an ideal integrator with a gain of 5×10^3 is used in order to achieve a comparable settling time to analog implementations introduced before. Table 4.3 lists simulation results of the settling time and IBN with different settings of k_L. Larger k_L means larger step size of the compensation voltage in each integration cycle and thus shorter settling time. Nevertheless, larger step size results in higher error to the ideal value when the controller settles down. Suppose $V_{\text{err}} = V_{\text{compC,0}} - Nk_L > 0$. When $|V_{\text{err}}| < k_L$, the counter steps up by one and thus $V_{\text{compC,0}} - (N+1)\,k_L < 0$. In the next integration cycle, the counter steps down by one and this process repeats. This results in the ringing in the compensation voltage because the counter value doesn't converge as depicted in Figure 4.30a. In the table, $k_L = 5\,\text{mV}$ can exactly divide $V_{\text{compC,0}}$ and thus fulfills the condition of ideal compensation. With a slight change to $k_L = 6\,\text{mV}$, the IBN decreases significantly and more with lower resolution.

Table 4.4 lists simulation results of the settling time and IBN with different settings of the threshold. One can observe that the IBN increases when the threshold becomes smaller. The reason is that the period of integration cycle decreases as the threshold decreases. Thus, the frequency of changing the counter value becomes higher, which causes more ringings in V_{compC}.

Table 4.3: The simulation result of the ΔΣ-modulator with integrate-dump compensation controller with different k_L.

Threshold	k_L [mV]	Settling Time [ms]	IBN [dBFS]
-1, 1	5	50	-105
-1, 1	6	50	-92
-1, 1	10	25	-83
-1, 1	20	12	-77

Table 4.4: The simulation result of the ΔΣ-modulator with integrate-dump compensation controller with different thresholds.

Threshold	Settling Time [s]	k_L [mV]	IBN [dBFS]
-1, 1	10	25	-83
-0.5, 0.5	10	12	-81
-0.1, 0.1	10	5	-78

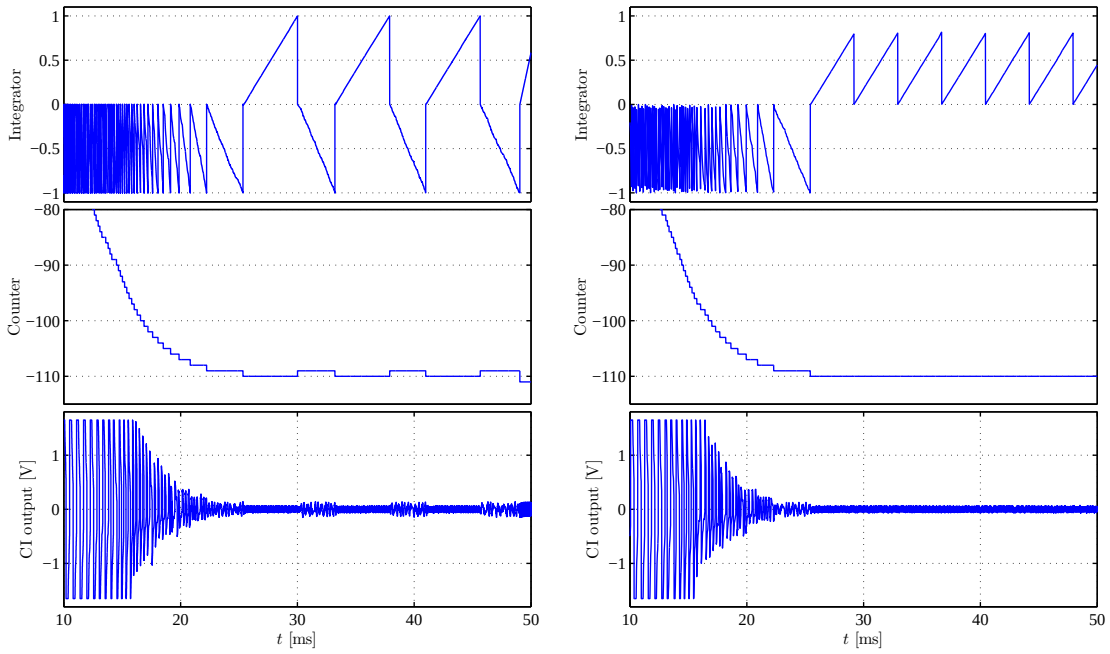


Figure 4.30: The waveform during the compensation process of the integrate-dump controller. (a) shows the changing counter value which causes the ringing on the CI output. With the watch-dog option the ringing is eliminated as shown in (b).

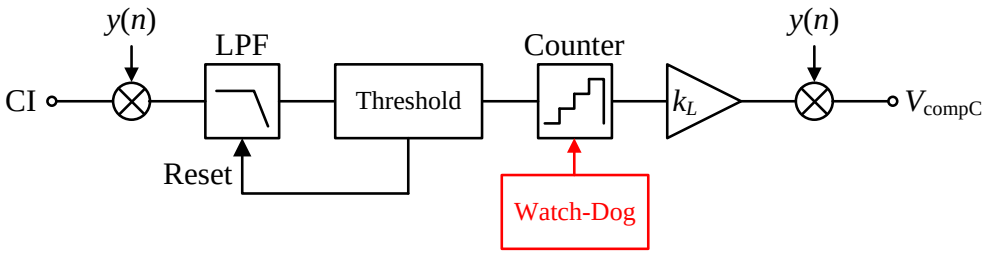


Figure 4.31: A block diagram of the integrate-dump compensation controller with the option of watch-dog.

4.4.3 Option: Watch-Dog

As described in subsection 4.4.2, the counter value as well as the compensation voltage will bounce around the balancing value, because it is impossible to achieve an integral N for an ideal compensation in real system. Besides, there is always non-zero output from the integrator because of the loop noise at the CI output. An improved IBN comes from the trade-off among several parameters of the controller, including the step size, loop gain, threshold and clock speed. A small step size may decrease the chance of rippling, but it requires more steps to complete the compensation process, which means high demand on the time to stability as well as the volume of counter. This causes huge challenge in the design of DAC.

Here, an option called watch-dog for the integrate-dump structure as depicted in Figure 4.31 is introduced for the improvement of the IBN. The name comes from its principle of limitation on the integration time. From Equation 4.28, the period of integration cycle increases when the disturbance decreases. During the compensation process, the period will exceed the limit and thus the counter is deactivated. This prevents V_{comp} to swing around the expected value after the expected magnitude of compensation is achieved. The average of the minimum error equals to $k_L H_{\text{compC}}/2$. Supposing $k_L = 10\,\text{mV}$, we have the result of $44\,\text{mV}$. From Equation 4.27, the corresponding integration cycle can be calculated, which determines the setting of watch-dog. Besides, the limitation can be represented as a count of T_s, which is straightforward for a digital block with clock. In this case, the limit can be set as $300T_s$ when the threshold of window comparator is (-1, 1). A smaller range of window causes shorter integration cycle and thus lower limit for the watch-dog. The compensation voltage will be closest to the ideal value by the best setting of the time limit. If the counter is deactivated too late, the ringing still exists. If the counter is deactivated too early, the residual error is large.

Table 4.5 and Table 4.6 list the simulation result of the settling time to the balancing state and the corresponding achieved IBN in the case of the watch-dog option

with different settings of k_L and threshold, respectively. In comparison to the original structure of integrate-dump controller, the watch-dog option offers significant improvement on the IBN and less dependence on k_L.

Table 4.5: The simulation result of the $\Delta\Sigma$-modulator with integrate-dump compensation controller with the watch-dog option by different k_L.

Threshold	k_L [mV]	Settling Time [ms]	IBN [dBFS]
-1, 1	6	50	-91
-1, 1	10	25	-105
-1, 1	20	12	-108
-1, 1	50	5	-105

Table 4.6: The simulation result of the $\Delta\Sigma$-modulator with integrate-dump compensation controller with the watch-dog option by different thresholds.

Threshold	k_L [mV]	Settling Time [ms]	IBN [dBFS]
-1, 1	10	25	-105
-0.5, 0.5	10	14	-112
-0.1, 0.1	10	4	-109

5 Verilog-A implementation

In the previous chapter, different implementations of the automatic compensation controller are simulated and analyzed regarding the performance and the stability in the system level. This simulation environment provides a relatively ideal parameter setting. Nevertheless, one must consider various kinds of additional factors in the real circuit, such as parasitic resistors and capacitors, dynamic range and bandwidth of devices, propagation delay and noise. By the consideration of these factors, it provides a more persuasive simulation result and thus a more realistic performance of the controller can be observed.

The circuit level simulation is implemented in Cadence® with the hardware description language Verilog-A. Verilog-A is an industry standard modeling language for analog circuits as the continuous-time subset of Verilog-AMS. A benefit of Verilog-A language is the creation of a circuit by the description of its behavior, especially in the cases of modules described in transfer functions. Cadence Virtuoso® supports the implementation of electrical or mechanical functional modules by Verilog-A. One of the most conveniences of this method is that the transfer function in Laplace form can be directly complied and simulated. It saves time for the implementation of the prototype from system level design.

Figure 5.1 illustrates the test bench of the electromechanical $\Delta\Sigma$-modulator in circuit level. The model "MD_423200" for the gyroscope is constructed in Verilog-A. Differential capacitors are built for driving the primary side as well as sensing on the secondary side, which matches the working mode of the real sensor. Thus, all functional blocks including the CI, the loop filter, the quantizer, voltage generator and compensation controller are implemented as fully differential circuits. This strategy is beneficial for the suppression on common-mode variations in the $\Delta\Sigma$-modulator loop. The CI is built in the transistor level based on a differential difference amplifier (DDA) and resistor-capacitor (RC) network for its feedback path as well as for the resistive and the capacitive compensation as shown previously in Figure 3.4a. This CI with configurable RC-network is originally utilized for manual compensation by setting the control bits. Here, the RC network is set as $R_{\mathrm{int}} = 1\,\mathrm{G\Omega}$, $C_{\mathrm{int}} = 125\,\mathrm{fF}$, $C_{\mathrm{comp}} = 900\,\mathrm{fF}$. The quantizer is realized by a rail-to-rail comparator with differential output. The feedback and the resistive compensation signal with the fixed amplitude come from the voltage generator block while the capacitive compensation signal is generated by the automatic controller realized in different implementations presented in the previous chapter. The transition time of the feedback and compensation path is set as 250 ns, similar to the transition time of the corresponding

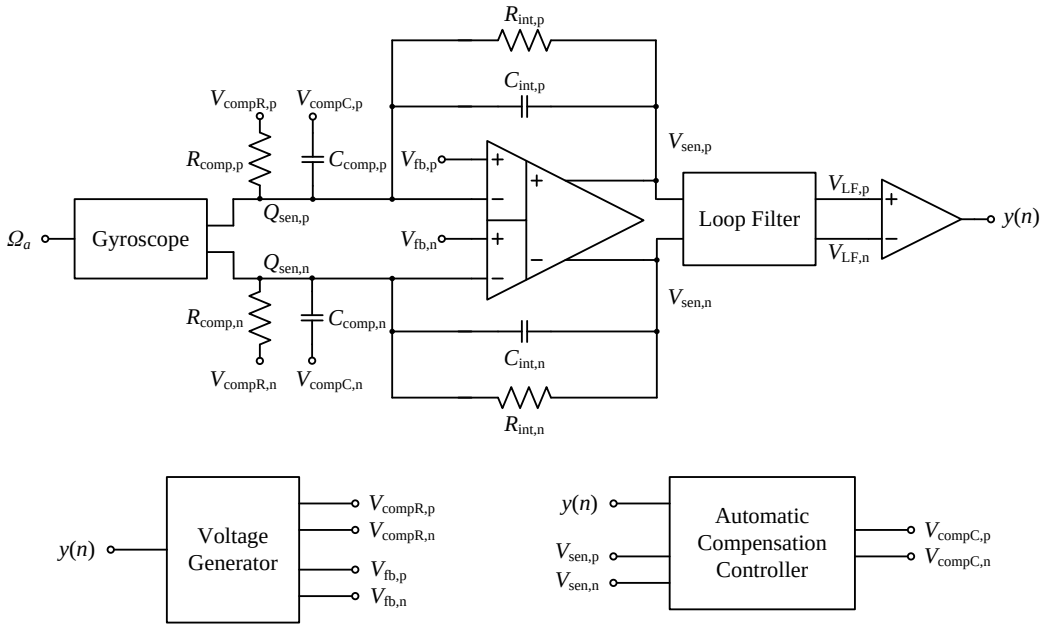


Figure 5.1: The schematic of the $\Delta\Sigma$-modulator with the automatic compensation controller in Cadence.

transistor-level implementations.

Each type of compensation controller consists of several blocks written in Verilog-A. The modulation and demodulation blocks and the LPF are particularly utilized among several of controller structure. The modulation and demodulation blocks are implemented by an analog multiplexer, which consists of two signal inputs, two signal outputs and one control port. The inputs are connected to the output pair of CI. A multiplexing between two differential signals is equivalent to multiplying either signal with a square wave with corresponding amplitude of (-1, 1). Besides, it is easier to implement a multiplexer than multiplier in the circuit. Options of internal resistance between signal ports and transition characteristics are integrated in order to achieve more realistic behavior. The LPF is implemented by either the transfer function expression or a fully differential amplifier. The intrinsic bandwidth of the amplifier might deteriorate the stability of the control loop. The integrate-dump controller, as a specialized type, consists of blocks which are mostly built digitally. Any unexpected spikes as well as unknown trace delay might cause fake actions in logical blocks. Therefore the system clock equal to f_s is implemented as the synchronization signal for the integrator, comparator and counter block. The transition characteristics including rise time, fall time and transmission delay at output ports of each block are also implemented for more realistic simulation.

Table 5.1: The simulation setup for the electromechanical ΔΣ-modulator with the automatic compensation controller in Cadence.

f_{drv} [Hz]	f_s [Hz]	Ω_a [°]	f_a [Hz]	V_{fb} [V]	V_{compR} [V]	V_{pol} [V]	Points
10^4	8×10^4	1	$f_s/4096$	0.12	0.24	7.5	2^{14}

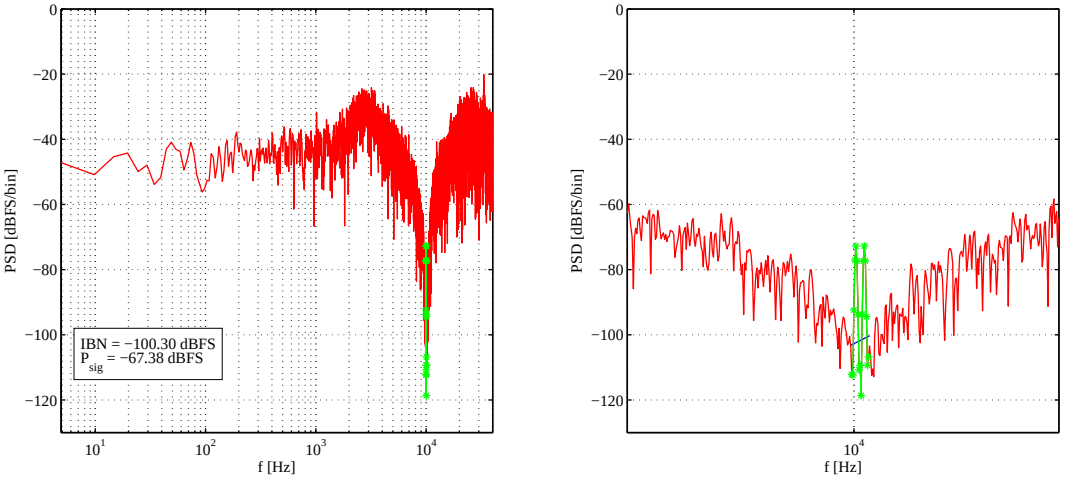
Table 5.1 summarizes the simulation setup for the test bench in Cadence. Ω_a and f_a are the amplitude and frequency of the angular rate signal, respectively. One can observe two peaks in the spectrum located symmetical to the center frequency f_{drv}. The quantity of sample points equals to 2^{14}, same as the setting in MATLAB. The bitstream is recorded after the balancing of CI is achieved. The settling time may change due to the loop gain of the controller. From Figure 5.2 to Figure 5.6 depict the simulated PSD of the ΔΣ-modulator with the compensation controller of each type mentioned in the previous chapter. In the case of demodulation type, the IBN is -100 dBFS for $k_L = 100$, $f_c = 0.5\,\mathrm{Hz}$ in Figure 5.2 and -98 dBFS for $k_L = 100$, $f_c = 5\,\mathrm{Hz}$ with the duty-cycle LPF option in Figure 5.3. In the case of differential type as shown in Figure 5.4, the IBN is -102 dBFS for $k_L = 100$ and $f_c = 0.5\,\mathrm{Hz}$. In the case of integrate-dump type, the IBN reaches -75 dBFS in Figure 5.5 and -109 dBFS with the watch-dog option in Figure 5.6, of which the time threshold is set as $10T_s$. It manifests considerable improvement on the SNR with this option. For both integrate-dump blocks $k_L = 5 \times 10^{-3}$. In comparison to the simulation result from MATLAB, the IBN results are larger because here it includes additional parasitic components from the transistor-level model of the CI. From Figure 5.7 to Figure 5.11depict the simulated PSD of the ΔΣ-modulator with the compensation controller involving electrical noise with the noise floor of -91 dBFS in Figure 5.7. In the case of demodulation type, the IBN is -94 dBFS for $k_L = 100$, $f_c = 0.5\,\mathrm{Hz}$ in Figure 5.8 and -97 dBFS for $k_L = 100$, $f_c = 5\,\mathrm{Hz}$ with the duty-cycle LPF option in Figure 5.9, respectively. In the case of differential type as shown in Figure 5.10, the IBN is -91 dBFS for $k_L = 100$ and $f_c = 0.5\,\mathrm{Hz}$. In the case of integrate-dump type, the IBN reaches -92 dBFS with the watch-dog option in Figure 5.11 with the time threshold set as before. One can discover that the difference in performance among these types of controllers has been mostly suppressed to the noise floor. Thus, the performance of the ΔΣ-modulator is not deteriorated by the controller. The settling time determines the speed of compensation process. Table 5.2 summarizes settling times of different types of controllers. Since the sensor system requires an intrinsic startup time of 44 ms[21], the time consumption by the compensation controller will not impact the total speed of the sensor system.

Till now, all implementations of the automatic compensation controller have been analyzed. They are able to achieve the required balancing condition, with the IBN less than the equivalent 1% deviation of V_{compC}. Considering the application in the future designs, the integrate-dump structure would be proposed. One reason is that it is capable of sharing the integrate-dump structure among several compensation

Table 5.2: The settling time of different types of compensation controller.

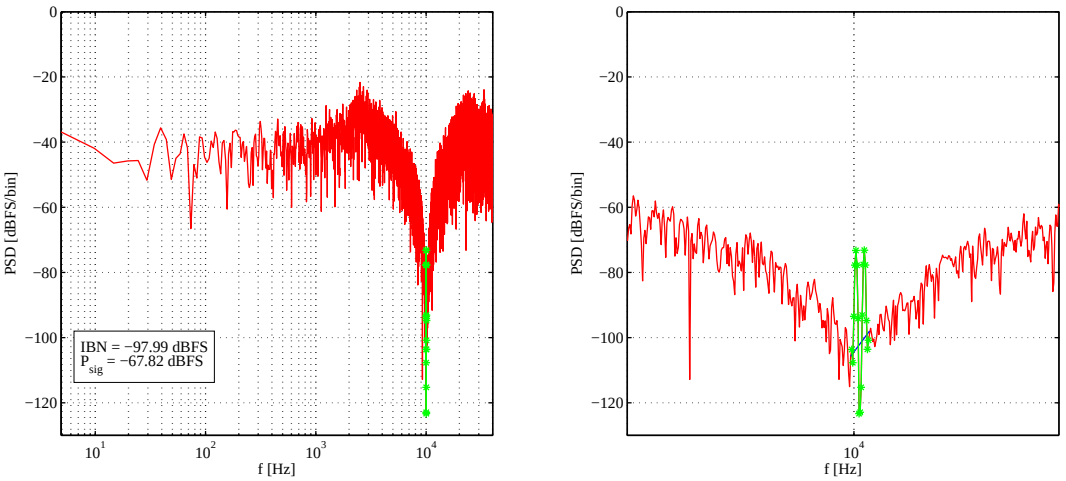
Type	Settling Time [ms]
Demodulation	6
Demodulation (duty-cycle LPF)	4
Differential	2
Integrate-Dump	50
Integrate-Dump (watch-dog)	50

paths as long as a memorizing element is equipped to each path. For example, a 3-axis gyroscope requires only one integrate-dump structure to generate the correct compensation voltage for one of the axis and store the value in the register for this axis. Then the integrate-dump module is connected to the other two axes and the process is the same. At the next startup, the initial compensation voltage can be directly converted from the value in the register for each axis. This strategy is highly beneficial for decreasing the time for compensation as well as saving the area on the chip.



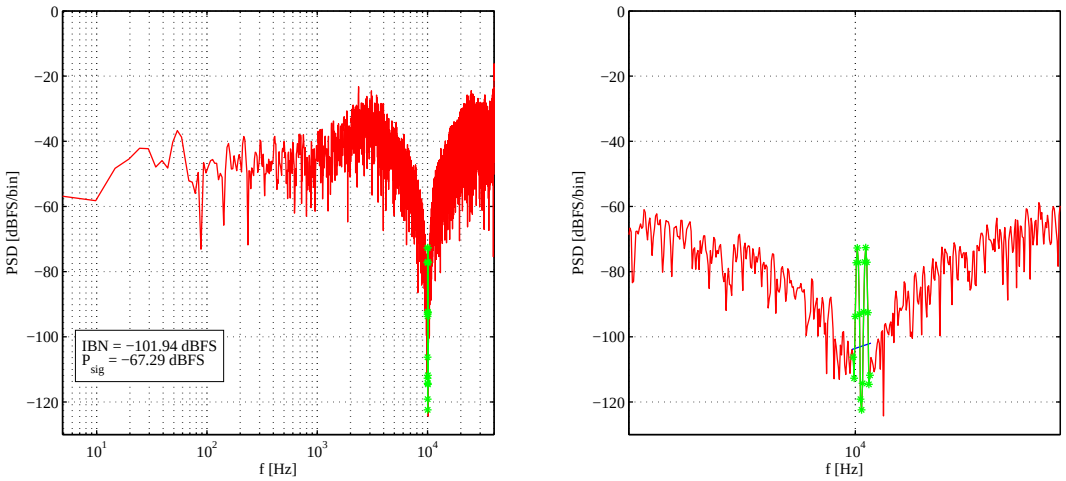
(a) (b)

Figure 5.2: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator with the demodulation type compensation controller with $k_L = 100$ and $f_c = 0.5\,\text{Hz}$. (b) is the detailed view of the NTF notch.



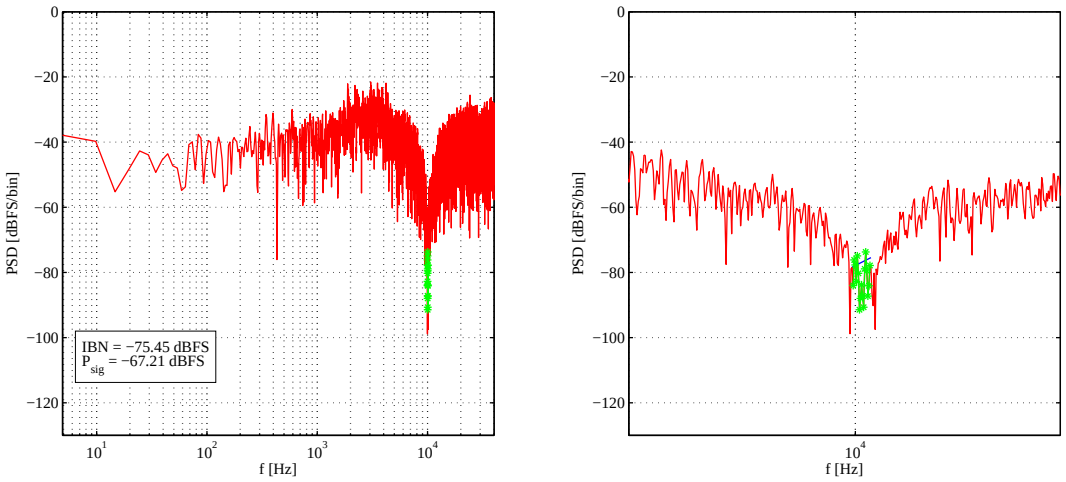
(a) (b)

Figure 5.3: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator with the demodulation type (duty-cycle LPF option) compensation controller with $k_L = 100$ and $f_c = 5\,\text{Hz}$. (b) is the detailed view of the NTF notch.



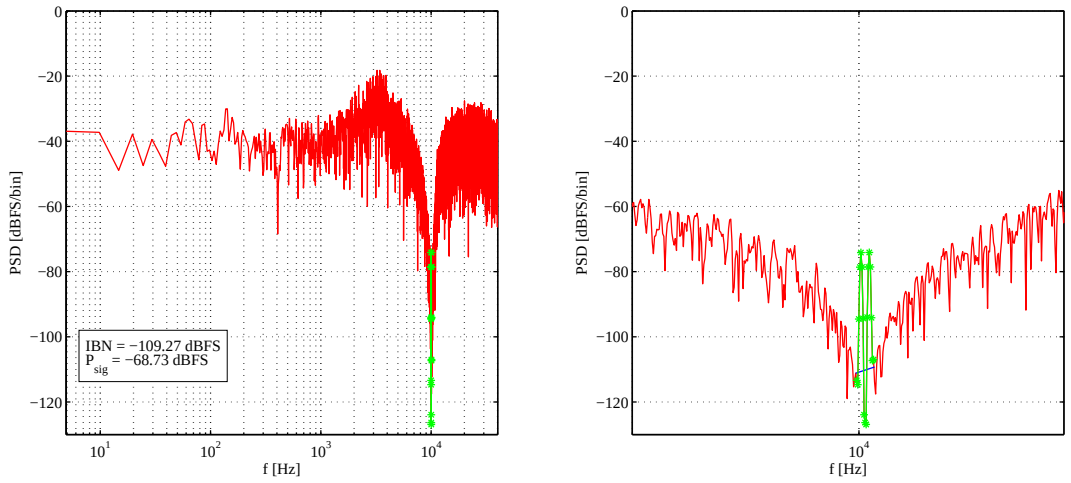
(a) (b)

Figure 5.4: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator with the differential type compensation controller with $k_L = 10^4$ and $f_c = 0.5\,\mathrm{Hz}$. (b) is the detailed view of the NTF notch.



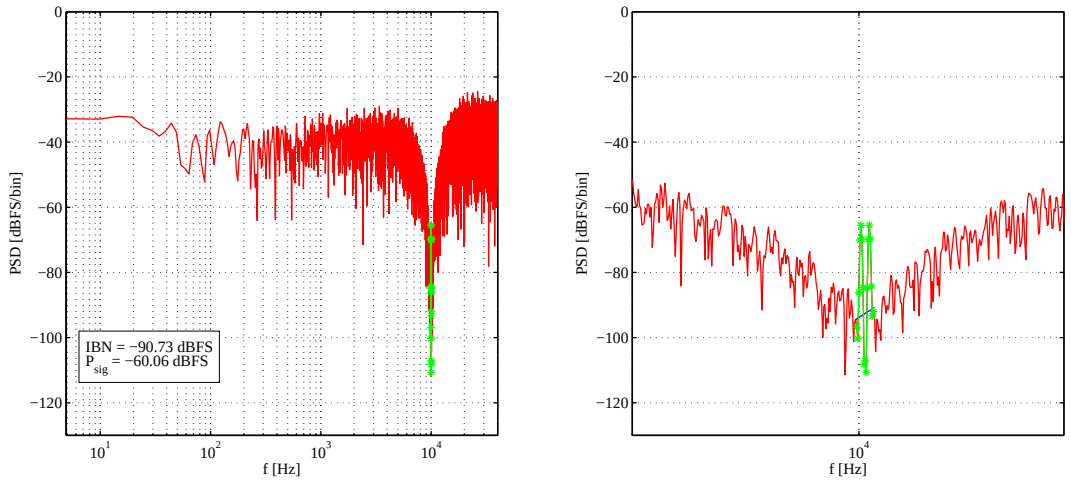
(a) (b)

Figure 5.5: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator with the integrate-dump type compensation controller with $k_L = 5\,\mathrm{mV}$. (b) is the detailed view of the NTF notch.



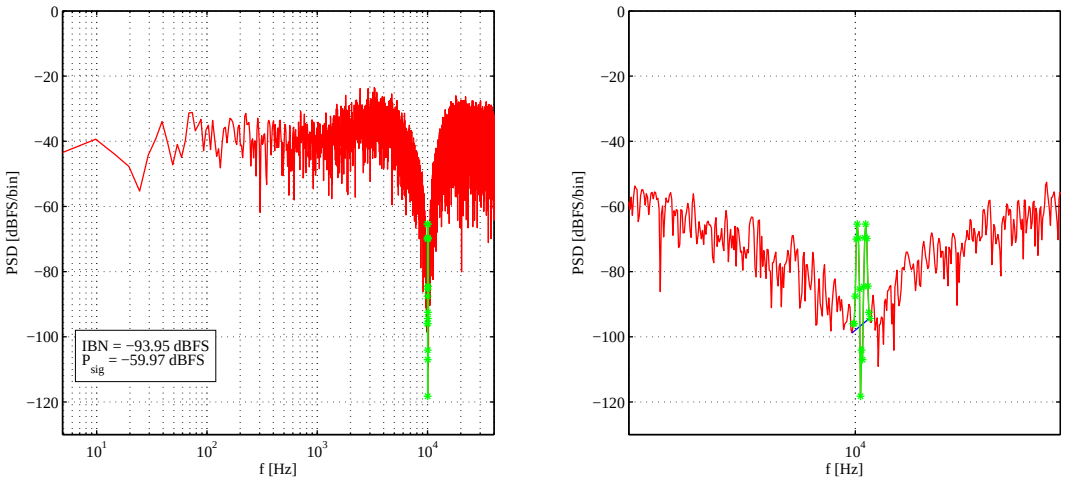
(a) (b)

Figure 5.6: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator with the integrate-dump type (watch-dog option) compensation controller with $k_L = 5\,\mathrm{mV}$ and time limit of $10T_s$. (b) is the detailed view of the NTF notch.



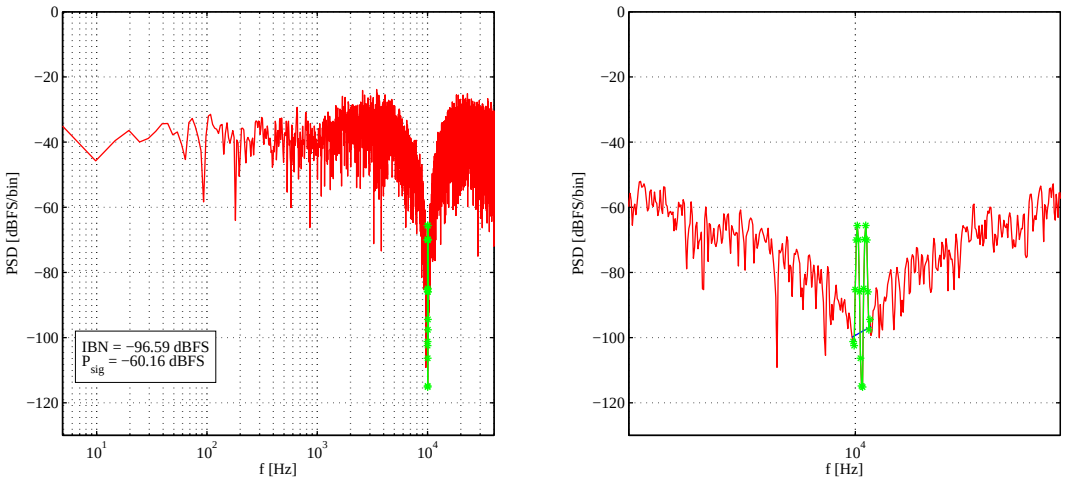
(a) (b)

Figure 5.7: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator involving noise without the compensation controller. (b) is the detailed view of the NTF notch.



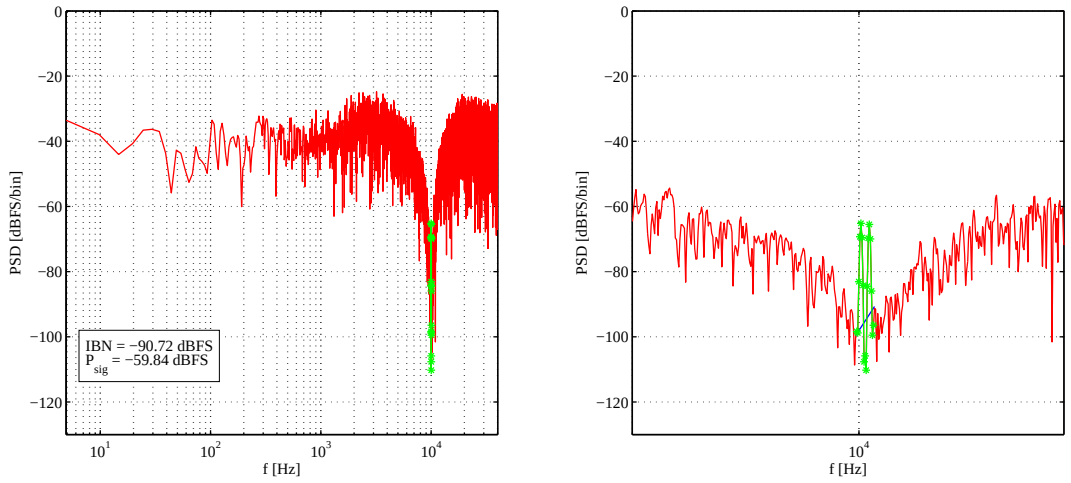
(a) (b)

Figure 5.8: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator involving noise with the demodulation type compensation controller with $k_L = 100$ and $f_c = 0.5\,\text{Hz}$. (b) is the detailed view of the NTF notch.



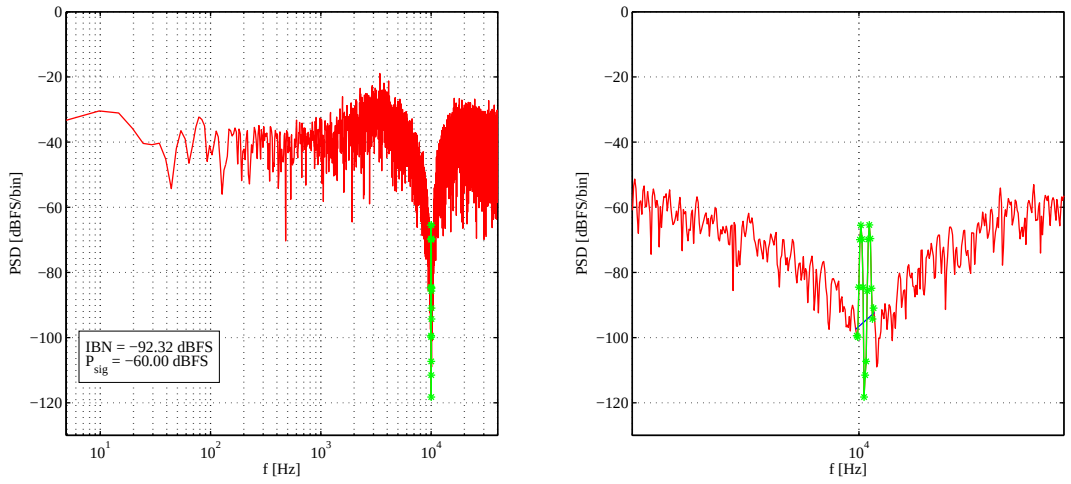
(a) (b)

Figure 5.9: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator involving noise with the demodulation type (duty-cycle LPF option) compensation controller with $k_L = 100$ and $f_c = 5\,\text{Hz}$. (b) is the detailed view of the NTF notch.



(a) (b)

Figure 5.10: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator involving noies with the differential type compensation controller with $k_L = 10^4$ and $f_c = 0.5\,\text{Hz}$. (b) is the detailed view of the NTF notch.



(a) (b)

Figure 5.11: (a) shows the simulated PSD of the $\Delta\Sigma$-modulator with the integrate-dump type (watch-dog option) compensation controller with $k_L = 5\,\text{mV}$ and time limit of $10T_s$. (b) is the detailed view of the NTF notch.

6 Conclusion and Outlook

In this research, a novel concept of an automatic compensation controller for the electromechanical $\Delta\Sigma$-modulator has been developed. The controller includes three stages: detection, controlling and voltage generation. Three implementations for the automatic compensation controller have been introduced. The demodulation and differential type are of the analog structure, while the integrate-dump type includes digital modules and thus belongs to the mixed-signal structure. The analog structure directly generates the compensation voltage, while the mixed-signal structure requires a DAC to convert the digital value referring to the magnitude of compensation. These controllers also distinguish on the frequency range of the disturbance detected. The DC component of imbalance is observed by the demodulation and integrate-dump controller, while high frequency components from transition characteristics are detected by the differential controller. For the integrate-dump controller, only the polarity of the DC component is considered.

In principle, the accuracy of the compensation mostly depends on the open loop gain of the controller. Here, the residual disturbance as the error of the control loop decreases when the loop gain increases. Nevertheless, the sensor signal in the $\Delta\Sigma$-modulator is inevitably processed by the controller and thus the loop transfer function of the $\Delta\Sigma$-modulator changes. One can notice that a high loop gain may cause the instability of the $\Delta\Sigma$-modulator, which can be illustrated through its root locus. Although the transfer characteristic of the control loop can be approximated to 1^{st}-order behavior, ringing appears in the step response when the open loop gain is high. As a result, there exists an optimized loop gain where the IBN shows the minimum. Besides, a lower corner frequency f_c causes a general decrease of the IBN regardless of the loop gain. For the demodulation type, the minimum IBN can reach around -104 dBFS when $f_c = 0.5\,\mathrm{Hz}$. By the duty-cycle LPF option the controller with $f_c = 5\,\mathrm{Hz}$ LPF can achieve -108 dBFS of IBN. For the differential type, the minimum IBN can reach around -116 dBFS when $f_c = 5\,\mathrm{Hz}$ and -112 dBFS when $f_c = 0.5\,\mathrm{Hz}$, with the given transfer function of the differentiation block from Equation 4.21. In the consideration of electrical noise of the CI, the noise floor raises to -91 dBFS, which is dominant for all implementations of the compensation controller. The transmission delay between the feedback and compensation paths might cause additional disturbance to the $\Delta\Sigma$-modulator and thus must be considered. However, the sampling period T_s is much larger than the common delay in the expected layout of the ASIC. The accuracy that the integrate-dump controller can achieve is determined by the resolution, which is restricted by the hardware complexity and linearity of the DAC. Since the amplitude of V_{compC} is discrete, there exists a max-

imum voltage step of $2\% V_{\mathrm{compC},0} = 21.9\,\mathrm{mV}$. Option of watch-dog is designed for the integrate-dump controller by limiting the maximum integration time in order to avoid the fluctuation of V_{compC}.

In this research, the electrical noise from the $\Delta\Sigma$-modulator – especially from other active elements such as the loop filter – and the thermal noise from the mechanical part of the gyroscope are not fully considered during the system level simulation. The noise from the loop filter is shaped by the $\Delta\Sigma$-modulator loop and thus is attenuated before coupling to the controller input.

For the fully analog approach of compensation like demodulation and differential structure, a memorizing block can be integrated into the voltage generation. The magnitude of compensation is detected by an ADC and stored in a register. The value can be set either periodically updated or fixed after the required accuracy of balancing is achieved. By this method a function of preset compensation is realized and thus the time for the compensation process is mostly saved supposing little change in the balancing condition is required for each startup of the readout system.

Several tasks will be implemented in the next step. The Verilog-A blocks will be successively replaced by transistor-level models to verify the corresponding performance of the test bench. The goal is a fully transistor-level automatic compensation controller with the completed layout. The integrate-dump structure owns quite a few beneficial features as mention before. It can be further improved based on the practical requirement such as the noise observation frequency tuning (NOFT) introduced in [22].

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