Chroma

VLSI Test System

338x

Maintenance Manual

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Version 1.3
Oct 2016

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CHROMA ATE INC.
66 Hwaya 1st Rd., Kueishan Hwaya Technology Park, Taoyuan County 33383, Taiwan

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CHROMA ATE INC.
66 Hwaya 1st Rd., Kueishan Hwaya Technology Park,
Taoyuan County 33383, Taiwan
Tel: 886-3-327-9999
Fax: 886-3-327-2886
e-mail: info@chromaate.com
http://www.chromaate.com

Material Contents Declaration

The recycling label shown on the product indicates the Hazardous Substances contained in the product as the table listed below.


: See **<Table 1>**.


: See **<Table 2>**.

<Table 1>

Part Name	Hazardous Substances					
	Lead	Mercury	Cadmium	Hexavalent Chromium	Polybrominated Biphenyls	Polybromodiphenyl Ethers
	Pb	Hg	Cd	Cr^{6+}	PBB	PBDE
PCBA	O	O	O	O	O	O
CHASSIS	O	O	O	O	O	O
ACCESSORY	O	O	O	O	O	O
PACKAGE	O	O	O	O	O	O

“O” indicates that the level of the specified chemical substance is less than the threshold level specified in the standards of SJ/T-11363-2006 and EU 2005/618/EC.

“×” indicates that the level of the specified chemical substance exceeds the threshold level specified in the standards of SJ/T-11363-2006 and EU 2005/618/EC.

Disposal

Do not dispose of electrical appliances as unsorted municipal waste; use separate collection facilities. Contact your local government for information regarding the collection systems available. If electrical appliances are disposed of in landfills or dumps, hazardous substances can leak into the groundwater and get into the food chain, damaging your health and well-being. When replacing old appliances with a new one, the retailer is legally obligated to take back your old appliances for disposal free of charge.

<Table 2>

Part Name	Hazardous Substances					
	Lead	Mercury	Cadmium	Hexavalent Chromium	Polybrominated Biphenyls	Polybromodiphenyl Ethers
	Pb	Hg	Cd	Cr^{6+}	PBB	PBDE
PCBA	×	O	O	O	O	O
CHASSIS	×	O	O	O	O	O
ACCESSORY	×	O	O	O	O	O
PACKAGE	O	O	O	O	O	O

"O" indicates that the level of the specified chemical substance is less than the threshold level specified in the standards of SJ/T-11363-2006 and EU 2005/618/EC.

"×" indicates that the level of the specified chemical substance exceeds the threshold level specified in the standards of SJ/T-11363-2006 and EU 2005/618/EC.

1. Chroma is not fully transitioned to lead-free solder assembly at this moment; however, most of the components used are RoHS compliant.
2. The environment-friendly usage period of the product is assumed under the operating environment specified in each product's specification.

Disposal

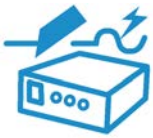
Do not dispose of electrical appliances as unsorted municipal waste; use separate collection facilities. Contact your local government for information regarding the collection systems available. If electrical appliances are disposed of in landfills or dumps, hazardous substances can leak into the groundwater and get into the food chain, damaging your health and well-being. When replacing old appliances with a new one, the retailer is legally obligated to take back your old appliances for disposal free of charge.

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or specific WARNINGS given elsewhere in this manual will violate safety standards of design, manufacture, and intended use of the instrument. *Chroma* assumes no liability for the customer's failure to comply with these requirements.

BEFORE APPLYING POWER
Verify that the power is set to match the rated input of this power supply.

PROTECTIVE GROUNDING
Make sure to connect the protective grounding to prevent an electric shock before turning on the power.



NECESSITY OF PROTECTIVE GROUNDING
Never cut off the internal or external protective grounding wire, or disconnect the wiring of protective grounding terminal. Doing so will cause a potential shock hazard that may bring injury to a person.

FUSES
Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE
Do not operate the instrument in the presence of flammable gases or fumes. The instrument should be used in an environment of good ventilation.

DO NOT REMOVE THE COVER OF THE INSTRUMENT
Operating personnel must not remove the cover of the instrument. Component replacement and internal adjustment can be done only by qualified service personnel.

Safety Symbols

	**DANGER –** High voltage.
	**Explanation:** To avoid injury, death of personnel, or damage to the instrument, the operator must refer to the explanation in the instruction manual.
	**High temperature:** This symbol indicates the temperature is hazardous to human beings. Do not touch it to avoid any personal injury.
	**Protective grounding terminal:** This symbol indicates that the terminal must be connected to ground before operation of the equipment to protect against electrical shock in case of a fault.
	**Functional grounding:** To identify an earth (ground) terminal in cases where the protective ground is not explicitly stated. This symbol indicates the power connector does not provide grounding.
	**Frame or chassis:** To identify a frame or chassis terminal.
	**Alternating Current (AC)**
	**Direct Current (DC) / Alternating Current (AC)**
	**Direct Current (DC)**
	**Push-on/Push-off power switch**
	The **WARNING** sign highlights an essential operating or maintenance procedure, practice, condition, statement, etc., which if not strictly observed, could result in injury to, or death of, personnel or long term health hazards.
	The **CAUTION** sign highlights an essential operating or maintenance procedure, practice, condition, statement, etc., which if not strictly observed, could result in damage to, or destruction of, equipment.
	The **Notice** sign highlights an essential operating or maintenance procedure, condition, or statement.

Revision History

The following lists the additions, deletions and modifications in this manual at each revision.

Date	Version	Revised Sections
Jun. 2014	1.0	Complete this manual.
Feb.2015	1.1	Update 3380D, and Win7 restore operation
Jun.2016	1.2	Update MXLPC Spec
Oct.2016	1.3	Update MLDPS Spec

Table of Contents

1. Overview

This chapter explains the outlines of Chroma 3380/3380P/3380D Test System. .

1.1 Chroma 338x Test System

3380/3380P/3380D can test any types of IO drivers, such as STN, and controller drives. It deploys a per-pin architecture, which provides a timing generator and DC measurement function for every digital pin.

Since a comparator is provided for every IO pin, the test time for devices such as STN and controller drivers requires long test patterns.

1.2 Hardware Configuration

This section explains the hardware configuration of Chroma 3380/3380P/3380D Test System.

1.2.1 Basic System Configuration

The basic configuration of the 3380/3380P/3380D test system with a test head is shown as below. The test system consists of a mainframe, a test head, and a CRAFT for mass-production operation. Each component unit of the test contains various hardware devices as shown in the block diagram below.

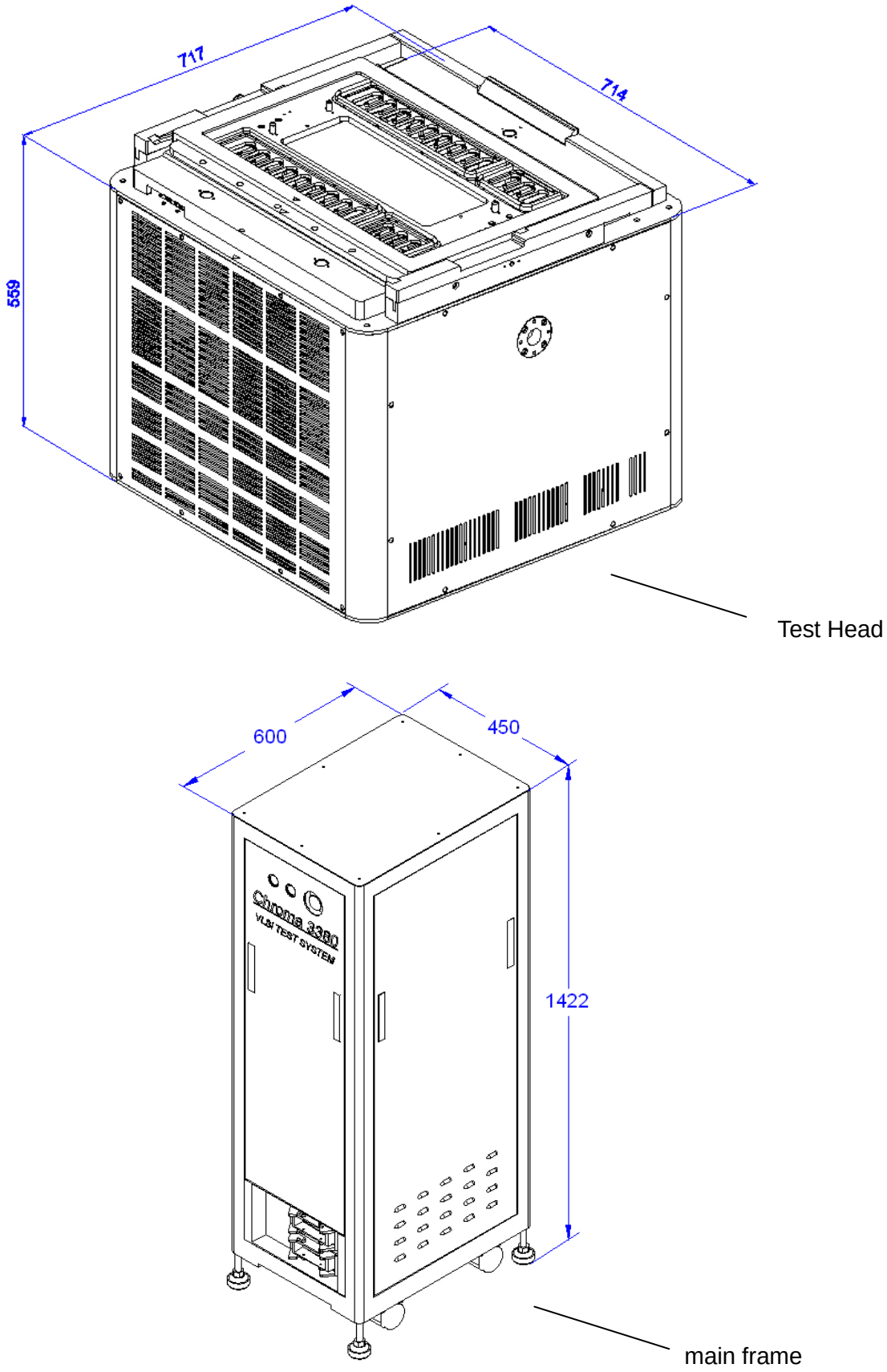


Figure 1-1 Hardware Configuration for 3380 Test System

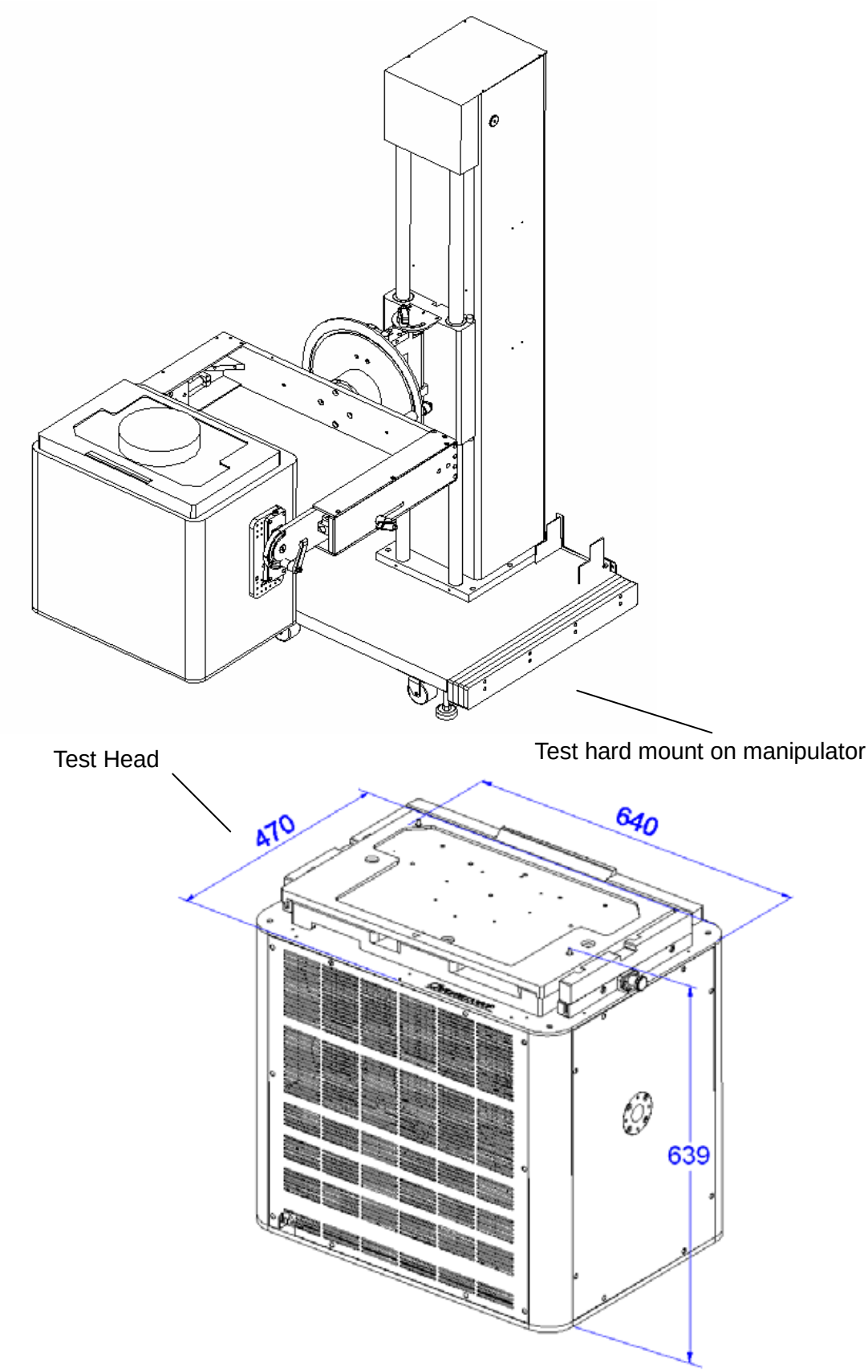


Figure 1-2 Hardware Configuration for 3380P Test System

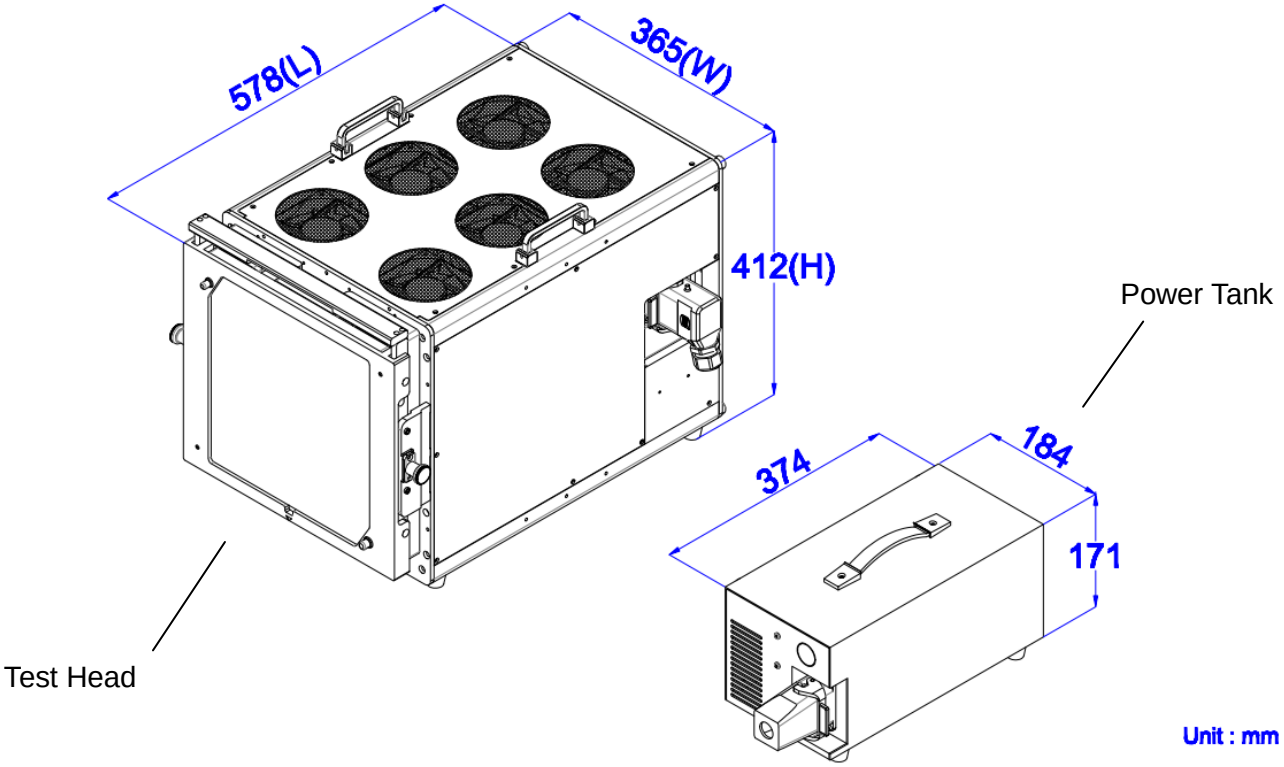


Figure 1-3 Hardware Configuration for 3380D Test System

1.2.2 System Structure

The system contains three parts, the Test Head, Manipulator, and a Control PC. The test head provides room for all electronic board and power supply unit, every thing in one box. The manipulator incorporates with test head to dock to probe or handle. The control PC runs with Microsoft Windows XP or Windows 7 OS. The software package “CRAFT” is special development for 3380/3380P/3380D IC tester operation.

1.2.3 Mechanical Specifications

3380:

Configuration	Weight (Kg)	Dimensions (mm)		
		Width	Depth	Height
Test head	110 (empty) 200 (fully)	714	717	559
Main Frame		450	600	1422

3380P:

Configuration	Weight (Kg)	Dimensions (mm)		
		Width	Depth	Height
Test head	55(empty) 100(fully)	640	470	639
Manipulator	350			
Computer & Desk	20	600	700	1200

3380D:

Configuration	Weight (Kg)	Dimensions (mm)		
		Width	Depth	Height
Test head	35(empty) 47(fully)	365	578	412
Power Tank	15	184	374	171

1.2.4 Block Diagram

The block diagram shows the overall hardware configuration. Refer to next chapter for a detail description of each block.

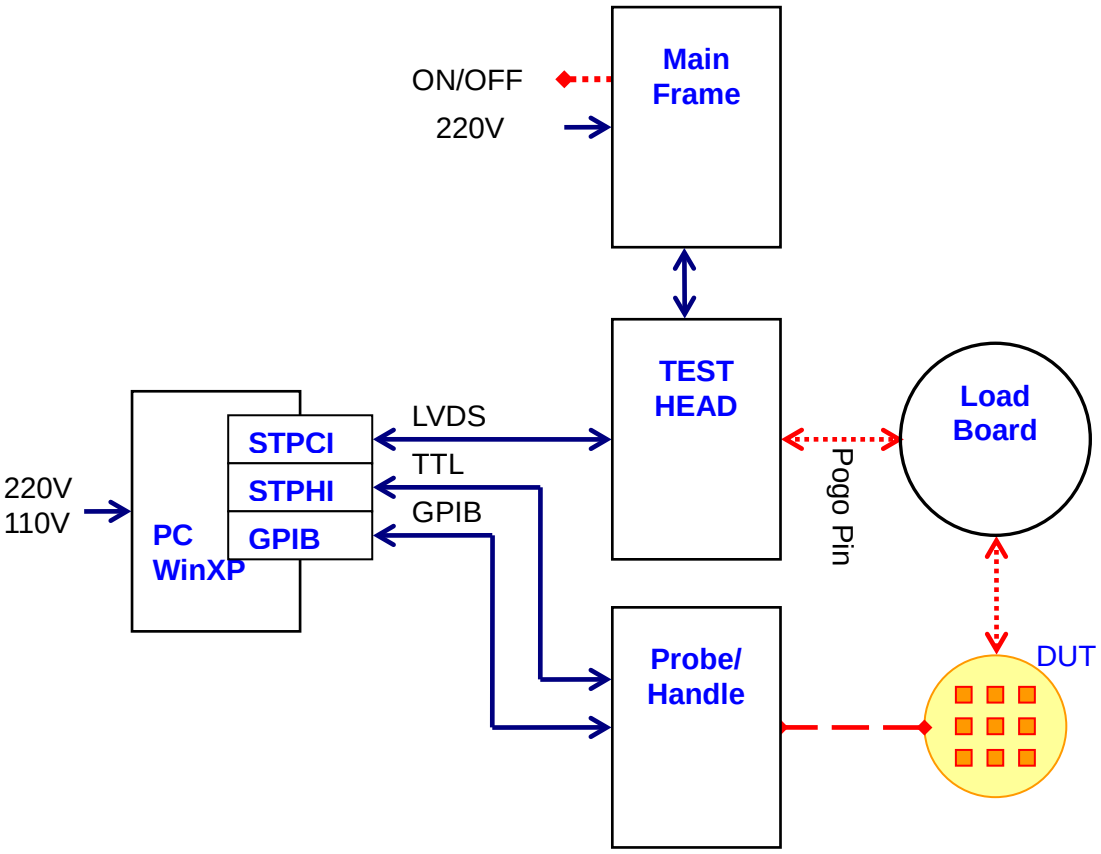


Figure 1-4 3380 Block Diagram of Hardware

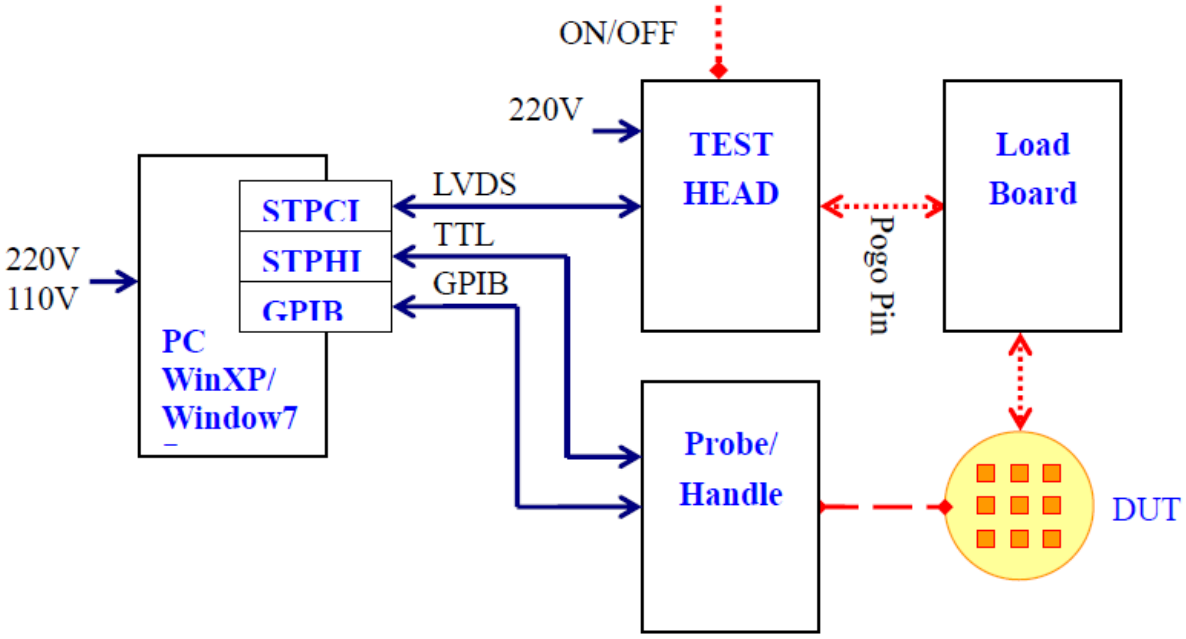


Figure 1-5 3380P Block Diagram of Hardware

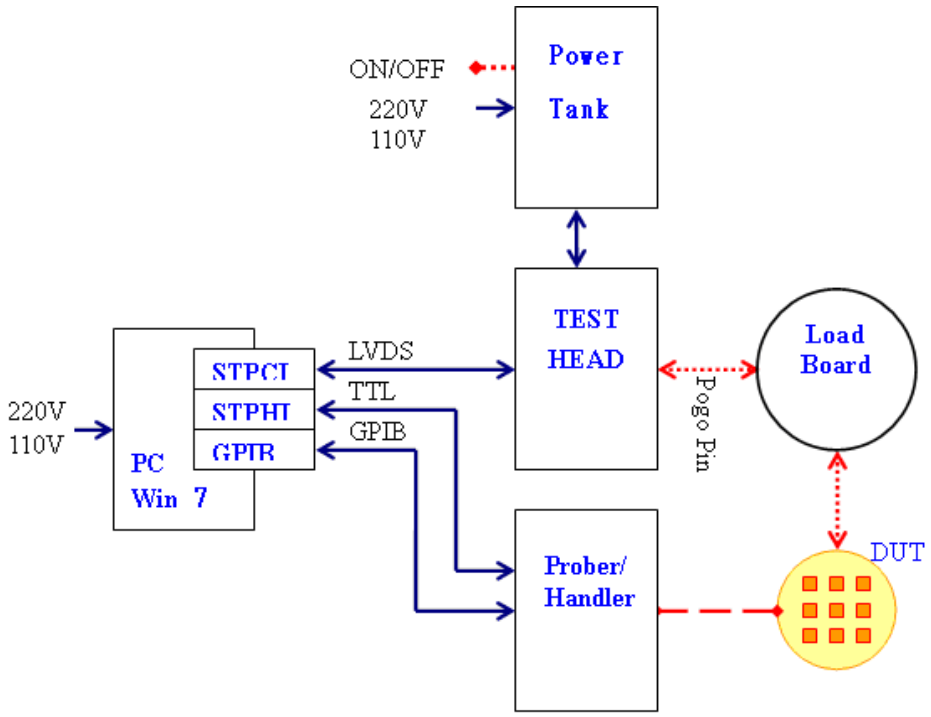


Figure 1-6 3380D Block Diagram of Hardware

1.3 Software Configuration

This section explains the software configuration of Chroma 3380/3380P/3380D Test System.

1.3.1 Software Configuration Diagram

The software configuration of Chroma 3380/3380P/3380D Test System is shown below. For a description of operating environment and software development, refer to the *Chroma* 3380/3380P/3380D *Test System Operation Manual*.

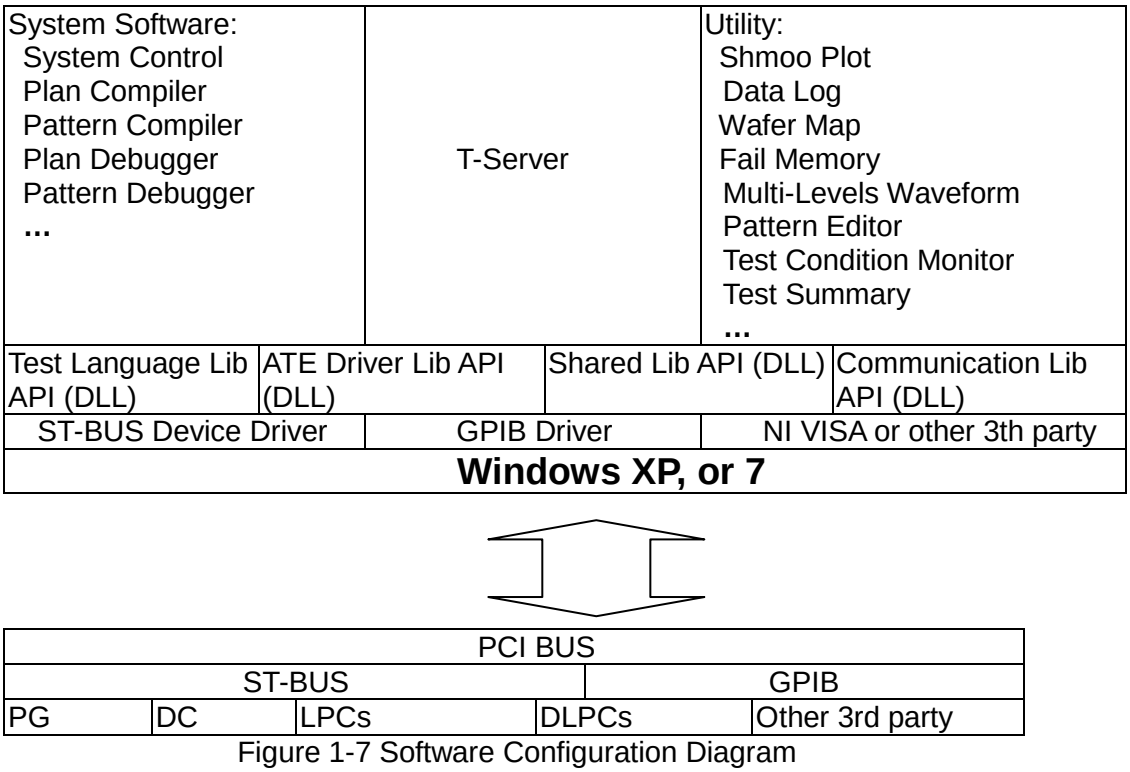


Figure 1-7 Software Configuration Diagram

1.4 Features of the Test System

This section explains the main features of Chroma 3380/3380P/3380D Test System.

1.4.1 Test Systems

3380:

Test head:	All AC+DC board
Manipulator:	For test head
Mainframe:	For power supply
Controller:	PC
Controller OS:	Microsoft Windows XP
Associate and option:	GPIB, PHI, ALPG, Scan

3380P:

Test head:	All AC+DC board
Manipulator:	For test head
Mainframe:	none
Controller:	PC
Controller OS:	Microsoft Windows XP, or Windows 7
Associate and option:	GPIB, PHI, ALPG, and Scan

3380D:

Test head:	All AC + DC board + DC-DC power supply
Manipulator:	AMP50 for 3380D
Mainframe:	none
Controller:	PC
Controller OS:	Microsoft Windows 7
Associate and option:	GPIB, PHI, ALPG, Scan

1.4.2 Pin Count Configuration

3380:

	Model Name & Type	**Fully 1024 Pin**	**Reduced 768 Pin**	**Reduced 512 Pin**	**Notes**
Configuration	IO Pin No.	1024	768	512	
	PMU Ch No.	32	32	32	
	DPS Ch. No.	16	16	16	
	UVI Ch. No.	0	0	32	
Boards Installation	MXLPC	16	12	8	64 pin per board
	MXPMU	2	2	2	16 channel per board
	MXDPS	2	2	2	8 channel per board
	MXPG3	*1*	*1*	*1*	*Sequence Controller*
	MXBUS	1	1	1	Controller interface
	MXUVI	0	0	2	16 channel per board
	(Empty)	2	0	2	Option
Interface	STPCI	1	1	1	Controller interface
	STPHI	1	1	1	option

3380P:

	Model Name	**Logic Tester**	**Notes**
configuration	IO Pin No.	512	
	PMU Ch. No.	16	
	DPS Ch. No.	8	
Boards	MXLPC	8	64 pin per board

Installation	MXPMU	1	16 channel per board
	MXDPS	1	8 channel per board
	MXPG3	1	
	MXBUS	1	
	(Empty)	1	Option, TBD
	STPCI	1	
	STPHI	1	option

3380D:

	Model Name	3380D 256 pins configuration	Notes
configuration	IO Pin No.	256	
	PMU Pin No.	16	
	DPS Pin No.	16	
Boards Installation	MXLPC	4	IO Pin.
	MLDPS-16	1	16 CH DPS.
	MXPMU	1	PMU
	MXBUS	1	Host Interface
	MXPG3	1	Sequence Controller
Option Boards	MLDPS	-	32 CH DPS.
	MXDPS	-	DPS.
	MXUVI	-	VI Source.
	MXREF	-	VI Source.
	MXAWI	-	ADDA
	MAWI2	-	ADDA

1.4.3 Resolution Summary

Board Name	DAC Resolution	ADC Resolution
MXLPC	PE : 14 bits PPMU:16 Bits	PPMU:16 Bits
MXPMU	16 Bits	16 Bits
MXUVI	16 Bits	16 Bits
MXREF	16 Bits	16 Bits
MXDPS	16 Bits	18 Bits
MLDPS	16 Bits	18 Bits
MXAWI	16 Bits	16 Bits
MXAVO	TBD	TBD

1.4.4 AC Power Requirement

3380:

Item/Model	3380 Logic Tester
AC Inlet Specification	AC 204V ~ 250V (30A ~ 25A) 47Hz ~ 63Hz 3 phase with 4 wires, or single phase with 3 wires
KVA:	6.0 KVA, continue

3380P:

Item/Model	3380P Logic Tester
AC Inlet Specification	AC 204V ~250V (15A~12A) 47Hz ~ 63Hz 3Ø4W, or 1Ø3W
KVA:	3.0KVA, continue

3380D:

Item/Model	3380P Logic Tester
AC Input Rating Voltage: (configuration @192 pins)	110 - 220V +-10% VLN 47 - 63 Hz
KVA:	1.5 KVA, continue

1.4.5 Environment

Temperature	Operating: +20'C ~ +26'C Storage: -20'C ~ +50'C Change rate: Re-calibration are require while temperature change more than +/- 1'C
Humidity	Operating: 50% ~ 70% Storage: 20% ~ 90%

1.4.6 Control PC Requirement

PCI 2.0 Slot	*2, for STPCI, and STPHI
PCIe Slot	*2, for GPIB, or others option

2. Hardware Descriptions

This chapter provides information on the hardware of Chroma 3380/3380P/3380D Test System.

2.1 Test Head

Each test head of 3380P can accommodate I/O pins (512 pins max), MXDPS (8 channels max), MXPMU (16 channels max), MXBUS, MXPG3 and other option board (MXUVI, MXREF, and MXAWI).

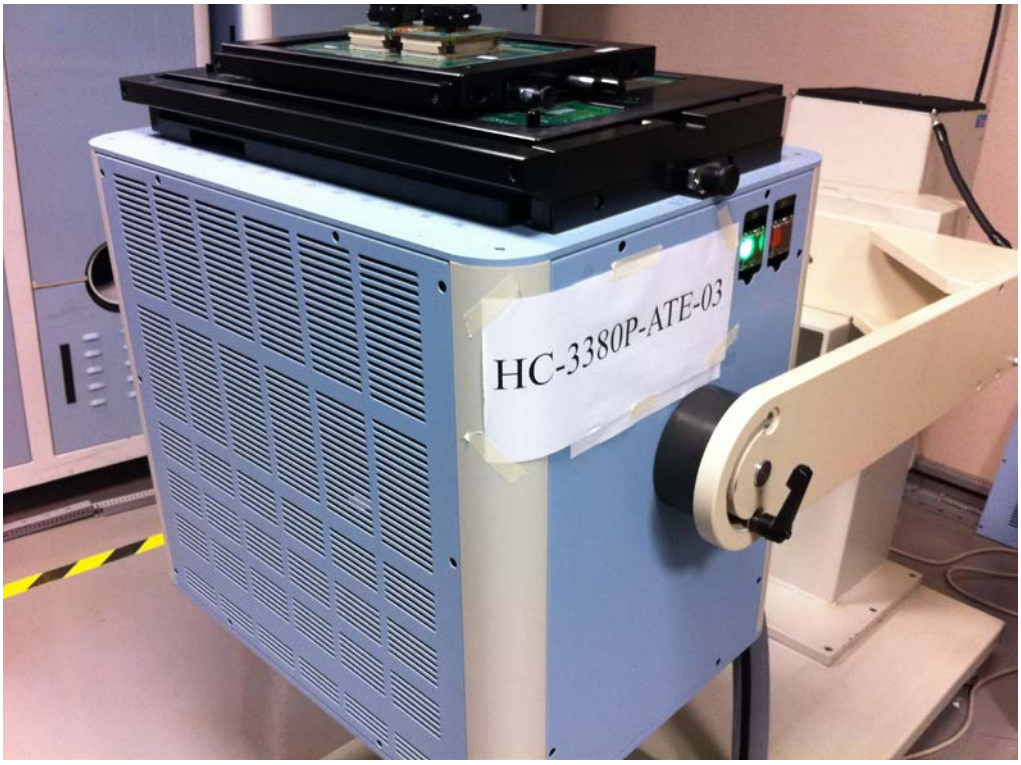


Figure 2-1 3380P Test Head

The power panel is located at the right side door cover (see Figure 2-2) has two Light-Emitting Diodes (LEDs) to indicate tester power status. The tester power switch controls the power on/off by pushing the green or red button.

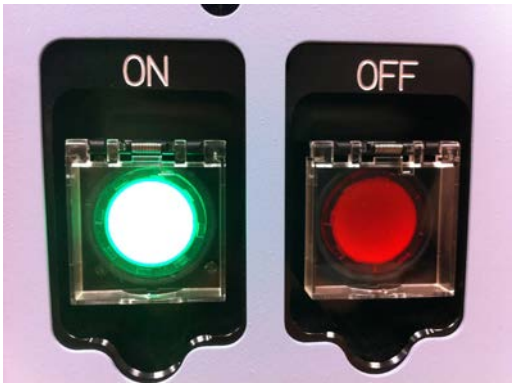


Figure 2-2 Power Panel

Figure 2-3 3380P Test Head Top View

Table 2-1 Board Location at 3380 Test Head

TBUS	LPC12	LPC0	LPC6	LPC18 (OPT0)	LPC20 (DPS0)	LPC22 (PMU0)	LPC4	LPC10	LPC16	LPC8	LPC2	LPC14
SQPG	LPC13	LPC1	LPC7	LPC19 (OPT1)	LPC21 (DPS1)	LPC23 (PMU1)	LPC5	LPC11	LPC17	LPC9	LPC3	LPC15

Table 2-2 Board Location at 3380P Test Head

Slot	1	2	3	4	5	6	7	8	9	10	11	12	13
Board	MXBUS	MXDPS	MXLPC2	MXLPC4	MXLPC0	MXLPC6	MXLPC8	MXLPC7	MXLPC1	MXLPC5	MXLPC3	MXPG3	MXPMU

Table 2-3 Board Location at 3380D Test Head

Board	MLDPS (LPC4)	LPC3	LPC1	MXBUS	MXPG3	LPC0	LPC2	PMU0 (LPC5)

2.2 MXLPC Function

This section describes the MXLPC system from the perspective of programmer.

2.2.1 MXLPC (Logic Pin Control) AC Specification Summary

Configuration

Pin number per board	64 pins / board
Maximum pattern rate:	100Mhz.
Controller:	3380/3380P MXPG3
PE Level DAC	Mega
PE Level DAC	14Bits
PPMU DAC & ADC	16Bits

Pattern Generator

FPM Pattern Memory: **(Fast Pattern Memory)**	1K deep
SPM Pattern Memory: **(Sequential Pattern Memory)** **(16M & 32M Option)** **(1M reserved for system always)**	16M Option: Max user pattern deep: 15M, 30M(2X Mode) 32M Option: Max user pattern deep: 31M, 62M(2X Mode)
Fail log Memory: **Memory Size:** **Log information:**	1K, PEH, PEL, Pin fail;
Capture Memory **Memory deep Size:** **Capture information**	8k per pin, 64K maximum. PEL/PEH/PFAIL selectable, 1 bit / pin
ALPG Pattern Memory configuration **Pattern Memory Size:** **Pattern Memory width**	Option, Embedded in MXLPC 1K, remapped from FPM pattern memory *16X Address/*16Y Address/*16Data
SCAN Pattern Memory configuration **Scan Chain Number** **Scan Pattern Memory Size**	2,4,8 scan chain / Board, configurable 1G bits / chain default, 2G bits / chain option

Timing Generator

Timing generator scheme: **Driver marker edge** **Strobe marker edge** **IO marker edge**	8 edges / pin. 4 edges / pin 2 edges / pin 2 edges / pin
Number of timing set:	16 sets;
Edge setting range:	0 ns ~ (2cycle – 1.25ns)
Edge placement accuracy (EPA)	+/- 400 ps
Rate setting range:	10ns to 5ms (19 bits)
Rate setting resolution:	625 ps

Free run clock generator

Timing generator scheme:	8 clock/board
Marker number:	2 edges / clock
Maximum clock rate:	200Mhz
Edge setting range:	0ns ~ (1rate – 1.25ns)
Rate setting range:	5ns to 5ms (19 bits)
Rate setting resolution:	625 ps

Pins function

Driver waveform format:	NRZ, RO, RZ, 1, 0, SBC, DNRZ, DDR
Compare marker type:	Edge, Window strobe (min tw=20ns);
IO format	WNRZ, WRZ, 0, 1
Pin or data multiplex:	Not support

Time and Frequency measurement unit

Number of measurement unit:	8 unit / Board
Per pin measurement:	Yes,
Maximum Frequency measurement:	400Mhz
Maximum Time measurement:	40sec(0.025Hz) Measurement resolution : 10ns
Input stage:	Embedded in IO pin PE Followed by Compare level (VOH/VOL)
Edge transient detect mode:	Normal level mode: by VOL Schmitt trigger mode: by VOL & VOH
Trigger Mode	By micro-instruction By HOST CPU
Measurement counter size	Time:32 bits Frequency: 50 bits
Frequency measurement accuracy:	10ppm (typical)
Signal Shot Time measurement mode	Pulse low, Pulse high, Cycle

2.2.2 MXLPC DC Specification Summary

Pin Driver Part

Driver Rise Time/Fall Time	1.4 V/1ns (measurement at VIH=3V, VIL=0V, unterminated; 10% to 90%)
Output voltage range **VIH** **VIL**	-1.9V to +6.0V -2.0V to +5.9V
Output voltage precision	±(0.5%+20mV)
Output voltage resolution	0.61mV
Output current limit	75mA
Output voltage amplitude	0.05Vp-p to 8.0Vp-p
Output impedance	50±5Ω
I/O switching ON time	7ns (Typical)
I/O switching OFF time	5ns (Typical)

Comparator Part

Input voltage range	-2.0V to +6.0V
Input compare precision	±(0.5%+20mV)
Input voltage resolution	0.61mV
Input voltage amplitude	±0.1 to ±8V
Input resistance/capacity	10MΩ or more / 100pf or less
Comparator switching time	2ns

Programmable Active Load

Current range	IOH: 0mA to –12mA IOL: 0mA to +12mA
Current resolution	1.464uA
Current accuracy	± (0.5%+25uA)
VREF assigned range	-1.75V to +5.75V
VREF resolution	0.61mV
VREF accuracy	±(0.5%+20mV)
Minimum ON time	11ns
Minimum OFF time	8ns

Programmable Clamp

Clamp voltage	Clamp+:-1.5V to +6.0V Clamp-:-2.0V to +5.0V
Clamp voltage precision	±(0.5%+50mV)
Clamp voltage resolution	0.61mV
Clamp current limit	60mA

HV Pin Driver Part (Per Board 4 channel)

Driver Rise Time/Fall Time	30mV/ns
Output voltage range **VIH** **VIL** **VHH**	-0.1V to +6V -0.1V to +6V +5.9V to +13.5V
Output voltage precision	±(0.5%+20mV)
Output voltage resolution **VIH** **VIL** **VHH**	0.61mV 0.61mV 1.22mV
Output impedance	1 ohm (Typ), 10 ohm(Max)
Output current capability	60mA

PPMU (16 Bits DAC & 16 Bits ADC)
Output forcing voltage specification:

Range	Force Voltage Range	Resolution	Max Current	Accuracy
±2uA ±20uA, ±200uA ±2mA ±32mA	-2V~+6V	152uV	±2uA ±20uA ±200uA ±2mA ±32mA	+/-0.1%+/-5mV

Output force current specification:

Range	force current range	Resolution	Max. Current	Compliance Voltage range	Accuracy
±2uA	-2uA~ +2uA	122pA	±2.2uA	-2~+6V	±(0.2% + 10nA)
±20uA	-20uA~ +20uA	1.22nA	±22uA	-2~+6V	±(0.2% + 100nA)
±200uA	-200A~ +200uA	12.2nA	±220uA	-2~+6V	±(0.2% + 1uA)
±2mA	-2mA~ +2mA	122nA	±2mA	-2~+6V	±(0.2% + 10uA)
±32mA	-32mA~ +32mA	1.52uA	±32mA	-2~+6V	±(0.2% + 100uA)

Measure voltage specification:

Range	Measure range	Resolution	Accuracy
-2V~+6V	-2V~+6V	152uV	±0.1%±10mV

Measure current specification:

Range	Measure range	Resolution	Max. Current	Accuracy
±2uA	-2uA ~ +2uA	61pA	±2uA	±(0.2% + 10nA)
±20uA	-20uA ~ +20uA	610pA	±20uA	±(0.2% + 100nA)
±200uA	-200uA ~ +200uA	6.1nA	±200uA	±(0.2% + 1uA)
±2mA	-2mA ~ +2mA	61nA	±2mA	±(0.2% + 10uA)
±32mA	-32mA ~ +32mA	984nA	±32mA	±(0.2% + 100uA)

2.3 Device Power Supply (DPS) Resources

This section describes the MXDPS system from the perspective of programmer.

2.3.1 Specification Summary

Configuration

Channel number:	8 channel / Board, 1 board / System (Default)
V range:	4V, 8V, 12V, 16V
I range:	1uA, 10uA, 100uA, 1mA, 10mA, 100mA, 1A, 2A
Outlet:	Go through pogo pin directly to load board
Measurement Trigger by:	CPU, Pattern
Function:	Force V, Force I, Measure I, Measure V, Clamp I, Clamp V, Constant current load, Clamp flag

Force V Specification (16 bit DAC)

Range	Output Voltage	Resolution	Max current	Accuracy
4V	-4V ~ +4V	0.1272mV	+/- 2 A	+/-(0.1%+1mV)
8V	-8V ~ +8V	0.2543mV	+/- 2 A	+/-(0.1%+2mV)
12V	-8V ~ +12V	0.3815mV	+/- 2 A	+/-(0.1%+3mV)
16V	-8V ~ +16V	0.5088mV	+/- 1.8 A	+/-(0.1%+4mV)

Force I Specification (16 bit DAC)

Range	Max Current	Resolution	Accuracy
100uA	-100uA ~ +100uA	3.81nA	+/-(0.1% + 0.1uA)
1mA	-1.00mA ~ +1.00mA	38.1nA	+/-(0.1% +1uA)
10mA	-10.0mA ~ +10.0mA	381nA	+/-(0.1% + 10uA)
100mA	-100mA ~ +100mA	3.81uA	+/-(0.1% + 0.1mA)
1A	-1.0A ~ +1.0A	38.1uA	+/-(0.1% +1mA)
2A	-2A ~ +2A	72.2uA	+/-(0.1% +2mA)

Measure I Specification (18 bit ADC)

Range	Measuring	Resolution	Accuracy
1uA	-1.0uA ~ +1.0uA	11.7pA	+/-(0.1% +5nA)
10uA	-10.0uA ~ +10.0uA	117pA	+/-(0.1% + 10nA)
100uA	-100uA ~ +100A	1.17nA	+/-(0.1% + 100nA)
1mA	-1.00mA ~ +1.00mA	11.7nA	+/-(0.1% + 1uA)
10mA	-10.0mA ~ +10.0mA	117nA	+/-(0.1% + 10uA)
100mA	-100mA ~ +100mA	1.17uA	+/-(0.1% + 100uA)
1A	-100A ~ +1.00A	11.7uA	+/-(0.1% +1mA)
2A	-2.00A ~ +2.00A	23.4uA	+/-(0.1% +2mA)

Measure V Specification (18 bit ADC)

Range	Output Voltage	Resolution	Accuracy
4V	-4.0V ~ +4.0V	31.25uV	+/-(0.1%+1mV)
8V	-8.0V ~ +8.0V	62.5uV	+/-(0.1%+2mV)
12V	-12.0V ~ +12.0V	93.75uV	+/-(0.1%+3mV)
16V	-16.0V ~ +16.0V	125uV	+/-(0.1%+4mV)

Clamp I Specification (Over current clamp & under current clamp, 16 bit ADC)

Range	Max Current	Resolution	Accuracy
100uA	-125uA ~ +125uA	3.81nA	+/-(0.1% + 0.1uA)
1mA	-1.25mA ~ +1.25mA	38.1nA	+/-(0.1% +1uA)
10mA	-12.5mA ~ +12.5mA	381nA	+/-(0.1% + 10uA)
100mA	-125mA ~ +125mA	3.81uA	+/-(0.1% + 0.1mA)
1A	-1.25A ~ +1.25A	38.1uA	+/-(0.1% +1mA)
2A	-2.5A ~ +2.5A	72.2uA	+/-(0.1% +2mA)

Clamp V Specification

Range	Output Voltage	Resolution	Accuracy
16V	-8V ~ +16V	0.515mV	+/-(0.1%+4mV)

Constant current load

Range	Max Current	Resolution	Accuracy
100uA	-100uA ~ +100uA	3.81nA	+/-(0.1% + 0.1uA)
1mA	-1.0mA ~ +1.0mA	38.1nA	+/-(0.1% +1uA)
10mA	-10.0mA ~ +10.0mA	381nA	+/-(0.1% + 10uA)
100mA	-100mA ~ +100mA	3.81uA	+/-(0.1% + 0.1mA)
1A	-1.0A ~ +1.0A	38.1uA	+/-(0.1% +1mA)
2A	-2.0A ~ +2.0A	72.2uA	+/-(0.1% +2mA)

2.4 Precision Measurement Unit (PMU)

This section describes the Parameter Measure Unit (MXPMU) system from the perspective of programmer.

2.4.1 Specification Summary

Configuration

Number of channel:	16 channel / board
Number of board in a system:	3380P/3380D: 1 board / system 3380: 2 board / system
Number of V range:	6V, 12V, 24V, 48V,
Number of I range:	1uA, 10uA, 100uA, 1mA, 10mA, 100mA
Outlet:	Go through pogo pin of ATE tester pin
Measurement Trigger by:	CPU
DAC and ADC chip:	16 bits
Clamp:	Programmable

V_RANGE specification

V_Range	Resolution	Accuracy
± 6V	250uV	± (0.1% +± 5mV)
± 12V	500uV	± (0.1% +± 10mV)
± 24V	1mV	± (0.1% + 20mV)
± 48V	2mV	± (0.1% + 40mV)

I_RANGE specification

I_Range	Resolution	Accuracy
± 1uA	40pA	± (0.2% + 5nA)
± 10uA	400pA	± (0.2% + 50nA)
± 100uA	4nA	± (0.2% + 500nA)
± 1mA	40nA	± (0.2% + 5uA)
± 10mA	400nA	± (0.2% + 50uA)
± 100mA	4uA	± (0.2% + 500uA)

2.5 Pin Voltage Reference (MXREF, Option)

This section describes the Pin Voltage Reference, MXREF (option board) system from the perspective of programmer.

2.5.1 Specification Summary

Configuration

Number of channel:	16 channels UVI per board
Number of board in a system:	optional
V range:	6V, 12V, 24V, 48V
I range:	1uA, 10uA, 100uA, 1mA, 10mA,100mA,250mA
Outlet:	Go through pogo pin directly
Measurement Trigger by:	By CPU Trigger
DAC and ADC chip:	16 bits
Clamp:	Programmable

V_RANGE specification

Voltage Range Name	Voltage Output Maximum	Resolution	Accuracy
6V	+/- 6V	250uV	+/- (0.1% + 4mV)
12V	+/- 12V	500uV	+/- (0.1% + 8mV)
24V	+/- 24V	1mV	+/- (0.1% + 16mV)
48V	+/- 48V	2mV	+/- (0.1% + 32mV)

I_RANGE specification

I_Range	Resolution	Accuracy
+/-1uA	40pA	+/- (0.2% + 5nA)
+/- 10uA	400pA	+/- (0.2% + 50nA)
+/- 100uA	4nA	+/- (0.2% + 500nA)
+/- 1mA	40nA	+/- (0.2% + 5uA)
+/- 10mA	400nA	+/- (0.2% + 50uA)
+/- 100mA	4uA	+/- (0.2% + 500uA)
+/- 250mA	10uA	+/- (0.2% + 1.5mA)

Application Notes:

- MXREF share with the common slot 1~8.
- Provide additional 16 channels.
- Please consult application engineer for system re-configuration.

2.6 SQPG (Sequential Pattern Generator) Function

This section explains how test patterns are generated by 3380/3380P.

2.6.1 SQPG Block Diagram

The Rate I generates a rate signal and the SQPG controls pattern generation. The SQPG sent PMA and control bit via PMA & CPM base on the Rate I. The SQPG controls pattern generation per rate.

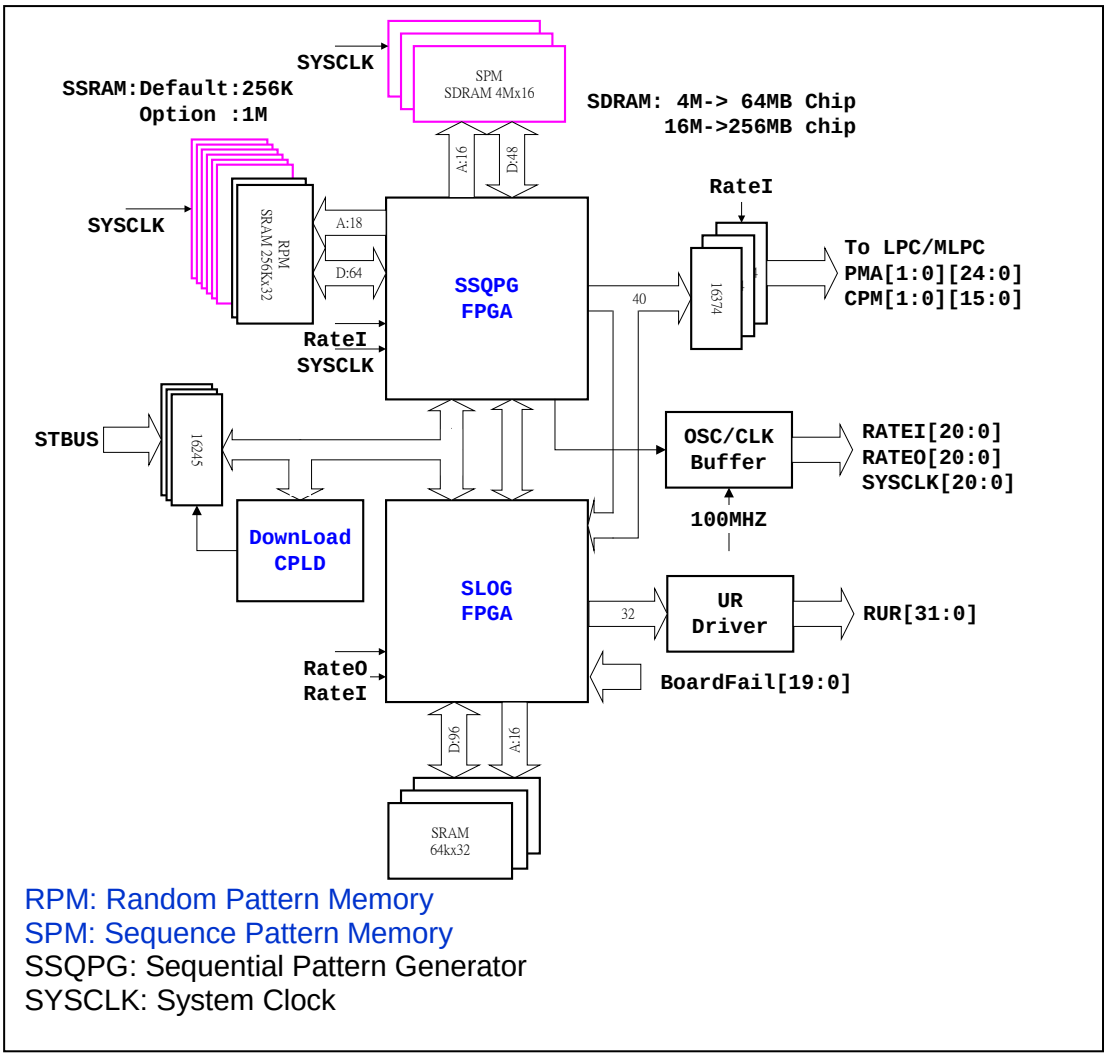


Figure 2-4 SSQPG Block Diagram

2.6.2 SQPG Instructions

This section explains SSQPG instructions. The table below lists of SSQPG Instructions. For detail information, refer to the language manual.

Micro Instruction	Description
NOP	No operation
RPT	Repeat count: repeat the same address
STOP	Stop pattern execution
SETM	Match count: set match count to index match register
IMATCH	Immediately match
DPS	High speed pattern trigger to measure the DPS current simultaneously
PREF	High speed pattern trigger to measure PREF current simultaneously
SETXi	Count_value , i = 0~3:
SETS	Count_value : Set Subroutine Counter
JNZi	label, i = 0~3 :
JMP label	Unconditional jump

JCONT label	Continuous loop jump
JSR label	Subroutine call
RET label	Returning from the subroutine to the label
TFTM	Trigger of Freq. And Time Measurement
LCDC	LCD convert each pin's pattern level to comparator
LCDS	Strobe LCD pins
LCDW	Window hold
UISYNC	From u-instruction send trigger signal to test head BNC

Table 2-2 SQPG Instructions

2.6.3 Specification Summary

2.6.3.1 MXPG3

Sequence controller

Sequence control memory:	FPM: 1K SPM: 16 mega Default 32 mega Option SPM,2X mode : 32M, 64M
Multi-site support:	512 Site / System
Match mode:	Immediate match.
Micro instruction support:	Refer to language for detail.
Log memory size:	1K

Note SPM: Sequential Pattern Memory
FPM: Fast Pattern Memory

ALPG(option)

Pattern memory size:	1K
Pattern bits	16 bits X Address 16 bits Y Address 16 bits Z Data
Multi-site support:	(Same as logic pattern)

2.7 MXBUS Function

This section explains the MXBUS function.

2.7.1 ST-Bus Subsystem Overview

The Tester Bus (ST-Bus) subsystem is the internal communication bus inside the Test Head from a Control Computer to each hardware subsystem. ST-Bus subsystem contains software and hardware segments to complete the communication task.

2.7.1.1 Purpose of ST-Bus Subsystem

The main purpose of ST-Bus subsystem is to provide a set of Application Programming Interface (API) to read/write data from/to specific address location on the Test Head Hardware subsystem, and to generate a predefined set of ST-Bus-protocol signals to each Test Head Hardware subsystem over the Test Head Back Plane PCB.

2.7.1.2 Purpose of ST-Bus Software Segment

The main purpose of software (S/W) segment of ST-Bus subsystem is to provide a set of Application Programming Interface (API) for the System S/W on Windows XP platform to read/write data from/to specific address location on the Test Head Hardware subsystem.

2.7.1.3 Purpose of ST-Bus Hardware Segment

The main purpose of hardware segment of ST-Bus subsystem is to convert the PCI-protocol signal on the Control Computer into a proprietary Tester Bus (ST-Bus)-protocol signal. The PCI bus signals will act following the request from API-call of the S/W segment. The resulting ST-Bus-protocol signal will be transmitted to each Test Head Hardware subsystem over the Test Head Back Plane PCB.

2.7.2 Block Diagram(s)

2.7.2.1 Overview of HLD ST-Bus Block Diagram

Following is a set of block diagrams for 3380/3380P Tester System and Tester Bus (ST-Bus) subsystem. Detailed description can be found in the next section.

2.7.2.2 338x System Block Diagram

Following is a brief block diagram of the Chroma 3380/3380P Driver Test System.

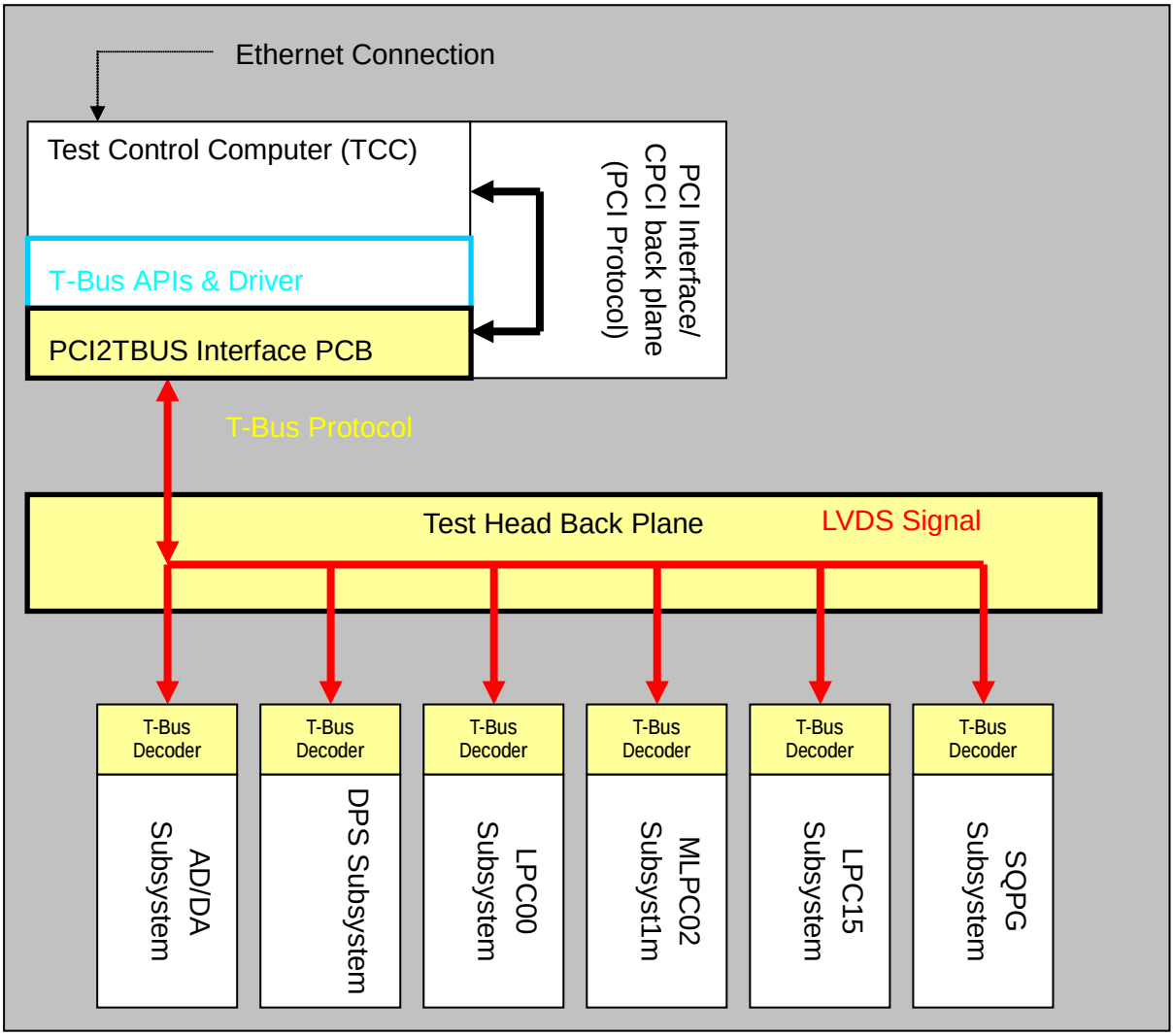


Figure 2-5 Block Diagram of Chroma 3380/3380P Driver Test System

The 3380/3380P System contains a Test Control Computer (TCC), which provides the System S/W for user to encode/compile/debug the test program, and a set of H/W subsystems located in the Test Head Mechanism subsystem. All these Test-Head H/W subsystems are interconnected via Test-Head Back Plane (THBP), and the Test Head H/W are connected to the Control Computer through the Control Computer Interface PCB. The Control Computer I/F PCB and THBP, with S/W APIs and Drivers, are collectively called the Tester Bus (ST-Bus) subsystem.

2.7.2.3 ST-Bus Block Diagram

Following is the ST-Bus block diagram:

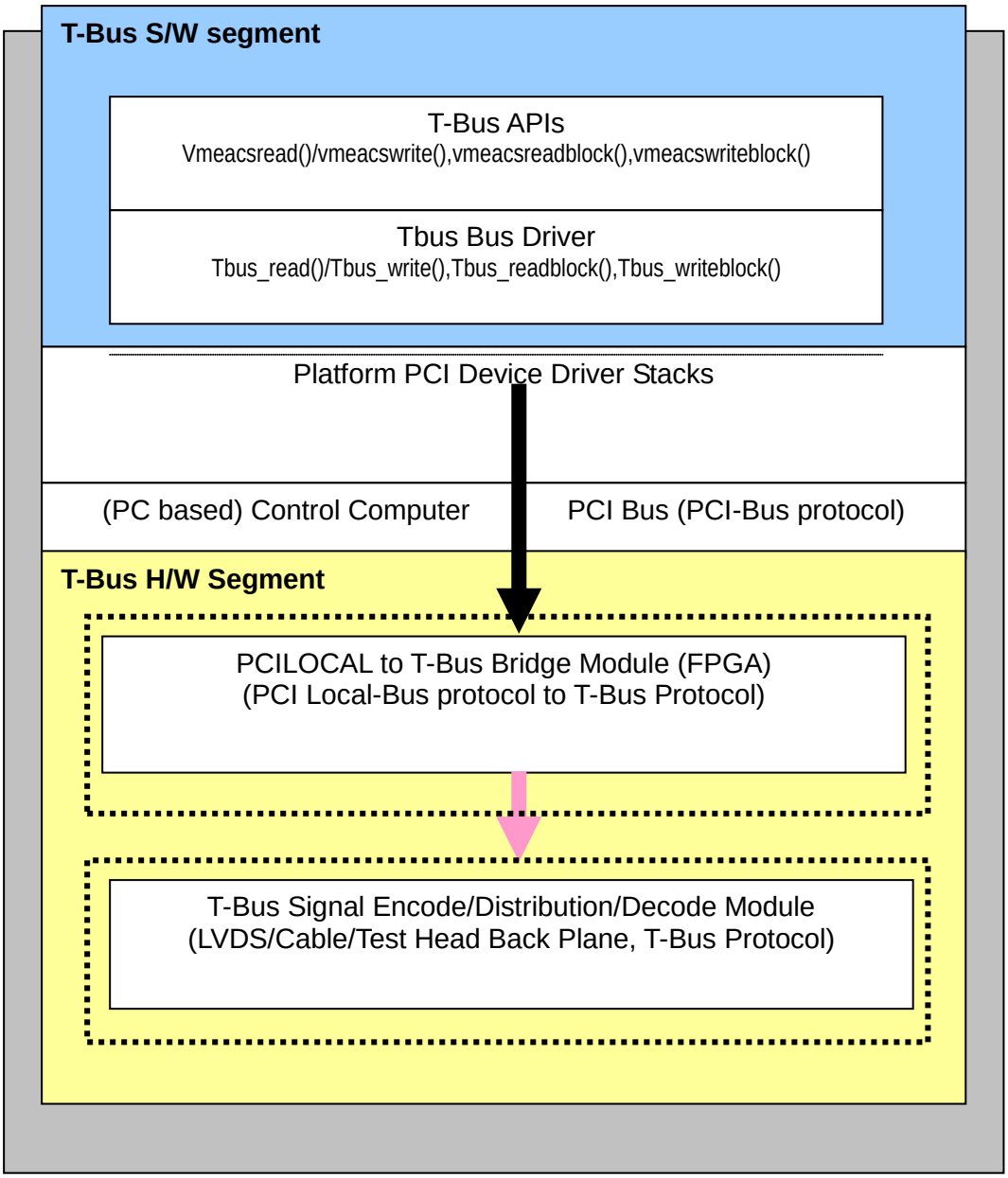


Figure 2-6 Block Diagram of ST-Bus Subsystem

The 3380/3380P ST-Bus subsystem contains ST-Bus S/W segments which provide the APIs for System S/W to invoke, and a ST-Bus H/W segment which translates Control Computer PCI-bus-protocol signals into ST-Bus-protocol LVDS signals as well as distributes ST-Bus LVDS signals to the Test-Head H/W Subsystems.

2.7.3 Functional Description

The main purposes of the ST-Bus subsystem are:

- To provide a bi-directional data channel between Control Computer and Test Head hardware subsystems. Data can be sent (written) to each subsystem from Control Computer in the Test Head and can be retrieved (read) from each subsystem back to Control Computer.

- To convert the Control Computer PCI-protocol signals into proprietary Tester Bus (ST-Bus)-protocol signals.

- To provide a high-performance yet reliable data transfer bus. Due to the fact that each subsystem takes commands from Control Computer, the ST-Bus should be high-performance and high-reliable bus such that Tester System can perform the testing well.

- 64 Channel of user relay control (URC) signals.

- Serial relay interface for user expandable up to 128 user relay.

- User relay power outlet: 5V with 8A.

2.8 STPHI (Prober/Handler Interface) Function

This section explains the STPHI function.

2.8.1 Function Description

The prober/handler interface is designed to allow connection of a handler/prober and to control them.

2.8.1.1 Signals from Prober/Handler to Tester

START: This signal indicates the beginning of a test. It outputs when the prober/handler becomes ready for testing.

RESTART: This signal outputs when a retest is conducted for continuous fail check back or other purposes.

EOW: This signal outputs when a device test on a wafer ends or when a wafer test is unloaded. In other words, it informs the current wafer test has finished.

ON_SITE[3..0]: This signal outputs when doing multi-site testing.

2.8.1.2 Signal from Tester to Prober/Handler

BIN[31..0]: This signal identifies the bin into which the result has been classified.

EOT[3..0]: This signal is used by the tester to request the handler/prober to end the test.

REPORBE: This signal indicates that the tester requests prober to probe again.

STOP: This signal is used by the tester to request the prober to stop operating temporarily.

2.8.2 Signal Timing Charts

2.8.2.1 The Output Signals Timing Charts

There are 4 modes implemented for output wave generating. They are named as mode 0, mode 1, mode 2, and mode 3. In the mean time 4 delayed time registers are defined for these timing control modes. They are called tx, t0, t1, and t2.

The tx is fixed at 6us while the t0, t1, and t2 are user programmable. A 1us time base can be used for delay time registers. The timing waveform is described as below.
(1) The BINENn are used to enable the output of BIN-data, REPROBE, and STOP signals.
(2) The RBINWRn means host computer issue the binning command.

2.8.2.2 The Mode 0 Signal Waveform

The BINENn is de-asserted same time as EOT. User should guarantee all waveforms could be done before the next STARINn asserts.

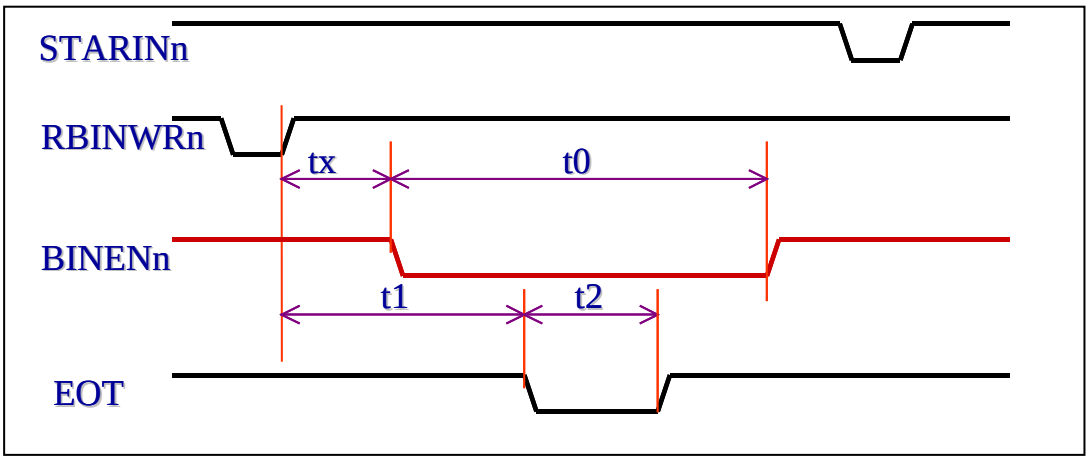


Figure 2-7 Mode 0 Timing Chart

2.8.2.3 The Mode 1 Signal Waveform

The bin data may latch at either rising or falling of EOT. This waveform is the most often used one. It is same as mode 0 while tx + t0 = t1 +t2.

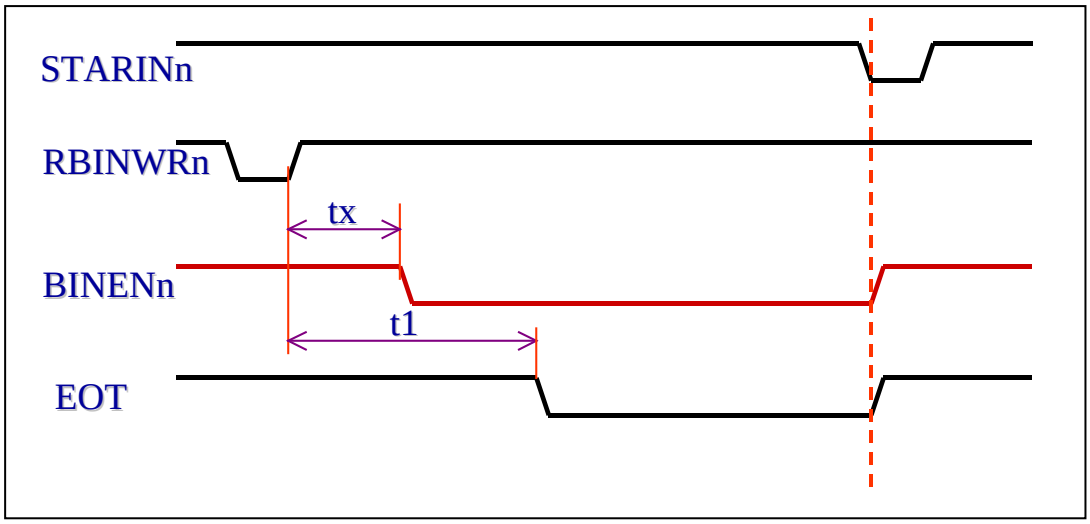


Figure 2-8 Mode 1 Timing Chart

2.8.2.4 The Mode 2 Signal Waveform

The EOT and BINENn are de-asserted until STARINn asserts. The unused register t0 and t2 should load with 0x0000.

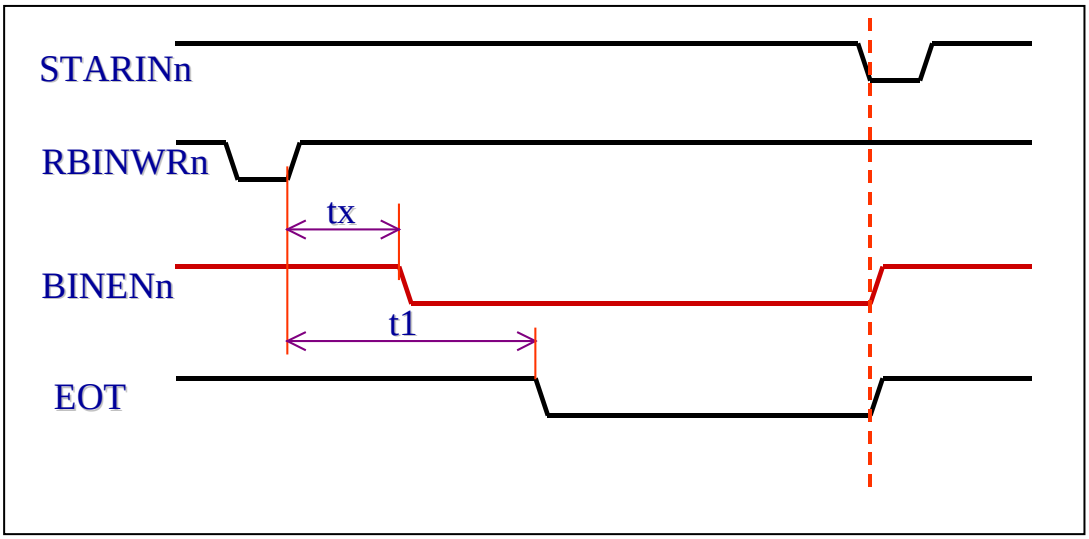


Figure 2-9 Mode 2 Timing Chart

2.8.2.5 The Mode 3 Signal Waveform

The EOT are de-asserted until STARINn asserts. The unused register t2 should load with 0x0000.

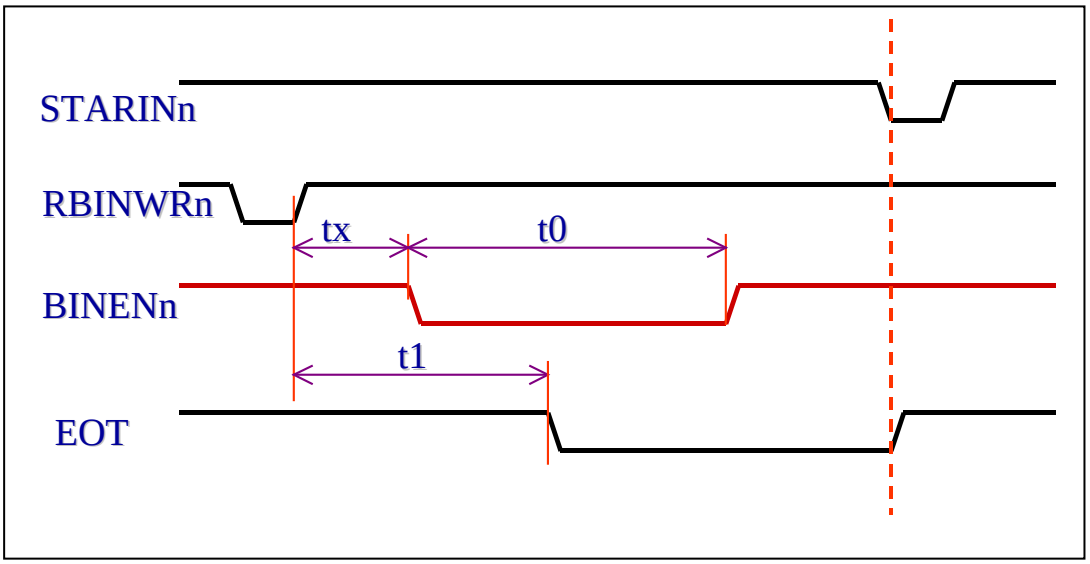


Figure 2-10 Mode 3 Timing Chart

2.8.3 PHI Input Signals Process

Following are the prober and handler input signals: STARTn, RESTARTn, EOWn and ON_SITE[3..0].

The input signals can generate interruption if it is enabled. The interruption status can be read back and used to see which input signals had been asserted. The interruption clear should be issued once it is enabled and generated; otherwise, no subsequent interruption can be generated.

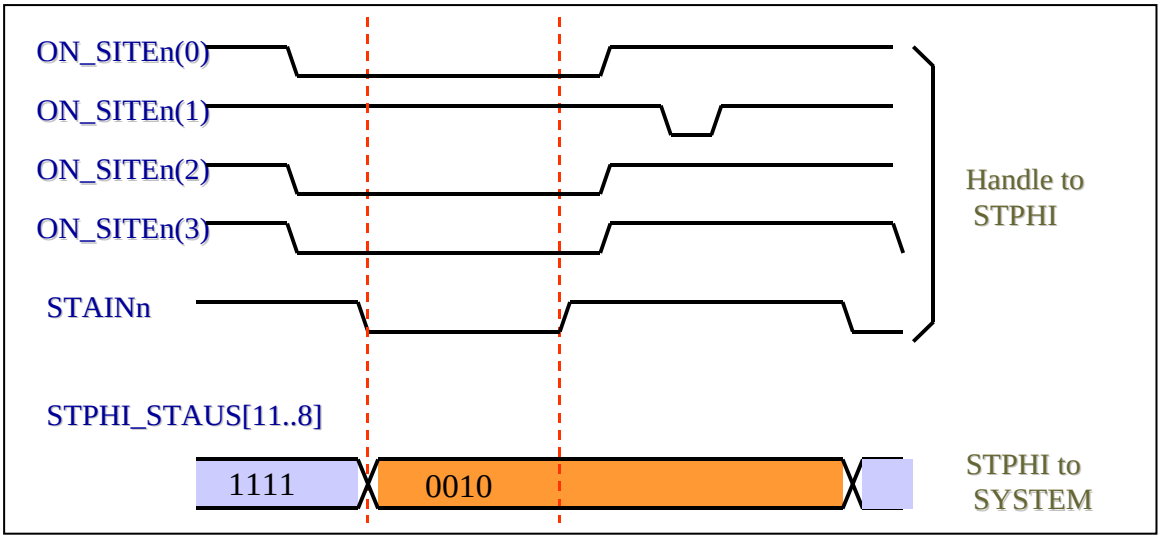


Figure 2-11 Multi-Site Timing Chart

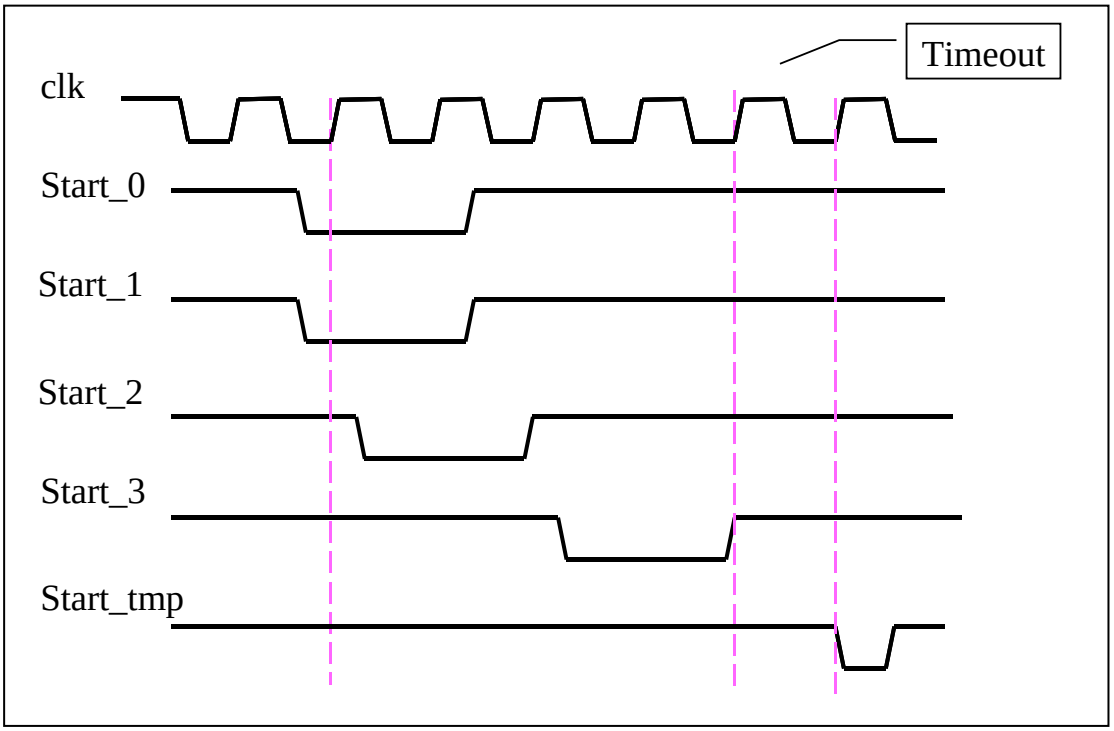


Figure 2-12 Four Start Signals Timing Waveform (1/3)

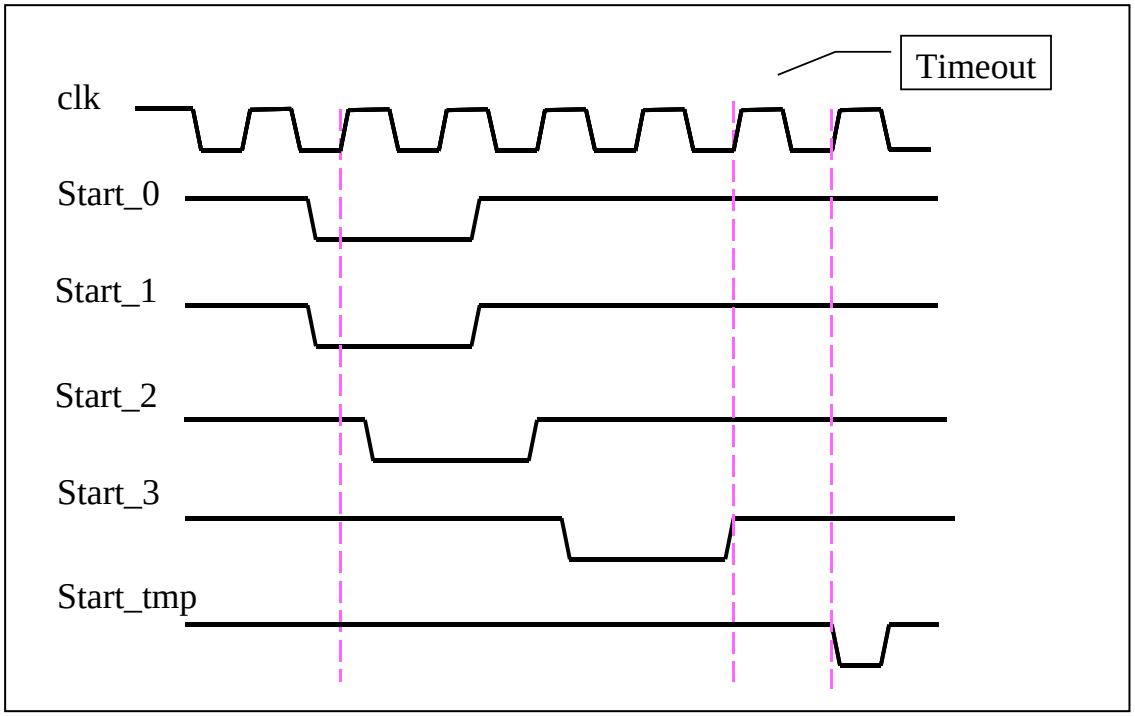


Figure 2-13 Four Start Signals Timing Waveform (2/3)

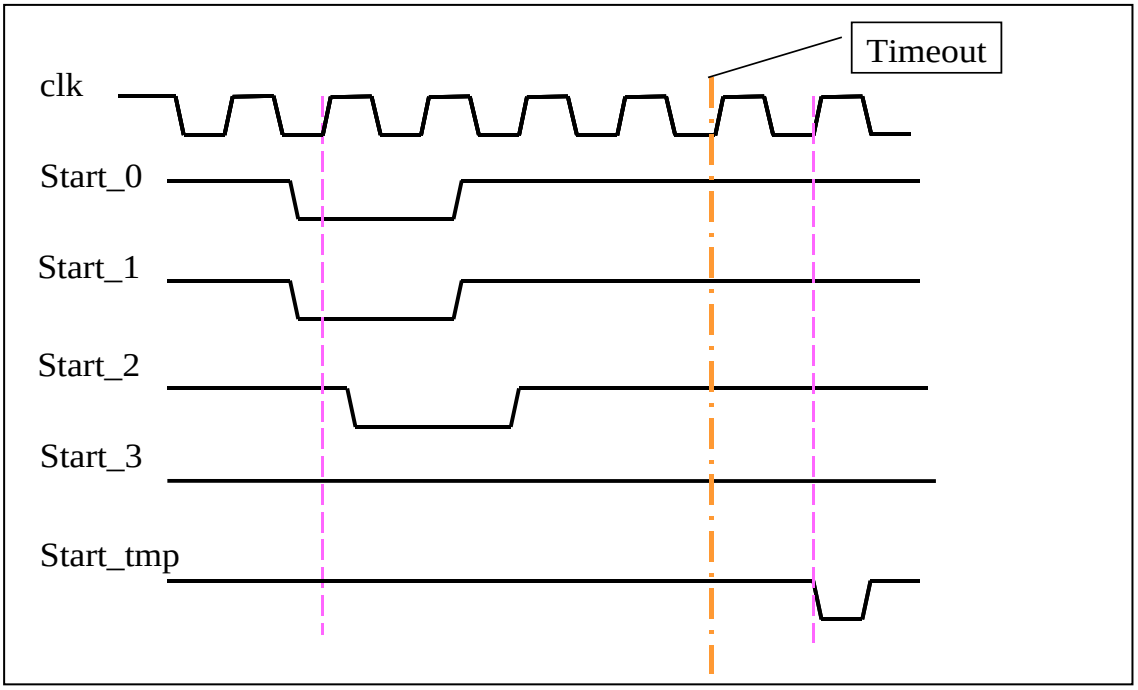


Figure 2-14 Four Start Signals Timing Waveform (3/3)

2.8.4 STPHI Block Diagram

It uses the FPGA (Field-Programmable Gate Arrays IC) as the communication bridge between Computer and Handler, and its main function is to accept the control data sent by the PCI Slot in computer of which is converted to the form Handler can be accepted by internal circuit. It also receives the data from Handler and sends it to computer.

IC 74245 is a data buffer that can supply TTL 5V voltage to Handler and protect the FPGA against damaging by the abnormal input voltage from outside.

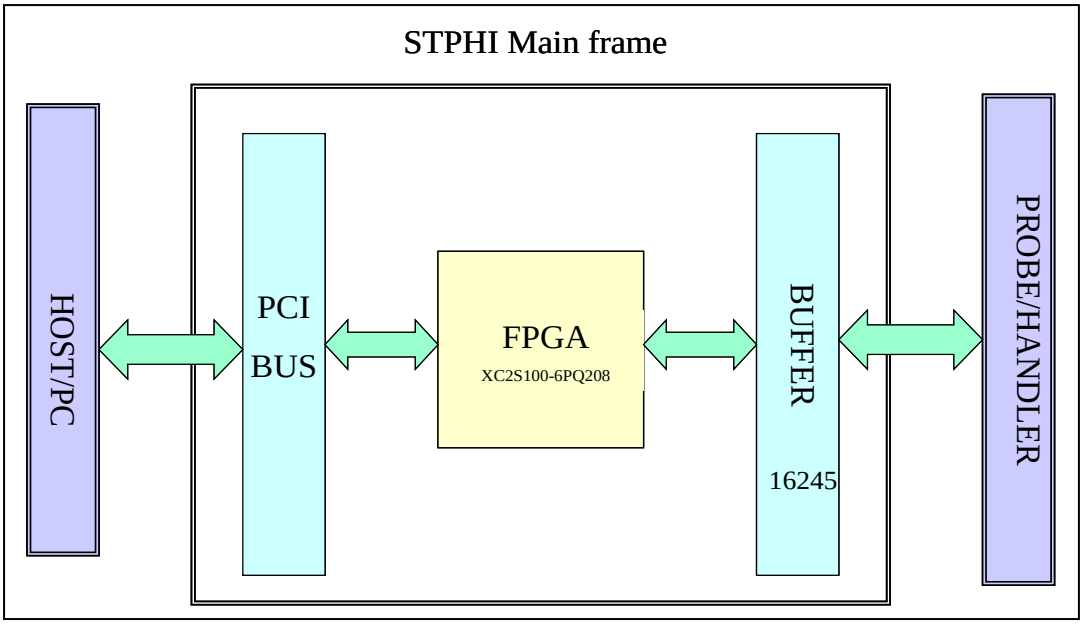
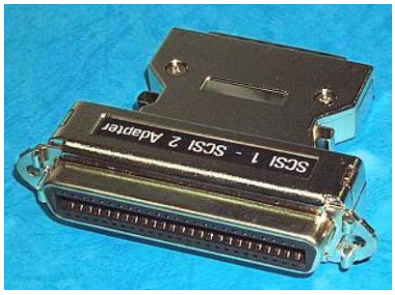


Figure 2-15 STPHI Hardware Block Diagram

2.8.5 Connector Pin Assignment

This prober/handler connector is located on the 3380/3380P computer. The connector can be used for either prober or handler. Pin assignment of the connector is given in the table below.

- **Centronic Connecter (Female)**



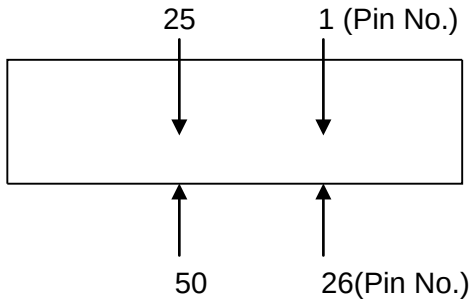


Figure 2-16 Centronic Connector Profile

- **SCSI II D-SUB Connecter**

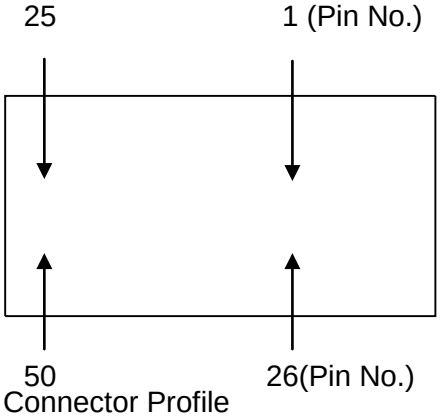


Figure 2-17 SCSI II D-SUB Connector Profile

Table 2-3 Pin Assignment Table

Pin No.	Pin Name	Pin No.	Pin Name
01	GND	26	ATE5V
02	BIN0	27	System Reserved
03	BIN2	28	RESTART
04	BIN4	29	ON_SITE_3/START3
05	BIN6	30	ON_SITE_1/START1
06	BIN8	31	EOT_3
07	BIN10	32	EOT_1
08	BIN12	33	REPROBE
09	BIN14	34	BIN31
10	BIN16	35	BIN29
11	BIN18	36	BIN27
12	BIN20	37	BIN25
13	BIN22	38	BIN23
14	BIN24	39	BIN21
15	BIN26	40	BIN19
16	BIN28	41	BIN17
17	BIN30	42	BIN15
18	STOP	43	BIN13
19	EOT_0	44	BIN11

20	EOT_2	45	BIN9
21	ON_SITE_0/START0	46	BIN7
22	ON_SITE_2/START2	47	BIN5
23	START	48	BIN3
24	EOW	49	BIN1
25	ATE5V	50	GND

2.9 Universal Voltage/Current (MXUVI, Option)

This section describes the MXUVI system from the perspective of programmer.

2.9.1 Specification Summary

Configuration:

Number of channel:	16 channels UVI per board
Number of board in a system:	optional
V range:	2V, 4V, 6V, 12V
I range:	1uA, 10uA, 100uA, 1mA, 10mA,100mA, 1A
Outlet:	Go through pogo pin directly
Measurement Trigger by:	By CPU Trigger
DAC and ADC chip:	16 bits
Clamp:	Programmable

V_RANGE specification

Voltage Range Name	Voltage Output Maximum	Resolution	Accuracy
2V	+/- 2V	75uV	+/- (0.1% + 1.75mV)
4V	+/- 4V	150uV	+/- (0.1% + 3.5mV)
6V	+/- 6V	225uV	+/- (0.1% + 5mV)
12V	+/- 12V	450uV	+/- (0.1% + 10mV)

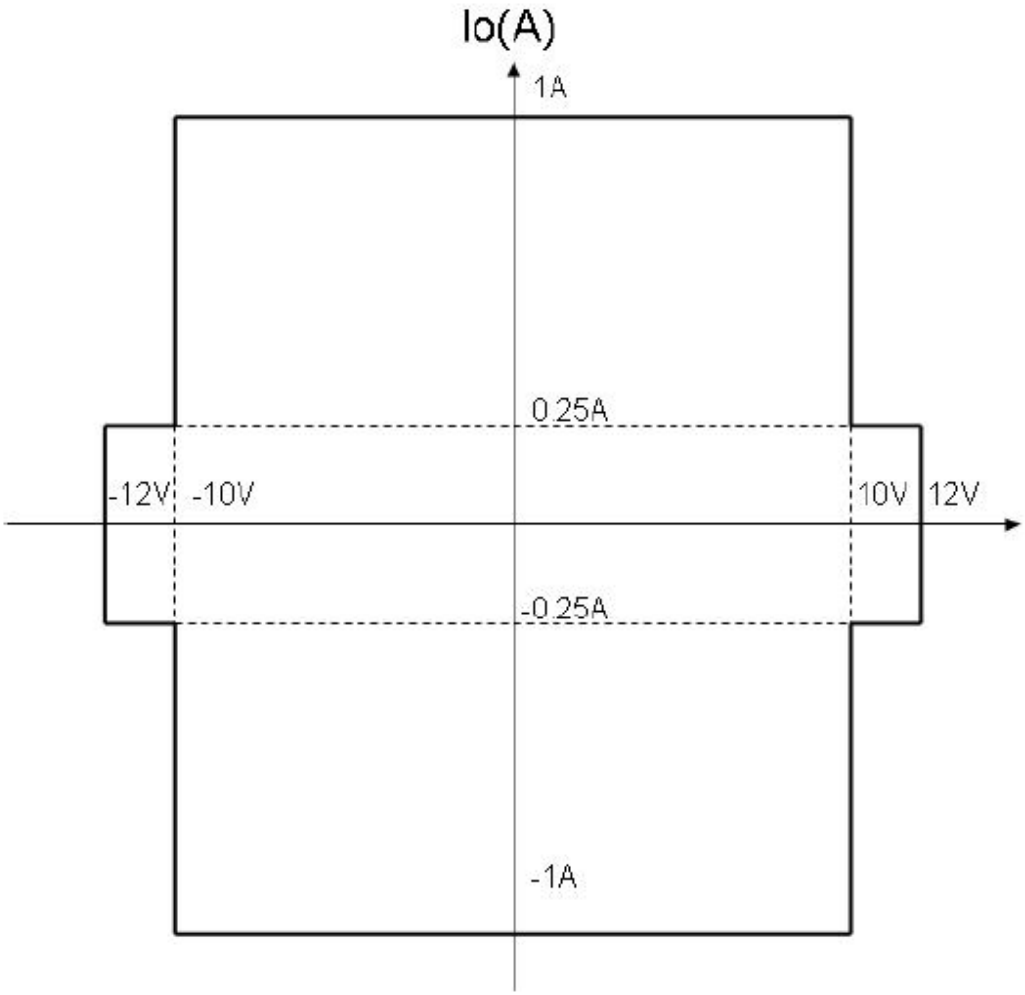
I_RANGE specification

I_Range	Resolution	Accuracy
+/-1uA	40pA	+/- (0.2% + 5nA)
+/- 10uA	400pA	+/- (0.2% + 50nA)
+/- 100uA	4nA	+/- (0.2% + 500nA)
+/- 1mA	40nA	+/- (0.2% + 5uA)
+/- 10mA	400nA	+/- (0.2% + 50uA)
+/- 100mA	4uA	+/- (0.2% + 500uA)
+/- 1A	40uA	+/- (0.2% + 5mA)

Application Notes:

- MXUVI share with the common slot 1~8.
- Provide additional 16 channel of low-voltage.
- Please consult application engineer for system re-configuration.

Operating V/I curve



2.10 Device Power Supply (MLDPS, Option)

This section describes the MLDPS system from the perspective of programmer.

2.10.1 Specification Summary

Configuration:

Number of channel:	32 channels per board
Number of board in a system:	optional
Force V range:	12V,6V(Only 6V support 1A I range)
Measure I range:	5uA, 25uA, 250uA, 2.5mA, 25mA,500mA, 1A
Force I range:	25mA,500mA, 1A
Measure V range:	12V
DAC chip:	16 bits
ADC chip:	18 bits
Outlet:	Go through pogo pin directly

Measurement Trigger by:	By CPU Trigger
Clamp:	Programmable

Force V_RANGE specification

Voltage Range Name	Voltage Output Maximum	Resolution	Accuracy
6V	-6V~+12V	0.39mV	+/-(0.05%+2mV)
12V	-6V~+12V	0.39mV	+/-(0.05%+2mV)

Measure I_RANGE specification

I_Range	Resolution	Accuracy
+/-5uA	38.1pA	+/-(0.1% + 5nA)
+/- 25uA	190pA	+/-(0.1% +25nA)
+/- 250uA	1.9nA	+/-(0.1% + 250nA)
+/- 2.5mA	19uA	+/-(0.1% + 2.5uA)
+/- 25mA	190uA	+/-(0.1% + 25uA)
+/- 500mA	7.62uA	+/-(0.1% +500uA)
+/- 1A	15.24uA	+/-(0.1% +1mA)

Force I_RANGE specification

I_Range	Current Output Maximum	Resolution	Accuracy
25mA	-25.625mA~+25.625mA	782nA	+/-(0.05% + 12.5uA)
500mA	-512.5mA~+512.5mA	31.28uA	+/-(0.05% +1mA)
1A	-1.025A~+1.025A	31.28uA	+/-(0.05% +1mA)

Measure V_RANGE specification

V_Range	Resolution	Accuracy
12V	93.75uV	+/-(0.05%+2mV)

Clamp I_RANGE specification

I_Range	Resolution	Accuracy
+/- 250uA	7.82nA	+10% F.S
+/- 2.5mA	78.2nA	+10% F.S
+/- 25mA	782nA	+10% F.S
+/- 500mA	15.7uA	+10% F.S
+/- 1A	30.14uA	+10% F.S

Clamp V_RANGE specification

V_Range	Resolution	Accuracy
12V	0.39mV	+10% F.S

Gang mode

Gang mode: Maximum channels at gang mode are consecutive 32 channels.

N channels gang (N: Number of channels)

Range	Max current	Resolution	Accuracy
N*500mA	-N*500mA ~ +N*500mA	3.81uA	+/-(0.1% +N*0.5mA)
N*1A	- N*1A ~ + N*1A	7.62uA	+/-(0.1% + N*1mA)

Application Notes:

- MLDPS share with the common slot 0,2,4,6,9.

2.11 MXAWI (ADDA, Option)

This section describes the MXAWI system from the perspective of programmer.

2.11.1 Specification Summary

Feature:

- 4 channel waveform generator, and 4 channel waveform digitizer.
- 50MHz with 16 bits arbitrarily waveform generator.
- Compatible interface on Chroma 3380/3380P series ATE general slot.
- The Chroma 3380/3380P CRAFT software supported on test plan, test pattern, and GUI utilities.
- Fully pattern synchronization trigger working scheme.

WG (waveform generator) Specification:

Resolution	16 bits
Monotonicity	14 bits
Conversion rate	50 MSPS
Waveform memory	256K
Waveform setting time	1uS
Output voltage range:	+/-2.5V on LV(Low Voltage Range) +/-10V on HV(High Voltage Range) (default)
Output voltage accuracy::	0.5 mV on LV(Low Voltage Range) 1.5 mV on HV(High Voltage Range)
Output current	10mA
Output voltage range	+/- 2.5V; +/- 10V(default)
Output mode	Single end or Differential
Output filter	20K , Through
Trigger method	By pattern, 8M pattern memory depth
Waveform offset DAC resolution	16 bits
Offset voltage range	-10.0V ~ +10.0V
Default common mode voltage	0.0V

WD (waveform digitizer) Specification:

Waveform capture ADC resolution	16 bits
Conversion rate	250 KSPS
Capture memory	256K
Input voltage range	+/- 10.0 V; +/- 2.5 V(Default)
Input mode	Single end or Differential
filter	20K, 50K, Through
Trigger method	By pattern, 8M pattern memory depth
Waveform offset DAC resolution	16 bits
Offset voltage range	-10.0V ~ +10.0V

Default common mode voltage	0.0V
Voltage Measurement Accuracy:	1.5 mV on LV(Low Voltage Range) 2.5 mV on HV(High Voltage Range)

Application notes:

- MXAWI share with the common slot.

2.12 338x Pogo Pin Define

This section explains the 3380/3380P all board pogo pin definition.

2.12.1 MXBUS

Left side:

MXBUS PoGo Pin Define

Pogo Pin No	define	define	define	define
	a	b	c	d
1	LBLVDSIN_P0	**DG**	**DG**	**DG**
2	LBLVDSIN_N0	**LBLVDSIN_G0**	**DG**	**DG**
3	LBLVDSIN_P1	**LBLVDSIN_G1**	**DG**	**DG**
4	LBLVDSIN_N1	**DG**	**DG**	**DG**
5	**LB_SCLK**	**LB_nCS**	**LB_DIN**	**nRESET**
6	**UR0**	**UR8**	**UR16**	**UR24**
7	**UR1**	**UR9**	**UR17**	**UR25**
8	**UR2**	**UR10**	**UR18**	**UR26**
9	**UR3**	**UR11**	**UR19**	**UR27**
10	**UR4**	**UR12**	**UR20**	**UR28**
11	**UR5**	**UR13**	**UR21**	**UR29**
12	**UR6**	**UR14**	**UR22**	**UR30**
13	**UR7**	**UR15**	**UR23**	**UR31**
14	**LB_DOUT**			
15	**LB_D5V**	**LB_D5V**	**LB_D5V**	**LB_D5V**
16	**LB_D5V**	**LB_D5V**	**LB_D5V**	**LB_D5V**
17	**LB_D5V**	**LB_D5V**	**LB_D5V**	**LB_D5V**
18				
19				
20				
21				
22				
23				

24				
25				

Right side:

MXBUS PoGo Pin Define				
define	define	define	define	Pogo Pin No
e	f	g	h	
AG	**AG**	**AG**	LBLVDSOUT_P0	1
AG	**AG**	**LBLVDSOUT_G0**	LBLVDSOUT_N0	2
AG	**AG**	**LBLVDSOUT_G0**	LBLVDSOUT_P1	3
AG	**AG**	**AG**	LBLVDSOUT_N1	4
SPI_SCK	**SPI_nCS**	**SPI_DIN**	**SPI_DOUT**	5
UR32	**UR40**	**UR48**	**UR56**	6
UR33	**UR41**	**UR49**	**UR57**	7
UR34	**UR42**	**UR50**	**UR58**	8
UR35	**UR43**	**UR51**	**UR59**	9
UR36	**UR44**	**UR52**	**UR60**	10
UR37	**UR45**	**UR53**	**UR61**	11
UR38	**UR46**	**UR54**	**UR62**	12
UR39	**UR47**	**UR55**	**UR63**	13
				14
	LB_A5V	**LB_A5V**	**LB_A5V**	15
	LB_A5V	**LB_A5V**	**LB_A5V**	16
	LB_A5V	**LB_A5V**	**LB_A5V**	17
				18
				19
				20
				21
				22
				23
				24
				25

2.12.2 MXPG3

Left side:

MXPG3 PoGo Pin Define				
Pogo Pin No	define	define	define	define
	a	b	c	d

1	**NC**	**NC**	**AG**	**AG**
2	**+15V**	NC	**IMH_MEET**	**AG**
3	NC	**NC**	NC	**POGO_0**
4	**+15V**	NC	**SYSFAIL**	**AG**
5	NC	**NC**	NC	**POGO_1**
6	**DGND**	NC	**RATEICLK**	**AG**
7	NC	**NC**	NC	**POGO_2**
8	**DGND**	NC	**RATEOCLK**	**AG**
9	NC	**NC**	NC	**POGO_3**
10	**SYSCLK**	NC	**RPEN**	**AG**
11	NC	**PATEND**	NC	**POGO_4**
12	**IMH_RATE**	NC	**PRINT**	**AG**
13	NC	**N_SPM_CE**	NC	**POGO_5**
14	**BUSY**	NC	**FMEM1_DQ31**	**AG**
15	NC	**LOCKED**	NC	**POGO_6**
16	**SYNC_FT0**	NC	**POGO_26**	**AG**
17	NC	**SQPG**	NC	**POGO_7**
18				
19				
20				
21				
22				
23				
24				
25				

Right side:

MXPG3 PoGo Pin Define

define	define	define	define	Pogo Pin No
e	f	g	h	
AG	**AG**	**NC**	**AG**	1
POGO_8	NC	**NC**	NC	2
AG	**POGO_16**	NC	**-15V**	3
POGO_9	NC	**NC**	NC	4
AG	**POGO_17**	NC	**-15V**	5
POGO_10	NC	**NC**	NC	6
AG	**POGO_18**	NC	**+3.3V**	7
POGO_11	NC	**NC**	NC	8
AG	**POGO_19**	NC	**+3.3V**	9

POGO_12	NC	**NC**	NC	10
AG	**POGO_20**	NC	**FROM_DI**	11
POGO_13	NC	**POGO_24**	NC	12
AG	**POGO_21**	NC	**FROM_DO**	13
POGO_14	NC	**POGO_25**	NC	14
AG	**POGO_22**	NC	**FROM_CLK**	15
POGO_15	NC	**FROM_CS1**	NC	16
AG	**POGO_23**	NC	**FROM_CS0**	17
				18
				19
				20
				21
				22
				23
				24
				25

2.12.3 MXLPC

Left side:

MXLPC PoGo Pin Define				
Pogo Pin No	define	define	define	define
	a	b	c	d
1	**AG**	**AG**	**AG**	**TC**
2	**ch-0**	AG	**ch-1**	**AG**
3	AG	**ch-4**	AG	**ch-5**
4	**ch-8**	AG	**ch-9**	**AG**
5	AG	**ch-12**	AG	**ch-13**
6	**ch-16**	AG	**ch-17**	**AG**
7	AG	**ch-20**	AG	**ch-21**
8	**ch-24**	AG	**ch-25**	**AG**
9	AG	**ch-28**	AG	**ch-29**
10	**ch-32**	AG	**ch-33**	**AG**
11	AG	**ch-36**	AG	**ch-37**
12	**ch-40**	AG	**ch-41**	**AG**
13	AG	**ch-44**	AG	**ch-45**
14	**ch-48**	AG	**ch-49**	**AG**
15	AG	**ch-52**	AG	**ch-53**
16	**ch-56**	AG	**ch-57**	**AG**

17	AG	**ch-60**	AG	**ch-61**
18	64		65	**AG**
19		68		69
20	72		73	**AG**
21		76		77
22	80		81	**AG**
23		84		85
24	88		89	**AG**
25		92		93

Right side:

MXLPC PoGo Pin Define				
define	define	define	define	Pogo Pin No
e	f	g	h	
AG	**AG**	**AG**	**AG**	1
ch-2	AG	**ch3**	AG	2
AG	**ch-6**	AG	**ch-7**	3
ch-10	AG	**ch-11**	AG	4
AG	**ch-14**	AG	**ch-15**	5
ch-18	AG	**ch-19**	AG	6
AG	**ch-22**	AG	**ch-23**	7
ch-26	AG	**ch-27**	AG	8
AG	**ch-30**	AG	**ch-31**	9
ch-34	AG	**ch-35**	AG	10
AG	**ch-38**	AG	**ch-39**	11
ch-42	AG	**ch-43**	AG	12
AG	**ch-46**	AG	**ch-47**	13
ch-50	AG	**ch-51**	AG	14
AG	**ch-54**	AG	**ch-55**	15
ch-58	AG	**ch-59**	AG	16
AG	**ch-62**	AG	**ch-63**	17
66		67		18
AG	70		71	19
74		75		20
AG	78		79	21
82		83		22
AG	86		87	23
90		91		24
AG	94		95	25

2.12.4 MXDPS

Left side:

MXDPS PoGo Pin Define				
Pogo Pin No	define	define	define	define
	a	b	c	d
1	**AG**	**AG**	**AG**	**TC**
2	**DPS-0F+**	DPS-0F+	**DPS-0S+**	**AG**
3	DPS-0F+	**DPS-0F+**	**NC**	**DPS-0S+**
4	**DPS-1F+**	DPS-1F+	**DPS-1S+**	**AG**
5	DPS-1F+	**DPS-1F+**	**NC**	**DPS-1S+**
6	**DPS-2F+**	DPS-2F+	**DPS-2S+**	**AG**
7	DPS-2F+	**DPS-2F+**	**NC**	**DPS-2S+**
8	**DPS-3F+**	DPS-3F+	**DPS-3S+**	**AG**
9	DPS-3F+	**DPS-3F+**	**NC**	**DPS-3S+**
10	**DPS-4F+**	DPS-4F+	**DPS-4S+**	**AG**
11	DPS-4F+	**DPS-4F+**	**NC**	**DPS-4S+**
12	**DPS-5F+**	DPS-5F+	**DPS-5S+**	**AG**
13	DPS-5F+	**DPS-5F+**	**NC**	**DPS-5S+**
14	**DPS-6F+**	DPS-6F+	**DPS-6S+**	**AG**
15	DPS-6F+	**DPS-6F+**	**NC**	**DPS-6S+**
16	**DPS-7F+**	DPS-7F+	**DPS-7S+**	**AG**
17	DPS-7F+	**DPS-7F+**	**NC**	**DPS-7S+**
18				
19				
20				
21				
22				
23				
24				
25				

Right side:

MXDPS PoGo Pin Define				
define	define	define	define	Pogo Pin No
e	f	g	h	
AG	**AG**	**AG**	**AG**	1
DPS-0S-	**NC**	**DPS-0F-**	DPS-0F-	2
AG	**DPS-0S-**	DPS-0F-	**DPS-0F-**	3
DPS-1S-	**NC**	**DPS-1F-**	DPS-1F-	4
AG	**DPS-1S-**	DPS-1F-	**DPS-1F-**	5
DPS-2S-	**NC**	**DPS-2F-**	DPS-2F-	6
AG	**DPS-2S-**	DPS-2F-	**DPS-2F-**	7
DPS-3S-	**NC**	**DPS-3F-**	DPS-3F-	8
AG	**DPS-3S-**	DPS-3F-	**DPS-3F-**	9
DPS-4S-	**NC**	**DPS-4F-**	DPS-4F-	10
AG	**DPS-4S-**	DPS-4F-	**DPS-4F-**	11
DPS-5S-	**NC**	**DPS-5F-**	DPS-5F-	12
AG	**DPS-5S-**	DPS-5F-	**DPS-5F-**	13
DPS-6S-	**NC**	**DPS-6F-**	DPS-6F-	14
AG	**DPS-6S-**	DPS-6F-	**DPS-6F-**	15
DPS-7S-	**NC**	**DPS-7F-**	DPS-7F-	16
AG	**DPS-7S-**	DPS-7F-	**DPS-7F-**	17
				18
				19
				20
				21
				22
				23
				24
				25

2.12.5 MXPMU

Only one pogo pin: Tcom

MXPMU PoGo Pin Define									
Pogo Pin No	define	define	define	define	define	define	define	define	Pogo Pin No
	a	b	c	d	e	f	g	h	
1				**TC**					1
2									2
3									3

4									4
5									5
6									6
7									7
8									8
9									9
10									10
11									11
12									12
13									13
14									14
15									15
16									16
17									17
18									18
19									19
20									20
21									21
22									22
23									23
24									24
25									25

2.12.6 MXREF (Option)

Left side:

MXREF PoGo Pin Define				
Pogo Pin No	define	define	define	define
	a	b	c	d
1	**AG**	**AG**	**AG**	**TC**
2	**REF-0F+**	REF-0F+	**REF-0S+**	**AG**
3	REF-1F+	**REF-1F+**	NC	**REF-1S+**
4	**REF-2F+**	REF-2F+	**REF-2S+**	**AG**
5	REF-3F+	**REF-3F+**	NC	**REF-3S+**
6	**REF-4F+**	REF-4F+	**REF-4S+**	**AG**
7	REF-5F+	**REF-5F+**	NC	**REF-5S+**
8	**REF-6F+**	REF-6F+	**REF-6S+**	**AG**
9	REF-7F+	**REF-7F+**	NC	**REF-7S+**
10	**REF-8F+**	REF-8F+	**REF-8S+**	**AG**

11	REF-9F+	**REF-9F+**	NC	**REF-9S+**
12	**REF-10F+**	REF-10F+	**REF-10S+**	**AG**
13	REF-11F+	**REF-11F+**	NC	**REF-11S+**
14	**REF-12F+**	REF-12F+	**REF-12S+**	**AG**
15	REF-13F+	**REF-13F+**	NC	**REF-13S+**
16	**REF-14F+**	REF-14F+	**REF-14S+**	**AG**
17	REF-15F+	**REF-15F+**	NC	**REF-15S+**
18	64		65	**AG**
19		68		69
20	72		73	**AG**
21		76		77
22	80		81	**AG**
23		84		85
24	88		89	**AG**
25		92		93

Right side:

MXREF PoGo Pin Define

define	define	define	define	Pogo Pin No
e	f	g	h	
AG	**AG**	**AG**	**AG**	1
REF-0S-	NC	**REF-0F-**	REF-0F-	2
AG	**REF-1S-**	REF-1F-	**REF-1F-**	3
REF-2S-	NC	**REF-2F-**	REF-2F-	4
AG	**REF-3S-**	REF-3F-	**REF-3F-**	5
REF-4S-	NC	**REF-4F-**	REF-4F-	6
AG	**REF-5S-**	REF-5F-	**REF-5F-**	7
REF-6S-	NC	**REF-6F-**	REF-6F-	8
AG	**REF-7S-**	REF-7F-	**REF-7F-**	9
REF-8S-	NC	**REF-8F-**	REF-8F-	10
AG	**REF-9S-**	REF-9F-	**REF-9F-**	11
REF-10S-	NC	**REF-10F-**	REF-10F-	12
AG	**REF-11S-**	REF-11F-	**REF-11F-**	13
REF-12S-	NC	**REF-12F-**	REF-12F-	14
AG	**REF-13S-**	REF-13F-	**REF-13F-**	15
REF-14S-	NC	**REF-14F-**	REF-14F-	16
AG	**REF-15S-**	REF-15F-	**REF-15F-**	17
66		67		18
AG	70		71	19

74		75		20
AG	78		79	21
82		83		22
AG	86		87	23
90		91		24
AG	94		95	25

2.12.7 MXUVI (Option)

Left side:

MXUVI PoGo Pin Define				
Pogo Pin No	define	define	define	define
	a	b	c	d
1	**AG**	**AG**	**AG**	**TC**
2	**UVI-0F+**	UVI-0F+	**UVI-0S+**	**AG**
3	UVI-1F+	**UVI-1F+**	NC	**UVI-1S+**
4	**UVI-2F+**	UVI-2F+	**UVI-2S+**	**AG**
5	UVI-3F+	**UVI-3F+**	NC	**UVI-3S+**
6	**UVI-4F+**	UVI-4F+	**UVI-4S+**	**AG**
7	UVI-5F+	**UVI-5F+**	NC	**UVI-5S+**
8	**UVI-6F+**	UVI-6F+	**UVI-6S+**	**AG**
9	UVI-7F+	**UVI-7F+**	NC	**UVI-7S+**
10	**UVI-8F+**	UVI-8F+	**UVI-8S+**	**AG**
11	UVI-9F+	**UVI-9F+**	NC	**UVI-9S+**
12	**UVI-10F+**	UVI-10F+	**UVI-10S+**	**AG**
13	UVI-11F+	**UVI-11F+**	NC	**UVI-11S+**
14	**UVI-12F+**	UVI-12F+	**UVI-12S+**	**AG**
15	UVI-13F+	**UVI-13F+**	NC	**UVI-13S+**
16	**UVI-14F+**	UVI-14F+	**UVI-14S+**	**AG**
17	UVI-15F+	**UVI-15F+**	NC	**UVI-15S+**
18	64		65	**AG**
19		68		69
20	72		73	**AG**
21		76		77
22	80		81	**AG**
23		84		85
24	88		89	**AG**
25		92		93

Right side:

MXUVI PoGo Pin Define				
define	define	define	define	Pogo Pin No
e	f	g	h	
AG	**AG**	**AG**	**AG**	1
UVI-0S-	NC	**UVI-0F-**	UVI-0F-	2
AG	**UVI-1S-**	UVI-1F-	**UVI-1F-**	3
UVI-2S-	NC	**UVI-2F-**	UVI-2F-	4
AG	**UVI-3S-**	UVI-3F-	**UVI-3F-**	5
UVI-4S-	NC	**UVI-4F-**	UVI-4F-	6
AG	**UVI-5S-**	UVI-5F-	**UVI-5F-**	7
UVI-6S-	NC	**UVI-6F-**	UVI-6F-	8
AG	**UVI-7S-**	UVI-7F-	**UVI-7F-**	9
UVI-8S-	NC	**UVI-8F-**	UVI-8F-	10
AG	**UVI-9S-**	UVI-9F-	**UVI-9F-**	11
UVI-10S-	NC	**UVI-10F-**	UVI-10F-	12
AG	**UVI-11S-**	UVI-11F-	**UVI-11F-**	13
UVI-12S-	NC	**UVI-12F-**	UVI-12F-	14
AG	**UVI-13S-**	UVI-13F-	**UVI-13F-**	15
UVI-14S-	NC	**UVI-14F-**	UVI-14F-	16
AG	**UVI-15S-**	UVI-15F-	**UVI-15F-**	17
66		67		18
AG	70		71	19
74		75		20
AG	78		79	21
82		83		22
AG	86		87	23
90		91		24
AG	94		95	25

2.12.8 MLDPS (Option)

Left side:

Pogo Pin No	define	define	define	define
	a	b	c	d
1	**AG**	**AG**	**AG**	**TC**
2	**0F+**	1F+	**0S+**	**AG**
3	2F+	**3F+**	2S+	**3S+**
4	**4F+**	5F+	**4S+**	**AG**

5	6F+	**7F+**	6S+	**7S+**
6	**8F+**	9F+	**8S+**	**AG**
7	10F+	**11F+**	10S+	**11S+**
8	**12F+**	13F+	**12S+**	**AG**
9	14F+	**15F+**	14S+	**15S+**
10	**16F+**	17F+	**16S+**	**AG**
11	18F+	**19F+**	18S+	**19S+**
12	**20F+**	21F+	**20S+**	**AG**
13	22F+	**23F+**	22S+	**23S+**
14	**24F+**	25F+	**24S+**	**AG**
15	26F+	**27F+**	26S+	**27S+**
16	**28F+**	29F+	**28S+**	**AG**
17	30F+	**31F+**	30S+	**31S+**
18				
19				
20				
21				
22				
23				
24				
25				

Right side:

define	define	define	define	Pogo Pin No
e	f	g	h	
AG	**AG**	**AG**	**AG**	1
0/1 S-	1S+	**1F-**	0F-	2
AG	**2/3 S-**	3F-	**2F-**	3
4/5 S-	5S+	**5F-**	4F-	4
AG	**6/7 S-**	7F-	**6F-**	5
8/9 S-	9S+	**9F-**	8F-	6
AG	**10/11 S-**	11F-	**10F-**	7
12/13 S-	13S+	**13F-**	12F-	8
AG	**14/15 S-**	15F-	**14F-**	9
16/17 S-	17S+	**17F-**	16F-	10
AG	**18/19 S-**	19F-	**18F-**	11
20/21 S-	21S+	**21F-**	20F-	12
AG	**22/23 S-**	23F-	**22F-**	13
24/25 S-	25S+	**25F-**	24F-	14
AG	**26/27 S-**	27F-	**26F-**	15
28/29 S-	29S+	**29F-**	28F-	16
AG	**30/31 S-**	31F-	**30F-**	17

				18
				19
				20
				21
				22
				23
				24
				25

2.12.9 MXAWI (Option)

Left side:

MXAWI PoGo Pin Define				
Pogo Pin No	define	define	define	define
	a	b	c	d
1	**AG**	**AG**	**AG**	**TC**
2	WD0+	AG	WD0-	AG
3	AG	NC	AG	NC
4	WD2+	AG	WD2-	AG
5	AG	NC	AG	NC
6	WD4+	AG	WD4-	AG
7	AG	NC	AG	NC
8	WD6+	AG	WD6-	AG
9	AG	NC	AG	NC
10	WG8_F+	AG	WG8_F-	AG
11	AG	NC	AG	NC
12	WG10_F+	AG	WG10_F-	AG
13	AG	NC	AG	NC
14	WG12_F+	AG	WG12_F-	AG
15	AG	NC	AG	NC
16	WG14_F+	AG	WG14_F-	AG
17	AG	NC	AG	NC
18				
19				
20				
21				
22				
23				
24				
25				

Right side:

MXAWI PoGo Pin Define				
define	define	define	define	Pogo Pin No
e	f	g	h	
AG	**AG**	**AG**	**AG**	1
NC	AG	NC	NC	2
AG	External Trigger0	NC	NC	3
NC	AG	NC	NC	4
AG	External Trigger2	NC	NC	5
NC	AG	NC	NC	6
AG	External Trigger4	NC	NC	7
NC	AG	NC	NC	8
AG	External Trigger6	NC	NC	9
AGS8	AG	NC	NC	10
AG	External Trigger8	NC	NC	11
AGS10	AG	NC	NC	12
AG	External Trigger10	NC	NC	13
AGS12	AG	NC	NC	14
AG	External Trigger12	NC	NC	15
AGS14	AG	NC	NC	16
AG	External Trigger14	NC	NC	17
				18
				19
				20
				21
				22
				23
				24
				25

2.12.10 3380P CM LB: 3M 64Pin Connector

2.12.10.1 URC SLOT

UR0~31, 64pin connector

URC0	**1**	**33**	**URC16**
URC1	**2**	**34**	**URC17**
URC2	**3**	**35**	**URC18**

URC3	4	36	URC19
URC4	5	37	URC20
URC5	6	38	URC21
URC6	7	39	URC22
URC7	8	40	URC23
URC8	9	41	URC24
URC9	10	42	URC25
URC10	11	43	URC26
URC11	12	44	URC27
URC12	13	45	URC28
URC13	14	46	URC29
URC14	15	47	URC30
URC15	16	48	URC31
	17	49	
5V	18	50	5V
	19	51	
15V	20	52	15V
	21	53	
-15V	22	54	-15V
	23	55	
R_5V	24	56	R_5V
R_5V	25	57	R_5V
R_5V	26	58	R_5V
R_5V	27	59	R_5V
	28	60	
G	29	61	G
G	30	62	G
G	31	63	G
G	32	64	G

UR32~63, 34pin connector

UR32	1	18	UR48
UR33	2	19	UR49
UR34	3	20	UR50
UR35	4	21	UR51
UR36	5	22	UR52
UR37	6	23	UR53
UR38	7	24	UR54
UR39	8	25	UR55
UR40	9	26	UR56
UR41	10	27	UR57
UR42	11	28	UR58
UR43	12	29	UR59
UR44	13	30	UR60
UR45	14	31	UR61
UR46	15	32	UR62

UR47	16	33	UR63
	17	34	

2.12.10.2 IO SLOT

p0	1	33	IO-TC
p1	2	34	IO-TC
p2	3	35	G
p3	4	36	G
p4	5	37	G
p5	6	38	G
p6	7	39	G
p7	8	40	G
p8	9	41	G
p9	10	42	G
p10	11	43	G
p11	12	44	G
p12	13	45	G
p13	14	46	G
p14	15	47	G
p15	16	48	G
p16	17	49	G
p17	18	50	G
p18	19	51	G
p19	20	52	G
p20	21	53	G
p21	22	54	G
p22	23	55	G
p23	24	56	G
p24	25	57	G
p25	26	58	G
p26	27	59	G
p27	28	60	G
p28	29	61	G
p29	30	62	G
p30	31	63	G
p31	32	64	G

p32	1	33	IO-TC
p33	2	34	G
p34	3	35	G
p35	4	36	G
p36	5	37	G
p37	6	38	G
p38	7	39	G

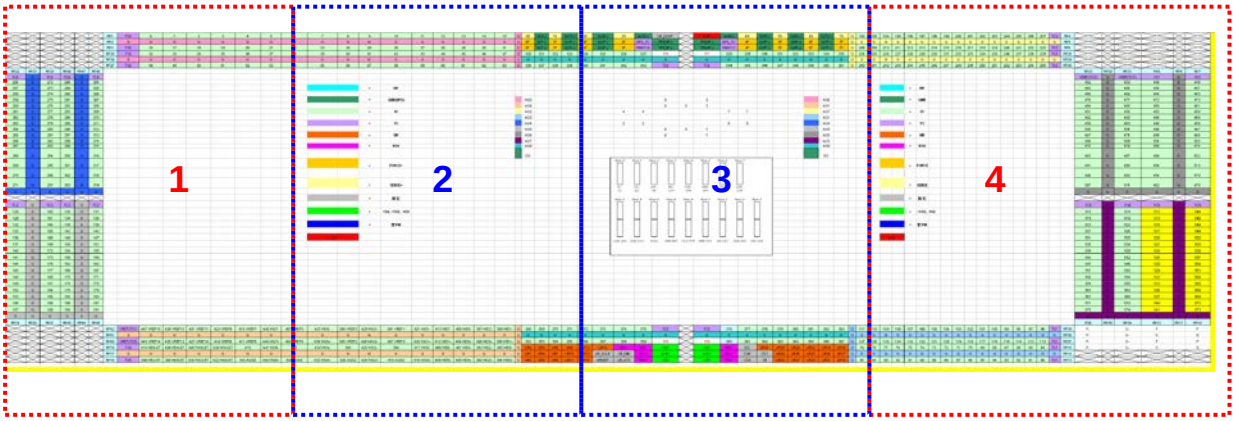
p39	8	40	G
p40	9	41	G
p41	10	42	G
p42	11	43	G
p43	12	44	G
p44	13	45	G
p45	14	46	G
p46	15	47	G
p47	16	48	G
p48	17	49	G
p49	18	50	G
p50	19	51	G
p51	20	52	G
p52	21	53	G
p53	22	54	G
p54	23	55	G
p55	24	56	G
p56	25	57	G
p57	26	58	G
p58	27	59	G
p59	28	60	G
p60	29	61	G
p61	30	62	G
p62	31	63	G
p63	32	64	G

2.12.10.3 POWER SLOT

TC_DPS	1	33	TC_DPS
DPS0F	2	34	DPS0F
DPS0S-	3	35	DPS0S
DPS1F	4	36	DPS1F
DPS1S-	5	37	DPS1S
G	6	38	G
DPS2F	7	39	DPS2F
DPS2S-	8	40	DPS2S
DPS3F	9	41	DPS3F
DPS3S-	10	42	DPS3S
G	11	43	G
DPS4F	12	44	DPS4F
DPS4S-	13	45	DPS4S
DPS5F	14	46	DPS5F

DPS5S-	15	47	DPS5S
G	16	48	G
DPS6F	17	49	DPS6F
DPS6S-	18	50	DPS6S
DPS7F	19	51	DPS7F
DPS7S-	20	52	DPS7S
G	21	53	G
SROM_CS	22	54	SROM_D0
SROM_CLK	23	55	SROM_D1
TP0	24	56	LB_DOUT
TP1	25	57	3.3V
TP2	26	58	PCROM_CS1
TP3	27	59	LB_nCS
TP4	28	60	nRESET
TP5	29	61	LB_DIN
TP6	30	62	LB_SCLK
TC_PMU0	31	63	TC_PMU0
TC_PMU1	32	64	TC_PMU1

2.12.11 3380P FT Ring Tower LB: Pin Define



3380P FT Ring Tower LB part of **1** (left)

RP1	TC0	0	1	2	3	4	5	6
RP2	G	G	G	G	G	G	G	G
RP3	TC0	16	17	18	19	20	21	22
RP25	TC0	32	33	34	35	36	37	38
RP26	G	G	G	G	G	G	G	G
RP27	TC0	48	49	50	51	52	53	54

RP22	RP23	RP24	RP46	RP47	RP48
TC4	G	TC4	TC4	G	TC4
256	G	272	288	G	304
257	G	273	289	G	305
258	G	274	290	G	306
259	G	275	291	G	307
260	G	276	292	G	308
261	G	277	293	G	309
262	G	278	294	G	310
263	G	279	295	G	311
264	G	280	296	G	312
265	G	281	297	G	313
266	G	282	298	G	314
267	G	283	299	G	315
268	G	284	300	G	316
269	G	285	301	G	317
270	G	286	302	G	318
271	G	287	303	G	319
G	G	G	G	G	G
TC2	G	TC2	TC2	G	TC2
128	G	160	130	G	131
129	G	161	134	G	135
132	G	164	138	G	139
133	G	165	142	G	143
136	G	168	146	G	147
137	G	169	150	G	151
140	G	172	154	G	155
141	G	173	158	G	159
144	G	176	162	G	163
145	G	177	166	G	167
148	G	180	170	G	171
149	G	181	174	G	175
152	G	184	178	G	179
153	G	185	182	G	183
156	G	188	186	G	187
157	G	189	190	G	191

G	G	G	G	G	G										
RP19	RP20	RP21	RP43	RP44	RP45										
						RP42	VREF (TC1)	447 VREF15	439 VREF13	431 VREF11	423 VREF9	415 VREF7	445 WG7-	407 VREF5
						RP41	G	G	G	G	G	G	G	G
						RP40	VREF (TC0)	443 VREF14	435 VREF12	427 VREF10	419 VREF8	411 VREF6	444 WG7+	403 VREF4
						RP18	TC6	414 WD6-ET	406 WD4-ET	446 WG6-ET	438 WG4-ET	410	441 WG6-	402
						RP17	G	G	G	G	G	G	G	G
						RP16	TC6	398 WD2-ET	390 WD0-ET	430 WG2-ET	422 WG0-ET	442 AGS6	440 WG6+	434 AGS4

3380P FT Ring Tower LB part of **2** (middle-left)

7	8	9	10	11	12	13	14	15	G	0S	G(S-)	1S	G(1S-)	2S	G(2S-)
G	G	G	G	G	G	G	G	G	G	0F	G(F-)	1F	G(1F-)	2F	G(2F-)
23	24	25	26	27	28	29	30	31	G	0F	G(F-)	1F	G(1F-)	2F	G(2F-)
39	40	41	42	43	44	45	46	47	G	320	321	322	323	324	325
G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
55	56	57	58	59	60	61	62	63	G	336	337	338	339	340	341

= **RP**

= **GND(DPS)**

= **IO**

= **TC**

= **UR**

= **R5V**

= **FORCE+**

= **SENSE+**

= **Others**

= **+5V, +15V, -15V**

= **Null PIN**

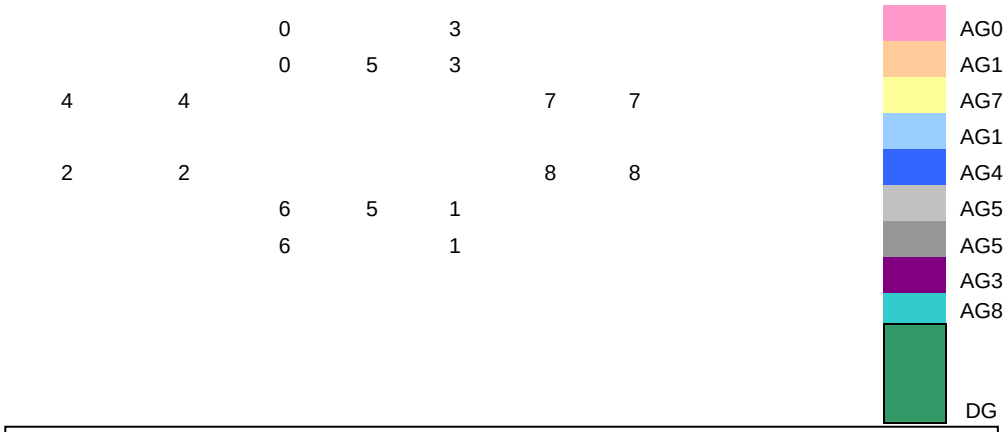
3.3V

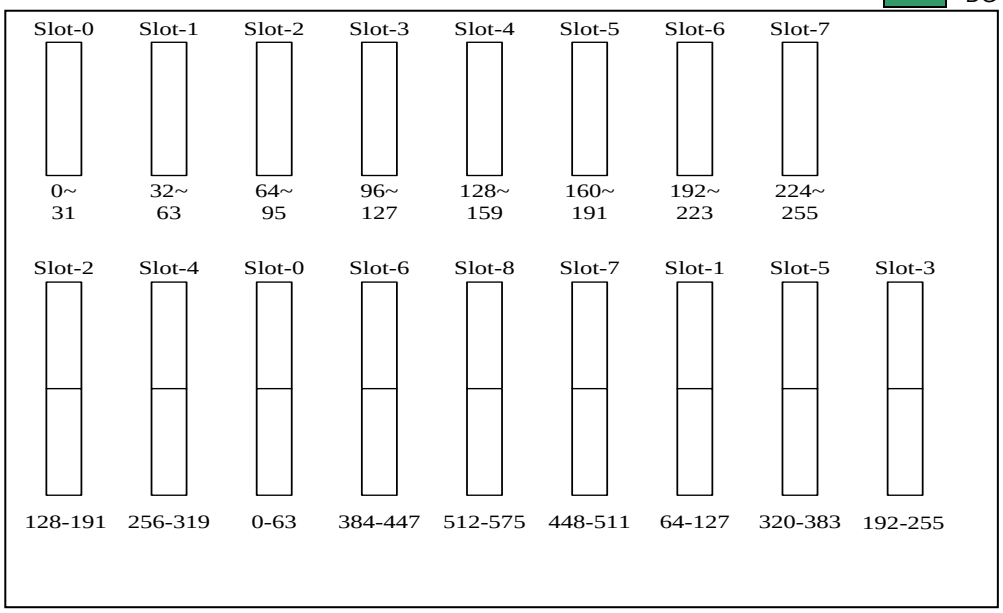
AG0
AG6
AG2
AG3
AG4
AG5
AG6
AG7
AG8
DG

437 WG5-	399 VREF3	429 WG3-	391 VREF1	421 WG1-	413 WD7-	405 WD5-	397 WD3-	389 WD1-	G	368	369	370	371	372	373
G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
436 WG5+	395 VREF2	428 WG3+	387 VREF0	420 WG1+	412 WD7+	404 WD5+	396 WD3+	388 WD1+	G	352	353	354	355	356	357
433 WG4-	394	425 WG2-	386	417 WG0-	409 WD6-	401 WD4-	393 WD2-	385 WD0-	G	UR0	UR3	UR6	UR9	UR12	UR15
G	G	G	G	G	G	G	G	G	G	UR1	UR4	UR7	UR10	UR13	LB_SCLK
432 WG4+	426 AGS2	424 WG2+	418 AGS0	416 WG0+	408 WD6+	400 WD4+	392 WD2+	384 WD0+	G	UR2	UR5	UR8	UR11	UR14	nRESET

3380P FT Ring Tower LB part of **3** (middle-right)

3S	G(3S-)	LB_DOUT		3.3V	G(4S-)	4S	G(5S-)	5S	G(6S-)	6S	G(7S-)	7S	G	192	193
3F	DPS_TC	TP2(3F-)		TP5(4F-)	DPS_TC	4F	G(5F-)	5F	G(6F-)	6F	G(7F-)	7F	G	G	G
3F	PMUTC0	TP3(3F-)		TP4(4F-)	PMUTC1	4F	G(5F-)	5F	G(6F-)	6F	G(7F-)	7F	G	208	209
326	327	TP6		TP7	328	329	330	331	332	333	334	335	G	224	225
G	G	G		G	G	G	G	G	G	G	G	G	G	G	G
342	343	TC5		TC5	344	345	346	347	348	349	350	351	G	240	241





374	375	TC5		TC5	376	377	378	379	380	381	382	383	G	111	110
G	G	G		G	G	G	G	G	G	G	G	G	G	G	G
358	359	TP8		TP9	360	361	362	363	364	365	366	367	G	127	126
R5V	R5V	+5V		+5V	R5V	DO	UR31	UR28	UR25	UR22	UR19	UR16	G	79	78
LB_DIN	R5V	+15V		+15V	R5V	CLK	CS1	UR29	UR26	UR23	UR20	UR17	G	G	G
LB_nCS	R5V	-15V		-15V	R5V	CS0	DI	UR30	UR27	UR24	UR21	UR18	G	95	94

3380P FT Ring Tower LB part of **4** (right)

194	195	196	197	198	199	200	201	202	203	204	205	206	207	TC3	RP4
G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	RP5
210	211	212	213	214	215	216	217	218	219	220	221	222	223	TC3	RP6
226	227	228	229	230	231	232	233	234	235	236	237	238	239	TC3	RP28
G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	RP29
242	243	244	245	246	247	248	249	250	251	252	253	254	255	TC3	RP30

RP33	RP32	RP31	RP9	RP8	RP7
VREF (TC7)	G	VREF (TC7)	TC7	G	TC7
452	G	453	448	G	449
460	G	461	456	G	457
468	G	469	464	G	465
476	G	477	472	G	473
484	G	485	480	G	481
451	G	455	482	G	450
492	G	493	488	G	489
459	G	463	490	G	458
500	G	501	496	G	497
467	G	471	498	G	466
508	G	509	504	G	505
475	G	479	506	G	474
483	G	487	486	G	502
491	G	495	494	G	510
499	G	503	454	G	470
507	G	511	462	G	478
G	G	G	G	G	G
TC8	G	TC8	TC8	G	TC8
515	G	514	512	G	544
519	G	518	513	G	545
523	G	522	516	G	548
527	G	526	517	G	549
531	G	530	520	G	552
535	G	534	521	G	553

= **RP**

= **GND**

= **IO**

= **TC**

= **UR**

= **R5V**

= **FORCE**

= **SENSE**

= **Others**

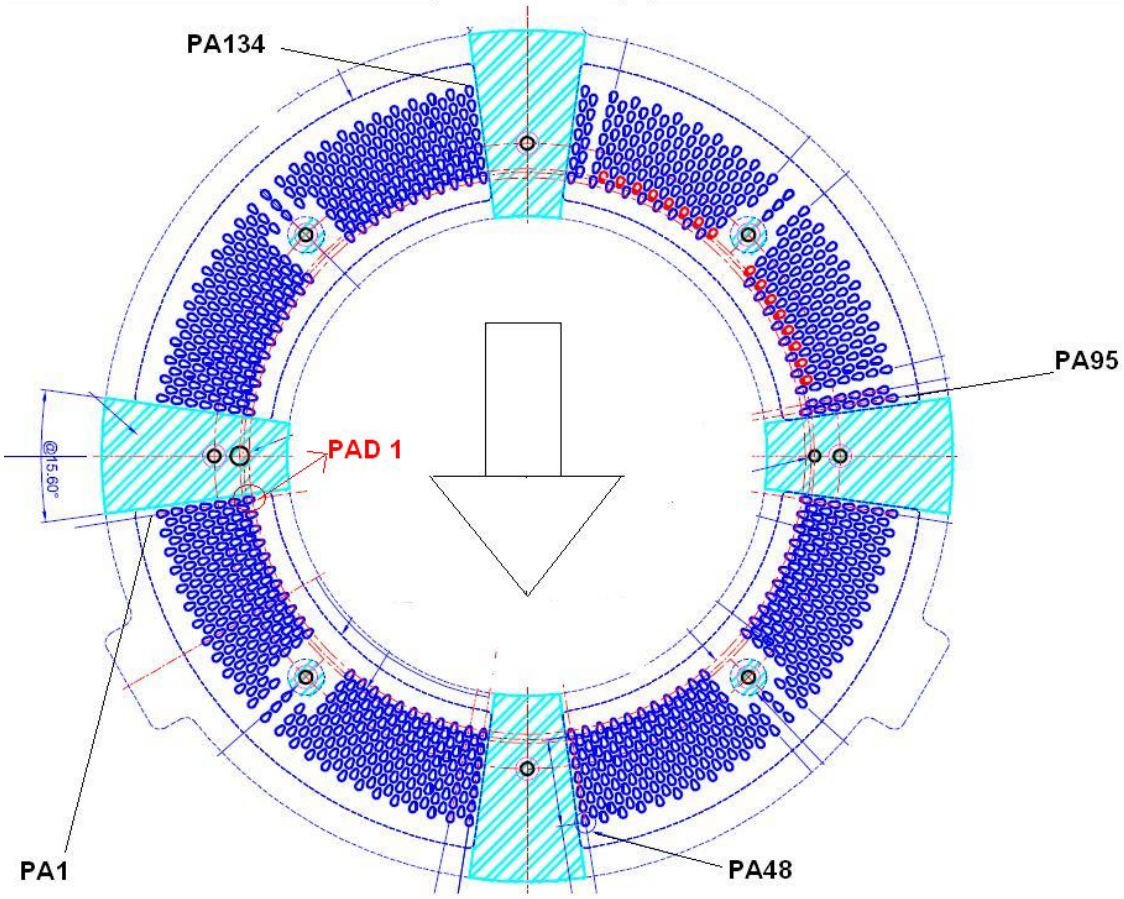
= **+5V, +15V, -15V**

= **Null PIN**

3.3V

																539	G	538	524	G	556
																543	G	542	525	G	557
																547	G	546	528	G	560
																551	G	550	529	G	561
																555	G	554	532	G	564
																559	G	558	533	G	565
																563	G	562	536	G	568
																567	G	566	537	G	569
																571	G	570	540	G	572
																575	G	574	541	G	573
																G	G	G	G	G	G
																R36	RP35	RP34	RP12	RP11	RP10
109	108	107	106	105	104	103	102	101	100	99	98	97	96	TC1	RP39	F-		S-	F		F
G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	RP38	F-		S-	S		S
125	124	123	122	121	120	119	118	117	116	115	114	113	112	TC1	RP37	F-		S-	F		F
77	76	75	74	73	72	71	70	69	68	67	66	65	64	TC1	RP15	F-		S-	S		S
G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	RP14						
93	92	91	90	89	88	87	86	85	84	83	82	81	80	TC1	RP13						

2.12.12 3380P CP Ring Tower LB: Pin Define



		1	2	3	4	5	6	7		X: NO PAD	
PA1		9F20	9S20	NC	6F24	6S24	6F24	NC			
PA2		P291	AG4	P290	P289	AG4	P288	X			Slot9
PA3		P295	GND	P294	P293	GND	P292	6F27			SLot6
PA4		P299	AG4	P298	P297	AG4	P296	X			
PA5		P303	AG4	P302	P301	AG4	P300	6S27			
PA6		P307	AG4	P306	P305	AG4	P304	X			
PA7		P311	AG4	P310	P309	AG4	P308	6F27			
PA8		P315	GND	P314	P313	GND	P312	X			
PA9		P319	AG4	P318	P317	AG4	P316	TC4			
PA10		P131	AG2	P130	P129	AG2	P128	X			
PA11		P135	GND	P134	P133	GND	P132	SROM_CLK			
PA12		P139	AG2	P138	P137	AG2	P136	X			
PA13		P143	AG2	P142	P141	AG2	P140	SROM_DO			
PA14		P147	AG2	P146	P145	AG2	P144	X			
PA15		P151	AG2	P150	P149	AG2	P148	SROM_DI			
PA16		P155	GND	P154	P153	GND	P152	X			
PA17		P159	AG2	P158	P157	AG2	P156	TC2			
PA18		6S18	GND	6F18	6S17	GND	6F17	X			
PA19		6S22	GND	6F22	6S21	GND	6F21	PCROM_CS1			
PA20		6S26	GND	6F26	6S25	GND	6F25	X			
PA21		6S30	GND	6F30	6S29	GND	6F29	TC_PMU0			
PA22		-15	+15	X	X	X	X	X			
PA23		UR2	UR1	UR0	X	X	X	X			
PA24		UR5	UR4	UR3	X	X	X	X			
PA25		RLY_5V	UR7	UR6	X	X	X	X			
PA26		+5V	NC	X	X	X	X	X			
PA27		NC	GND	NC	NC	GND	NC	NC			
PA28		NC	GND	NC	NC	GND	NC	X			
PA29		NC	GND	NC	NC	GND	NC	LB_Ncs			
PA30		NC	GND	NC	NC	GND	NC	X			
PA31		P547	AG8	P546	P545	AG8	P544	TC8			
PA32		P551	AG8	P550	P549	AG8	P548	X			
PA33		P555	GND	P554	P553	GND	P552	nreset			
PA34		P559	AG8	P558	P557	AG8	P556	X			
PA35		P563	AG8	P562	P561	AG8	P560	LB_DIN			
PA36		P567	AG8	P566	P565	AG8	P564	X			
PA37		P571	GND	P570	P569	GND	P568	LB_SCLK			
PA38		P575	AG8	P574	P573	AG8	P572	X			
PA39		P99	AG1	P98	P97	AG1	P96	TC1			
PA40		P103	GND	P102	P101	GND	P100	X			
PA41		P107	AG1	P106	P105	AG1	P104	6F28			
PA42		P111	AG1	P110	P109	AG1	P108	X			
PA43		P115	AG1	P114	P113	AG1	P112	6S28			
PA44		P119	AG1	P118	P117	AG1	P116	X			
PA45		P123	GND	P122	P121	GND	P120	6F28			
PA46		P127	AG1	P126	P125	AG1	P124	X			
PA47		9F16	9S16		6F31	6S31	6F31				

1											
2		1	2	3	4	5	6	7		X: NO PAD	
3	PA48	9F12	9S12	NC	6F0	6S0	6F0	NC			
5	PA49	P355	AG5	P354	P353	AG5	P352	X			Slot9
6	PA50	P359	GND	P358	P357	GND	P356	6F3			SLot6
7	PA51	P363	AG5	P362	P361	AG5	P360	X			
8	PA52	P367	AG5	P366	P365	AG5	P364	6S3			
9	PA53	P371	AG5	P370	P369	AG5	P368	X			
10	PA54	P375	AG5	P374	P373	AG5	P372	6F3			
11	PA55	P379	GND	P378	P377	GND	P376	X			
12	PA56	P383	AG5	P382	P381	AG5	P380	TC5			
14	PA57	P227	AG3	P226	P225	AG3	P224	X			
15	PA58	P231	GND	P230	P229	GND	P228	+3.3			
16	PA59	P235	AG3	P234	P233	AG3	P232	X			
17	PA60	P239	AG3	P238	P237	AG3	P236	TP6			
18	PA61	P243	AG3	P242	P241	AG3	P240	X			
19	PA62	P247	AG3	P246	P245	AG3	P244	TP7			
20	PA63	P251	GND	P250	P249	GND	P248	X			
21	PA64	P255	AG3	P254	P253	AG3	P252	TC3			
23	PA65	9S13	GND	9F13	9S17	GND	9F17	X			
24	PA66	9S9	GND	9F9	9S21	GND	9F21	6S-0			
25	PA67	9S5	GND	9F5	9S25	GND	9F25	X			
26	PA68	9S1	GND	9F1	9S29	GND	9F29	9S-1			
27	PA69	-15V	+15V	X	X	X	X	X			
28	PA70	UR10	UR9	UR8	X	X	X	X			
29	PA71	UR13	UR12	UR11	X	X	X	X			
30	PA72	RLY_5V	UR15	UR14	X	X	X	X			
31	PA73	+5V	NC	X	X	X	X	X			
32	PA74	9S14	GND	9F14	9S11	GND	9F11	TC-PMU1			
33	PA75	9S15	GND	9F15	9S10	GND	9F10	X			
34	PA76	9S3	GND	9F3	9S7	GND	9F7	9S-0			
35	PA77	9S2	GND	9F2	9S6	GND	9F6	X			
37	PA78	P483	AG7	P482	P481	AG7	P480	TC7			
38	PA79	P487	GND	P486	P485	GND	P484	X			
39	PA80	P491	AG7	P490	P489	AG7	P488	PREF-TC1			
40	PA81	P495	AG7	P494	P493	AG7	P492	X			
41	PA82	P499	AG7	P498	P497	AG7	P496				
42	PA83	P503	AG7	P502	P501	AG7	P500	X			
43	PA84	P507	GND	P506	P505	GND	P504				
44	PA85	P511	AG7	P510	P509	AG7	P508	X			
46	PA86	SMJ1	AG9	SMJ2	SMJ3	AG9	SMJ4	TC3			
47	PA87	NC	AG9	NC	NC	AG9	NC	X			
48	PA88	P196	AG3	P214	P198	AG3	P218	6F4			
49	PA89	P212	GND	P216	P200	GND	P202	X			
50	PA90	P195	AG3	P223	P207	AG3	P222	6S4			
51	PA91	P211	AG3	P206	P205	AG3	P221	X			
52	PA92	P194	AG3	P220	P219	AG3	P204	6F4			
53	PA93	P210	AG3	P201	P217	AG3	P203	X			
55	PA94	9F8	9S8	NC	6F7	6S7	6F7				

1												
2		1	2	3	4	5	6	7			X: NO PAD	
3	P95	9F4	9S4	NC	6F8	6S8	6F8	NC				
4	P96	GND	P193	P209	P215	GND	P199	X				Slot9
5	P97	AG3	P192	P208	P213	AG3	P197	6F11				SLot6
7	P98	AG1	P67	P66	P65	AG1	P64	X				
8	P99	GND	P71	P70	P69	GND	P68	6S11				
9	P100	AG1	P75	P74	P73	AG1	P72	X				
10	P101	AG1	P79	P78	P77	AG1	P76	6F11				
11	P102	AG1	P83	P82	P81	AG1	P80	X				
12	P103	AG1	P87	P86	P85	AG1	P84	TC1				
13	P104	GND	P91	P90	P89	GND	P88	X				
14	P105	AG1	P95	P94	P93	AG1	P92	AG1				
16	P106	AG7	P451	P450	P449	AG7	P448	X				
17	P107	GND	P455	P454	P453	GND	P452					
18	P108	AG7	P459	P458	P457	AG7	P456	X				
19	P109	AG7	P463	P462	P461	AG7	P460	AG7				
20	P110	AG7	P467	P466	P465	AG7	P464	X				
21	P111	AG7	P471	P470	P469	AG7	P468	TC7				
22	P112	GND	P475	P474	P473	GND	P472	X				
23	P113	UR18	UR17	UR16	X	X	X	X				
24	P114	UR21	UR20	UR19	X	X	X	X				
25	P115	RLY_5V	UR23	UR22	X	X	X	X				
26	P116	AG7	P479	P478	P477	AG7	P476	X				
28	P117	AG5	P323	P322	P321	AG5	P320	AG5				
29	P118	GND	P327	P326	P325	GND	P324	X				
30	P119	AG5	P331	P330	P329	AG5	P328	AG5				
31	P120	AG5	P335	P334	P333	AG5	P332	X				
32	P121	AG5	P339	P338	P337	AG5	P336	TC5				
33	P122	AG5	P343	P342	P341	AG5	P340	X				
34	P123	GND	P347	P346	P345	GND	P344	AG5				
35	P124	AG5	P351	P350	P349	AG5	P348	X				
37	P125	AG0	P63	P47	P62	AG0	P32	TC0				
38	P126	GND	P46	P49	P33	GND	P48	X				
39	P127	AG0	P61	P45	P60	AG0	P34	6F12				
40	P128	AG0	P44	P51	P35	AG0	P50	X				
41	P129	AG0	P59	P43	P58	AG0	P36	6S12				
42	P130	AG0	P42	P53	P37	AG0	P52	X				
43	P131	GND	P57	P41	P56	GND	P38	6F12				
44	P132	AG0	P40	P55	P39	AG0	P54	X				
45	P133	9F0	9S0		6F15	6S15	6F15					

1												
2			1	2	3	4	5	6	7			
3	PA134		9F28	9S28	NC	6F16	6S16	6F16	NC			
5	PA135		P259	AG4	P258	P257	AG4	P256	X			
6	PA136		P263	GND	P262	P261	GND	P260	6F19		X: NO PAD	
7	PA137		P267	AG4	P266	P265	AG4	P264	X			
8	PA138		P271	AG4	P270	P269	AG4	P268	6S19			Slot9
9	PA139		P275	AG4	P274	P273	AG4	P272	X			SLot6
10	PA140		P279	AG4	P278	P277	AG4	P276	6F19			
11	PA141		P263	GND	P262	P261	GND	P260	X			
12	PA142		P267	AG4	P266	P265	AG4	P264	TC4			
14	PA143		P163	AG2	P162	P161	AG2	P160	X			
15	PA144		P167	GND	P166	P165	GND	P164	TP8			
16	PA145		P171	AG2	P170	P169	AG2	P168	X			
17	PA146		P175	AG2	P174	P173	AG2	P172	TP9			
18	PA147		P179	AG2	P178	P177	AG2	P176	X			
19	PA148		P183	AG2	P182	P181	AG2	P180	TP10			
20	PA149		P187	GND	P186	P185	GND	P184	X			
21	PA150		P191	AG2	P190	P189	AG2	P188	TC2			
23	PA151		P515	AG8	P514	P513	AG8	P512	X			
24	PA152		P519	GND	P518	P517	GND	P516	TP11			
25	PA153		P523	AG8	P522	P521	AG8	P520	X			
26	PA154		P527	AG8	P526	P525	AG8	P524				
27	PA155		-15V	+15V	X	X	X	X	X			
28	PA156		UR26	UR25	UR24	X	X	X	X			
29	PA157		UR29	UR28	UR27	X	X	X	X			
30	PA158		RLY 5V	UR31	UR30	X	X	X	X			
31	PA159		+5V	TP12	X	X	X	X	X			
32	PA160		P531	AG8	P530	P529	AG8	P528	TC8			
33	PA161		P535	AG8	P534	P533	AG8	P532	X			
34	PA162		P539	GND	P538	P537	GND	P536	TP13			
35	PA163		P543	AG8	P542	P541	AG8	P540	X			
37	PA164		9S19	GND	9F19	9S18	GND	9F18	9S-2			
38	PA165		9S23	GND	9F23	9S22	GND	9F22	X			
39	PA166		9S27	GND	9F27	9S26	GND	9F26	TP14			
40	PA167		9S31	GND	9F31	9S30	GND	9F30	X			
41	PA168		6S2	GND	6F2	6S1	GND	6F1	TP15			
42	PA169		6S6	GND	6F6	6S5	GND	6F5	X			
43	PA170		6S10	GND	6F10	6S9	GND	6F9	TP16			
44	PA171		6S14	GND	6F14	6S13	GND	6F13	X			
46	PA172		P3	AG0	P2	P1	AG0	P0	TC0			
47	PA173		P7	GND	P6	P5	GND	P4	X			
48	PA174		P11	AG0	P10	P9	AG0	P8	6F20			
49	PA175		P15	AG0	P14	P13	AG0	P12	X			
50	PA176		P19	AG0	P18	P17	AG0	P16	6S20			
51	PA177		P23	AG0	P22	P21	AG0	P20	X			
52	PA178		P27	GND	P26	P25	GND	P24	6F20			
53	PA179		P31	AG0	P30	P29	AG0	P28	X			
55	PA180		9F24	9S24	NC	6F23	6S23	6F23	NC			

3. Maintenance of 338x Test System

3.1 Introduction

The regular maintenance of Chroma 3380/3380P Test System should be at fixed periods for one month. The maintenance tool is a utility for qualified maintenance personnel to diagnose and/or to calibrate the tester hardware. This utility combines the calibration and diagnostic modules into a single integrated module that standardize the operations.

If you have problems that are not described in this manual or in the referenced supplementary documents, contact the Customer Engineer (CE) of Chroma ATE Inc. near you.

3.1.1 Maintenance Procedures

This section gives a brief explanation of the maintenance procedures. **The procession standard of maintenance is DC calibration->DC diagnosis->AC calibration->AC diagnosis.**

3.1.1.1 About Diagnostics

Diagnostics is the process of verifying the operations of system hardware by a set of special designed programs for self-test. You can run the diagnostics procedure any time when the system is running normally.

The procedure should be followed in the order below:

- Replace a module or board first.
- Perform auto calibration.
- Run full diagnostics.

3.1.1.2 About Calibration

The calibration program is a user-interface software based on CRAFT for 3380/3380P.

This section describes how to perform Chroma 3380/3380P automatic calibration procedure to ensure the system operates within its defined specifications. Calibration is the process to adjust all of the DC and AC settings based on internal references.

The DC reference calibration is done every month to measure the DC reference voltage levels and enter the current values. The program then adjusts the DC accuracy.

Calibration can be done at any time when a significant change is requested by tester. A change such as a pin-group board replacement may affect the calibration least. In addition to the regular maintenance schedule, calibration should be executed after the replacement of any board or module, and before the diagnostics procedures are performed. Once calibration is done successfully, the system is guaranteed to meet the specifications.

3.1.1.3 About Servicing the System

You should run diagnostics every month. If diagnostics reports any faults, repair and run it again. You should also run calibration every month. Repair and run diagnostics as well as calibration again if calibration shows any problems.

3.1.1.4 Service Schedule

A summary of the maintenance procedures is given in the following table.

Table 3-1 Service Schedule

	1 Month	6 Month	12 Month	Time Required [b]
Running Calibration [a]	♣			60min
Running AC-Diagnostics	♣			30 min
Running DC-Diagnostics	♣			25 min
Check Active-Handler		♣		5 min
Lubricating the Wheel		♣		5 min
Check the Fan		♣		10 min
Check Power-Box			♣	10 min
Check Ring Tour		♣		5 min
Check Calibration Board	♣			5 min

a. The time for actions to be done after the system installation.
b. The estimated time required is based on the following assumptions.
   - Performed by experienced personnel.
   - All tools, material, and equipment are ready to hand.
   - Have quick access to all system components.

3.1.1.5 Preserve Maintenance (PM) Check Reference

Monthly PM(Preserve Maintenance) item:

- Clean mainframe & cover
- Check blowing machine
- Check all connections
- Check test head exhauster
- Check all power supplies
- Run DC_ Cal
  - PMU_ Cal
  - DPS_ Cal
  - IO_ Cal
  - REF_ Cal (option)
  - UVI_ Cal (option)
  - MLDPS_Cal (option)
  - AWI_ Cal (option)
- Run AC_ Cal
- Run DC_ Diag
- Run AC_ Diag

Semi-annual PM item:

- Clean mainframe & cover
- Check blowing machine
- Check all connections
- Check test head exhauster
- Check lubricating the wheel
- Check calibration board
- Check ring tour
- Check power box
- Check fan
- Check all power supplies (rang +2%, +5V power supply spec .+5.1V)
- Run DC_ Cal
  - PMU_ Cal
  - DPS_ Cal
  - IO_ Cal
  - REF_ Cal (option)
  - UVI_ Cal (option)
  - MLDPS_ Cal (option)
  - AWI_ Cal (option)
- Run AC_ Cal
- Run DC_ Diag
- Run AC_ Diag

3.2 Calibration

3.2.1 Overview

Calibration is a service function of the Chroma 3380/3380P VLSI Test System. Calibration is used to ensure the system is within the specification. It consists of many calibration programs.

The calibration programs calculate the measurement results of system modules, and then store the data in the system. Calibration ensures the accuracy of Chroma 3380/3380P Test System. The built-in calibration program is designed to compensate both DC and AC errors in the system. With the user-friendly interface design, few clicks are enough to perform the entire system calibration.

3.2.2 Starting Calibration Programs in Maintenance Window

After powering on successfully and before calibrating, please wait 20 minutes for test system warm up.

(1) Double click the Maintenance Utility icon in the System Control window or click the string of Maintenance Utility from the tree window to start it (see Figure 3-1).

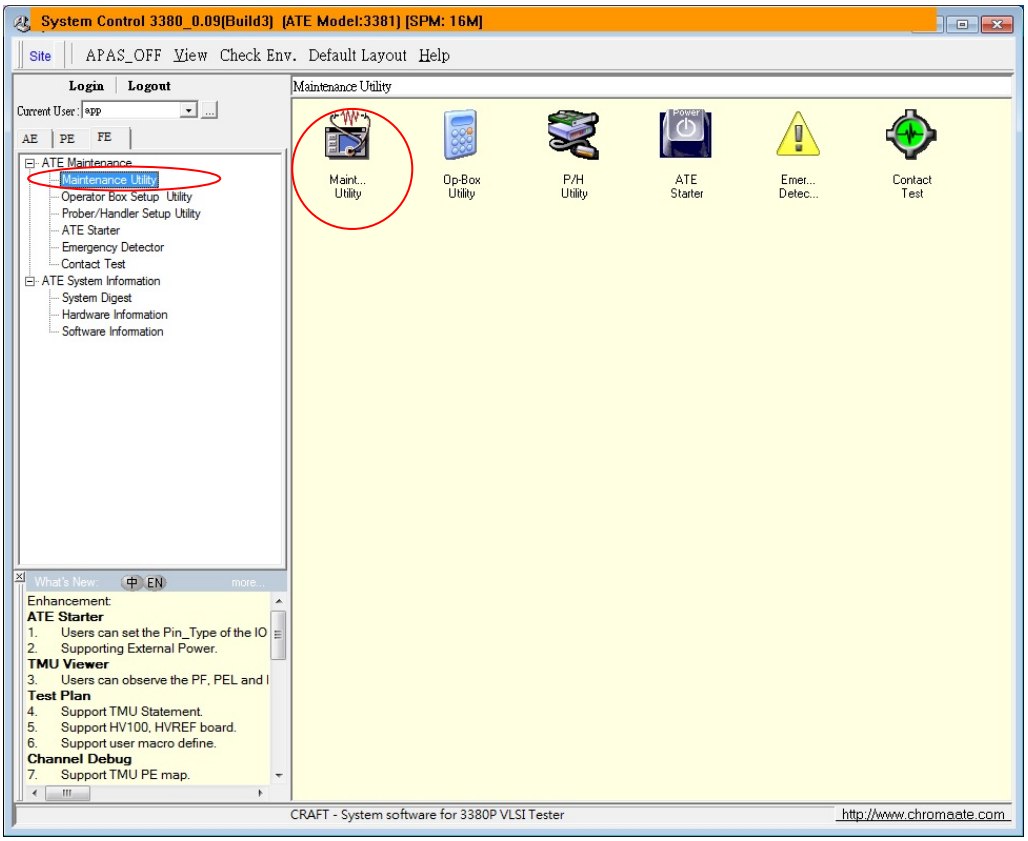


Figure 3-1 Maintenance Window on CRAFT

(2) Click the calibration icon in CRAFT to activate the calibration user interface (see *Figure 3-2*).

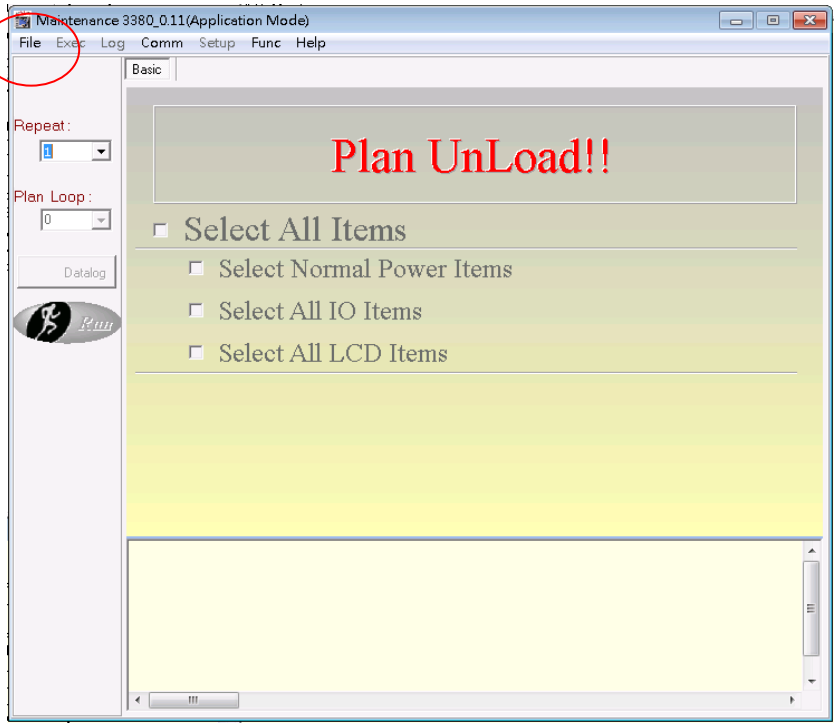


Figure 3-2 Calibration Program Icon in Maintenance

(3) Quitting Maintenance Utility. To quit Maintenance Utility, click the Close button in the

window (see *Figure 3-3*, *Figure 3-4*).

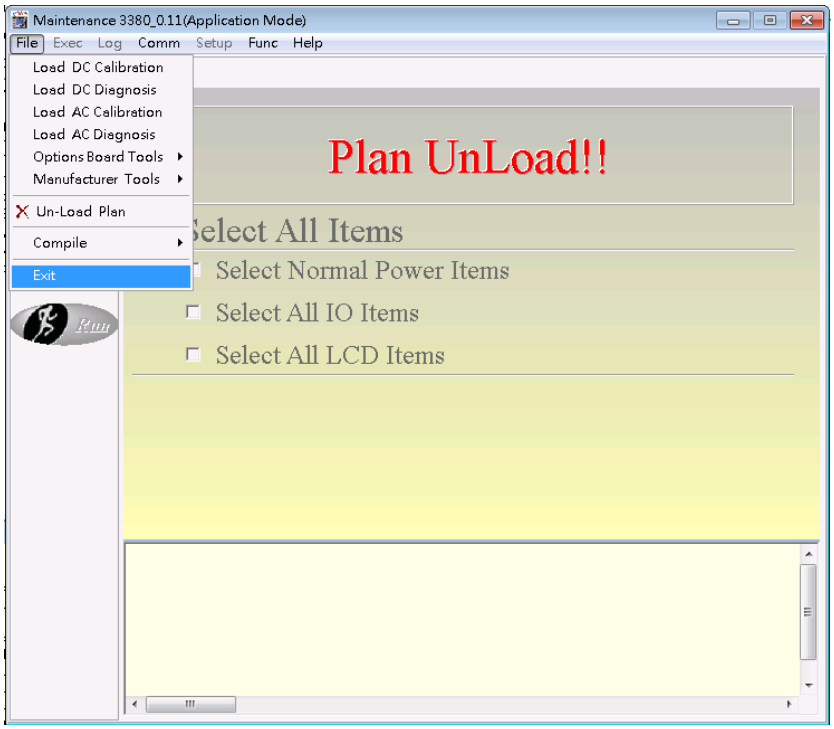


Figure 3-3 Quitting Maintenance Utility

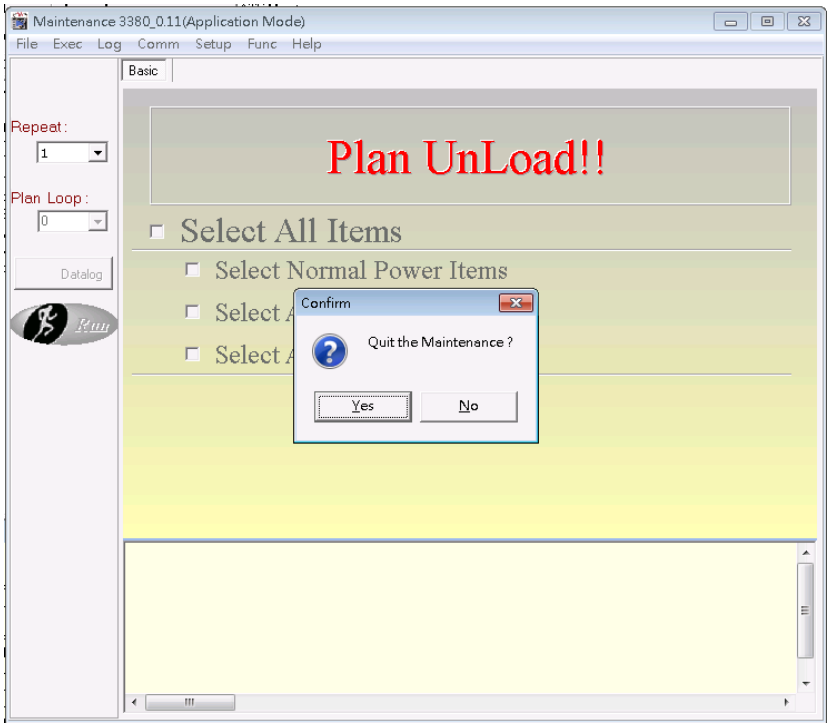


Figure 3-4 Quitting Maintenance Utility

For the detail operation, see the following section.

3.2.3 Calibration Items and Kit

The program contains both DC and AC calibrations. All items are listed as below.

Table 3-2 Calibration Items List

Main Item	Sub-item	Main Item	Sub-item
DC Calibration	DC_ALL_CAL	AC Calibration	AL_AC_CAL
	DC_POWER_CAL		AC_IO_CAL
	IO_CAL		
	DPS_CAL		
	PMU_CAL		
	MLDPS_DMM_CAL		

3.2.3.1 Calibration Kit

External equipment is required for DC calibration. For optimum calibration accuracy, Keysight 34410A, 34410A,34461A, 3458A Multi-meter is recommended (see *Figure 3-5*).

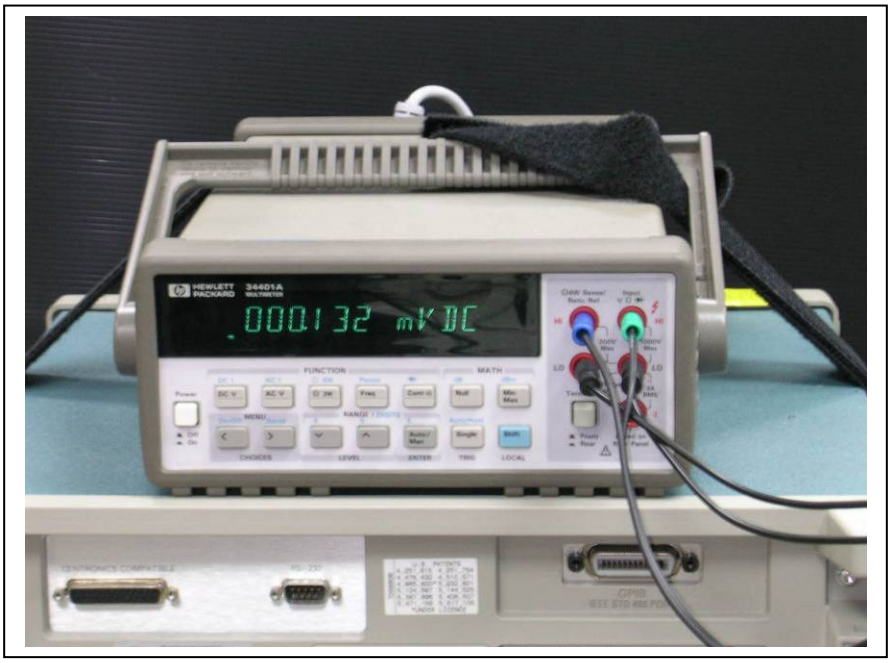
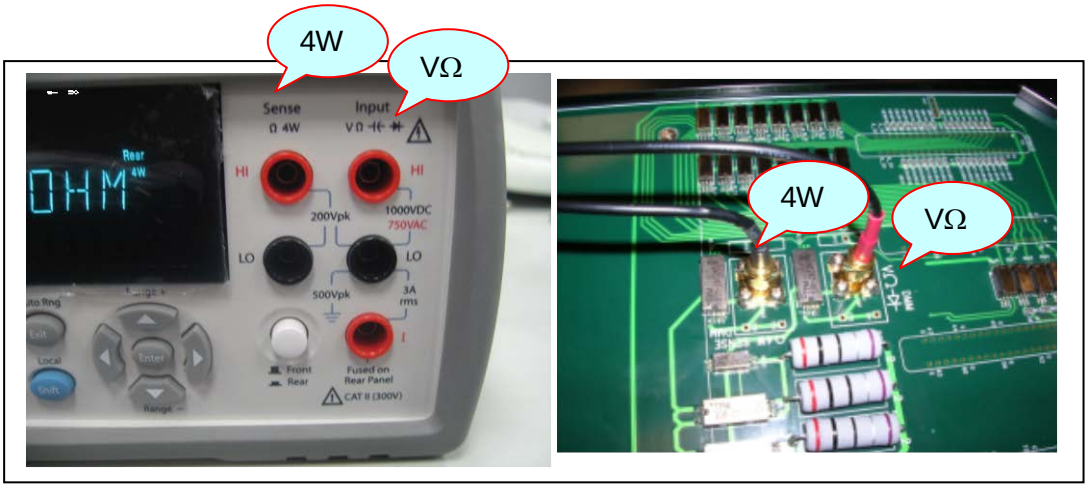


Figure 3-5 HP 34401A Multi-meter for DC Calibration

Note(Meter Address Settinig about GPIB):
34401A, 334410A, 344641A, 34465A => Address: 22
3458A=> Address: 23

The 4W of meter must be connected to the 4W of calibration load board. Similarly, the VΩ of meter must be connected to the VΩ of calibration load board. As the following figure:



3.3 DC Calibration

3.3.1 Overview

3380/3380P Test System needs calibration to correct the hardware functionality and then ensure its performance. If a calibration procedure fails, the maintenance engineer should repair the hardware or replace the failure module.

3.3.2 Write Tester_ID

(Only support Aftrer Maint1.20)

1. Power On

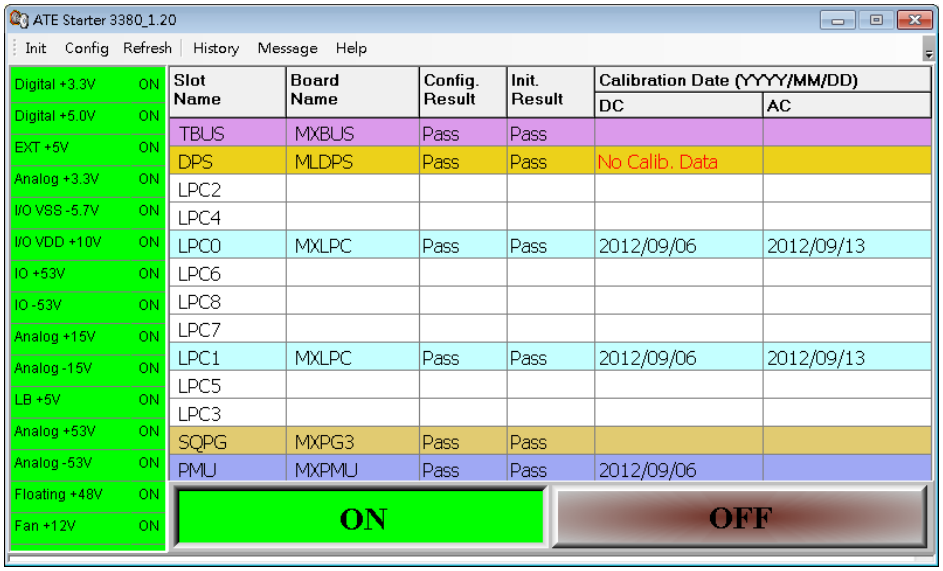


Figure 3-6 Power On

2. Click Maintenance

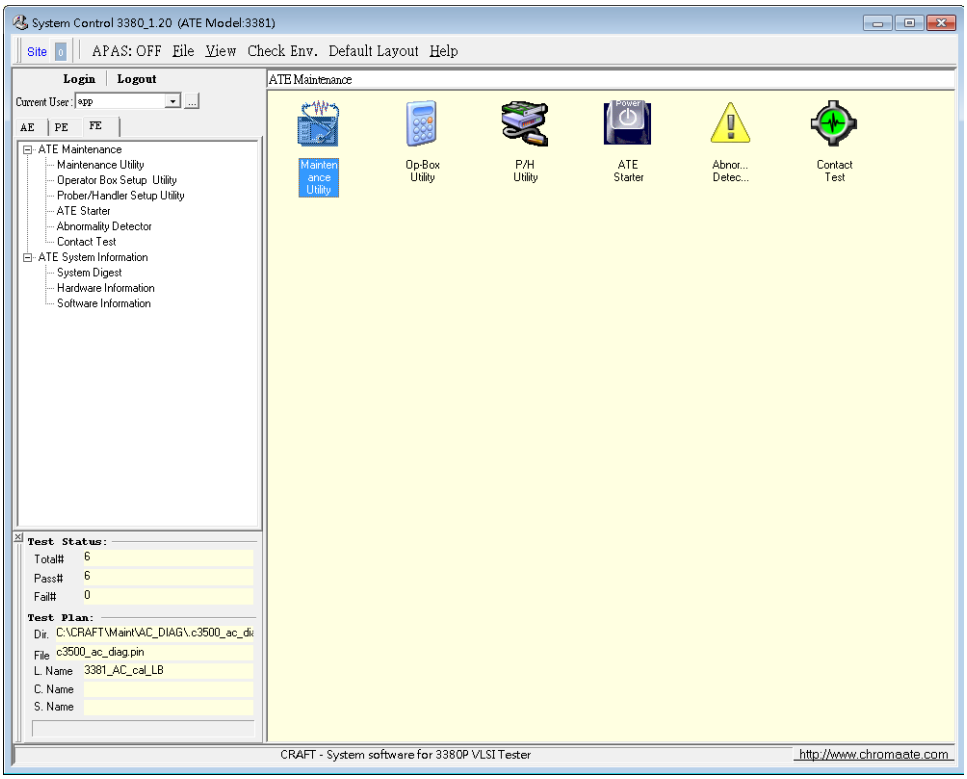


Figure 3-7Click Maintenance

3. Click Func -> Tester ID Management

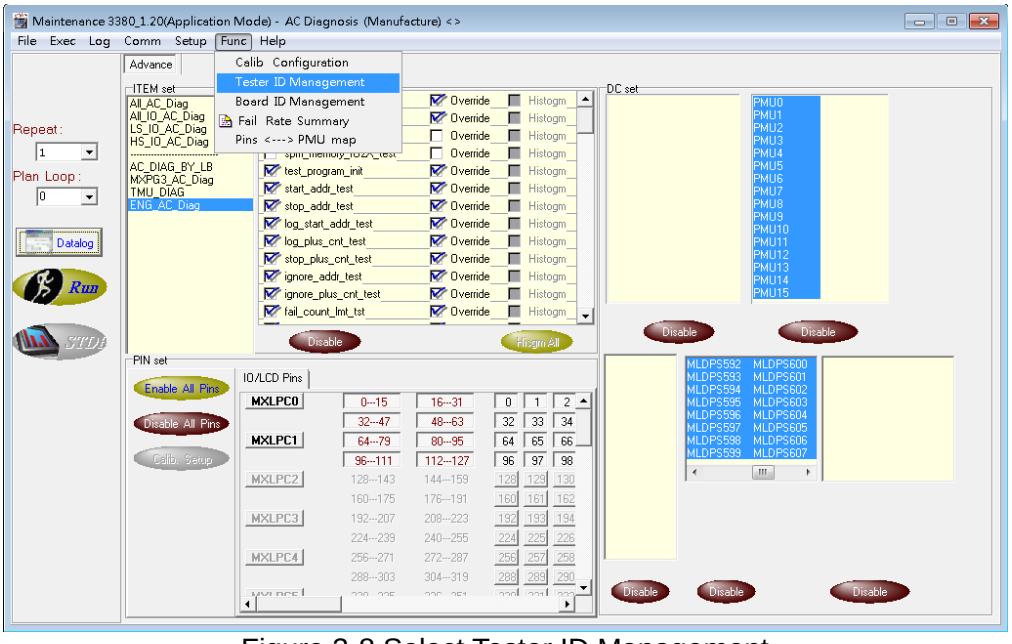


Figure 3-8 Select Tester ID Management

4. Copy System ID to Tester ID

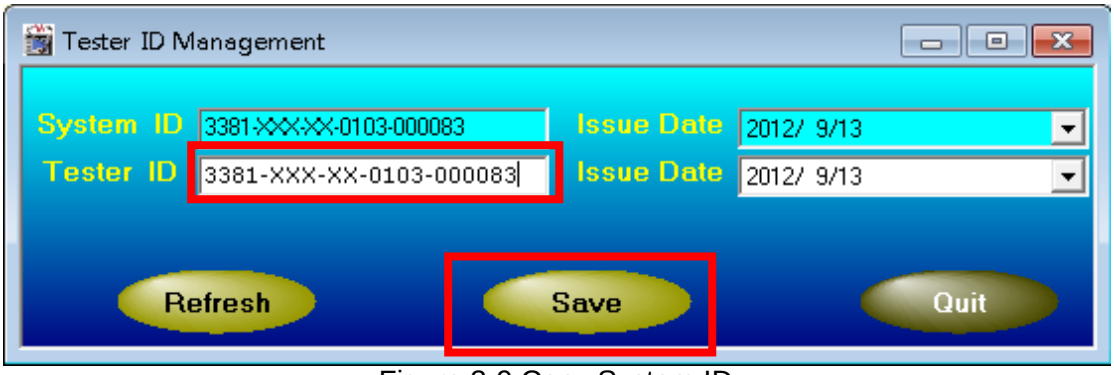


Figure 3-9 Copy System ID

5. Click Refresh -> Check Tester ID

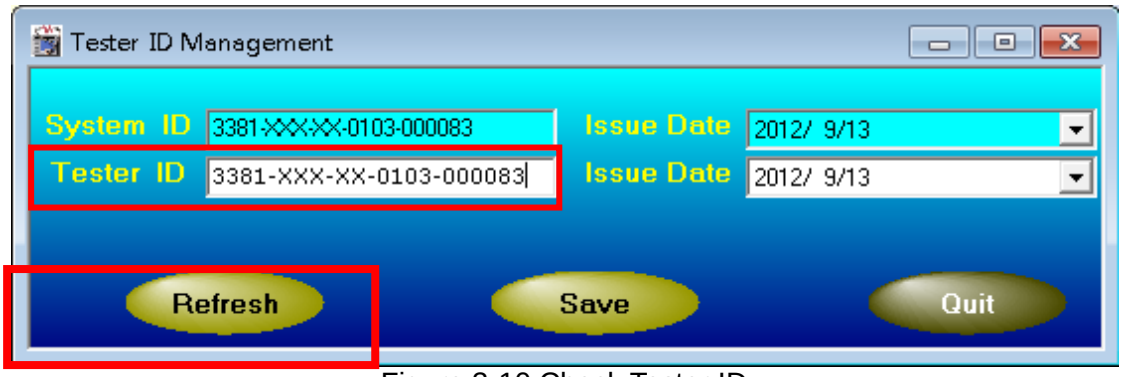


Figure 3-10 Check Tester ID

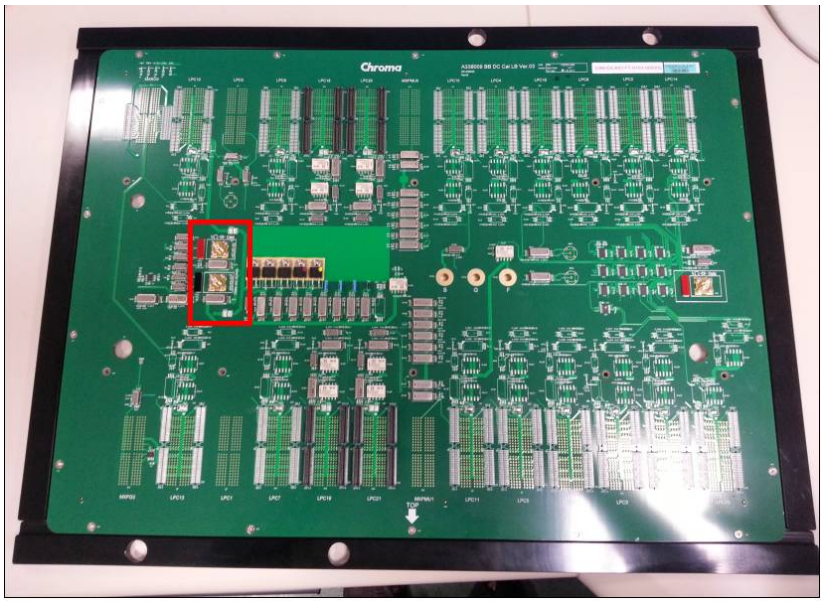
3.3.3 DC Calibration Items

There are three items to be calibrated by DC calibration.

- DC_ALL_CAL: It includes DPS_CAL, PMU_CAL, and IO_CAL .
- DC_POWER_CAL: It includes DPS, and PMU.
- DPS_CAL: Device power supplies are to be calibrated for accurate power source and measurement.
- PMU_CAL: Precision measurement units are to be calibrated for accurate FVMI (force voltage, measurement current) and FIMV (Force current, measurement voltage).
- IO_CAL: IO_Pin electronic circuits are to be calibrated for accurate level setting for digital pins.

3.3.4 Executing DC Calibration

3380/3380P test system requires a calibration board mounted on the test head for DC calibration (see *Figure 3-11* and *Figure 3-12*).



3380 Calibration Load Board

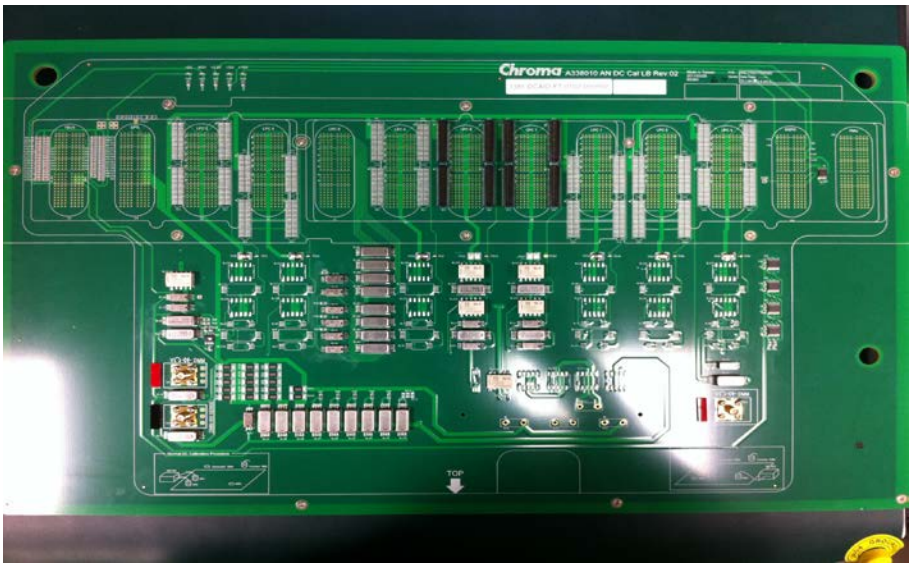


Figure 3-11 3380P Calibration Load Board

Figure 3-12 Calibration Load Board and Source Meter Connection

Procedures:

(1) Connect the calibration load board with Source Meter via a 4-wire test lead (refer to *Figure 3-12*).
(2) Connect the test system computer with Source Meter by a GPIB cable.
(3) To perform calibration, CRAFT must be started (refer to *Operation Manual chapter 1*) and maintenance utility icon is selected (see *Figure 3-1*).
(4) Select *Load DC Calibration* (see *Figure 3-13*).

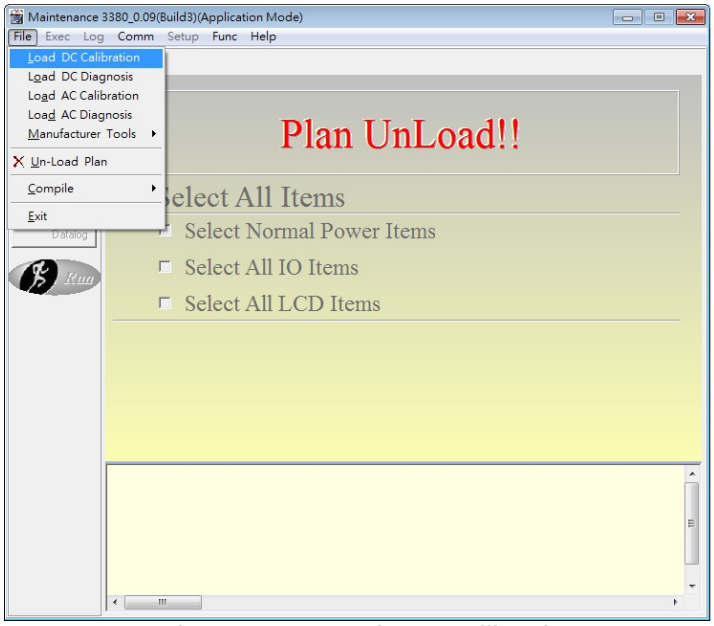


Figure 3-13 Load DC Calibration

(5) The DC Calibration Maintenance window as *Figure 3-14* shows which contains the following:

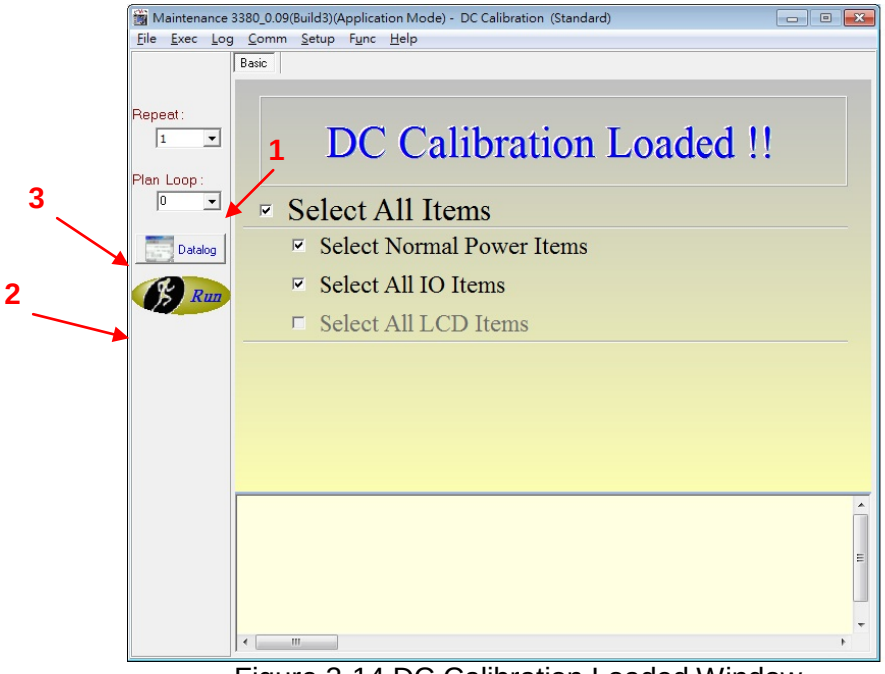


Figure 3-14 DC Calibration Loaded Window

1 : Mark “Select All Items” icon or any single item.
2 : Click “Run” to execute DC calibration, and it will prompt a Datalog window.

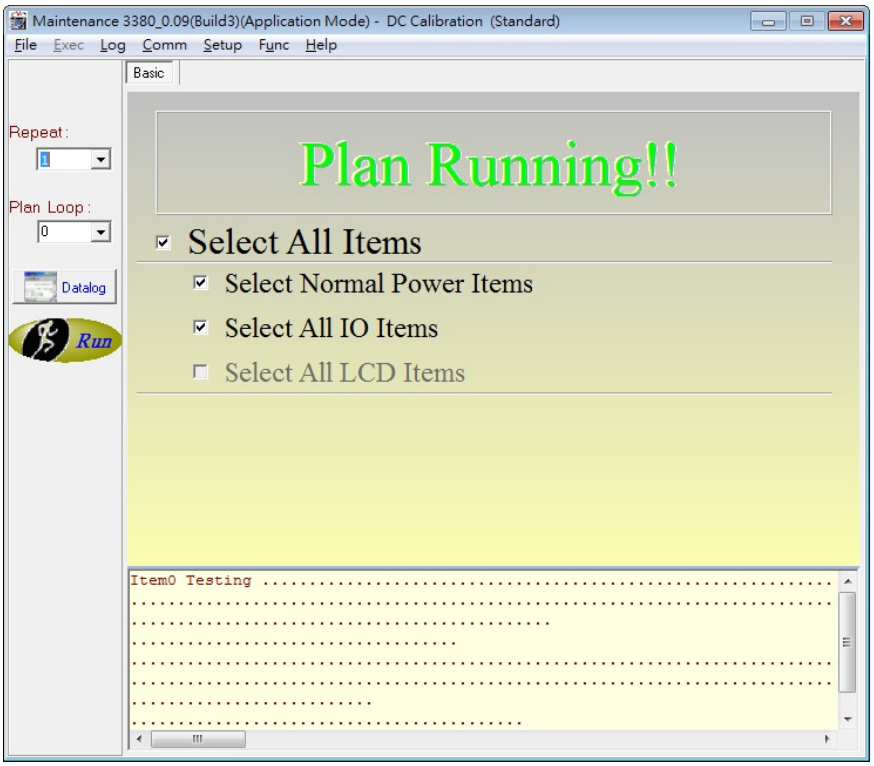


Figure 3-15 DC Calibration Running

3 : Click “Datalog” to switch to the Datalog window (refer to *Figure 3-16*).

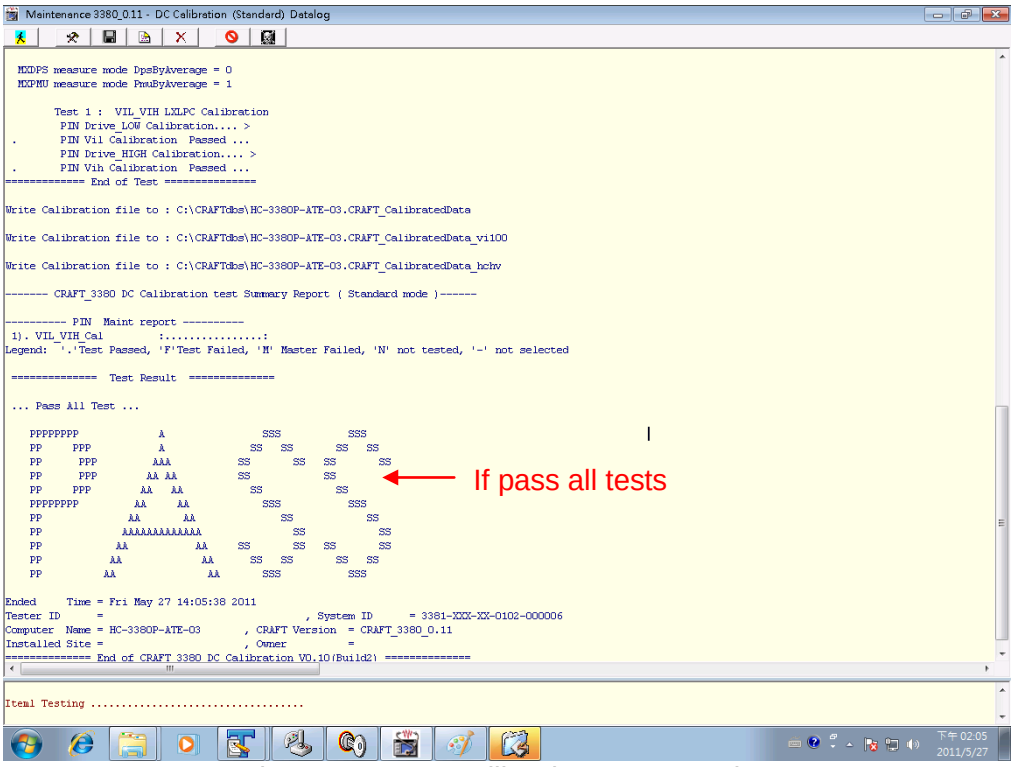


Figure 3-16 DC Calibration Pass Datalog

Finish the item, the screen will display “DC Calibration END”.

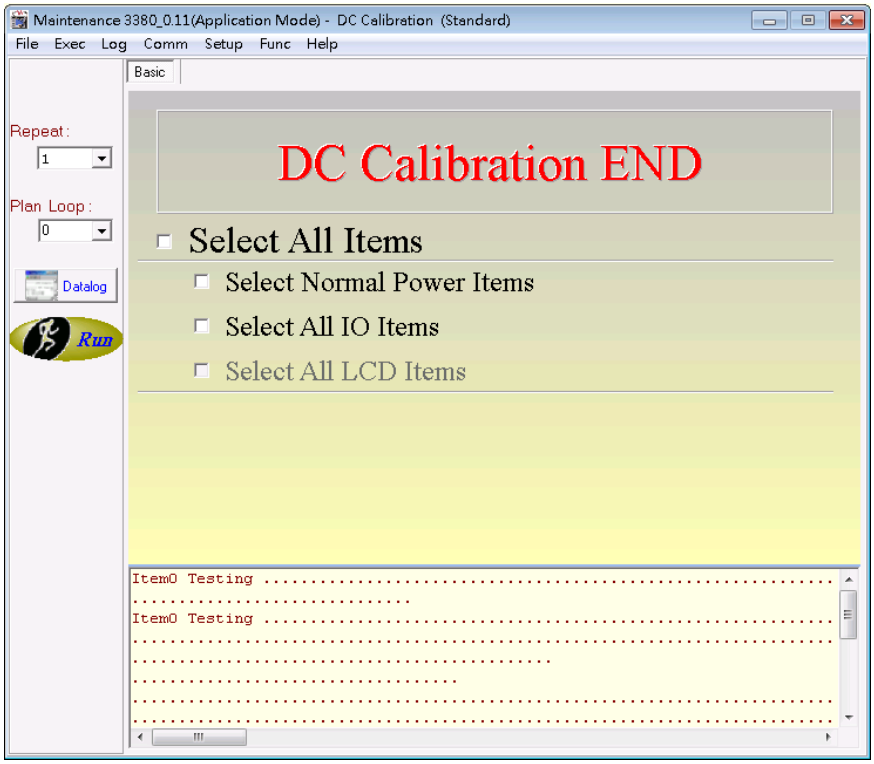


Figure 3-17 DC Calibration END

If users un-load DC Calibration Plan program, press “File” and “Un-Load Plan.”

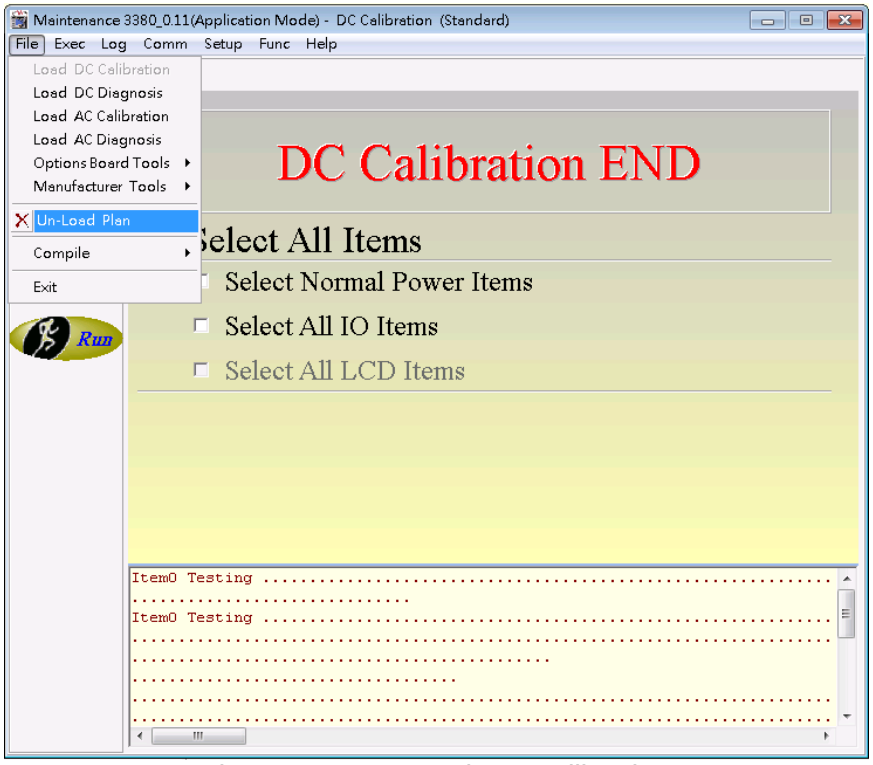


Figure 3-18 Un-Load DC Calibration

It displays “Are you sure to quit the DC calibration? ”, and press **Yes** to quit plan program.

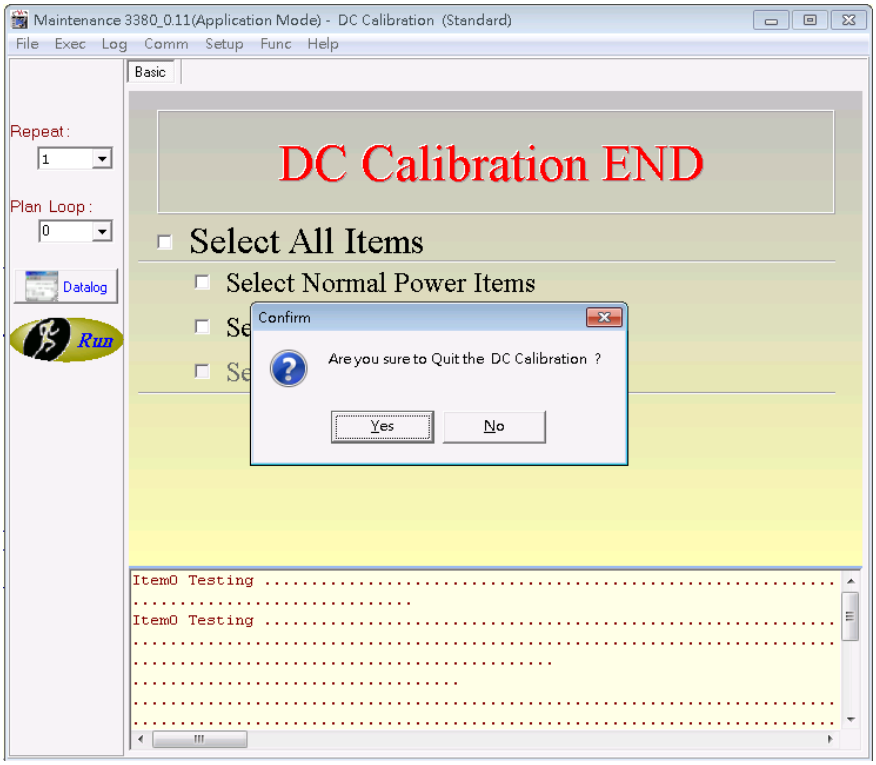
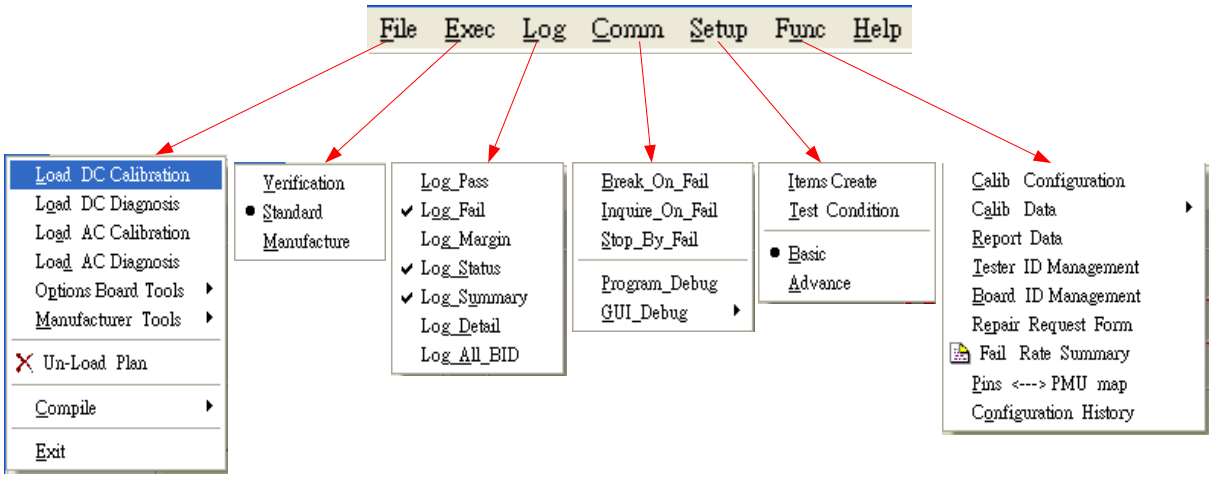


Figure 3-19 Quit DC Calibration

3.3.5 Function Menus



File Menu:

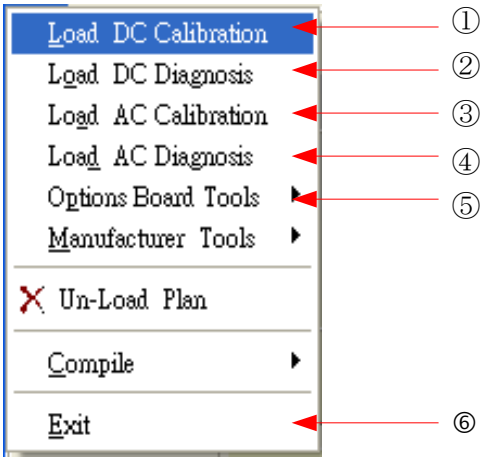


Table 3-3 File Menu Function List

No.	Function	Description
①	Load DC Calibration	Load DC Calibration program from CRAFT.
②	Load DC Diagnostic	Load DC Diagnostic program from CRAFT.
③	Load AC Calibration	Load AC Calibration program from CRAFT.
④	Load AC Diagnostic	Load AC Diagnostic program from CRAFT.
⑤	Options Board Tools->LXAWI Calibration & Diagnosis	Load LXAWI Calibration & Diagnosis program from CRAFT.
⑥	Exit	Exit the Maintenance window.

Exec Menu:

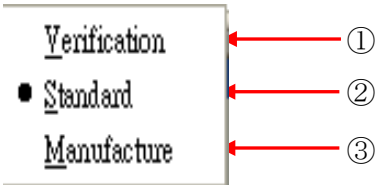


Table 3-4 Exec Menu Function List

No.	Function	Description
①	Verification	This operation is to perform a quick verification on the system for basic functions. Only a small set of tests is performed, and loose limits are applied on pass/fail judgment (default).
②	Standard	This is a typical application for regular system maintenance personnel; the complete set of diagnostics runs on the system to guarantee it meets the specification.
③	Extend	This operation generally takes place at the manufacturing stage. After the system is integrated, the components need to be tested for early faults. In this phase, diagnostics may run for several hours and exhaustive testing may be required.

Log Menu:

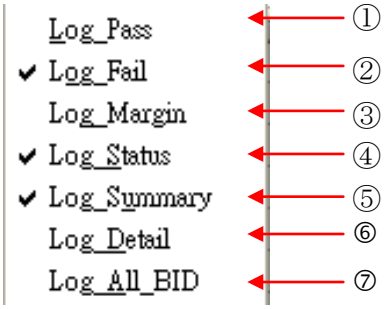


Table 3-5 Log Menu Function List

No.	Function	Description
①	Log_Pass	Log the pass data.
②	Log_Fail	Log the fail data.
③	Log_Margin	Log the Margin data.
④	Log_Status	Log the status without the message of selected test item.
⑤	Log_Summary	Log the summary data.
⑥	Log_Detail	Log the detail message for engineer/debugging use.
⑦	Log_All_BID	Log all Board ID data.

Comm Menu:

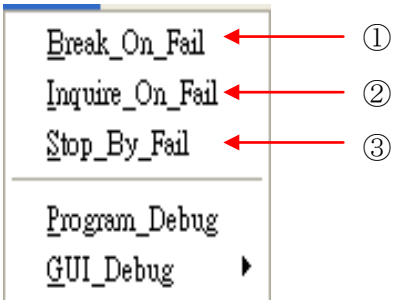


Table 3-6 Comm Menu Function List

No.	Function	Description
①	Break_On_Fail	When fail occurs, it will stop at the break point.
②	Inquire_On_Fail	When fail occurs, it will inquire by user.
③	Stop_By_Fail	When fail occurs, it will stop the program.

Setup Menu:

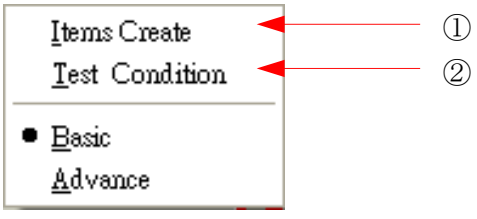
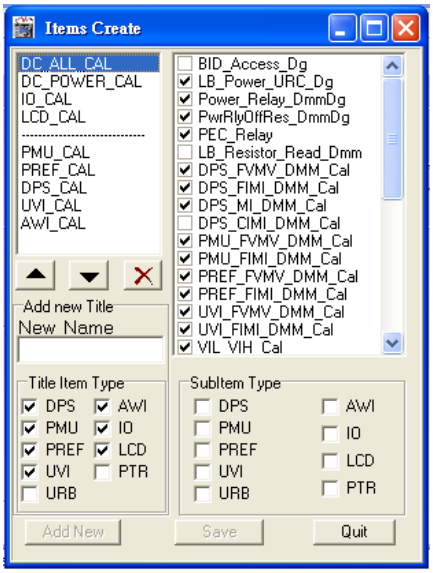


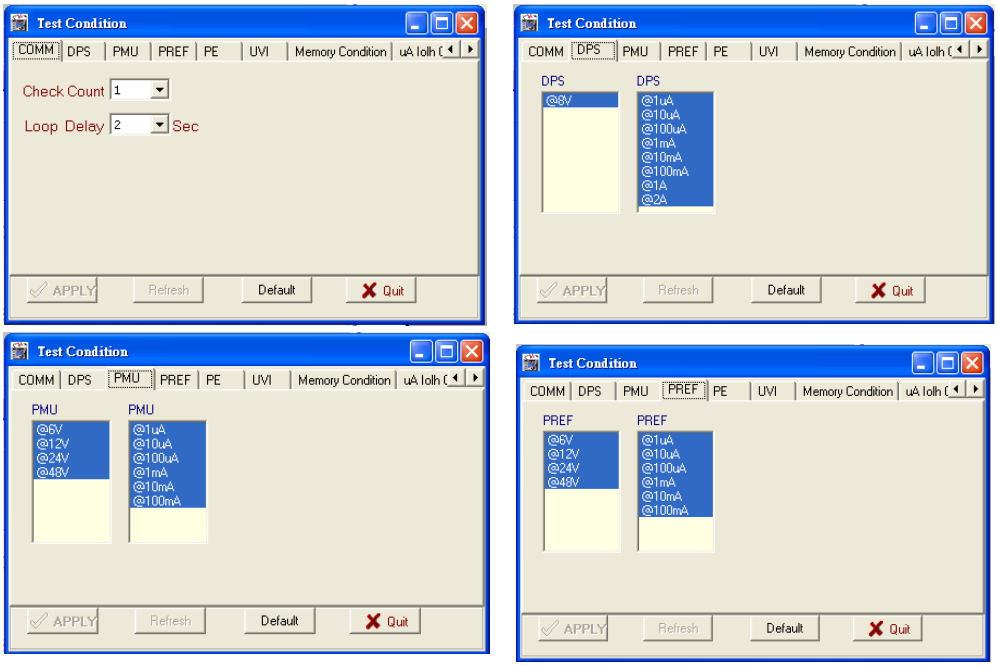
Table 3-7 Setup Menu Function List

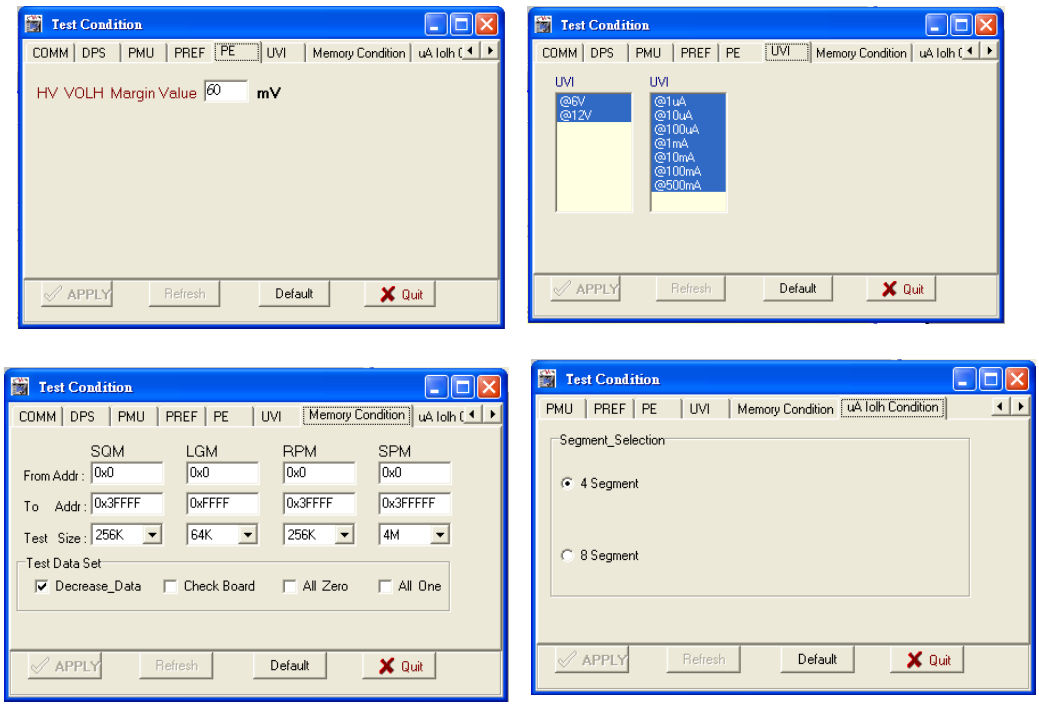
No.	Function	Description
①	Items Create	Create a new test item for DC calibration.
②	Test Condition	Define the test conditions for test items.

The Items Create are set as the figure shown below:



The test conditions are set as the figures shown below:





Func Menu:

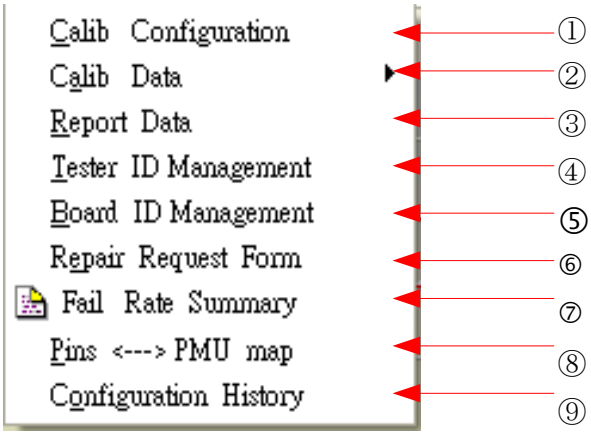
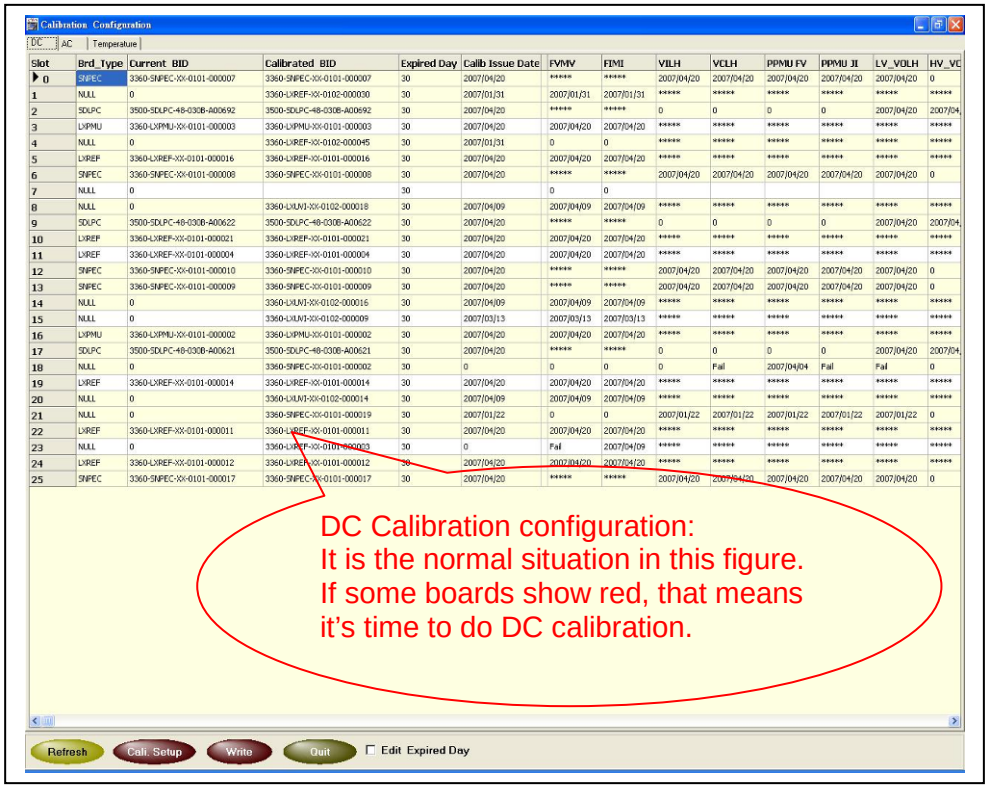
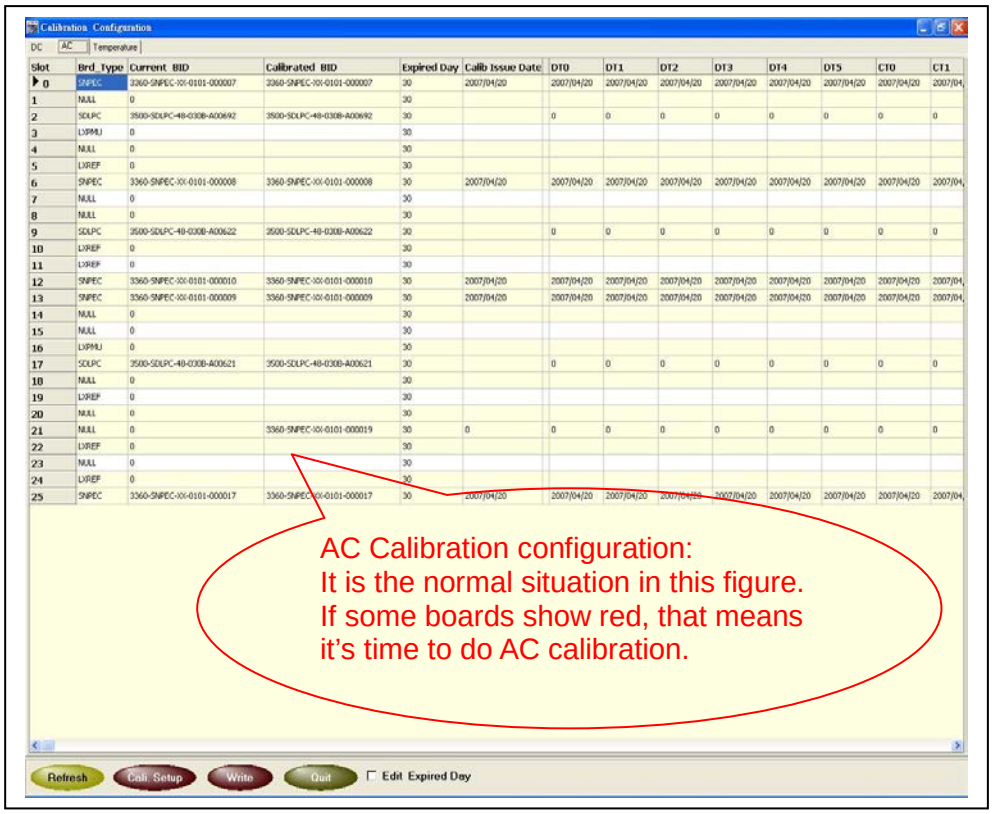


Table 3-8 Func Menu Function List

No.	Function	Description
①	Calib Configuration	List AC and DC calibration configuration
②	Calib Data	List calibration data on monitor, write calibration data to designated file and load calibration data to designated file.
③	Report Data	List AC's and DC's diagnostic and calibration.
④	Tester ID Management	Write and read tester ID from this interface.
⑤	Board ID Management	Write and read board ID from this interface.
⑥	Repair Request Form	List repair board history.
⑦	Fail Rate Summary	The rate of fail occurred.
⑧	Pins < -- > PMU map	List pins on PMU mapping.
⑨	Configuration History	Record the configuration history.

Calibration configuration





3.3.6 DataLog Menus

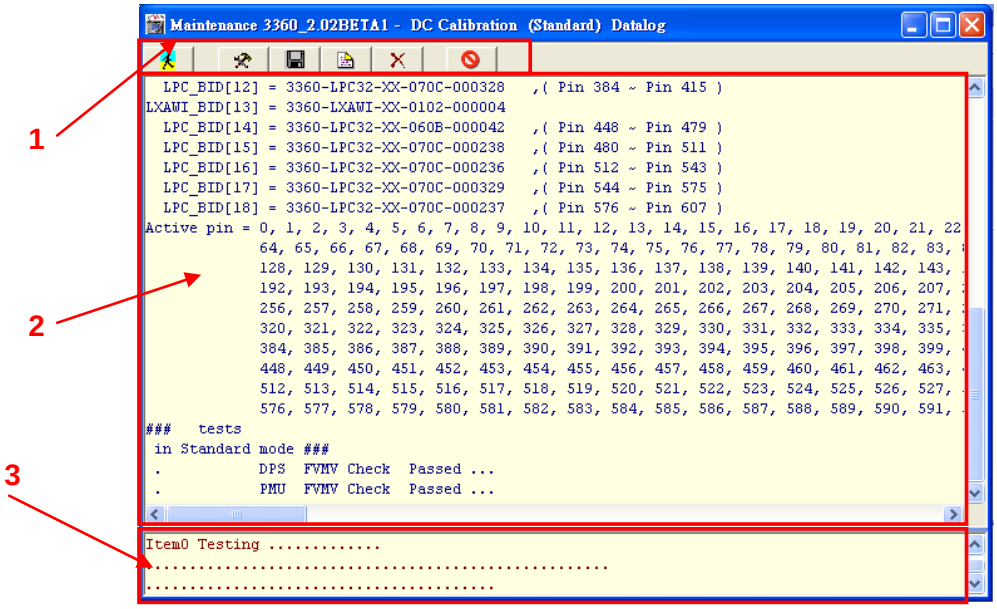


Table 3-9 Datalog Window Function List

No.	Function	Description
1	Main Menu	The main menu of Datalog window, including run, return to calibration window, save, delete, and stop etc.
2	Data display area	This area displays the test data.
3	Status display area	This area displays the test status.

Main Menu:

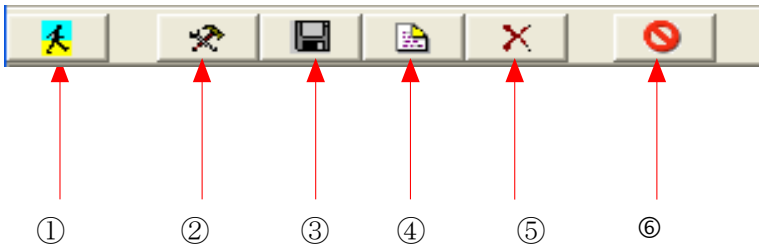


Table 3-10 Datalog Main Menu Function List

No.	Function	Description
①	Run button	It runs the calibration program.
②	Setup condition	It returns to Calibration window from Datalog window.
③	Save button	It saves the data to a file.
④	Fail rate summary	
⑤	Clear button	It clears the data in the Datalog.
⑥	Stop button	It stops the calibration program.

3.4 AC Calibration

3.4.1 Overview

AC calibration ensures the timing accuracy of 3380/3380P Test System. The target of timing calibration is to make all input signals arriver DUT simultaneously and output at the proper time.

3.4.2 When to Run the AC Calibration?

To ensure the accuracy of timing, calibration should be performed periodically or whenever there is a doubt of the accuracy. Furthermore, if any condition below is encountered, timing calibration must be done:

- The environment condition is changed.
- After PE is re-calibrated, since timing accuracy is related to the PE voltage level.
- After the MXLPC board is changed.

Note Calibration should be performed when the test system and environment are stable. It is recommended to wait for half hour after powered on.

3.4.3 Executing AC Calibration

Procedures:

(1) Click “Load AC Calibration” as *Figure 3-20* shown to activate the AC Calibration Maintenance window as *Figure 3-21* shown.

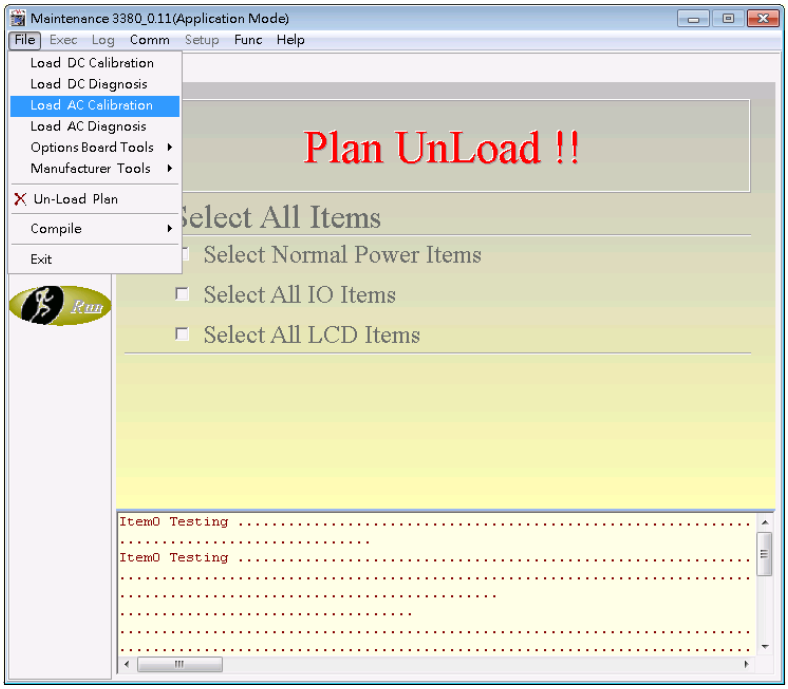


Figure 3-20 AC Calibration Window

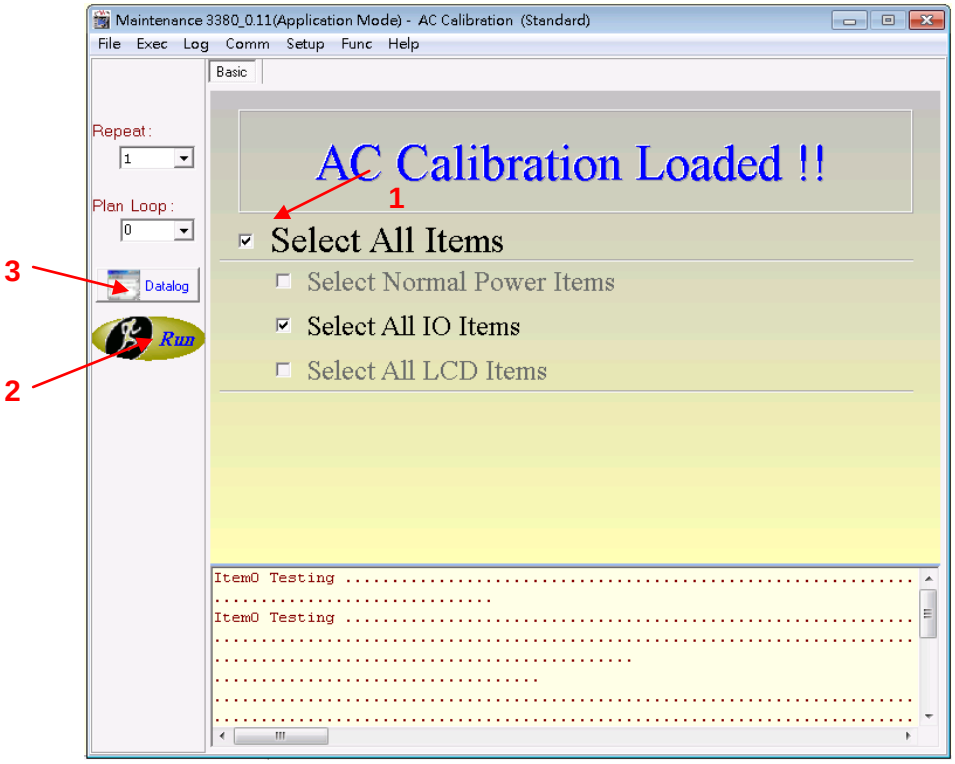


Figure 3-21 AC Calibration Window

1 : Mark “Select All Items”.
2 : Click “Run” to execute AC calibration, and it will prompt a Datalog window.

Note | To execute AC calibration must remove load board.

3 : Click “Datalog” to switch to the Datalog window (refer to *Figure 3-22*).

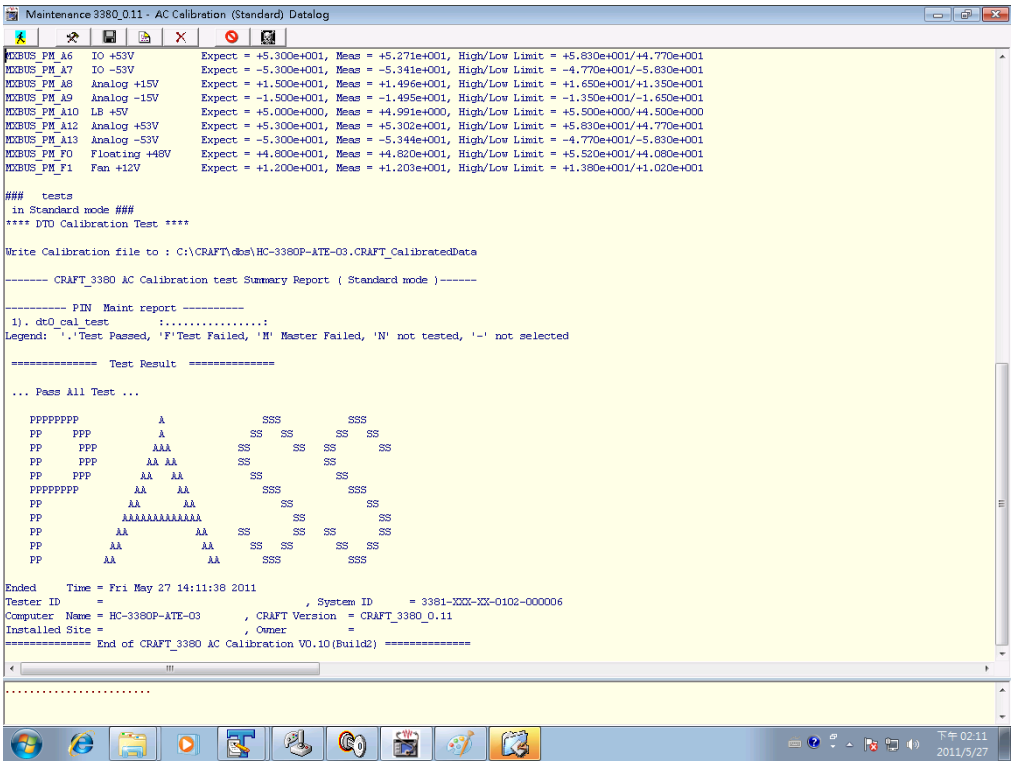


Figure 3-22 AC Calibration Datalog

(2) Finish the item and display “AC Calibration END”.

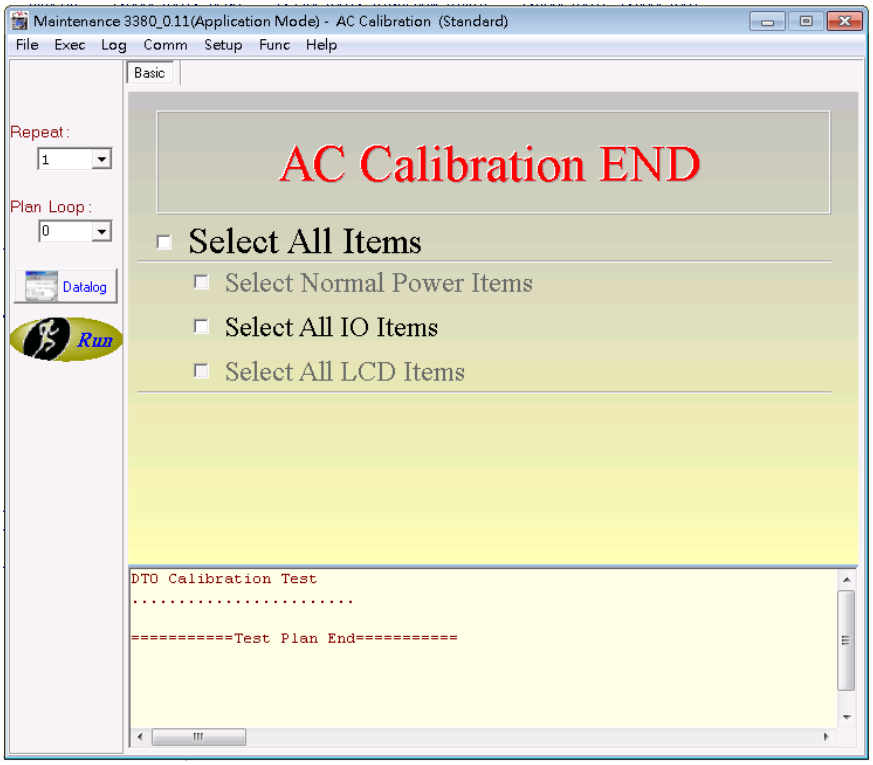


Figure 3-23 AC Calibration END

(3) If users un-load AC Calibration Plan program, press “File” and “Un-Load Plan.”

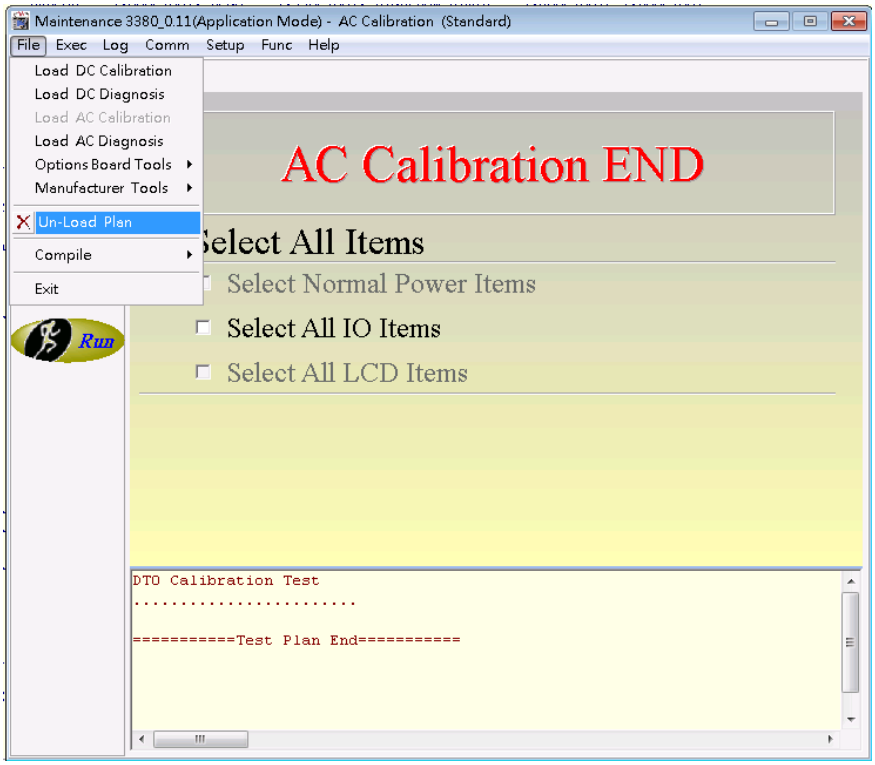


Figure 3-24 Un-Load AC Calibration

(4) Then display “Are you sure to quit the AC calibration? ”, and press **Yes** to quit plan program.

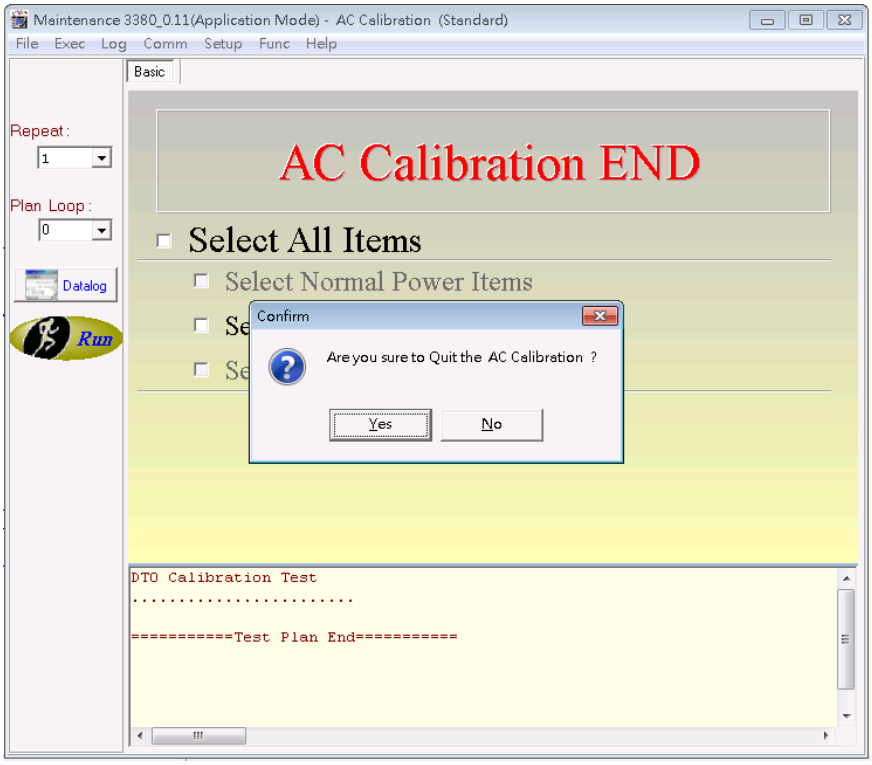


Figure 3-25 Quit AC Calibration

3.5 Diagnostics

The diagnosis program is a tool to help troubleshooting and repair failures of CRAFT. This section describes how to use the diagnostics routines included in the system software, and how to detect defects of system modules locally.

3.5.1 Introduction

The diagnosis program is designed to self-check system functions, and self-detect hardware failures for Chroma 3380/3380P IC Test System. From the GUI (Graphic User Interface), users may choose the diagnostic items for specific test. The program also contains the recommended test for daily and monthly use. The daily test is suggested to be performed at the beginning of each day, and the monthly test is suggested to be performed every month.

The diagnostics software checks functional failure in the system hardware, and identifies the hardware boards or modules that failed. If more than one module is failed, it is suggested to run diagnostics item by item. Please be noted that ONLY ONE item can be replaced at a time as it helps to isolate the defective module.

Before running the diagnosis program, be aware of the following constraints:

(1) All of the utilities and test-plans should be terminated before running the diagnosis program.
(2) No DUT is on the load board (performance-board) when executing the diagnosis program.
(3) If the diagnosis GUI exists, no other utilities and test-plans are available.
(4) When executing the diagnosis program, make sure that the socket is enabled through the system software UI.

3.5.2 Diagnostic Items

The program contains both DC and AC diagnostics. All items are listed as below.

Table 3-11 Calibration Items List

Main Item	Sub-item	Main Item	Sub-item
DC Diagnosis	DC_ALL_DIAG	AC Diagnostic	All_AC_Diag
	DC_POWER_Diag		All_IO_AC_Diag
	IO_Diag		LS_IO_AC_Diag
	DPS_Diag		HS_IO_AC_Diag
	PMU_Diag		
	MLDPS_DMM_Diag		

3.6 DC Diagnostics

3.6.1 Overview

DC Diagnostic comprises *PMU_Diag, DPS_Diag,* and *IO_Diag* modes.

- It uses several ranges of resister to simulate "**Force**"/"**Measure**" conditions for DC modules.
- It uses "User Relays" to switch between DC diagnosed modules and selected resister.
- By selecting suitable resister, it is able to diagnose the resolution and accuracy of each V_range multiply I_range force/measure/measure_clamp.

3.6.2 Executing DC Diagnostics

The section describes the procedures to run DC diagnostics. 3380/3380P test system requires a calibration & diagnosis load board mounted on the test head for DC diagnosis.

Preconditions:
In order to run Diagnostics correctly, the following preconditions should be met:
- The system must turn on correctly — the green System Ok LED on the mainframe control panel should be on.
- The CRAFT system software Focus power is switched on correctly.

DC Diagnostic Executing Procedure:
(1) Click "Load DC Diagnosis" on Maintenance window to prompt the diagnostic user interface (see *Figure 3-26* and *Figure 3-27*).

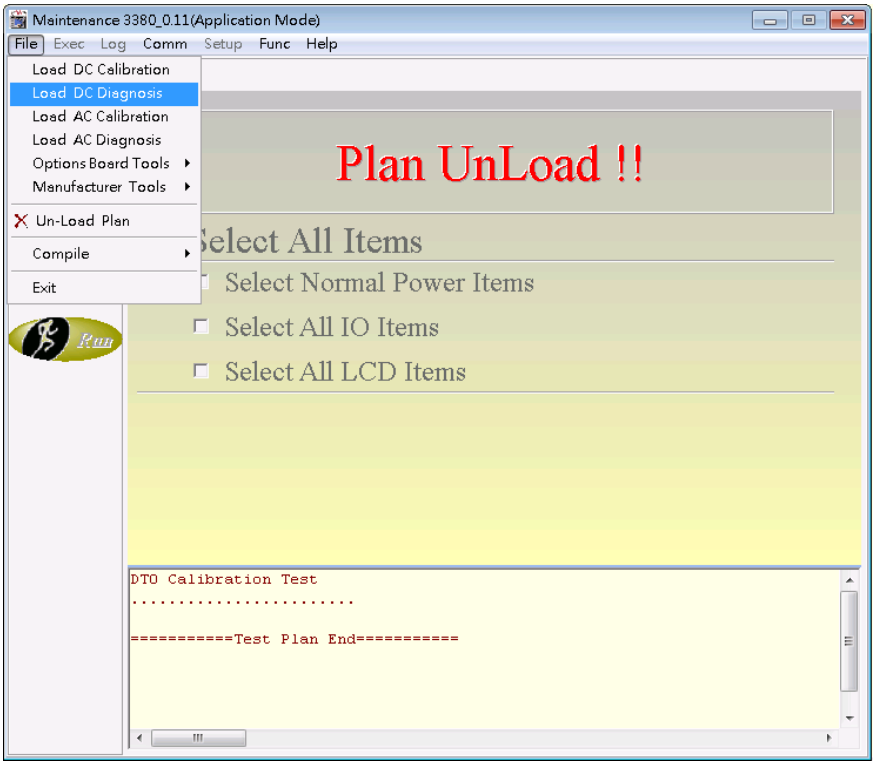


Figure 3-26 DC Diagnosis Window

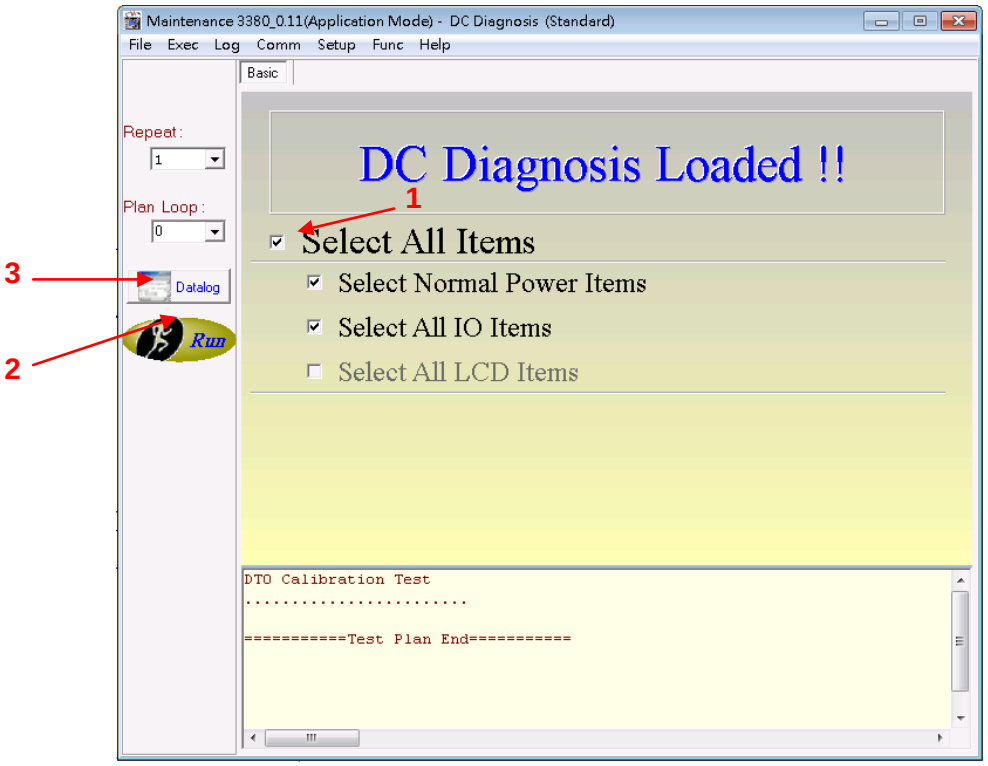


Figure 3-27 DC Diagnosis Window

1 : Mark “Select All Items” or any single item.
2 : Click “Run” to execute DC Diagnosis, and it will prompt a Datalog window.
3 : Click “Datalog” to switch to the Datalog window (refer to *Figure 3-28*).

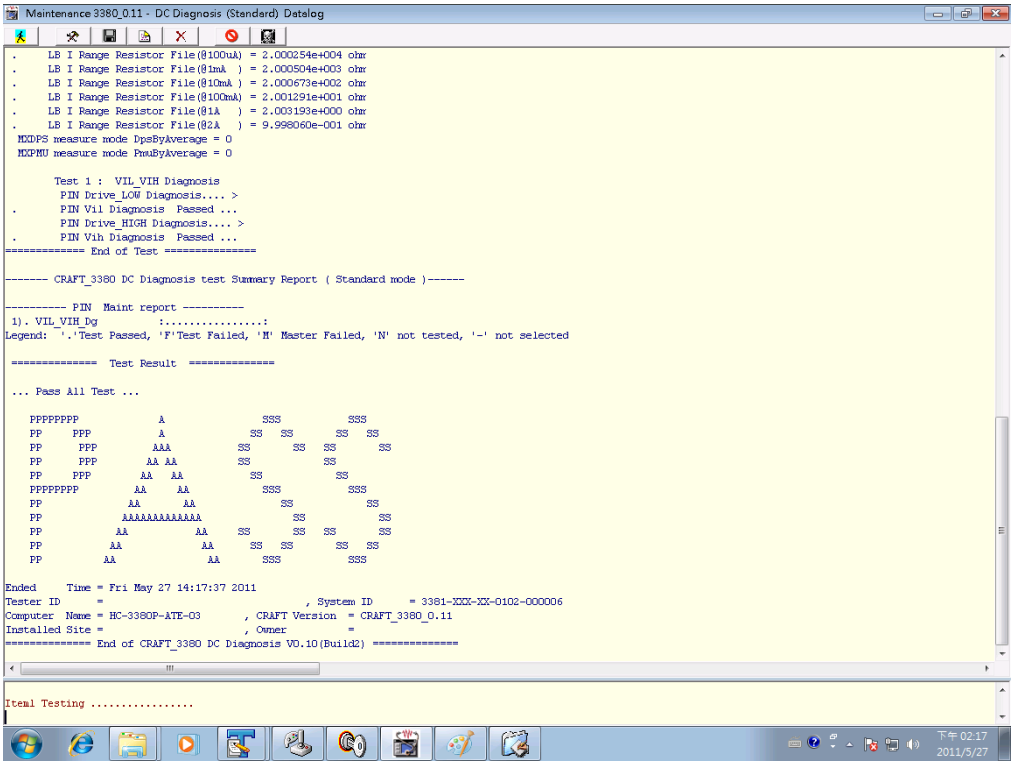


Figure 3-28 DC Diagnosis Datalog

(2) Finish the items and display “DC Diagnosis END”.

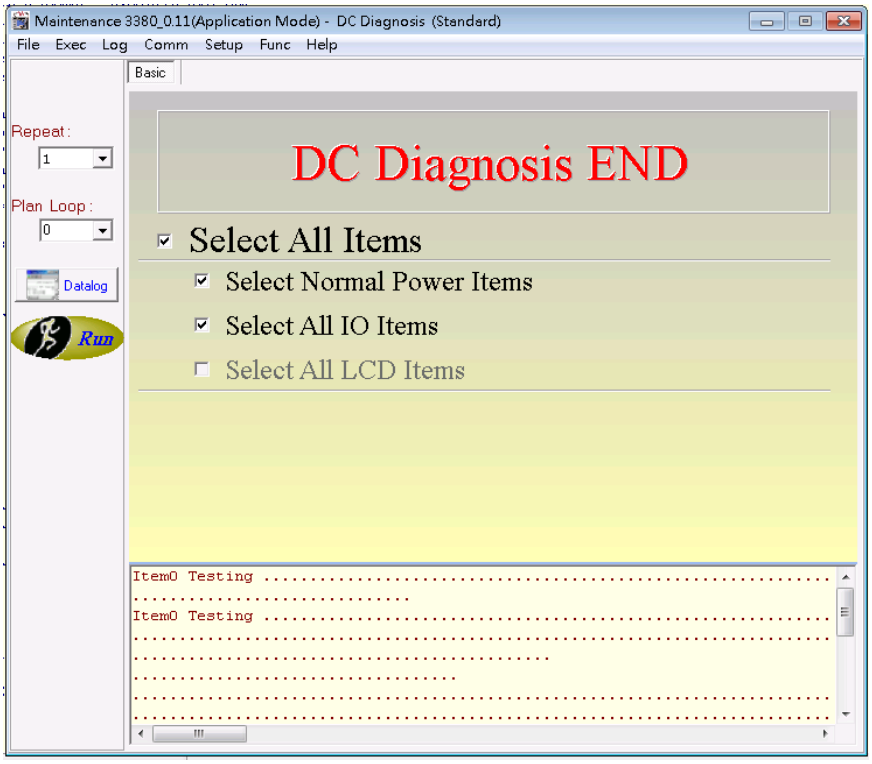


Figure 3-29 DC Diagnosis END

(3) If users un-load DC Diagnosis Plan program, press “File” and “Un-Load Plan.”

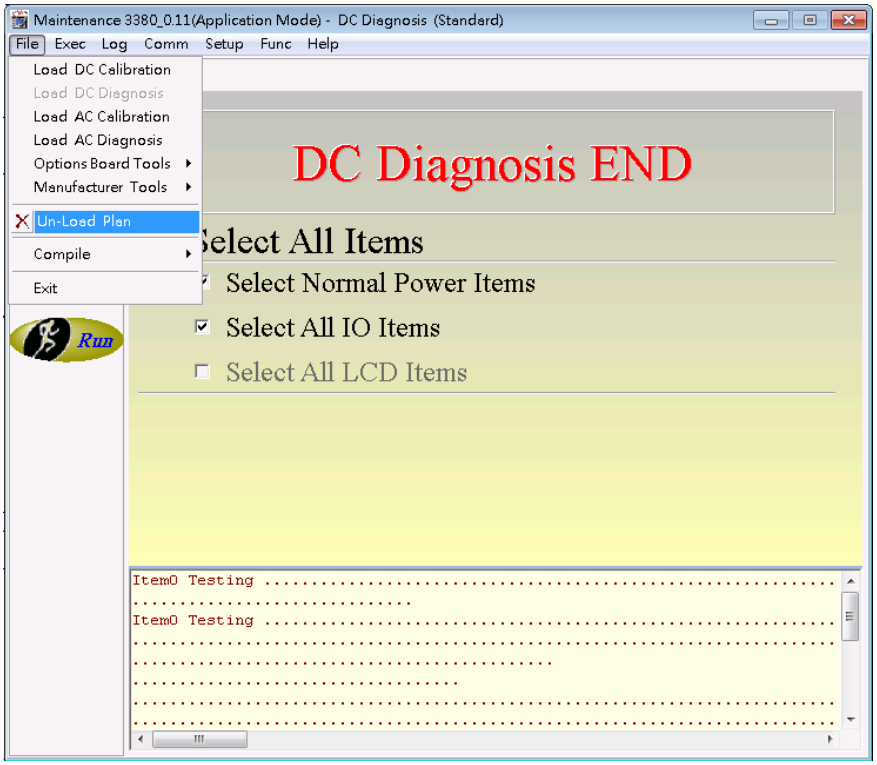


Figure 3-30 Un-Load DC Diagnosis

(4) Then display “Are you sure to quit the DC Diagnosis? ”, and press **Yes** to quit plan program.

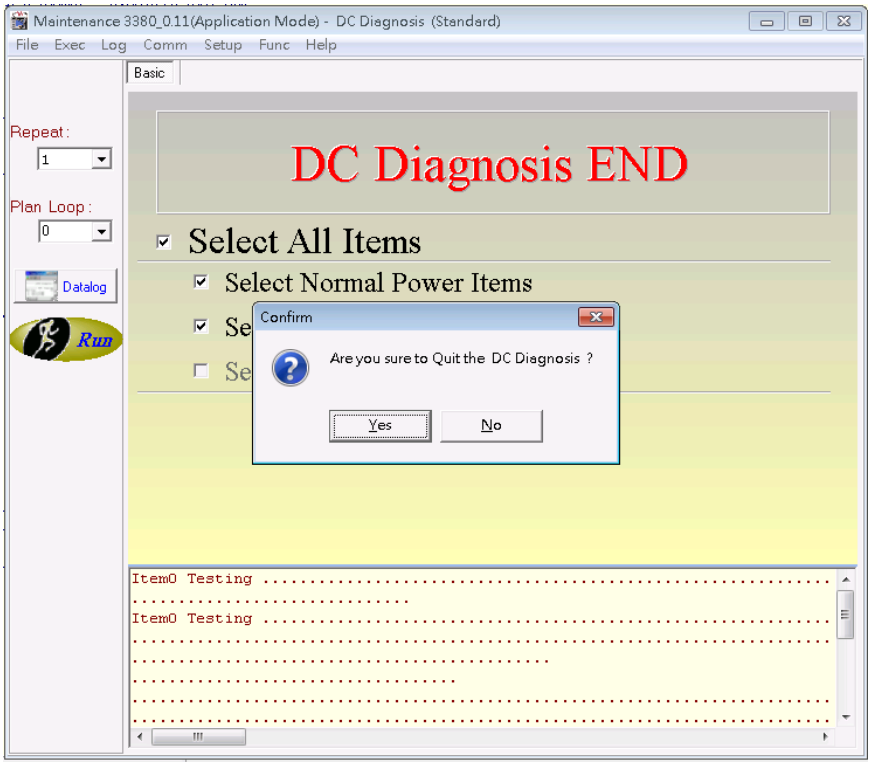


Figure 3-31 Quit DC Diagnosis

3.7 AC Diagnostics

3.7.1 Executing AC Diagnostics

The section describes the procedures to run AC diagnostics.

Procedures:

(1) Click “Load AC Diagnosis” in CRAFT software window as *Figure 3-32* shown. The AC Diagnosis user interface will be appeared (see *Figure 3-33*).

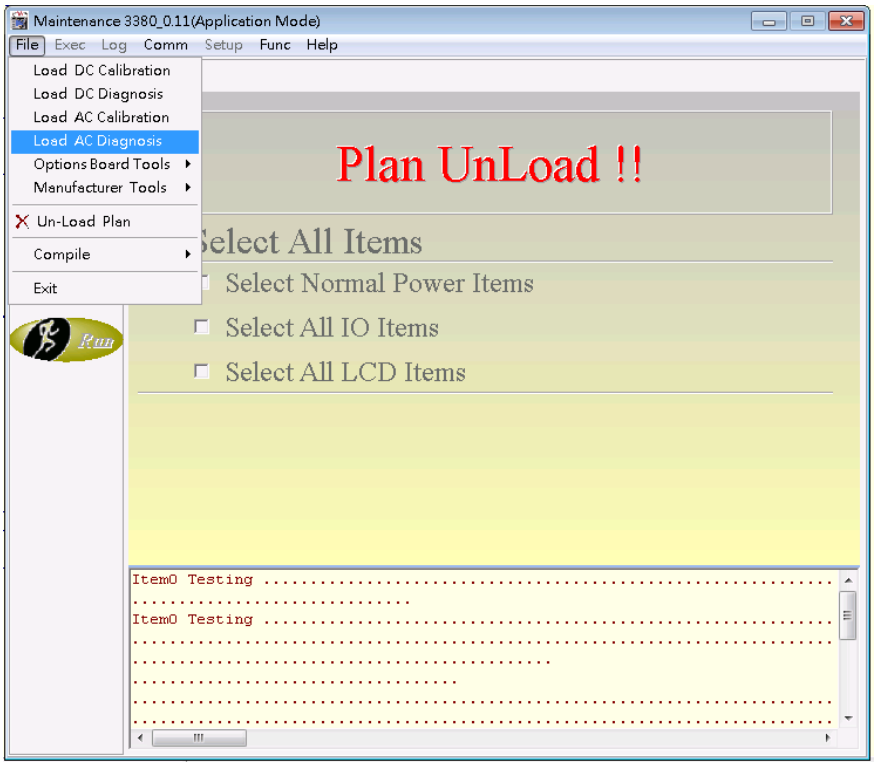


Figure 3-32 AC Diagnosis Window

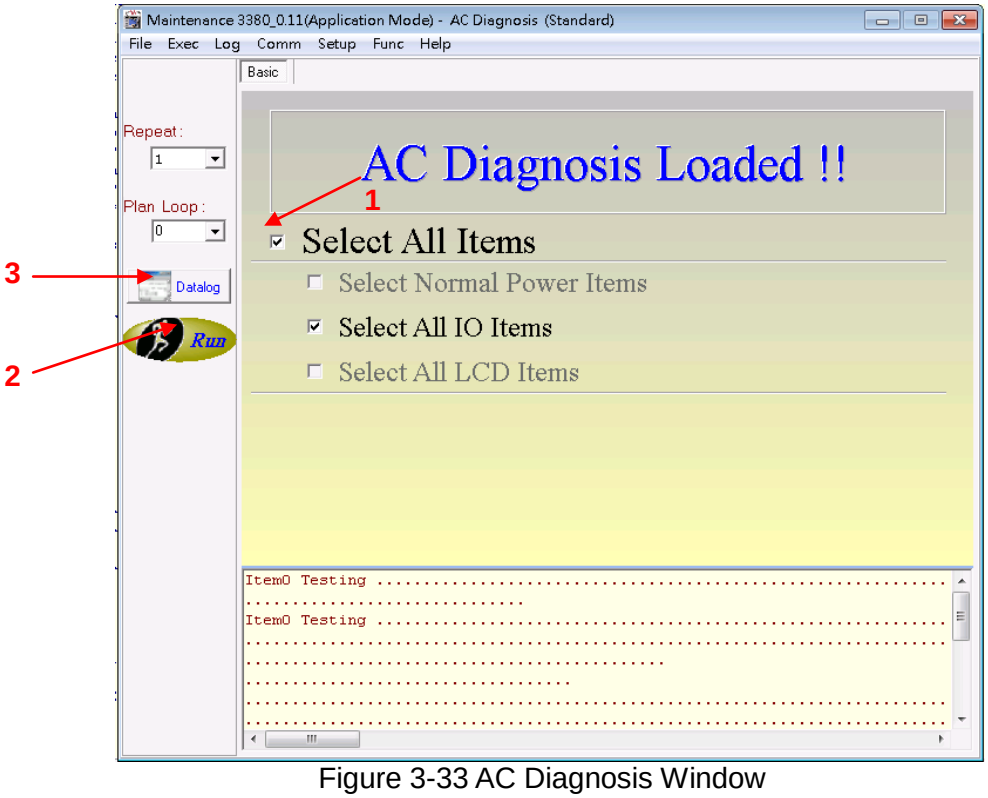


Figure 3-33 AC Diagnosis Window

1 : Mark “Select All Items” or any single item.
2 : Click “Run” to execute AC Diagnosis, and it will prompt a Datalog window.

Note | To execute AC Diagnosis must remove load board.

3 : Click “Datalog” to switch to the Datalog window (refer to *Figure 3-34*).

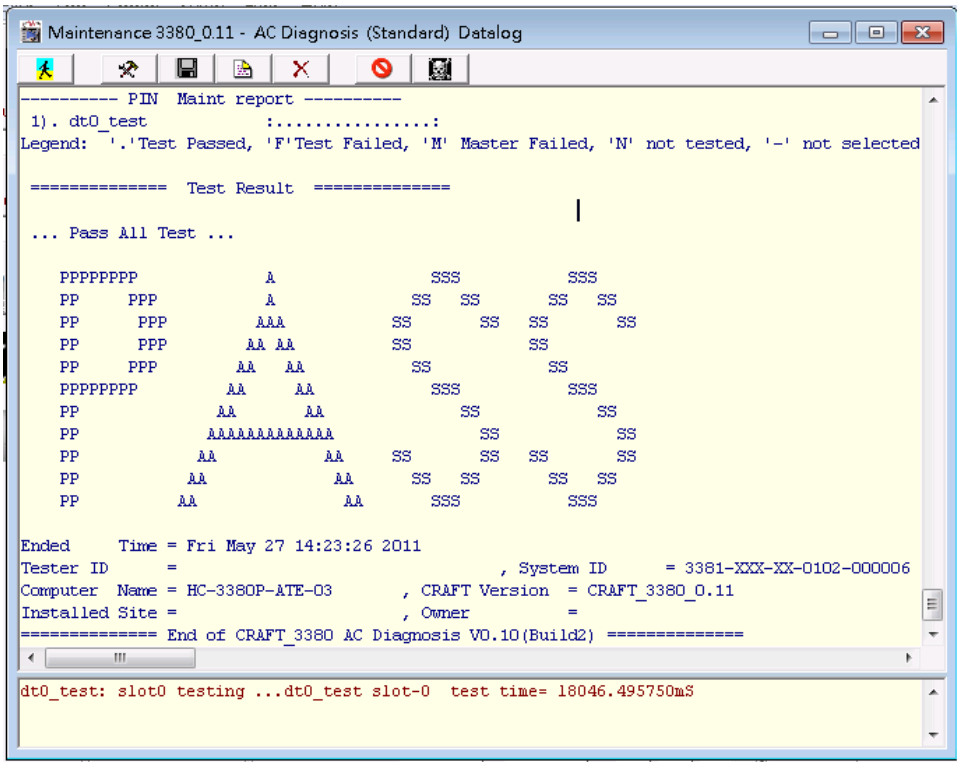


Figure 3-34 AC Diagnosis Datalog

(2) Finish the items and display “AC Diagnosis END”.
(3) If users un-load AC Diagnosis Plan program, select “File” and “Un-Load Plan.”

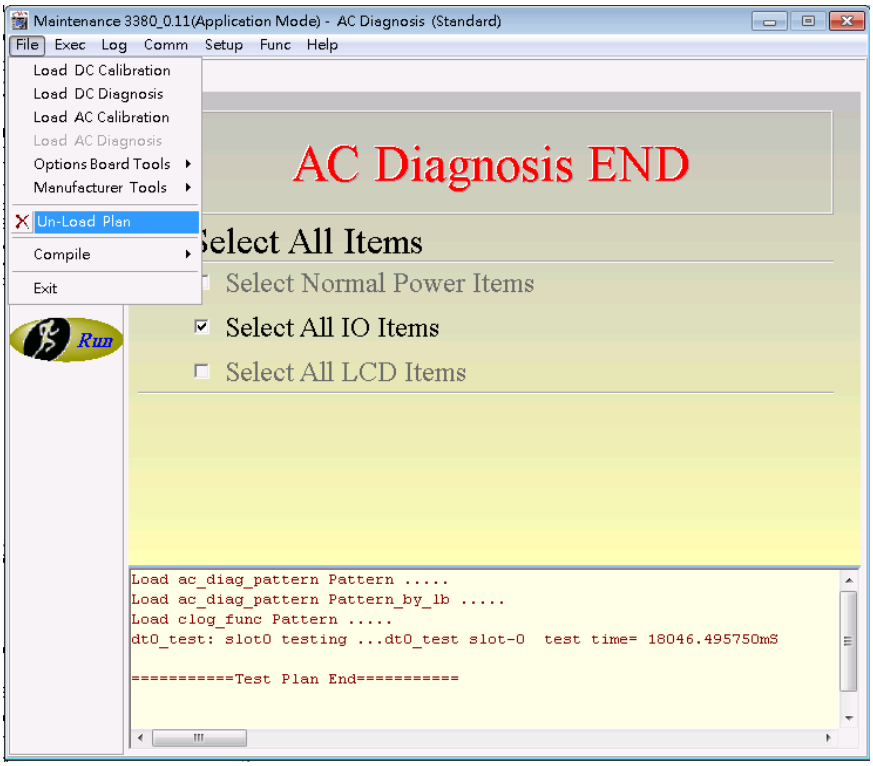


Figure 3-35 Un-Load AC Diagnosis

(4) Then display “Are you sure to quit the AC Diagnosis? ”, and click **Yes** to quit plan program.

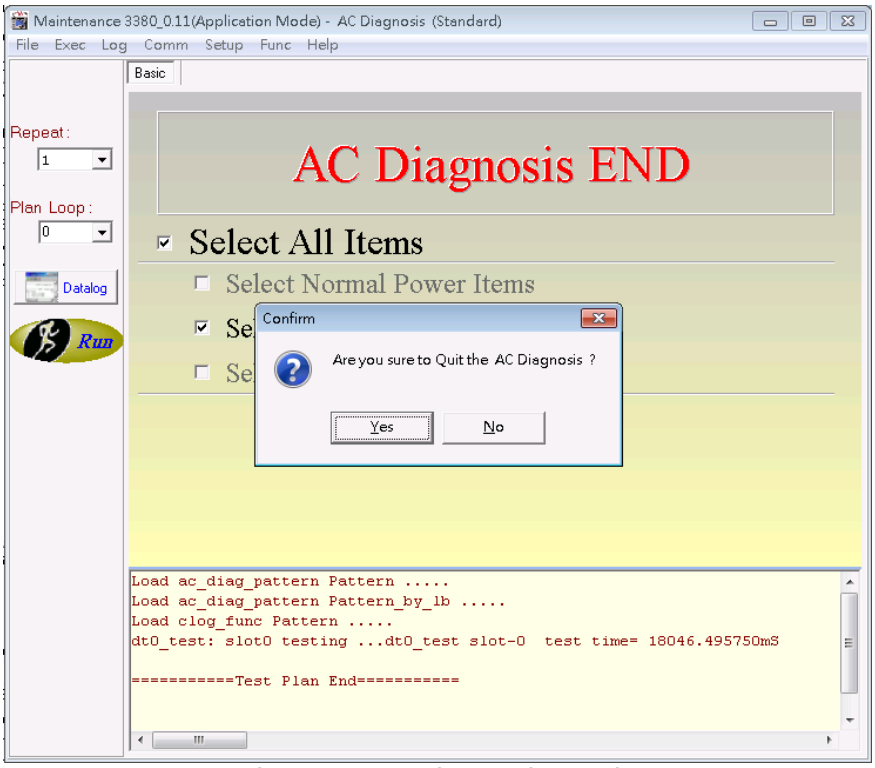


Figure 3-36 Quit AC Diagnosis

3.8 LB Timing Calibration

3.8.1 Executing LB AC Calibration

The section describes the procedures to run LB AC Calibration.

Procedures:

1. Click “Load LB AC Calibration” in CRAFT software window as *Figure 3-37* shown.

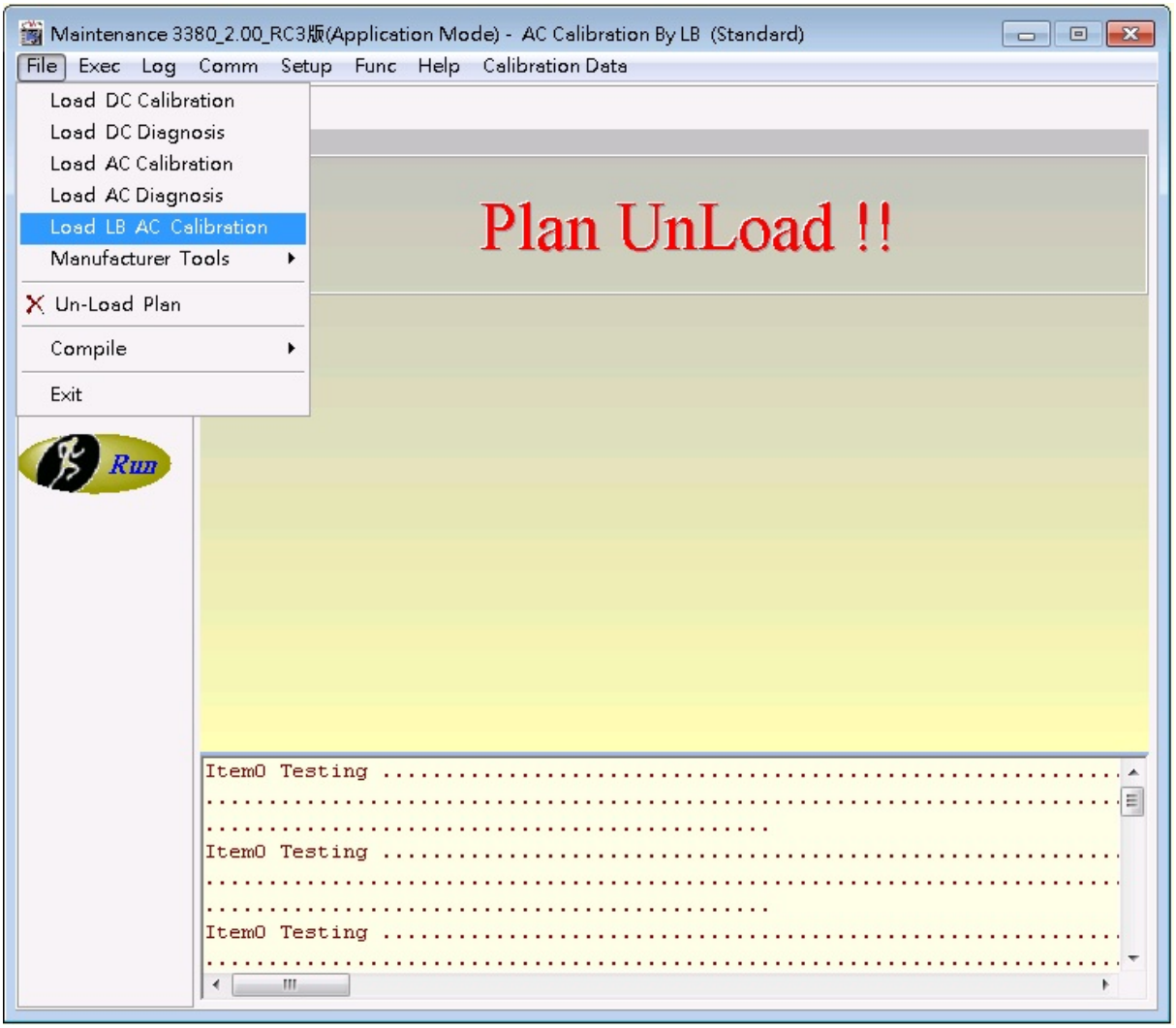


Figure 3-37 AC Diagnosis Window

2. Click “Load LB AC Calibration” in CRAFT software window as *Figure 3-37* shown.

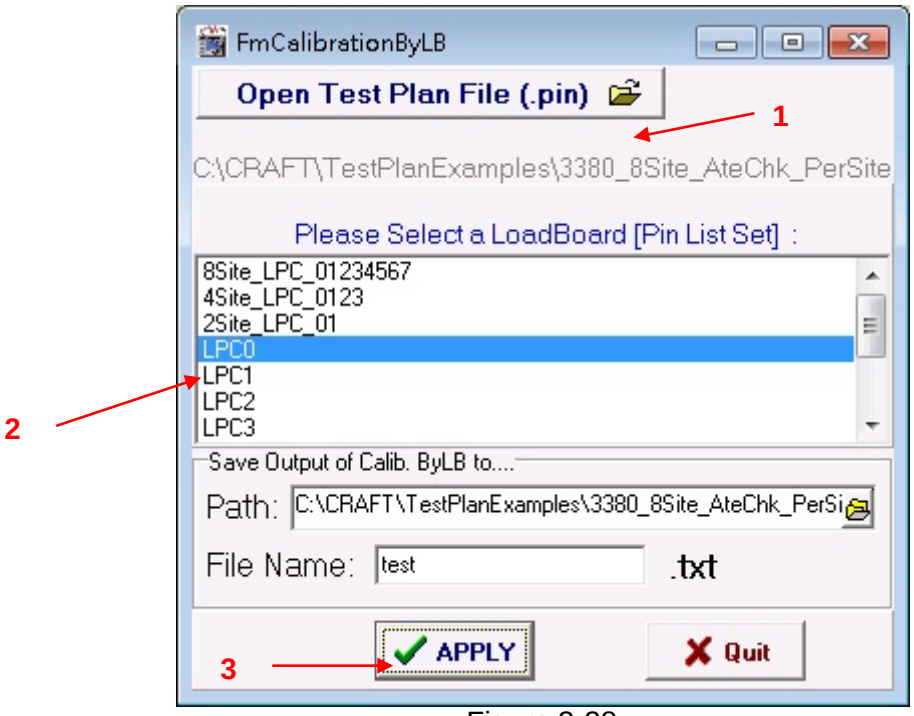


Figure 3-38

1 : Click “Open Test Plan File (.pin)” to select test Program.

2 : Select PIN_LIST

3 : Click “APPLY”

3. Click RUN” in CRAFT software window as *Figure 3-39* shown.

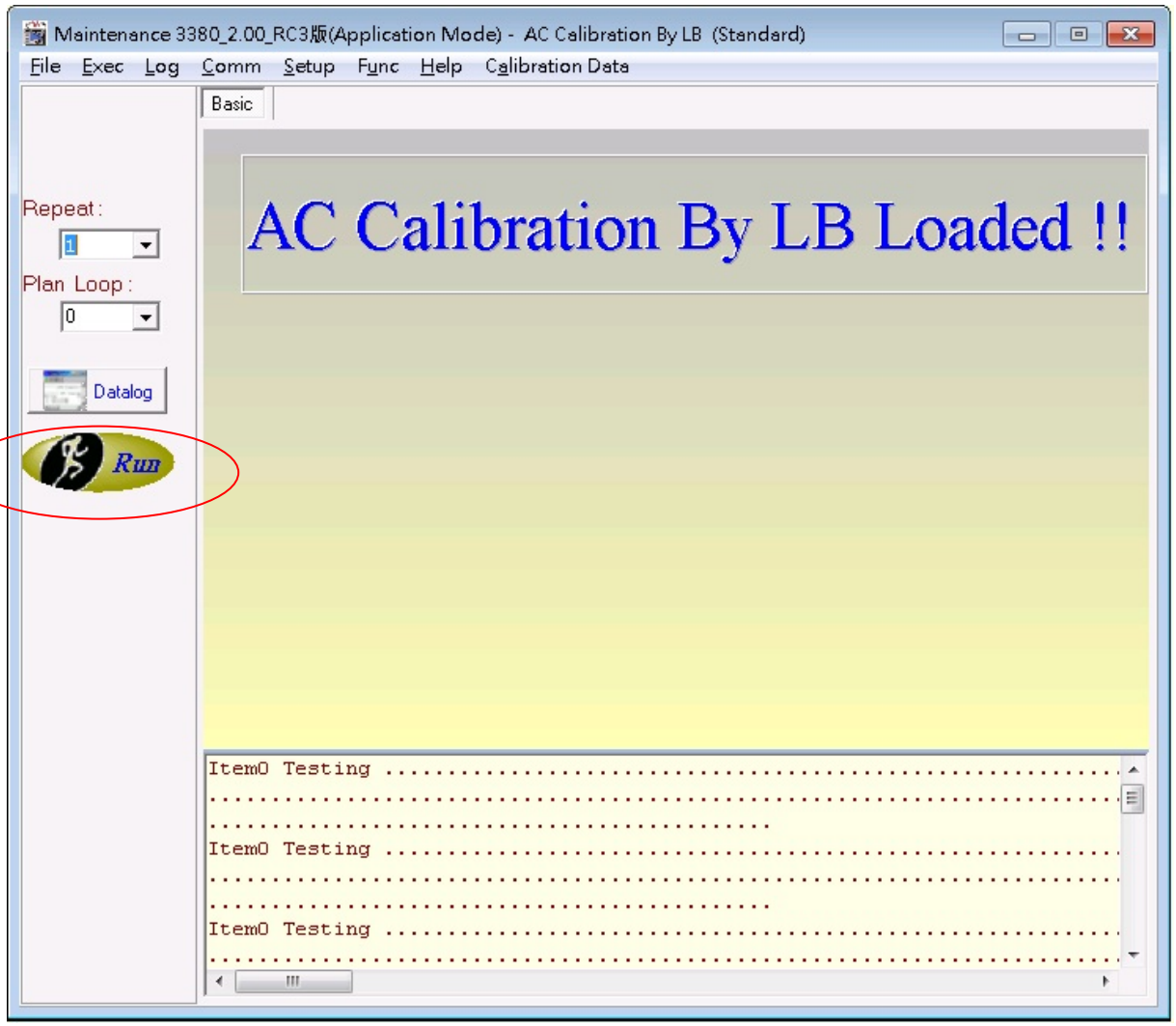


Figure 3-39

4. Check Result is PASS in CRAFT software window as *Figure 3-40* shown.

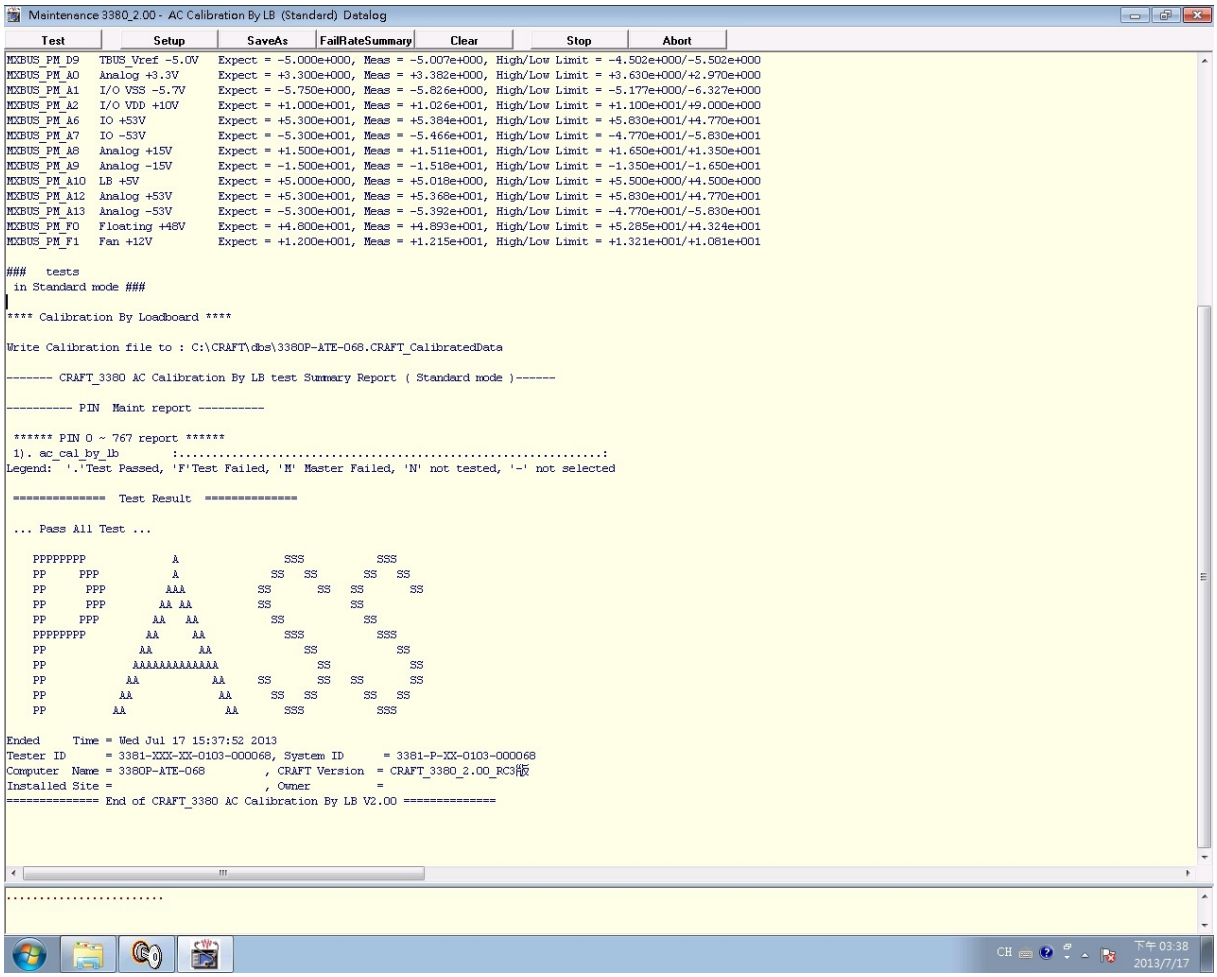


Figure 3-40

5. Check FILE Output in select folder

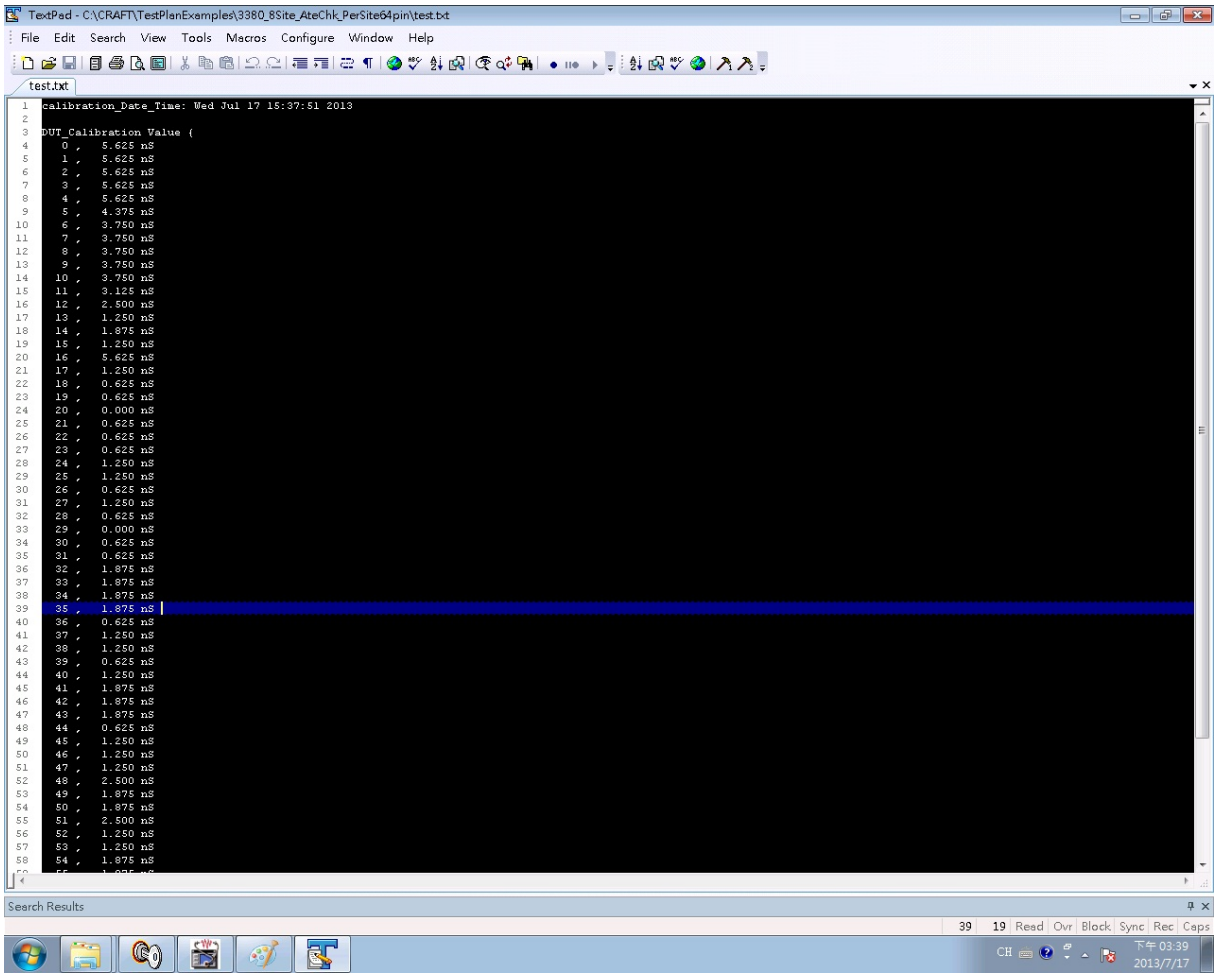


Figure 3-41

6. User use the file by the statement LOAD_FOCUS_CAL_FILE() at START_UP() in test Plan. (Refer to Language Manual)

```
START_UP()
{
   LOAD_FOCUS_CAL_FILE(TDR,"../AC_TDR.txt","3381-IO512-0102-RT");

   SET_LEVELN(rst_lvl, IO_ALLPINS, 0.0V, 0.0V, 0.0V, 0.0V, 0.0mA, 0.0mA, 0.0V, -2V, 7V);
   LEVELS(rst_lvl, 3mS);
   RELAY_OFF( IO_ALLPINS,PDCL, 1mS);
   LOAD_PAT("./PAT/3380_atechk_pat.ppo");
       }
```

Figure 3-42

4. Inspection SOP for 3380 Vacuum System

4.1 Getting Started

Follow SOP to find air leakage position quickly that helps to get vacuum failure problem and exclude air leakage doubt.
This is only support 3380(Model:3380)

4.2 Tool Used

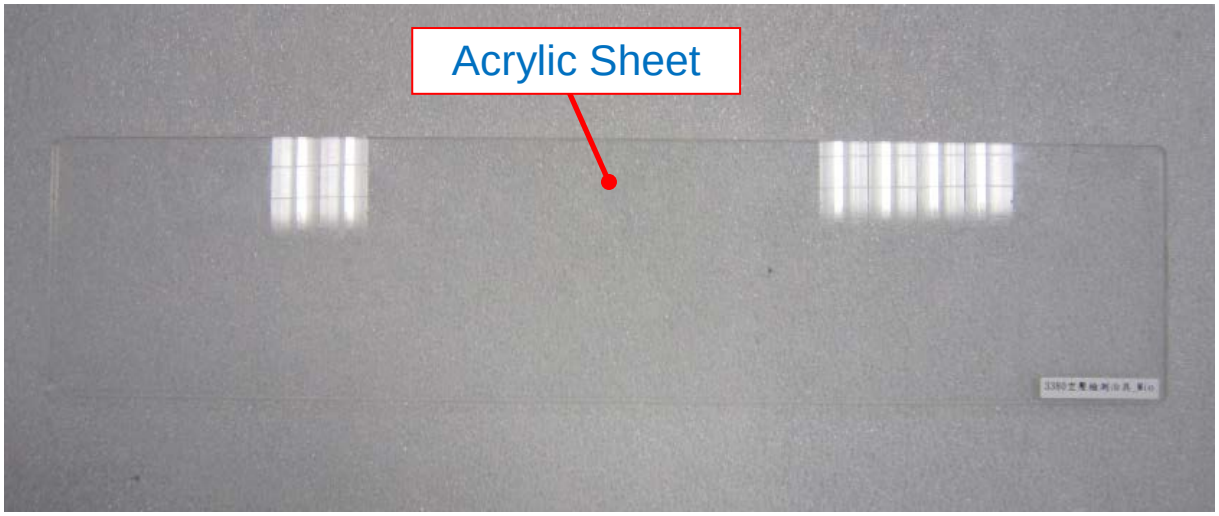


Figure 4-1 Acrylic Sheet

4.3 Introduction

Component of vacuum system includes two parts:

(1) Mainframe: It consists of air filter regulator, three-way magnetic valve, vacuum generator, vacuum solenoid valve and noise filter as *Figure 4-2* shows.

(2) Test Head: It consists of start button of vacuum system and digital pressure meter as *Figure 4-3* shows.

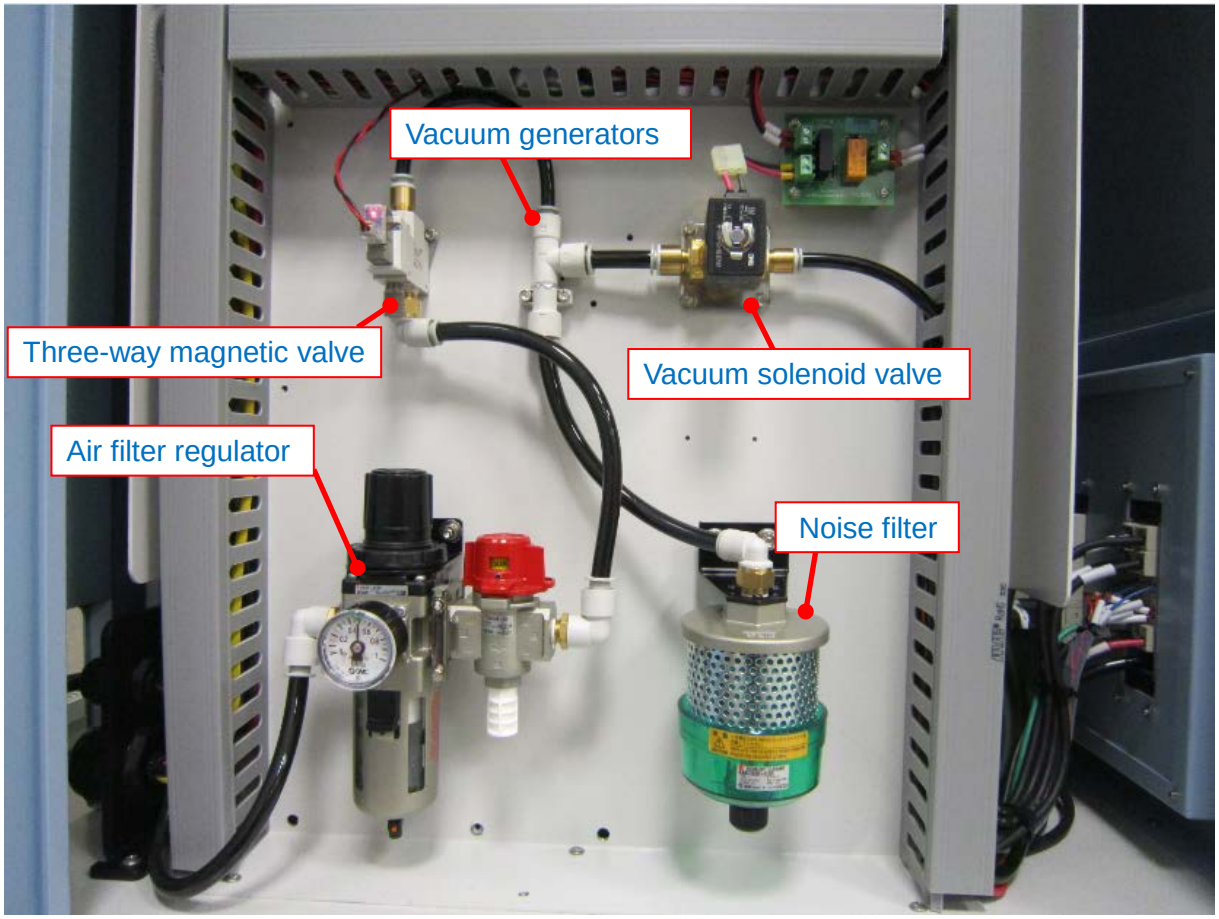


Figure 4-2 Vacuum system diagram

4.4 Inspection

4.4.1 Vacuum Pressure Abnormality

Negative pressure: It indicates gaseous state is lower than atmospheric pressure that is “vacuum” we called. The system is suggested not lower than -70Kpa when vacuum pressure is insufficient. The value can be observed from digital pressure meter at left of Test Head, for more detail see *Figure 4-3*. It means there is a certain part under air leaking that causes vacuum pressure value too low. Next to exclude the reasons of generating vacuum pressure too low.

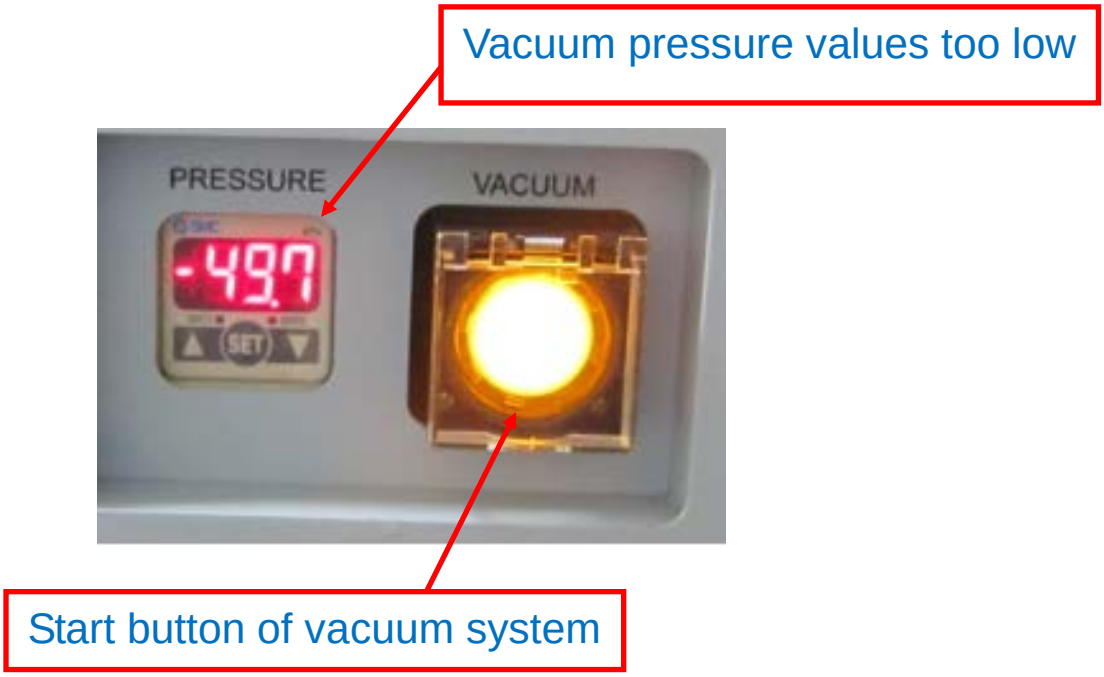


Figure 4-3 Vacuum pressure values too low example

The reasons for causing vacuum pressure insufficient are as follows.
(1) Air tube is loosened.
(2) Airtight rubber seal is broken.
(3) O-ring on Pin Block is broken.

4.4.2 Vacuum Absorbing Zone

Lock positioning plate set-A and positioning plate set-B to the machine if air tube inspection above described is without air leakage condition as *Figure 4-4* shows. Positioning plate set-A and positioning plate set-B each has a set of vacuum absorbing zone in red hatch.

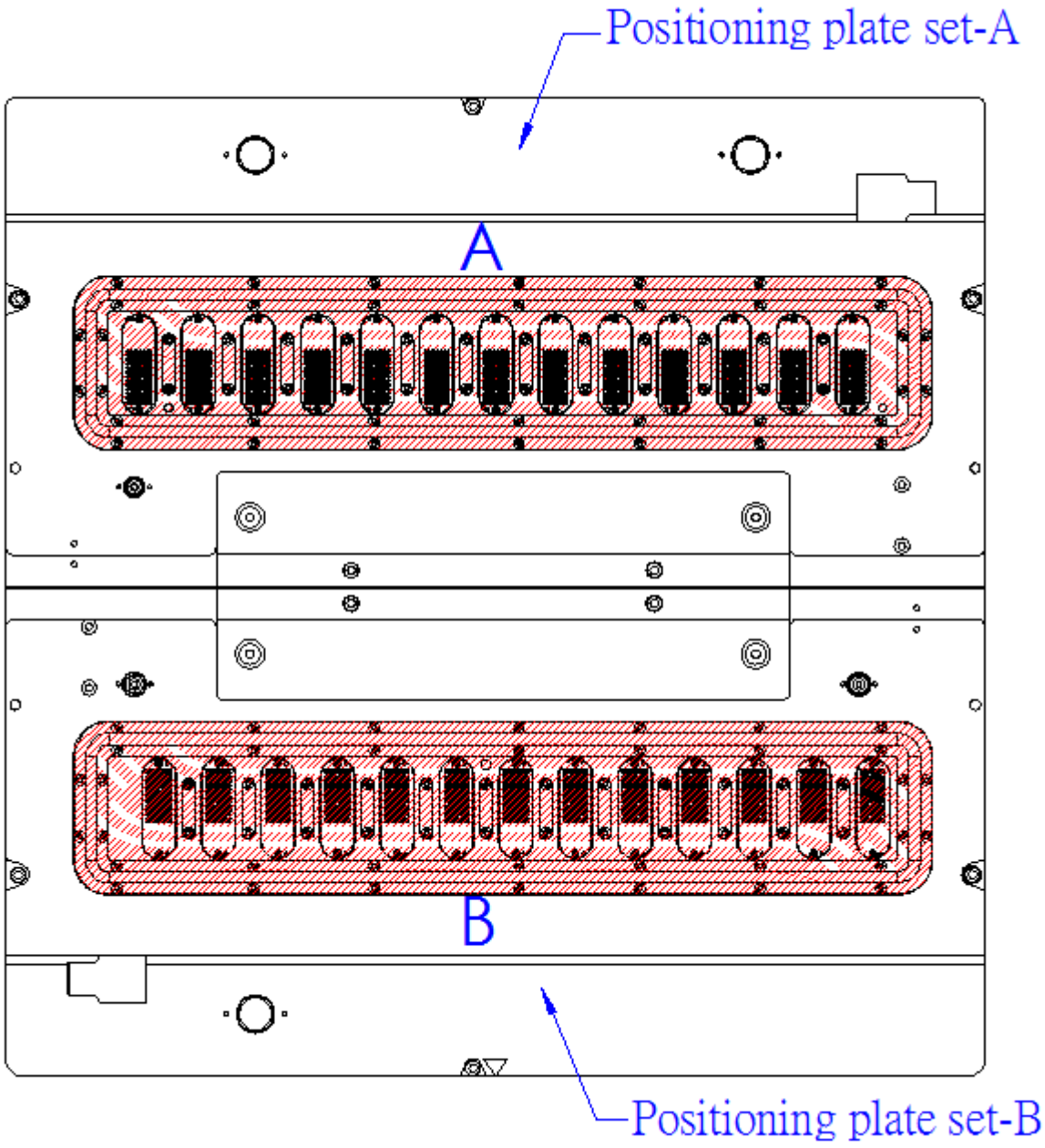


Figure 4-4 Inspection zone of vacuum system

4.4.3 Vacuum Absorbing Hole

There are 3 vacuum absorbing holes as red circle in *Figure 4-5*, positioning plate set-A contains 2 holes and set-B contains 1 hole. Pull away the air in the zone to get vacuum effect that Load Board can contact with pogo pin. The generated negative pressure is much larger than stylus pressure of Pogo Pin thus it makes Load Board to sink.

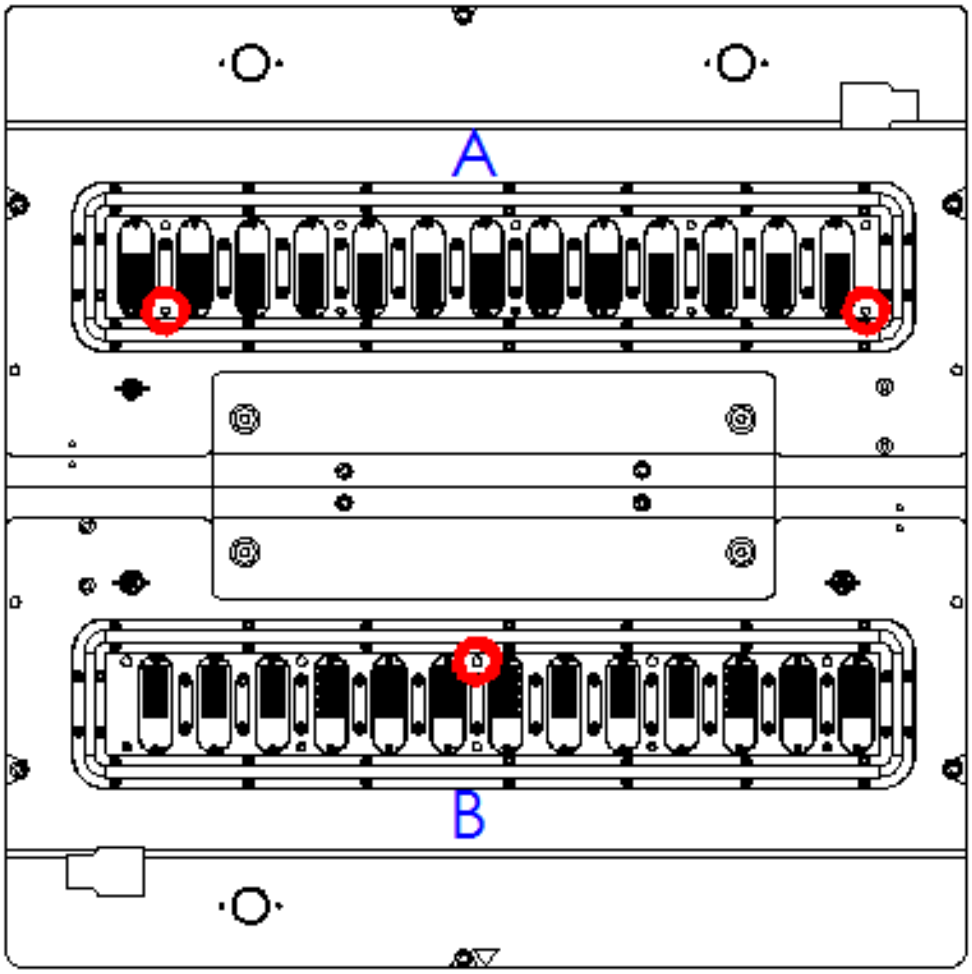


Figure 4-5 Vacuum absorbing hole

4.5 Testing Gas Density for Air Tube

Perform gas density test for air tube first and exclude air leakage problem one by one.

Step 1: Plug vacuum absorbing hole on positioning plate set-A and positioning plate set-B with fingers as *Figure 4-6* shows.

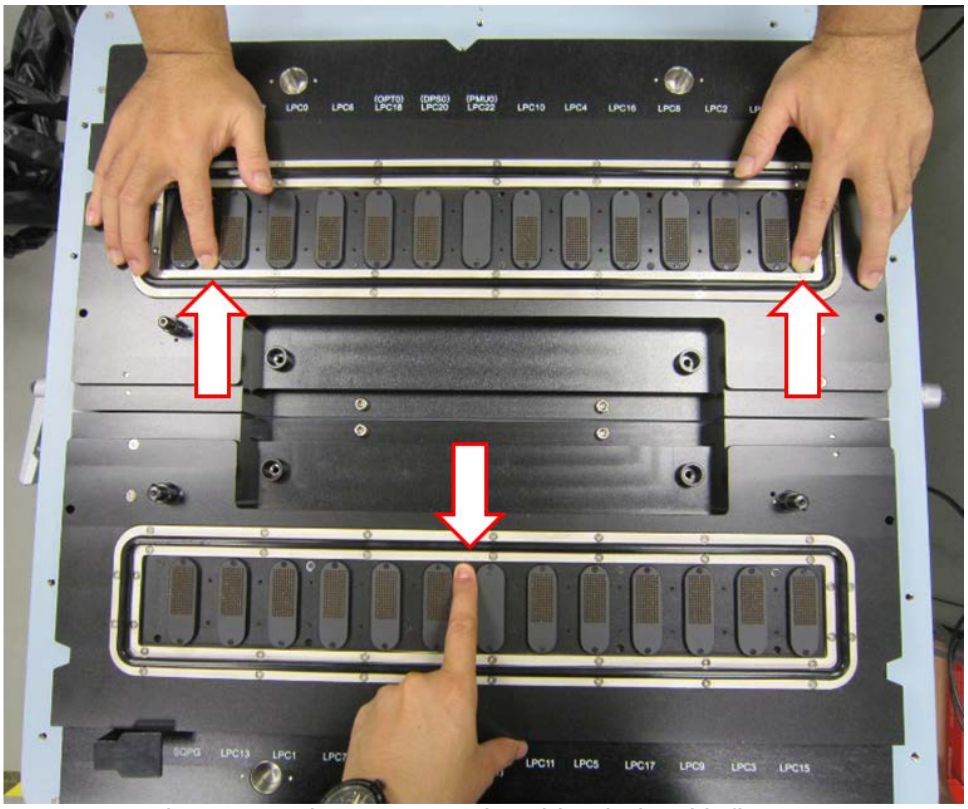


Figure 4-6 Plug vacuum absorbing hole with fingers

Step 2: Press start button of vacuum system to observe whether air pressure value of digital pressure switches are normal.
Two conditions as below will be occurred.

(1) It indicates air tube is without air leakage when air pressure value is larger than -70Kpa as *Figure 4-7* shows. Then go to *4.6 Testing Vacuum Gas Density for Single Zone*.

(2) It indicates air tube has air leakage condition when air pressure value is smaller than -70Kpa. Next go to the step 3.

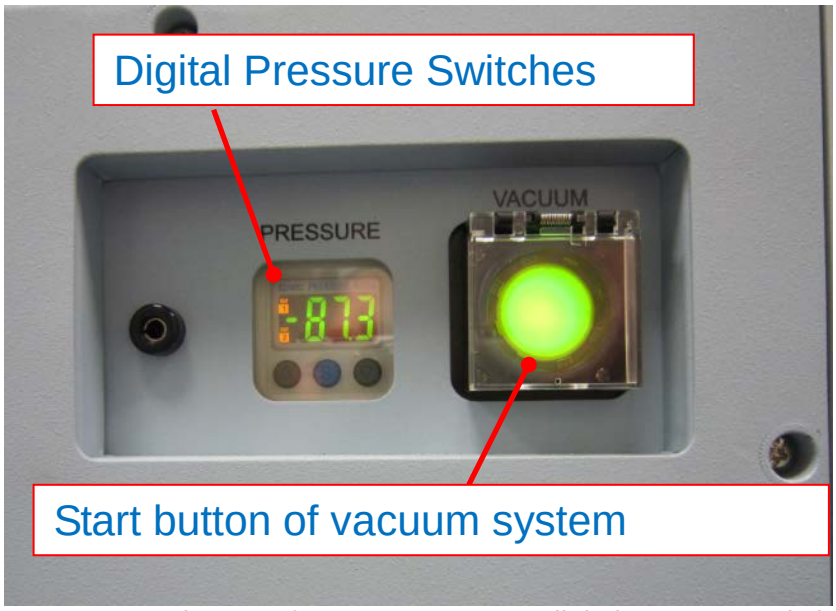


Figure 4-7 Start button of vacuum system & digital pressure switches

Step 3: Check whether the air tube on rear panel of positioning plate set-A and positioning plate set-B is loosened. Plug the air tube tight into air pressure connector if it is loosened.

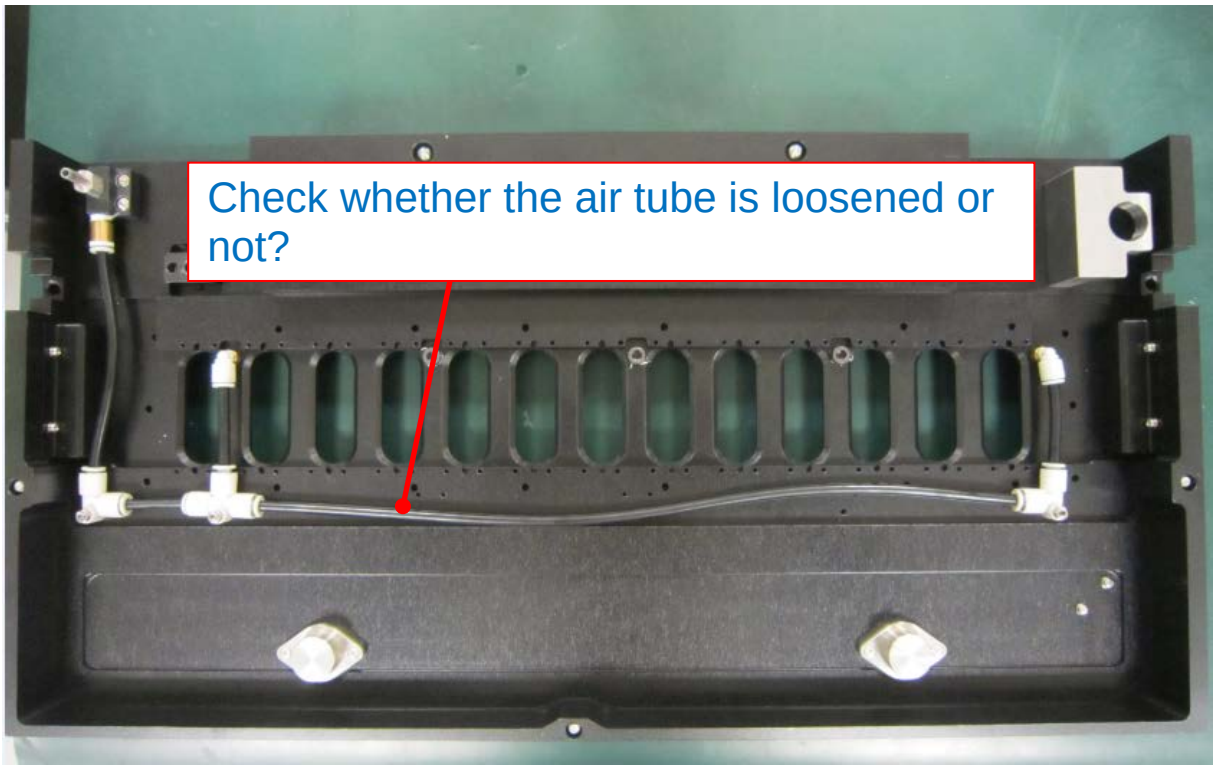


Figure 4-8 Rear panel of positioning plate set-A

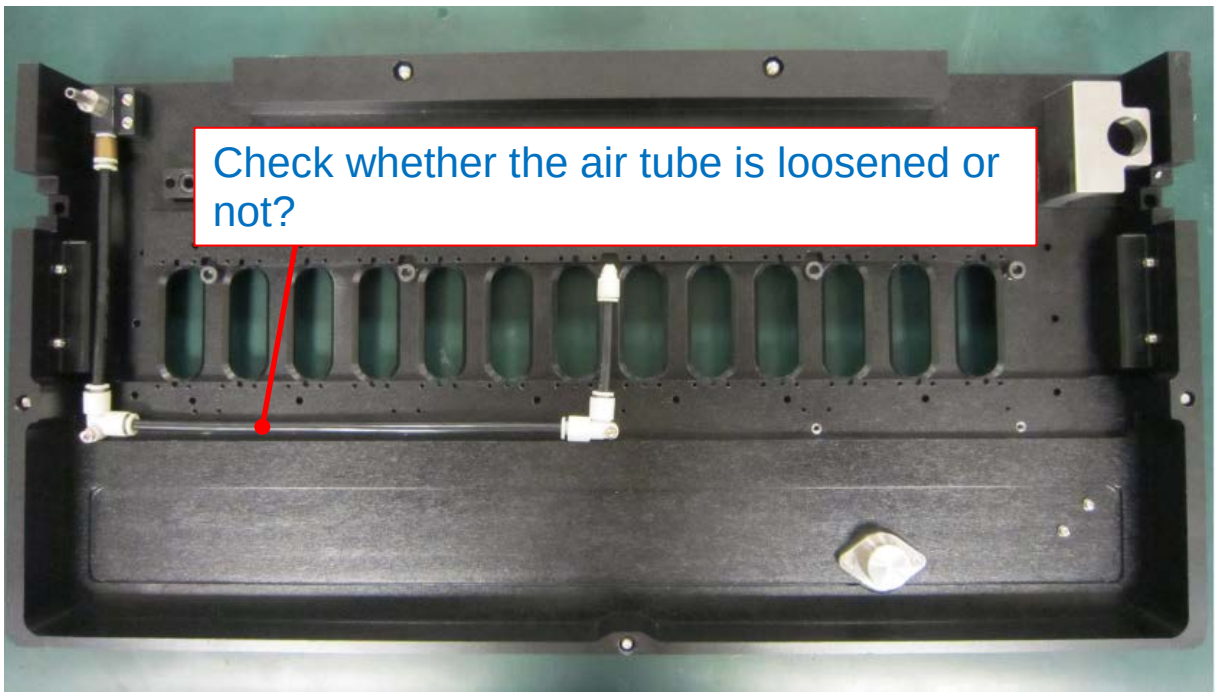


Figure 4-9 Rear panel of positioning plate set-B

4.6 Testing Vacuum Gas Density for Single Zone

4.6.1 Tool Used

Acrylic sheet is shown as *Figure 4-10*.

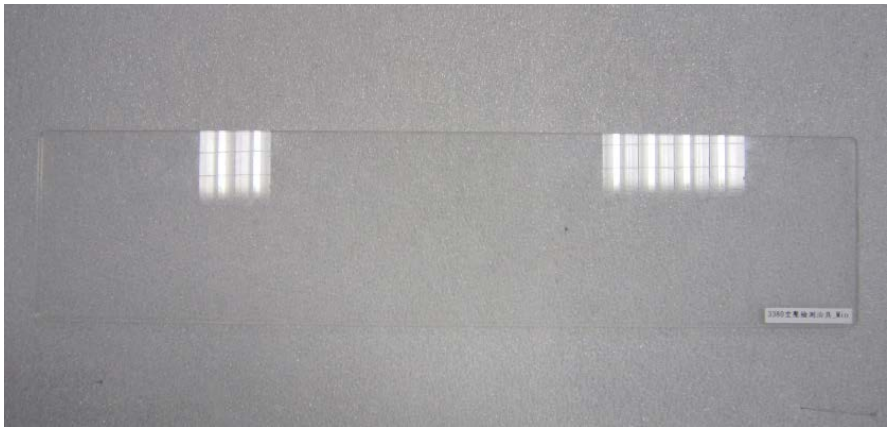


Figure 4-10 Acrylic Sheet

4.6.2 Testing Gas Density

Take zone A as an example:
Step 1: Place acrylic sheet on the top of zone A first as *Figure 4-8* shows.

Step 2: Plug the vacuum absorbing hole on zone B with fingers as *Figure 4-11* shows.

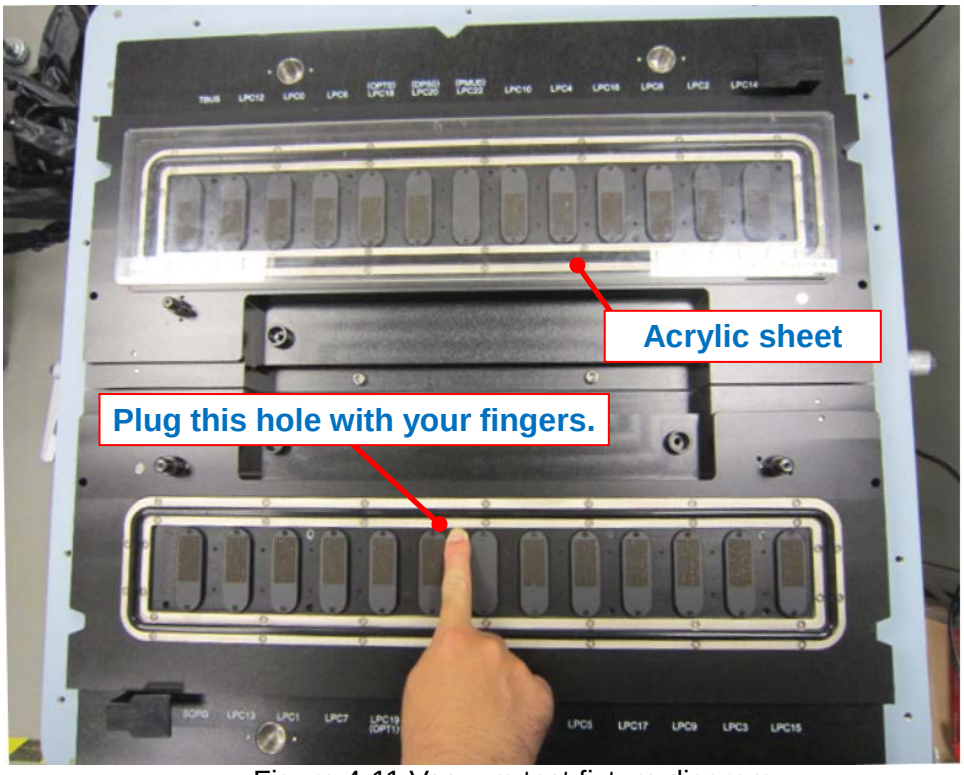


Figure 4-11 Vacuum test fixture diagram

Step 3: Press start button of vacuum system to observe the value of digital pressure switches as *Figure 4-12* shows. It is for distinguishing whether zone A contains air leakage condition.

After calculating formula and comparing the converted values of stylus pressure and vacuum pressure, the read values by pressure switch can't be lower than -40Kpa. It may cause Pogo Pin pressure higher than vacuum pressure that will result in acrylic sheet unable to sink. Wait the test in zone A is completed and follow the method to test whether air leakage is existed in zone B.

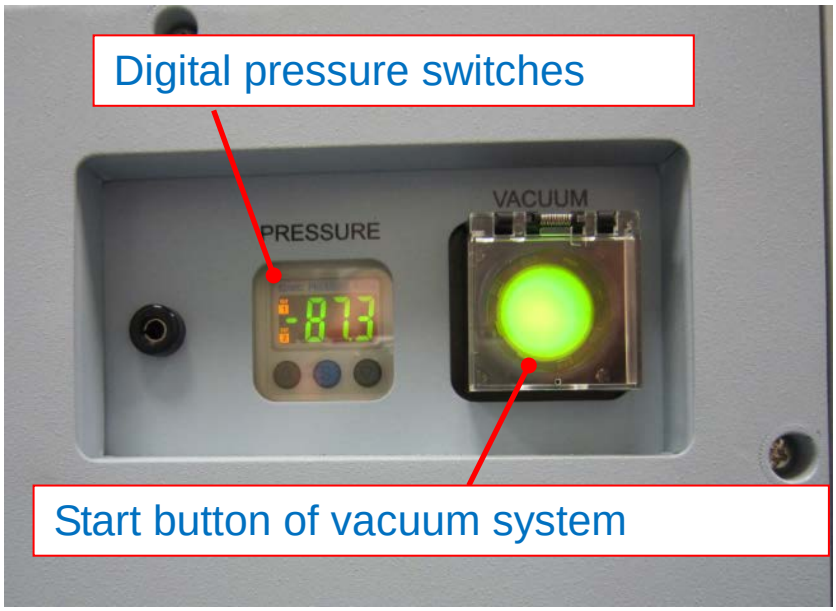


Figure 4-12 Start button of vacuum system

4.7 Check Airtight Rubber Seal

Find air leakage zone by the methods are described above. To assume the measured value in zone A is -45Kpa and in zone B is -83Kpa that indicates zone A with the doubt of air leakage and next to check whether airtight rubber seal on positioning plate set-A is broken or slash. Replace it immediately if broken is occurred. Airtight rubber seal broken condition is shown as *Figure 4-14*.

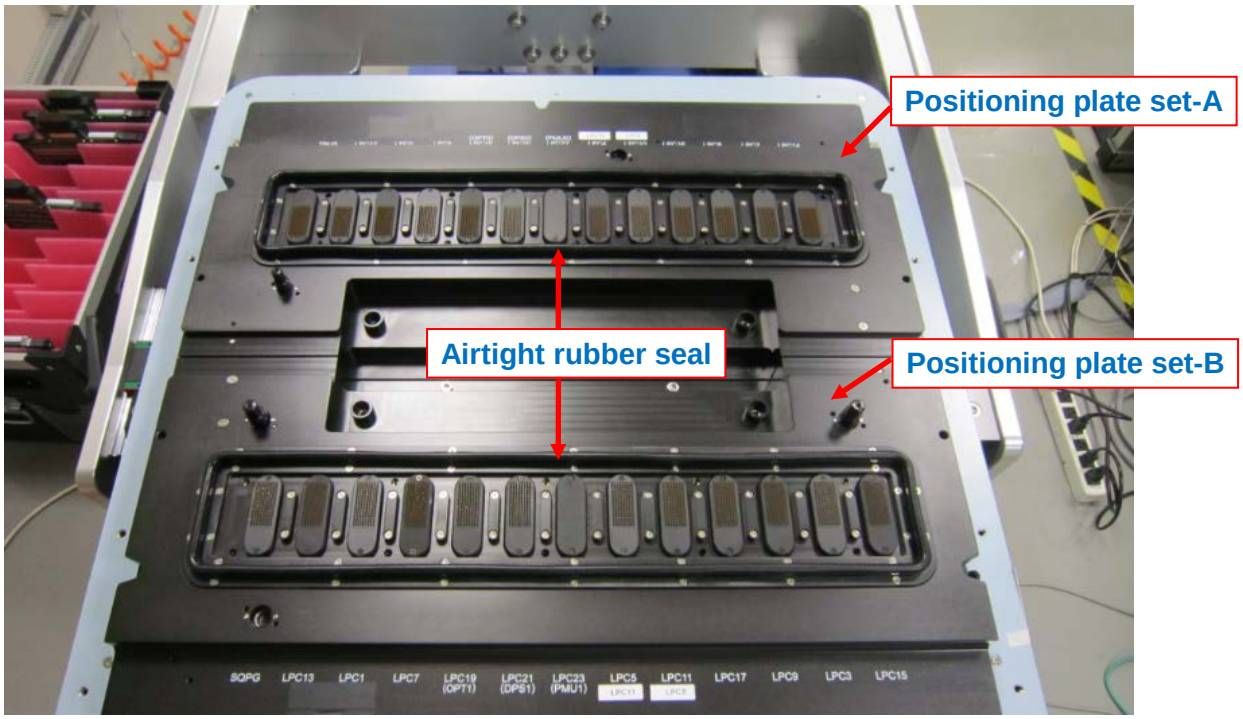


Figure 4-13 Airtight rubber seal position

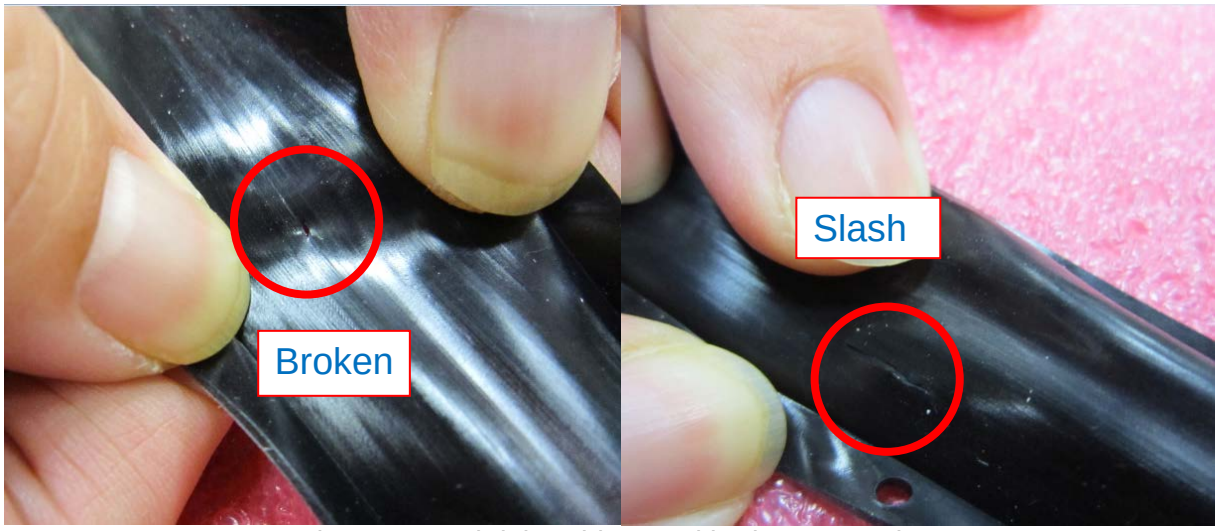


Figure 4-14 Airtight rubber seal broken example

4.8 Check O-ring

If airtight rubber seal is without broken condition, use No. 5 hex wrench to disassemble five M6 countersunk head screws on positioning plate set-A. Unscrew the screws that in red circle for removing positioning plate set-A as *Figure 4-15* shows. The disassembled method of positioning plate set-B is the same as A.

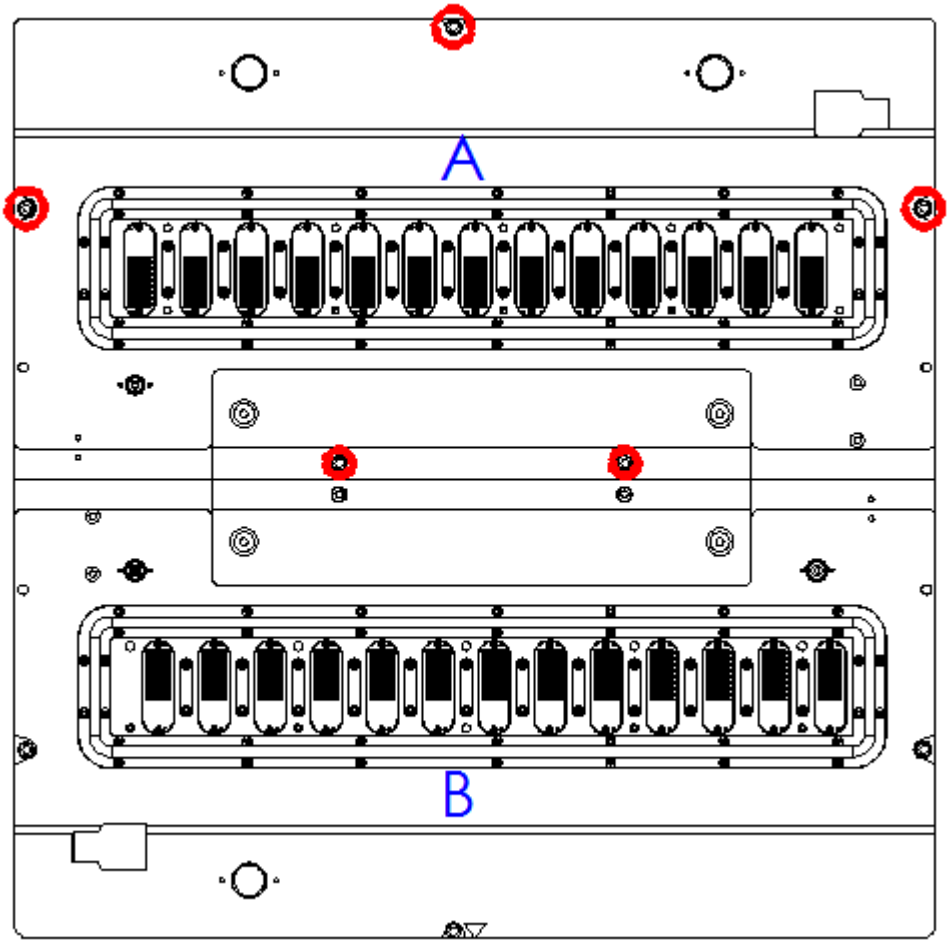


Figure 4-15 Screws removal location of positioning plate set-A

Next to check Pin Block on single plate as *Figure 4-16* shows. There is a Pin Block on each single plate and an O-ring on each Pin Block as *Figure 4-17* shows. Check whether O-ring on pin block is broken or slash. Replace it immediately if broken is occurred. O-ring broken condition is shown as *Figure 4-18*.

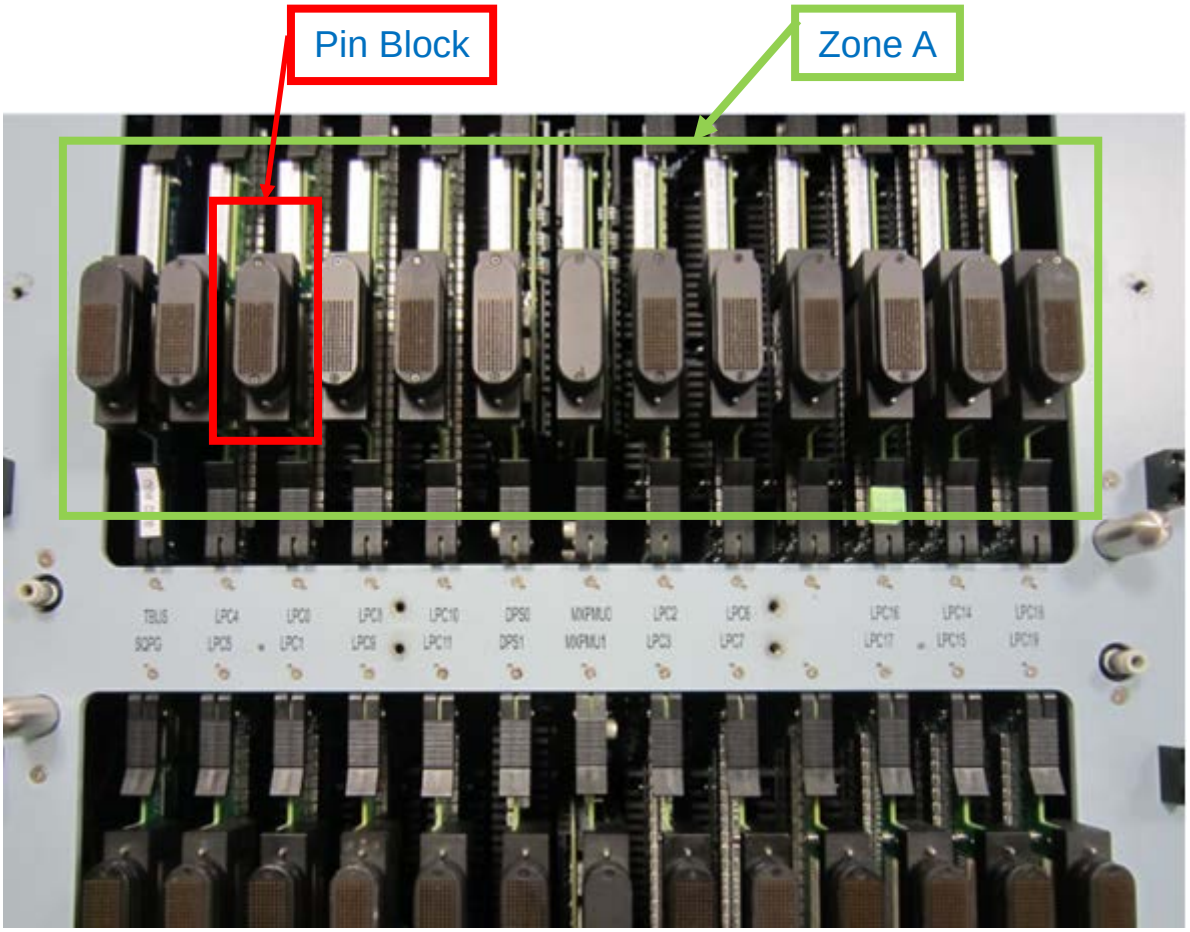


Figure 4-16 Pin Block on single plate

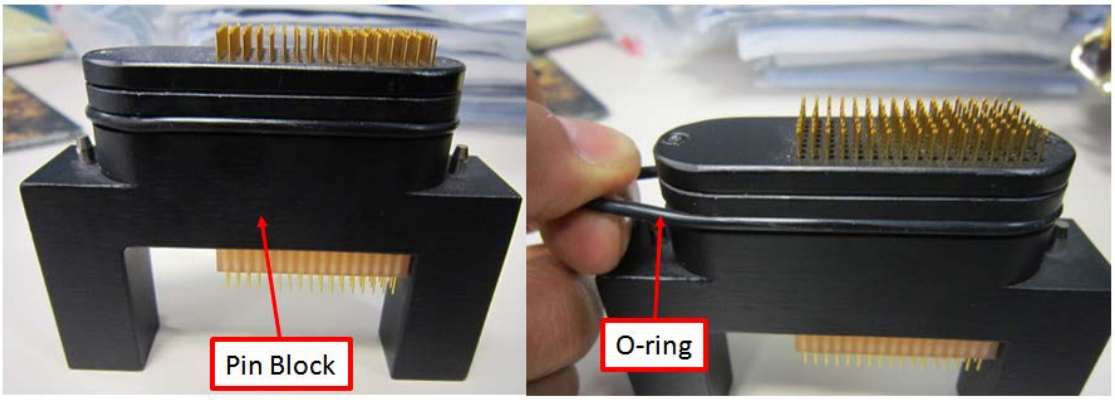


Figure 4-17 O-ring on Pin Block

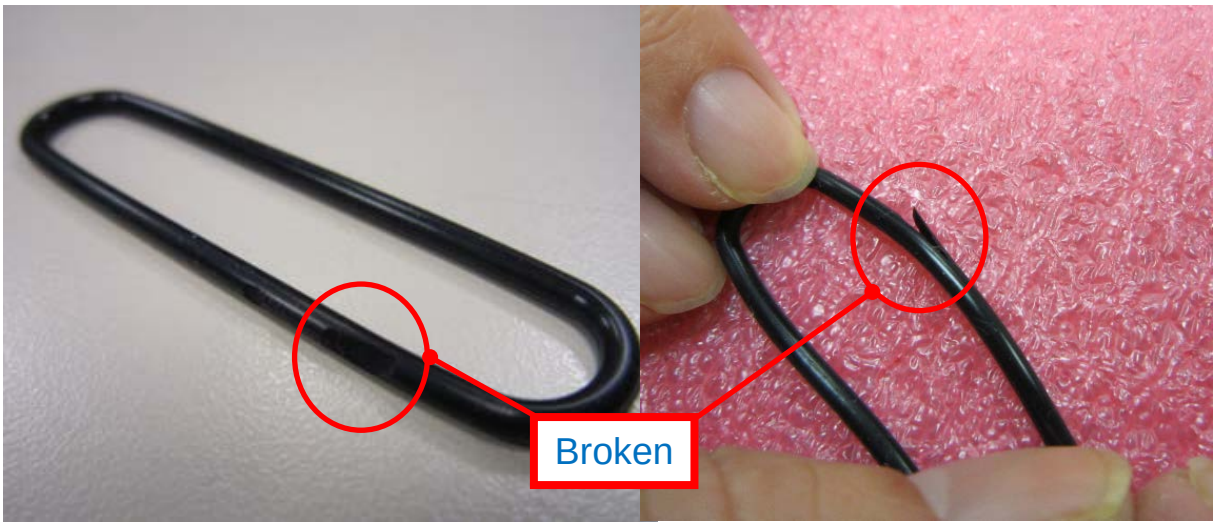
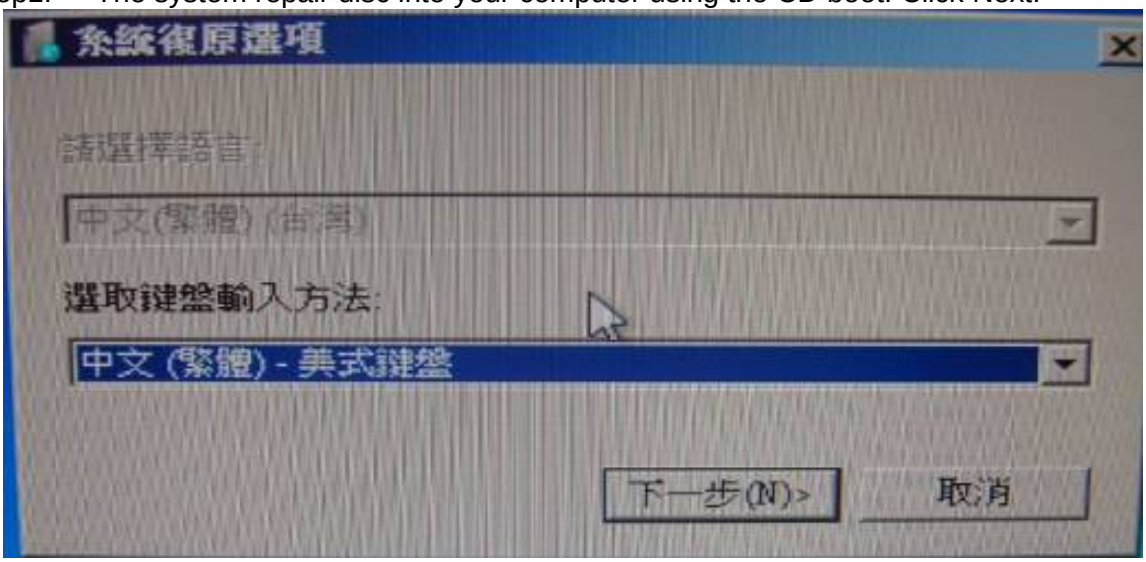


Figure 4-18 O-ring broken

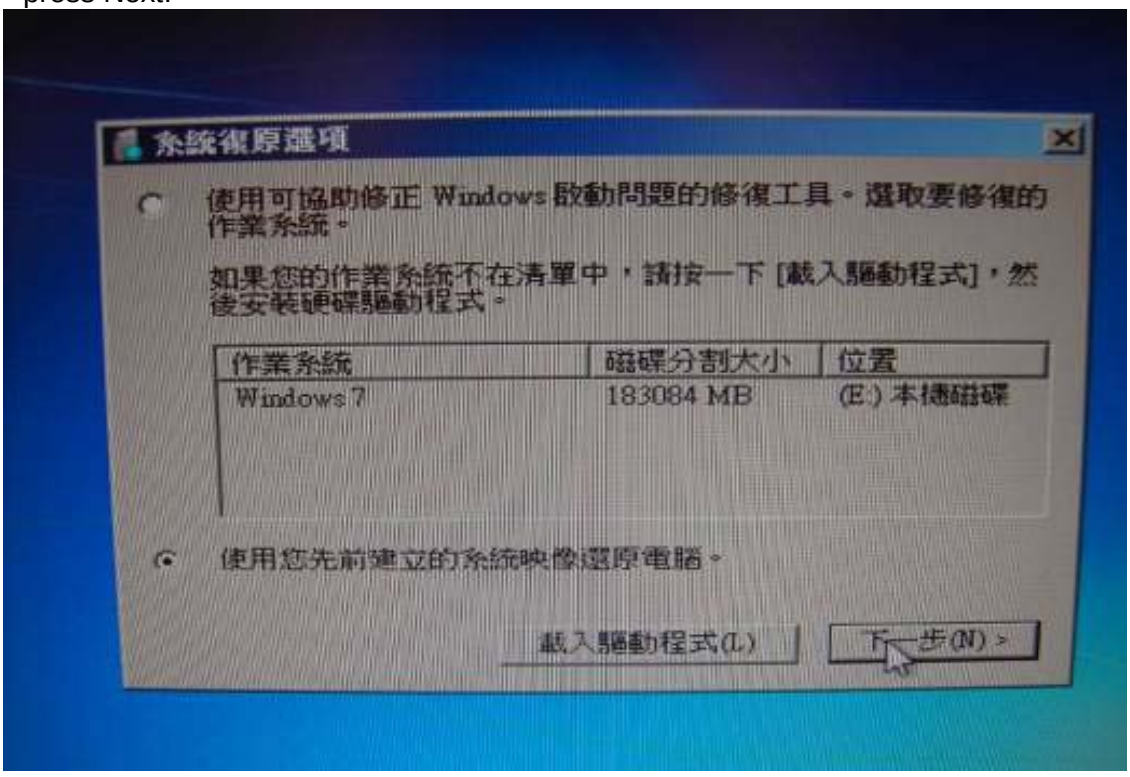
5. Appendix

5.1 Win7 restore operation of A

Step1. The system repair disc into your computer using the CD boot. Click Next.

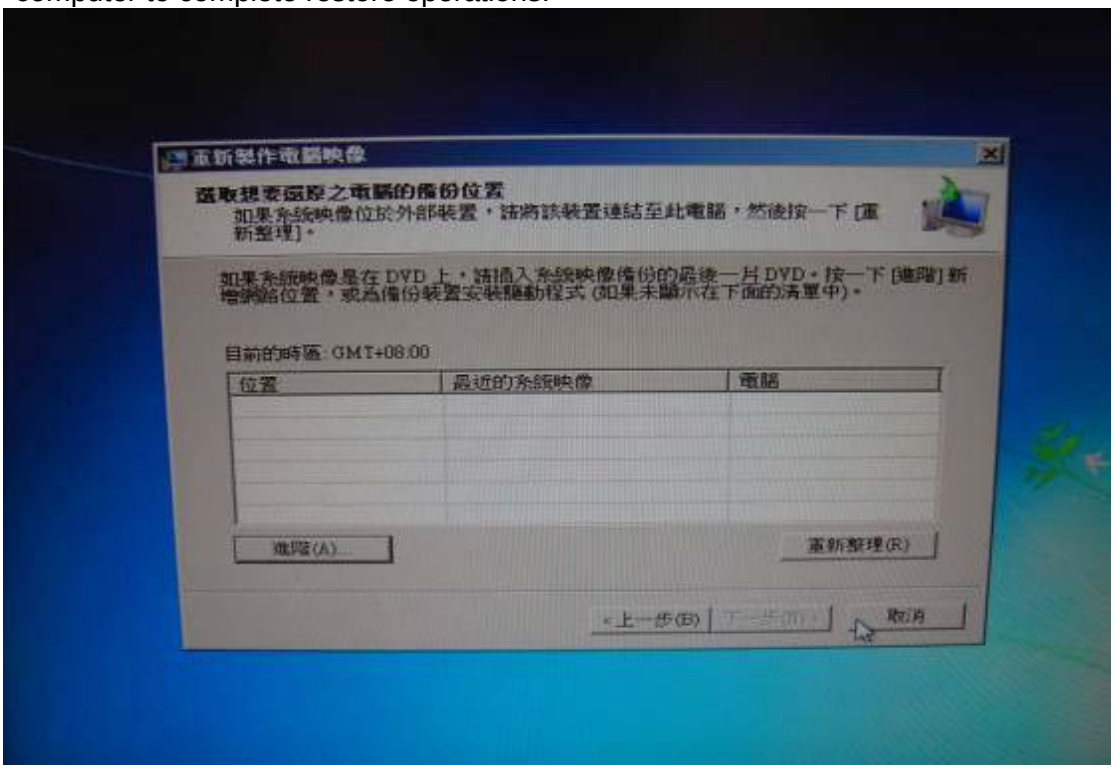


Step2. Choose to use your previously established system image restore the computer and press Next.



Step3. Accordance with the instructions on the screen and then sequentially into restore discs.

Once complete reboot the operating system to confirm the proper functioning of the computer to complete restore operations.

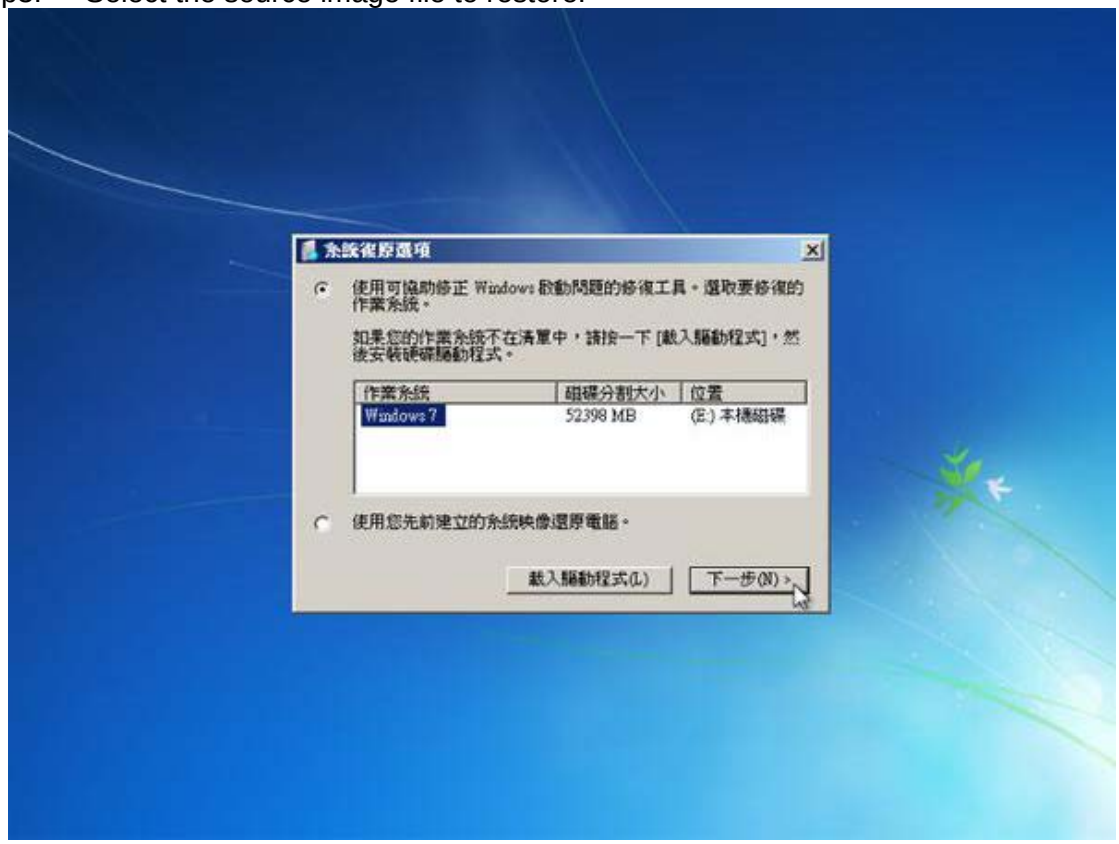


5.2 Win7 restore operation of B

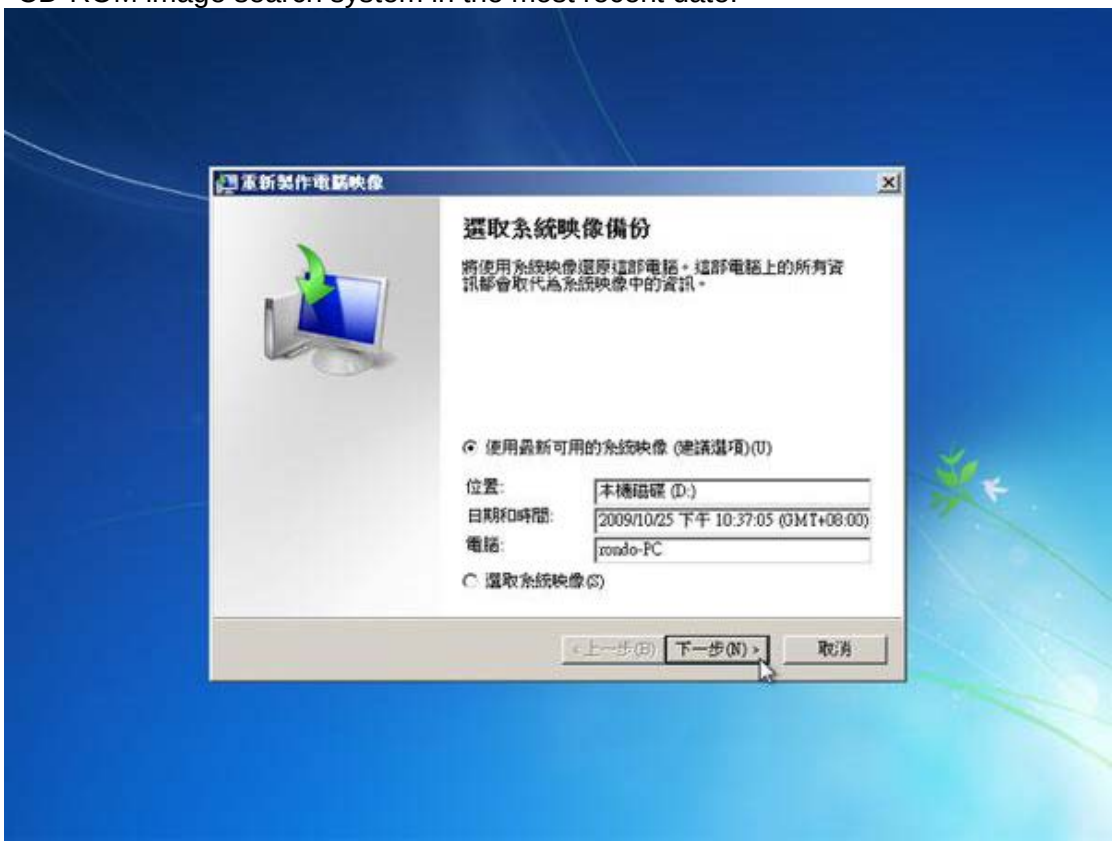
Step1. Use the original CD boot Windows 7, the next step.

Step2. Restore the image file into the 3380P series Win7 CD and remove the original CD, click on the bottom left of the "Repair your computer".

Step3. Select the source image file to restore.

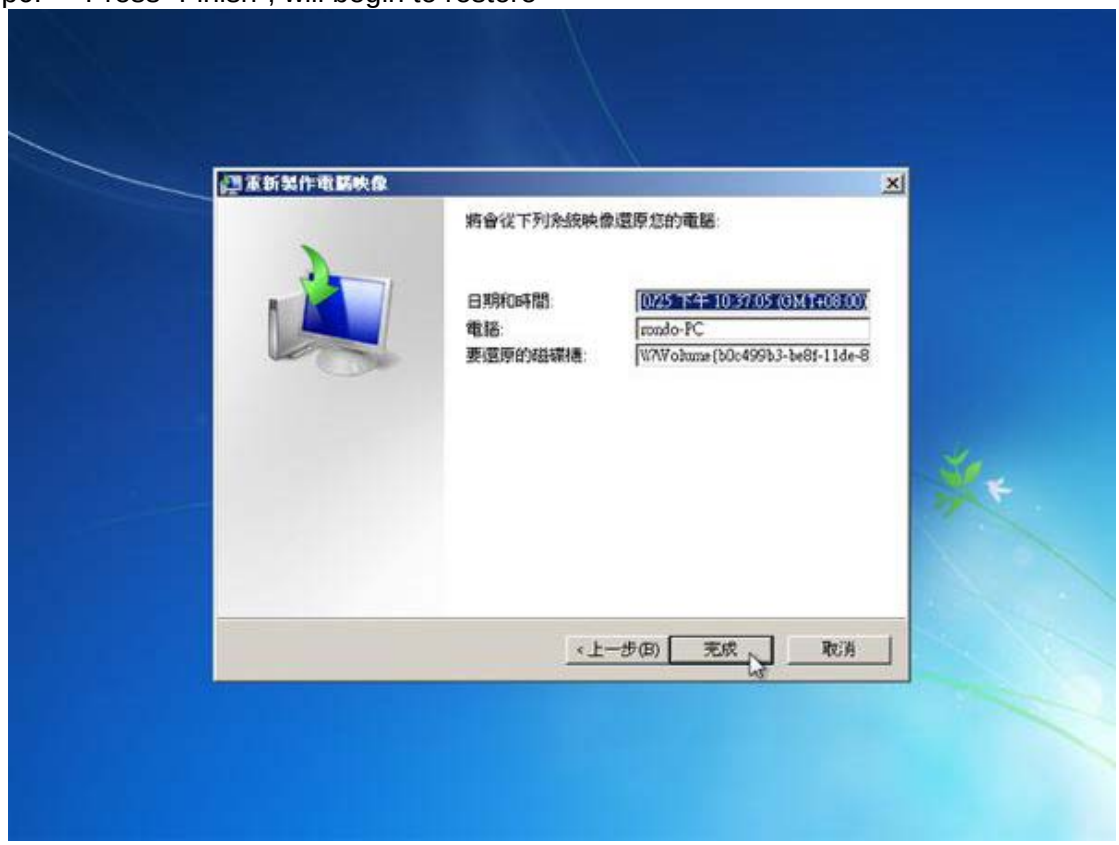


Step4. System image restoration, the default will automatically go to the hard disk or CD-ROM image search system in the most recent date.



Step5. Press "Next" to restore.

Step6. Press "Finish", will begin to restore



Step7. Also the system of the original picture, after the completion of the system will reboot, then the computer can use.

CHROMA ATE INC.

致茂電子股份有限公司

66 Hwaya 1st Rd.

Kuei-shan Hwaya Technology Park

Taoyuan County 33383, Taiwan

33383 台灣桃園縣龜山鄉

華亞科技園區華亞一路 66 號

T +886-3-327-9999

F +886-3-327-8898

Mail: info@chromaate.com

http://www.chromaate.com