



VITAL·IC

NMS4110

Electrochemical Sensor Readout IC

PRELIMINARY

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Data Sheet

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Introduction

NMS4110 is a versatile, precision electro-chemical read-out IC, optimized for low-power Continuous Glucose Monitoring (CGM) systems. It supports multiple electrochemical measurement techniques, including amperometry and voltammetry, providing an efficient solution for bio-signal analysis. Equipped with a switch matrix, sensor detector, system timer, and non-volatile memory, the NMS4110 is designed to maximize battery life and enhance overall user experience.

Switch Matrix offers flexible configurations of measuring blocks to support various sensors and variable terminology of sensor electrode, such as 2, 3, or 4 electrodes.

Sensor Detector detects insertion and prevents the chip from depleting the battery while in the shelf.

System Timer controls wake-up and sleep/shutdown status of NMS4110 and system to cut down the power consumption.

Non-Volatile Memory supports storing of configuration to make users do not care of reconfiguration at every time the system power-up and save the time and power consumption used for reconfiguration

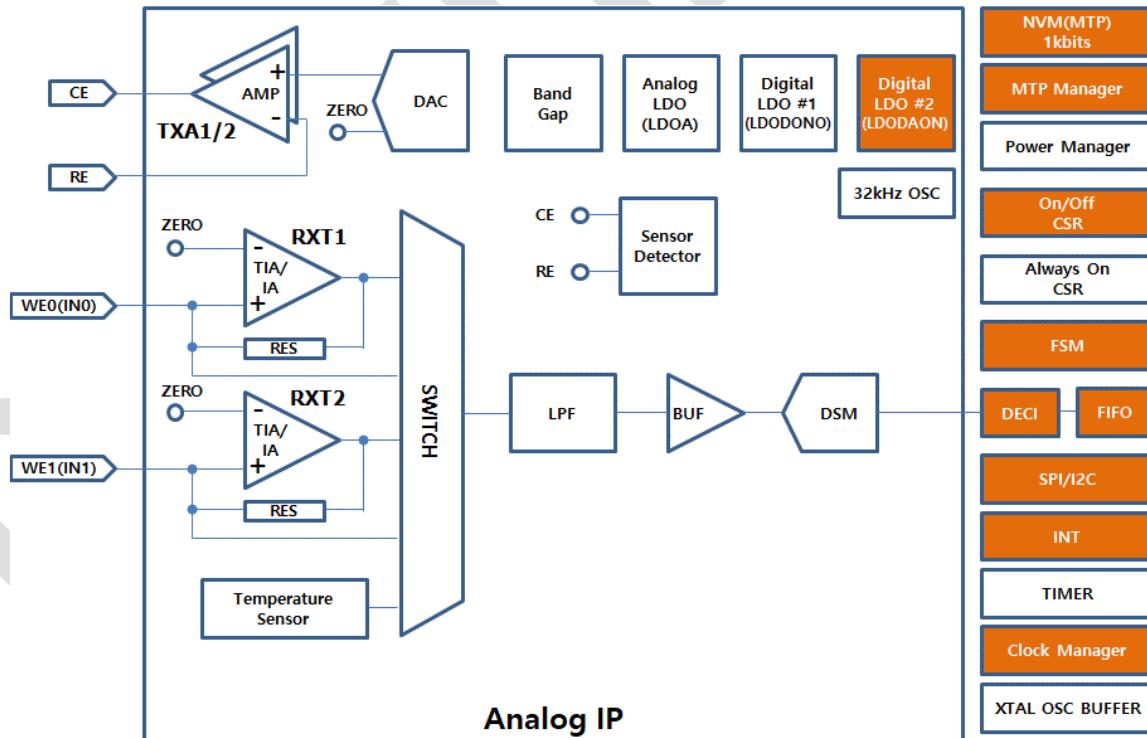


Figure 1 NMS4110 Block Diagram

2 Key Feature

- Flexible switch matrix
- Level & time variable potential generation
- Current or voltage (IA mode) measurement
- Precise current measurement (~500pA)
- 2/3/4-termial electrochemical sensor
- CA, CV, DPV, multistep amperometry support
- I2C/SPI interface
- Ultra-low power sensor detection
- On-chip temperature sensing
- Low power sleep/shutdown (system timer)
- NVM for configuration storage
- Sampling rate
 - Minimum rate: 48.8 SPS
 - Maximum rate: 100kSPS
- Input current range: 500pA ~ 200uA
- TIA Gain range: 500 to 550k Ohm (up to 5M Ohm in case of external configuration option)
- 16bit ADC (ENoB = 13bit)

- DAC resolution: 6bit or 12bit
 - DNL: under 0.5 LSB (6bit mode) / 0.1 LSB (12bit mode)
 - INL: under 0.5 LSB (6bit mode) / 1.5 LSB (12bit mode)
- Programmable potential: -0.8V ~ 0.8V
- LPF cut-off frequency: from 47k up to 4.7 MHz (can support lower cut-off in case of external configuration option)
- Interface speed
 - I2C: up to 100kbps
 - SPI: up to 1.8MHz
- System timer range: 0 to 16,777,215ms
- Internal temp. Sensor: 0.49°C resolution
- Operating voltage: 2.5 ~ 3.6V
- Operating temperature: 0 ~ 70 °C
- Standby current: 8uA (analog)
- 40P-QFN(5x5mm²)
- 49B-WLCSP(2.601x2.615mm²)

3 Package Information

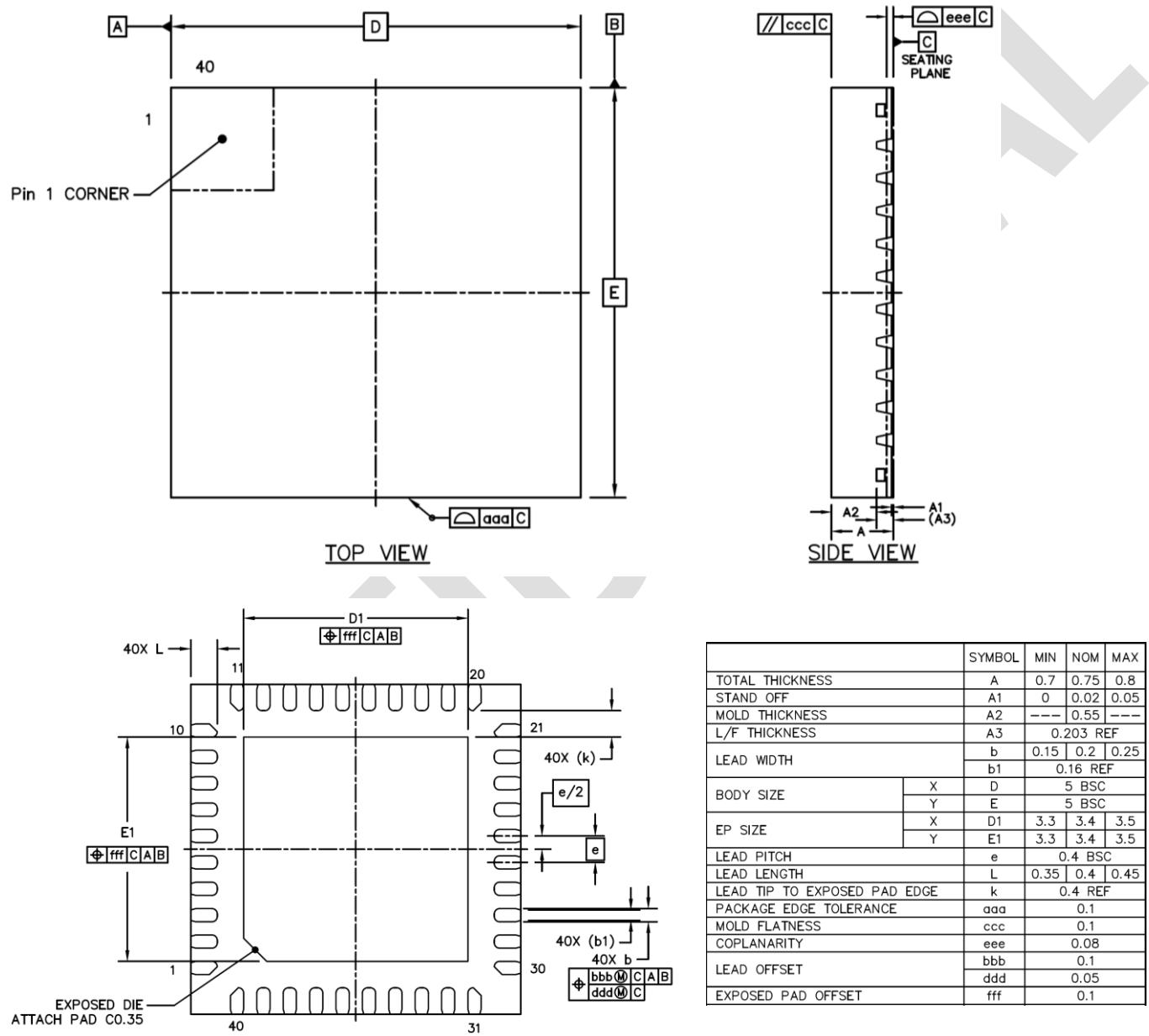


Figure 2 40QFN Package Physical Information

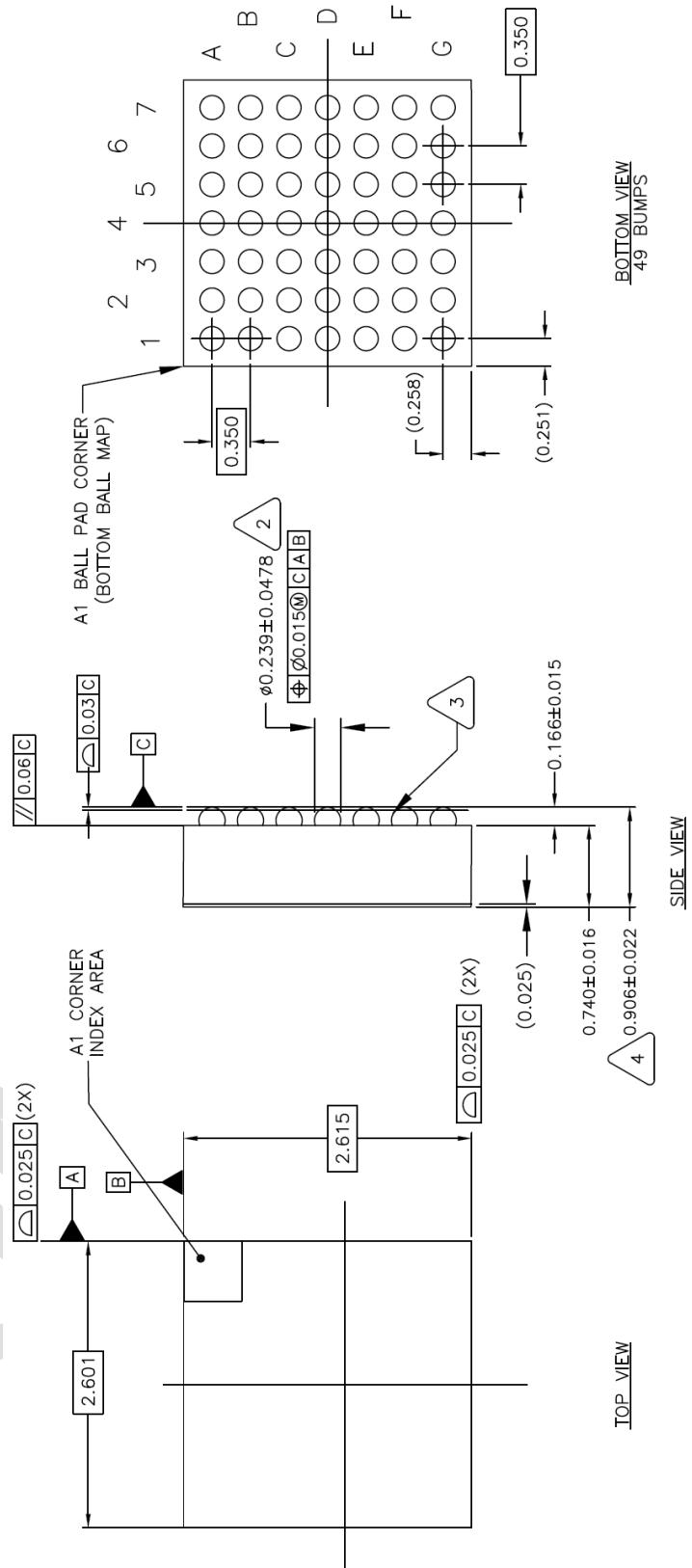


Figure 3 49WLCSP Package Physical Information

4 Pin Description

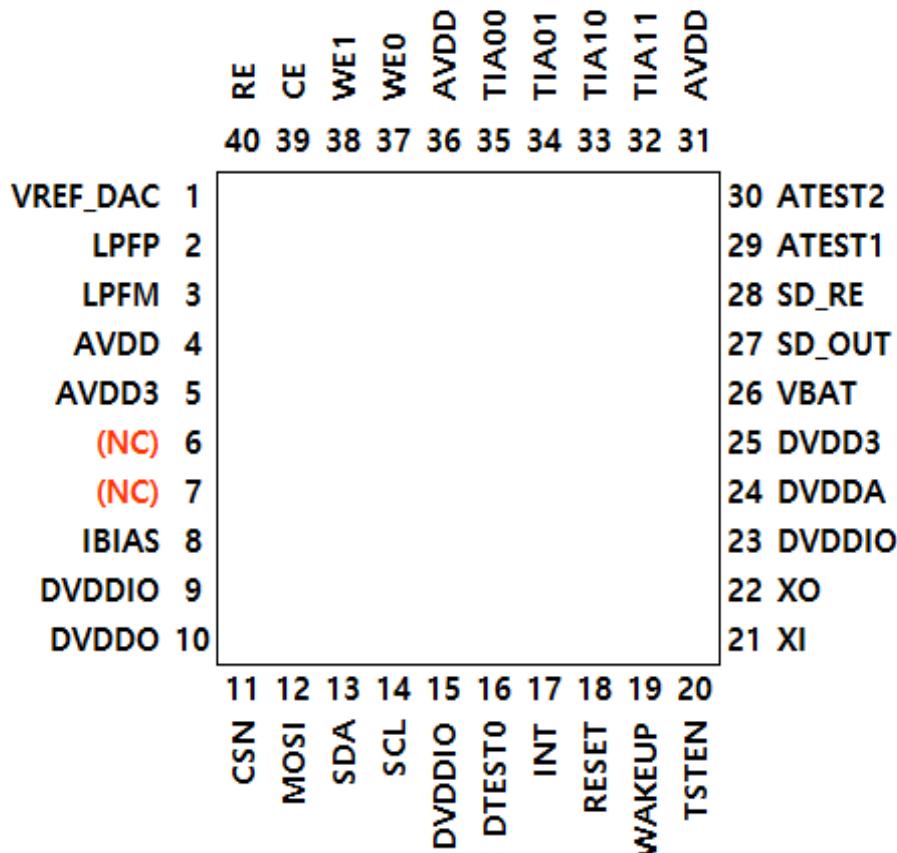


Figure 4 Pinout Top View of NMS4110 – 40QFN

Note: The exposed ground pad is located at the bottom of a chip and electrically connected to the die ground inside the package. It must be connected to a solid ground plane.

Table 1 40QFN Pin Description

Pin#	Name	Type	Description
1	VREF_DAC	Power	External reference voltage for DAC
2	LPFP	Analog I/O	External extra capacitor for low pass filter (optional)
3	LPFM	Analog I/O	External extra capacitor for low pass filter(optional)
4	AVDD	Power	1.8V analog supply voltage for decap
5	AVDD3	Power	3.3V analog supply voltage
6	(NC)		Not Connected
7	(NC)		Not Connected
8	IBIAS		MTP memory input bias : IBIAS must be connected to a current source
9	DVDDIO	Power	3.3V I/O power supply
10	DVDDO	Power	1.8V digital core supply voltage for decap (ONO)
11	CSN	Digital I/O	SPI chip select/Digital test out[2]**
12	MOSI	Digital I/O	SPI master output slave input
13	SDA	Digital I/O	I2C data / SPI master input slave output (MISO)
14	SCL	Digital Input	I2C clock / SPI clock (SCLK)
15	DVDDIO	Power	3.3V I/O power supply
16	DTEST0	Digital I/O	Digital test out[0](in test only)**/Test Command Input***
17	INT	Digital Output	Interrupt / Digital test out[3]
18	RESET	Digital Input	External reset (active low). Recommend: Connect to pull-up R
19	WAKEUP	Digital I/O	Wakeup enable(input)/ Wakeup indication(output)
20	TSTEN	Digital Input	test mode enable (ISP enable)
21	XI	Analog I/O	16MHz X-tal input
22	XO	Analog I/O	16MHz X-tal output
23	DVDDIO	Power	3.3V I/O power supply
24	DVDDA	Power	1.8V Digital supply voltage for decap (AON)
25	DVDD3	Power	3.3V power supply for LDOD
26	VBAT	Power	Power supply for sensor detector
27	SD_OUT	Analog Output	Sensor Detector Out
28	SD_RE	Analog Input	RE connection of Sensor Detector
29	ATEST1	Analog Output	Analog test output 1
30	ATEST2	Analog Output	Analog test output 2
31	AVDD	Power	1.8V analog supply voltage for decap
32	TIA11	Analog Output	TIA1 minus node
33	TIA10	Analog Output	TIA1 plus node
34	TIA01	Analog Output	TIA0 minus node
35	TIA00	Analog Output	TIA0 plus node
36	AVDD	Power	1.8V Analog supply voltage for decap
37	WE0	Analog Input	Working electrode 0
38	WE1	Analog Input	Working electrode 1
39	CE	Analog I/O	Counter electrode
40	RE	Analog I/O	Reference electrode

	1	2	3	4	5	6	7
A	AGND1	RE	CE	WE0	TIA00	TIA10	AGND2
B	VREF_DAC	AVDD2	WE1	AGND2	TIA01	TIA11	ATEST2
C	LPFP	LPFM	AGND2	AGND2	AGND2	ATEST1	AVDD3
D	AVDD1	(NC)	DGND1	DGND1	SD_RE	SD_OUT	VBAT
E	AVDD3_P3	IBIAS	DGND1	DGND1	TSTEN	DVDD1_O2	DVDD3_P3
F	DVDD1_O1	DVDDO	DVDDA	DGND2	INT	WAKEUP	XO
G	CSN	MOSI	SDA	SCL	DTEST0	RESET	XI

Bottom View**Figure 5 Pinout Bottom View of NMS4110 – 49WLCSP****Table 2 49WLCSP Pin Description**

Pin#	Name	Type	Description
B1	VREF_DAC	Power	External reference voltage for DAC
C1	LPFP	Analog I/O	External extra capacitor for low pass filter (optional)
C2	LPFM	Analog I/O	External extra capacitor for low pass filter(optional)
E2	IBIAS		MTP memory input bias : IBIAS must be connected to a current source
G1	CSN	Digital I/O	SPI chip select/Digital test out[2]**
G2	MOSI	Digital I/O	SPI master output slave input
G3	SDA	Digital I/O	I2C data / SPI master input slave output (MISO)
G4	SCL	Digital Input	I2C clock / SPI clock (SCLK)
G5	DTEST0	Digital I/O	Digital test out[0](in test only)**/Test Command Input***
F5	INT	Digital Output	Interrupt / Digital test out[3]
G6	RESET	Digital Input	External reset (active low). Recommend: Connect to pull-up R
F6	WAKEUP	Digital I/O	Wakeup enable(input, mode 1)/ Wakeup indication(output, mode 2)
E5	TSTEN	Digital Input	test mode enable (ISP enable)
G7	XI	Analog I/O	16MHz X-tal input
F7	XO	Analog I/O	16MHz X-tal output
D7	VBAT	Power	Power supply for sensor detector
D6	SD_OUT	Analog Output	Sensor Detector Out
D5	SD_RE	Analog Input	RE connection of Sensor Detector

C6	ATEST1	Analog Output	Analog test output 1
B7	ATEST2	Analog Output	Analog test output 2
B6	TIA11	Analog Output	TIA1 minus node
A6	TIA10	Analog Output	TIA1 plus node
B5	TIA01	Analog Output	TIA0 minus node
A5	TIA00	Analog Output	TIA0 plus node
A4	WE0	Analog Input	Working electrode 0
B3	WE1	Analog Input	Working electrode 1
A3	CE	Analog I/O	Counter electrode
A2	RE	Analog I/O	Reference electrode
D2	DVDDIO1	Power	3.3V I/O power supply input group 1
E6	DVDDIO2	Power	3.3V I/O power supply input group 2
F2	DVDDO	Power	1.8V digital supply output for decap
F3	DVDDA	Power	1.8V digital supply output for decap
E7	DVDD3P3	Power	3.3V digital supply input for digital LDO
D1	AVDD1	Power	1.8V analog supply output for decap
B2	AVDD2	Power	1.8V analog supply output for decap
C7	AVDD3	Power	1.8V analog supply output for decap
E1	AVDD3P3	Power	3.3V analog supply input for analog LDO
A1	AGND1	Power	Analog ground group 1
A7, B4, C3, C4, C5,	AGND2	Power	Analog ground group 2
D2	(NC)		Not Connected

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter	Min.	Max	Unit		
Supply Voltage (DVDD3, DVDDIO, AVDD3)	-0.3	3.6	V	All supply pins must have the same voltage.	
Core voltage(AVDD_RF12V, AVDD_ANA12V, VDD, XOSCI, XOSCO)	-0.3	1.32	V		
Storage Temperature	-40	150	°C		
ESD(TBD)	HBM(TBD)		2000	V	According to human-body model(JEDEC STD 22)(TBD)
	MM(TBD)		200	V	According to machine model(JEDEC STD 22) (TBD)
	CDM(TBD)		1000	V	According to charged-device model(JEDEC STD 22) (TBD)

5.2 Characteristics

PARAMETER	Symbol	Condition	Min	Typ	Max	Units
TX						
Current consumption	I _{TX_B0}	Boost0		4.09		uA
	I _{TX_B1}	Boost1		4.93		uA
	I _{TX_B2}	Boost2		6.62		uA
	I _{TX_B3}	Boost3		10		uA
TX-DAC1/2						
Resolution	RES _{DAC12}			6		Bits
Relative Accuracy	INL _{DAC12}		-0.4	±0.08	0.4	LSB
Differential Nonlinearity	DNL _{DAC12}		-0.45	±0.05	0.45	LSB
Offset Error	OFST _{DAC12}			±0.0001		mV
Output Voltage Range	V _{DAC12_O}		0.1		1.675	V
Output Settling Time	T _{DAC12_STL}					Sec
TX-DAC3						

Resolution	$\text{RES}_{\text{DAC}3}$			12		Bits
Relative Accuracy	$\text{INL}_{\text{DAC}3}$		-8	± 4.77	8	LSB
Differential Nonlinearity	$\text{DNL}_{\text{DAC}3}$		-8	± 0.75	8	LSB
Offset Error	$\text{OFST}_{\text{DAC}3}$			± 0.0001		mV
Output Voltage Range	$V_{\text{DAC}3_O}$		0.1		1.7	V
Output Settling Time	$T_{\text{DAC}3_STL}$					Sec
TX-VDRV						
Driving current range	$I_{\text{DRV_B}0}$	Boost0 @ 0.9V output	-200		200	uA
	$I_{\text{DRV_B}1}$	Boost1 @ 0.9V output	-500		500	uA
	$I_{\text{DRV_B}2}$	Boost2 @ 0.9V output	-1000		1000	uA
	$I_{\text{DRV_B}3}$	Boost3 @ 0.9V output	-2000		2000	uA
RX						
Current consumption	I_{RX}			591		uA
RX-TIA0/1						
TIA Stability Resistance R_s^1	$R_{\text{TIA}0}$	Control Value 0		31.54		Ω
	$R_{\text{TIA}1}$	Control Value 1		50.46		Ω
	$R_{\text{TIA}2}$	Control Value 2		87.64		Ω
	$R_{\text{TIA}3}$	Control Value 3		147.9		Ω
	$R_{\text{TIA}4}$	Control Value 4		270.6		Ω
	$R_{\text{TIA}5}$	Control Value 5		1775		Ω
	$R_{\text{TIA}6}$	Control Value 6		3272		Ω
TIA Gain (R_1 or R_2) Accuracy	$G_{\text{TIA}0}$	Gain setting 0	-3%	255	+3%	Ω
	$G_{\text{TIA}1}$	Gain setting 1	-3%	474	+3%	Ω
	$G_{\text{TIA}2}$	Gain setting 2	-3%	749	+3%	Ω
	$G_{\text{TIA}3}$	Gain setting 3	-3%	1290	+3%	Ω
	$G_{\text{TIA}4}$	Gain setting 4	-3%	2400	+3%	Ω
	$G_{\text{TIA}5}$	Gain setting 5	-3%	3480	+3%	Ω
	$G_{\text{TIA}6}$	Gain setting 6	-3%	4570	+3%	Ω
	$G_{\text{TIA}7}$	Gain setting 7	-3%	6740	+3%	Ω
	$G_{\text{TIA}8}$	Gain setting 8	-3%	8910	+3%	Ω
	$G_{\text{TIA}9}$	Gain setting 9	-3%	11.1	+3%	$K\Omega$
	$G_{\text{TIA}10}$	Gain setting 10	-3%	13.2	+3%	$K\Omega$
	$G_{\text{TIA}11}$	Gain setting 11	-3%	17.6	+3%	$K\Omega$
	$G_{\text{TIA}12}$	Gain setting 12	-3%	21.9	+3%	$K\Omega$
	$G_{\text{TIA}13}$	Gain setting 13	-3%	26.3	+3%	$K\Omega$

	G _{TIA14}	Gain setting 14	-3%	32.8	+3%	KΩ
	G _{TIA15}	Gain setting 15	-3%	34.9	+3%	KΩ
	G _{TIA16}	Gain setting 16	-3%	43.6	+3%	KΩ
	G _{TIA17}	Gain setting 17	-3%	52.3	+3%	KΩ
	G _{TIA18}	Gain setting 18	-3%	69.6	+3%	KΩ
	G _{TIA19}	Gain setting 19	-3%	92.3	+3%	KΩ
	G _{TIA20}	Gain setting 20	-3%	104	+3%	KΩ
	G _{TIA21}	Gain setting 21	-3%	109	+3%	KΩ
	G _{TIA22}	Gain setting 22	-3%	130	+3%	KΩ
	G _{TIA23}	Gain setting 23	-3%	139	+3%	KΩ
	G _{TIA24}	Gain setting 24	-3%	174	+3%	KΩ
	G _{TIA25}	Gain setting 25	-3%	213	+3%	KΩ
	G _{TIA26}	Gain setting 26	-3%	278	+3%	KΩ
	G _{TIA27}	Gain setting 27	-3%	553	+3%	KΩ
RX-LPF						
Antialias Filter 3dB Frequency Range ¹		MODE0(internal only)		2.4		kHz
		MODE1(internal only)		24.3		kHz
		MODE2(internal only)		243		kHz
RX-ADC						
Data Rate	ODR _{ADC}		48.8		100K	Hz
Input Voltage Ranges	V _{ADC}		-1		1	V
Resolution	RES _{ADC}			16		Bits
Integral Nonlinearity	INL _{ADC}	CIC = 4 stage, OSR = 1024	-64		64	LSB
Differential Nonlinearity	DNL _{ADC}	CIC = 4 stage, OSR = 1024	-2		2	LSB
Signal-to-Noise Ratio	SNR _{ADC}	CIC = 4 stage, OSR = 1024		78.556		dB
Total Harmonic Distortion	THD _{ADC}	CIC = 4 stage, OSR = 1024		-95.786		dB
Peak Harmonic or Spurious Noise	PHD _{ADC}	CIC = 4 stage, OSR = 1024		-86.34		dB
Noise(RMS)	NL _{ADC}	CIC = 4 stage, OSR = 1024		19		nV/√Hz
POWER-BGR/LDO						
Accuracy	ACC _{LDO}		-0.1		0.1	%
Load regulation	LDR _{LDO}					
Line regulation	LNR _{LDO}					

PSRR	PSRR _{LDO}					
POWER-System						
Current consumption	I _{SYSTEM}	@ Active mode		1.753		mA
		@ Sleep mode		0.88		mA
MISC-TEMPERATURE SENSOR						
Resolution ¹	RES _{TS}					°C
MISC- SENSOR DETECTOR						
Current consumption	I _{SD}			519		nA
MISC-LFOSC						
Accuracy	ACC _{LFOSC}			99.864		%
Frequency jitter	FJ _{LFOSC}					us
MISC-POR						
POR Trip Level ¹	V _{POR}	Power-On		1.04		V
Delay ¹	D _{POR}			5.7		ms
DIGITAL I/O						
Input Voltage Low	V _{IL}		-0.3		0.8	V
Input Voltage High	V _{IH}		2		3.6	V
Output High Voltage	V _{OH}	I _{OH} 2mA/4mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} 2mA/4mA			0.4	V
Low Level Output Current@V _{OL(max)}	I _{OL}	2mA			3.3	mA
		4mA			6.6	mA
High Level Output Current@V _{OL(max)}	I _{OH}	2mA			4.5	mA
		4mA			9	mA
Pull-Up Register	R _{PU}			47K		Ω
Pull-Down Register	R _{PD}			59K		Ω

¹ Guaranteed by design, not production tested.

5.3 MTP Memory

Symbol	Comment	Pin	Test Condition	Min	Typ	Max	Unit
IBIAS_IN		IBIAS		20	25	30	nA
VDDDONO		DVDDO	Program Erase	1.40(TBD)	1.80	2.0	V
			Read	1.4(TBD)	1.8	2.0	V
		DVDDA	Program Erase	1.40(TBD)	1.80	2.0	V
			Read	1.4(TBD)	1.8	2.0	V

5.4 Operating Characteristics

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6 DETAILED DESCRIPTION

6.1 ANALOG MISC

6.1.1 LDO

A Low Dropout (LDO) regulator is a block that supplies power to analog and digital blocks. It consists of one LDO for the analog block and two LDOs for the digital blocks. Based on the BGR voltage generated from the BGR, it produces an output of 1.8V. The LDOs for the digital blocks include an ONO LDO and an AON LDO. The digital AON LDO is always turned on, while the digital ONO LDO and the analog LDO can be controlled to enable or disable.

6.1.2 BGR

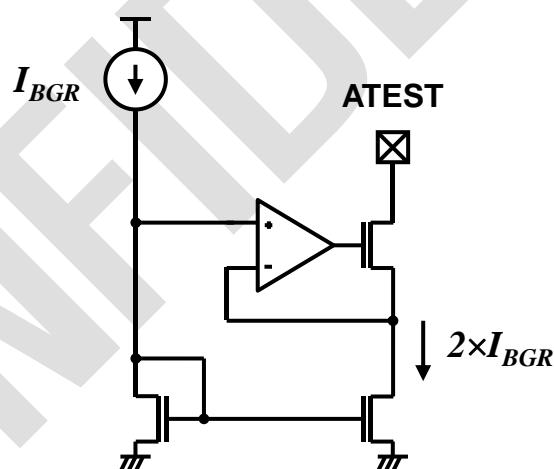


Figure 6 BGR current trimming circuit

The Bandgap Reference (BGR) block generates a bandgap current (I_{BGR}), which is insensitive to temperature variations and serves as the reference current for generating the bias current required for each circuit block. Additionally, it produces the bandgap voltage, which is the reference voltage used to create the LDO output voltage. As shown in Figure 3, I_{BGR} can be measured and trimmed via the ATESTx pin. Separate BGRs are integrated for the analog LDO and the digital LDO.

6.1.1 Global Bias

It receives the reference current of $0.13\mu\text{A}$ generated by the BGR and provides the bias current required for each block such as TIA, VDRV, and DSM. The current value can be adjusted through control registers.

Table 3 Bias Current vs. CUR_TIA_VDRV for VDDA3=3.0V

CUR_TIA_VDRV[3:0] (dec)	TIA, VDRV (nA)
0	24.93
1	30.13
2	35.34
3	40.54
4	45.77
5	50.96
6	56.18
7	61.37
8	66.62
9	71.81
10	77.03
11	82.22
12	87.45
13	92.65
14	97.86
15	103.10

Table 4 Bias Current vs. CUR_MUXBUF for VDDA3=3.0V

CUR_MUXBUF[1:0]	MUXBUF (uA)
0	0.6492
1	0.8655
2	1.082
3	1.298

Table 5 Bias Current vs. CUR_DSM for VDDA3=3.0V

CUR_DSM[1:0]	DSM (uA)
0	0.2976
1	0.4058
2	0.5139
3	0.6221

Table 6 Bias Current vs. CUR_DSM_VADC_BUF for VDDA3=3.0V

CUR_DSM_VADC_BUF[1:0]	DSM VREF BUF (uA)
0	0.4869
1	0.5951
2	0.7033
3	0.8114

Table 7 Bias Current vs. CUR_TEMPS for VDDA3=3.0V

CUR_TEMPS	TEMPS (nA)
0	54.12
1	108.20

GLOBAL BIAS CURRENT CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset					
0x80	-	CUR_TEMPS	CUR_MUXBUF[1:0]		CUR_DSM_VADC_BUF[1:0]		CUR_DSM[1:0]		0x2A					
	-	RW	RW		RW		RW							
Bit	Field			Type	Reset	Description								
6	CUR_TEMPS			R/W	0x00	Global Bias current control of TEMPS(temperature sensor)								
5:4	CUR_MUXBUF[1:0]			R/W	0x02	Global Bias current control of MUX Buffer								
3:2	CUR_DSM_VADC_BUF[1:0]			R/W	0x02	Global Bias current control of DSM VADC Buffer								
1:0	CUR_DSM[1:0]			R/W	0x02	Global Bias current control of DSM								

GLOBAL BIAS CURRENT CONTROL Register(AOM)

Address	7	6	5	4	3	2	1	0	reset			
0xC6	-	-	-	-	CUR_TIA_VDRV[3:0]			RW	0x2A			
	-	-	-	-	RW							
Bit	Field			Type	Reset	Description						
3:0	CUR_TIA_VDRV[3:0]			R/W	0x05	Global Bias current control of TIA/IA & VDRV						

6.1.1 TESTV

TESTV is a circuit block designed for testing purposes that applies the voltage generated internally to the DSM input. A resistor array (Res. Array) generates ΔV . The output voltage corresponding to the TESTV_DV value is shown in Table 8. It can be adjusted from 73.08 mV to 1.335 V

Table 8 Simulated Output Voltage for TESTV_VREF=15.

nTESTV_DV	OUT_P ("P") (V)	OUT_M ("M") (V)	OUT_P - OUT_M
0.000	923.1E-3	850.0E-3	73.08E-3
1.000	953.5E-3	818.4E-3	135.1E-3
2.000	983.8E-3	787.9E-3	195.9E-3
3.000	1.012	758.1E-3	253.6E-3
4.000	1.041	730.5E-3	311.0E-3
5.000	1.067	702.6E-3	364.8E-3
6.000	1.094	676.1E-3	417.8E-3
7.000	1.118	650.2E-3	467.8E-3
8.000	1.146	627.9E-3	518.5E-3
10.000	1.169	603.7E-3	565.2E-3
11.000	1.192	580.7E-3	611.5E-3
12.000	1.213	558.1E-3	655.2E-3
13.000	1.237	536.9E-3	700.2E-3
14.000	1.257	515.7E-3	741.2E-3
15.000	1.278	495.3E-3	782.3E-3
16.000	1.296	475.4E-3	820.9E-3
17.000	1.321	457.3E-3	863.5E-3
18.000	1.338	438.4E-3	900.1E-3
19.000	1.357	420.1E-3	937.0E-3
20.000	1.374	402.2E-3	971.5E-3
21.000	1.393	384.9E-3	1.008
22.000	1.409	368.1E-3	1.041
23.000	1.425	351.6E-3	1.074
24.000	1.440	335.7E-3	1.105
25.000	1.459	320.0E-3	1.139
26.000	1.473	304.9E-3	1.168
27.000	1.488	290.0E-3	1.198
28.000	1.502	275.7E-3	1.226
29.000	1.518	261.4E-3	1.256
30.000	1.530	247.8E-3	1.283
31.000	1.544	234.3E-3	1.310
32.000	1.556	221.3E-3	1.335

VOLTAGE ADJUSTS Register(ONM)

Address	7	6	5	4	3	2	1	0	reset		
0x8B	-	-	-	TESTV_DV[4:0]				RW			
	-	-	-								
Bit	Field		Type		Reset		Description				
4:0	TESTV_DV[4:0]		R/W		0x08		Adjusts DV voltage of TESTV				

VOLTAGE ADJUSTS Register(ONM)

Address	7	6	5	4	3	2	1	0	reset		
0x8C	-	-	-	TESTV_VREF[4:0]				RW			
	-	-	-								
Bit	Field		Type		Reset		Description				
4:0	TESTV_VREF[4:0]		R/W		0x10		Adjusts VREF voltage of TESTV				

6.1.2 Temperature Sensor

The temperature sensor is designed to flow different currents through two BJTs, allowing the output voltage to be proportional to the temperature, independent of current, BJT size, and supply voltage. Additionally, by using a shifter to connect the current mirror differently each time, the design achieves the effect of averaging device mismatch. The designed circuit is shown in Figure 4. As per the following equation, the output is determined in proportion to the current ratio M and the size ratio N of Q1 and Q2

$$V_{be1} = \ln(I_1/I_s/N) * kT/q$$

$$V_{be2} = \ln(I_2/I_s) * kT/q = \ln(M \times I_1/I_s) * kT/q$$

$$V_{out} = V_{be2} - V_{be1} = \ln(M \times N) * kT/q$$

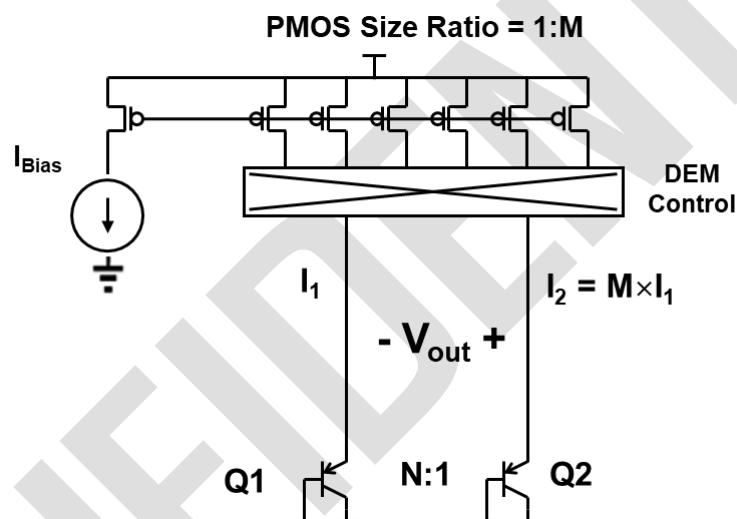


Figure 7 Temperature sensor(TEMPS) schematic.

TEMPS DEM CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset	
0x8D	-	-	TEMPS_DEM_MODE[1:0]			TEMPS_DEM_N1[3:0]			0x30	
	-	-	RW			RW				
Bit	Field			Type	Reset	Description				
5:4	TEMPS_DEM_MODE[1:0]			R/W	0x03	0: No DEM1: Shift every SOC 2: Shift every generated clk by TEMPS_DEM_N1 3: Shift every CLK_DEM by TEMPS_DEM_N1				
3:0	TEMPS_DEM_N1[3:0]			R/W	0x00	Clock divide ratio to generate DEM clock for temperature sensor				

6.1.1 Internal 32 kHz Low-frequency Oscillator

The internal 32 kHz low-frequency oscillator can be turned on or off by the ENB_LFOSC1_32K setting. It is connected to the always-on power supply VDDD_AON, and the moment ENB_LFOSC1_32K is set to 0, it immediately oscillates and generates a 32 kHz clock signal. The frequency can be trimmed using the TRIM_LFOSC1_32K register.

ENABLE LFOSC1 32K Register(AOM)

Address	7	6	5	4	3	2	1	0	reset
0xC9	-	-	-	-	-	-	-	ENB_LFOSC1_32K	0x01
	-	-	-	-	-	-	-	RW	
Bit	Field			Type			Reset		Description
0	ENB_LFOSC1_32K			R/W			0x01		

TRIM LFOSC1 32K Register(AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xC5	TRIM_LFOSC1_32K[7:0]								0x00	
	RW									
Bit	Field			Type		Reset	Description			
7:0	TRIM_LFOSC1_32K[7:0]			R/W		0x00	Frequency trimming of Low-freq osc (32kHz)			

6.1.2 Power-On-Reset (POR)

A power-on-reset (POR) signal is generated for the VDDD_AON power supply (1.8V). When the POR signal occurs, the POR_STATE signal goes high, and this can be confirmed by reading the 0x8F register.

POR STATUS Register (ONR)

Address	7	6	5	4	3	2	1	0	reset
0x8F	-	-	-	-	-	-	-	POR_STATE	0x00
	-	-	-	-	-	-	-	RO	
Bit	Field			Type			Reset		Description
0	POR_STATE			RO			0x00		

6.2 ADC CIRCUIT

6.2.1 DSM (Delta-Sigma Modulator)

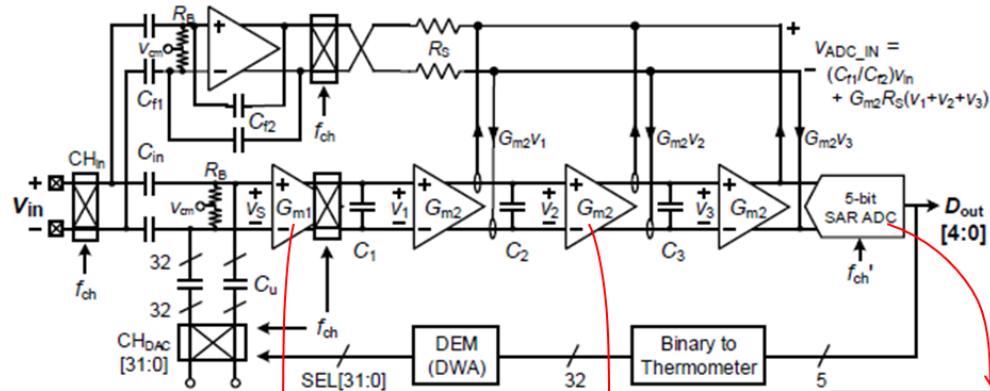


Figure 8 Block Diagram of DSM

Figure 8 is the circuit diagram of the delta-sigma modulator (DSM) using the designed 3rd-order Gm-C loop. It consists of a Gm-C stage, a 5-bit SAR ADC, a feedback capacitor, and an input chopper, among other components. The first Gm₁-C stage is designed with separate input and output paths to handle large inputs, and chopping techniques were applied to reduce low-frequency noise. The output of the second Gm₂-C stage is split into two: one is applied to the input of the next stage, and the other is summed into the final output current. The summed current is converted to voltage via a resistor and applied to the 5-bit SAR ADC. The 5-bit SAR ADC is composed of a CDAC, a comparator, and SAR logic. The comparator clock for SAR operation requires 5 pulses, and it is designed to generate the 5 pulses within the low phase of CLK_SH. The SAR ADC output undergoes thermometer decoding and DEM (Dynamic Element Matching) before being applied to the input CDAC (Cu).

CURRENT BIAS CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset					
0x82	DSM_REFI[1:0]		DSM_DSMI[1:0]		DSM_BYP_VREF	SEL_DUTY_R[2:0]			0x50					
	RW		RW		RW	RW								
Bit	Field		Type	Reset	Description									
7:6	DSM_REFI[1:0]		R/W	0x01	Current bias control for Reference voltage generator									
5:4	DSM_DSMI[1:0]		R/W	0x01	Current bias control for DSM									

					DSMI_BDSM[1:0]	Current(A)	
					00	450n	
					01	900n	
					10	1350n	
					11	1800n	
					REFI_BDSM[1:0]	REFI_Current(A)	REFI_Current(A)
						250n	500n
					01	500n	1000n
					10	750n	1500n
					11	1000n	2000n
					Bypass control for reference voltage generator		
					Control duty-cycled R. 0xx: Pseudo-R mode. xx=adjust R 1xx: Duty-cycled R mode. xx=adjust pulse width		
					SEL_DUTY_R[2:0], 0xx	RES.(Ohm)	
					000	1.14M	
					001	6.26G	
					010	11.8G	
					011	16.4G	
					SEL_DUTY_R[2:0], 1xx	Pulse width(nsec)	
					100	25	
					101	50	
					110	75	
					111	100	

DSM CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset	
0x83	-	-	DSM_GM1_CTRL[1:0]			DSM_GAIN[1:0]		DSM_BUFI[1:0]		0x21
	-	-	RW			RW		RW		
Bit	Field			Type	Reset	Description				
5:4	DSM_GM1_CTRL[1:0]			R/W	0x02	Gm1 value control of DSM 00: x1.1 01: x1 10: x0.9 11: x0.8				
3:2	DSM_GAIN[1:0]			R/W	0x00	Loop gain control of DSM 00: x1 01: x1.4 10: x1.6 11: x2				

								Current bias control for buffer	
1:0		DSM_BUFI[1:0]		R/W	0x01				
						BUFI_BDSM[1:0]	Current(A)		
						00	750n		
						01	1500n		
						10	2250n		
						11	3000n		

DEM MTHOD CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset		
0x84	-	DEM_MODE[2:0]			CLK_CMP_WIDTH[3:0]			RW			
	-	RW			RW						
Bit	Field			Type	Reset	Description					
6:4	DEM_MODE[2:0]			R/W	0x02	Controls DEM method. 0: New-1 1: New-2 2: Legacy DWA (Same as original BioDSM) 3: Shift 1 4: Shift 2 5: Shift 3 6: Shift 4 7: DEM off					
3:0	CLK_CMP_WIDTH[3:0]			R/W	0x02	Adjust delay to make CLK_CMP.					

DEM START POINT Register(ONM)

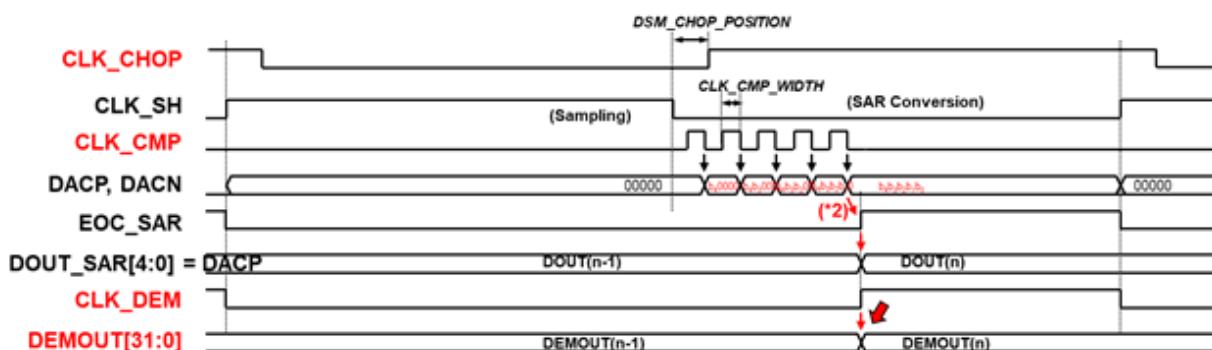
Address	7	6	5	4	3	2	1	0	reset			
0x85	-	-	-	DEM_ST_POINT[4:0]			RW					
	-	-	-	RW								
Bit	Field			Type	Reset	Description						
4:0	DEM_ST_POINT[4:0]			R/W	0x00	Adjusts DEM start point : set the starting point of DEM output Ex) If DEM_ST_POINT=0, the DEM output (DEM_OUT) starts from [0]. If DEM_ST_POINT=5, the DEM_OUT starts from [5].						

Fos CLOCK RETE CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset			
0x86				SET_FOS_CLKN[7:0]			RW					
				RW								
Bit	Field			Type	Reset	Description						
7:0	SET_FOS_CLKN[7:0]			R/W	0x05	Control of Fos clock rate in analog controller Input clock is divided by (2xSET_FOS_CLKN) to generate CLK_SH						

DSM CHOP POSITION CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset			
0x87	DSM_CHOP_POSITION[7:0]						0x00					
Bit	Field	Type	Reset	Description								
7:0	DSM_CHOP_POSITION[7:0]	R/W	0x00	Control the position of DSM의 CLK_CHOP. The rising signal of DSM_CHOP is generated after the DSM_CHOP_POSITION value from the fall edge of CLK_SH. The clock edge used varies depending on the SEL_DSM_CHOP setting.								



CLCOK EDGE SET FOR CLK_CHIP Register(ONM)

Address	7	6	5	4	3	2	1	0	reset
0x88	-	-	-	-	-	-	-	SEL_DSM_CHOP	0x01
Bit	Field	Type	Reset	Description					
0	SEL_DSM_CHOP	R/W	0x01	Sets the clock edge used for generating the CLK_CHOP signal.					

DSM VOLTAGE SELECT Register(ONM)

Address	7	6	5	4	3	2	1	0	reset
0x89	-	-	-	SEL_DSM_DV[4:0]					
Bit	Field	Type	Reset	Description					
4:0	SEL_DSM_DV[4:0]	R/W	0x17	Adjust DSM ref. voltage					

Table 9 Reference Voltage vs. SEL_DSM_DV

SEL_DV	VH (V)	VL (V)	ΔV (V)	SEL_DV	VH (V)	VL (V)	ΔV (V)
0	1.130	0.670	0.460	16	1.380	0.421	0.959
1	1.132	0.668	0.465	17	1.382	0.418	0.964
2	1.135	0.665	0.470	18	1.385	0.416	0.969
3	1.137	0.663	0.475	19	1.387	0.413	0.974

4	1.140	0.660	0.480	20	1.390	0.411	0.979
5	1.142	0.658	0.485	21	1.392	0.408	0.984
6	1.145	0.655	0.490	22	1.395	0.406	0.989
7	1.147	0.653	0.495	23	1.397	0.403	0.994
8	1.150	0.650	0.500	24	1.400	0.401	0.999
9	1.152	0.648	0.505	25	1.402	0.398	1.004
10	1.155	0.645	0.510	26	1.405	0.396	1.009
11	1.157	0.643	0.515	27	1.407	0.393	1.014
12	1.160	0.640	0.520	28	1.410	0.391	1.019
13	1.162	0.638	0.525	29	1.412	0.388	1.024
14	1.165	0.635	0.530	30	1.415	0.386	1.029
15	1.167	0.633	0.535	31	1.417	0.383	1.034

DSM VOLTAGE SET Register(ONM)

Address	7	6	5	4	3	2	1	0	reset				
0x8A	-	-	-	SEL_DSM_VOCM[1:0]		SEL_DSM_BGR[1:0]		SEL_PSEUDO_R	0x00				
	-	-	-	RW			RW						
Bit	Field			Type	Reset	Description							
4:3	SEL_DSM_VOCM[1:0]			R/W	0x00	Set the voltage level of DSM_VOCM 00: 1.2V 01: 1.0V 10: 0.9V (equal to VICM) 11: 0.8V							
2:1	SEL_DSM_BGR[1:0]			R/W	0x00	Set the source of BGR voltage for DSM 00: BGR voltage(1.25V) from BGR 01: 1.25V made by R-divide 10: 1.04V made by R-divide 11: 0.91V made by R-divide							
0	SEL_PSEUDO_R			R/W	0x00	0: Use Poly-R 1: Use Pseudo-R and Poly-R							

6.2.2 LPF & MUX

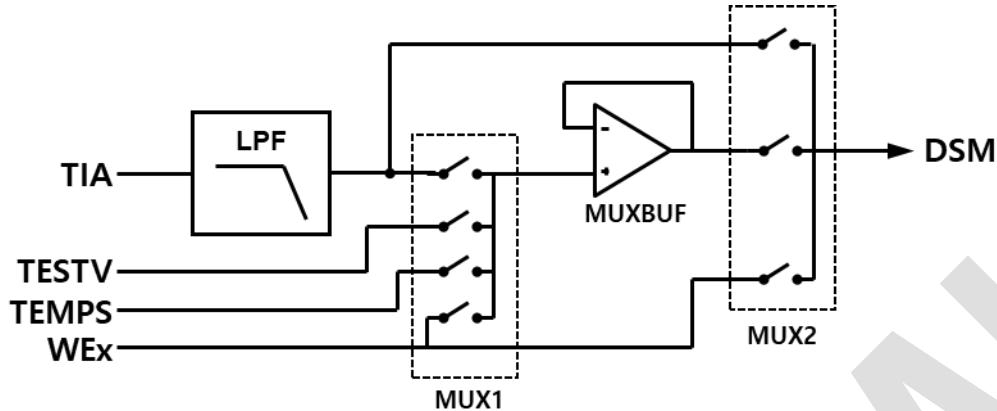


Figure 9 Block Diagram of LPF & MUX Block

Figure 9 is the block diagram of the LPF & MUX. The signal passes through the LPF and MUX1, then goes through the buffer (MUXBUF) composed of a class-AB opamp, and is applied to the DSM via MUX2. The signal assignments for SEL_MUX1 and SEL_MUX2 are shown in Table 10 and Table 11.

Table 10 SEL_MUX1

SEL_MUX1[1:0]	MUX1 Output	Note
0	LPF Output	
1	TEMPS Output	
2	TESTV Output	
3	Bypass (direct connection to inputs)	

Table 11 SEL_MUX2

SEL_MUX2[1:0]	MUX2 Output	Note
0	MUXBUF Output	
1	LPF Output (bypass MUXBUF)	
2	(not used)	
3	Bypass (direct connection to inputs)	

The LPF is composed of resistors and capacitors. The resistor can be 2-bit controlled with values of short, 47k, 471k, and 4711k. A 11.75pF capacitor is internally connected, and an additional switch is provided to allow the connection of a larger external capacitor. When the switch is set to on, it connects to the LPFP and LPFM pins, allowing an external capacitor to be connected. The MUXBUF is in a unity-gain configuration and functions as a signal buffer.

6.2.3 Decimation Filter

The decimation filter is crucial for reducing the environmental noises as it filters the target frequency information from various inputs. NMS4110 supports two different decimation filters: Cascaded integration comb (CIC) and the integrator along with a post-processing block and an average filter. The average filter is an accumulator that accumulates the post-processed output. Figure 10 displays the block diagram of the system.

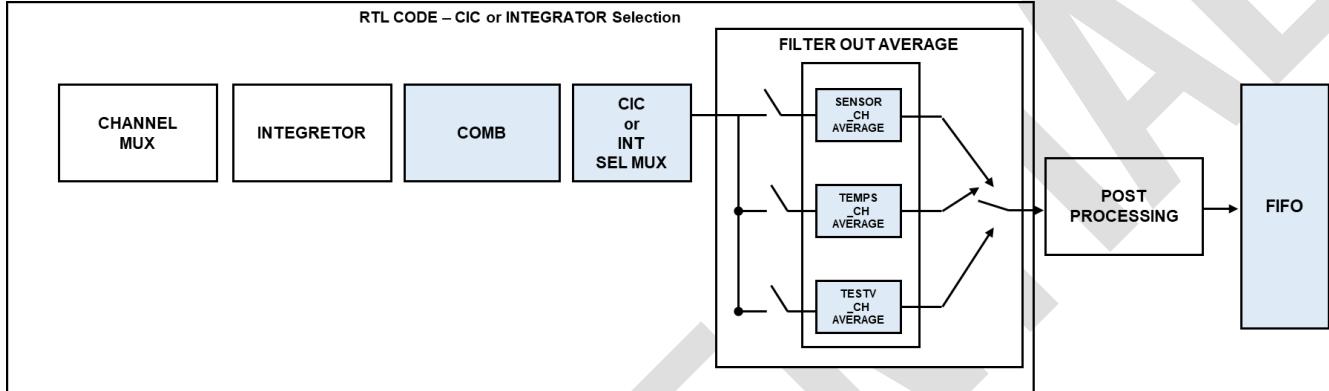


Figure 10 Decimation Filter Block Diagram

The decimation filter can be configured by adjusting the register setting. The user can either enable all the blocks and obtain more precise but slow data or get fast but relatively less accurate data. The shade indicates selective blocks. As shown in the block diagram, enabling the comb block determines the filter. The Figure 11 compares their magnitude response according to their frequency input. f_s indicates input frequency/(sampling frequency * over sampling rate), where sampling frequency is 800kHz and oversampling rate is 16.

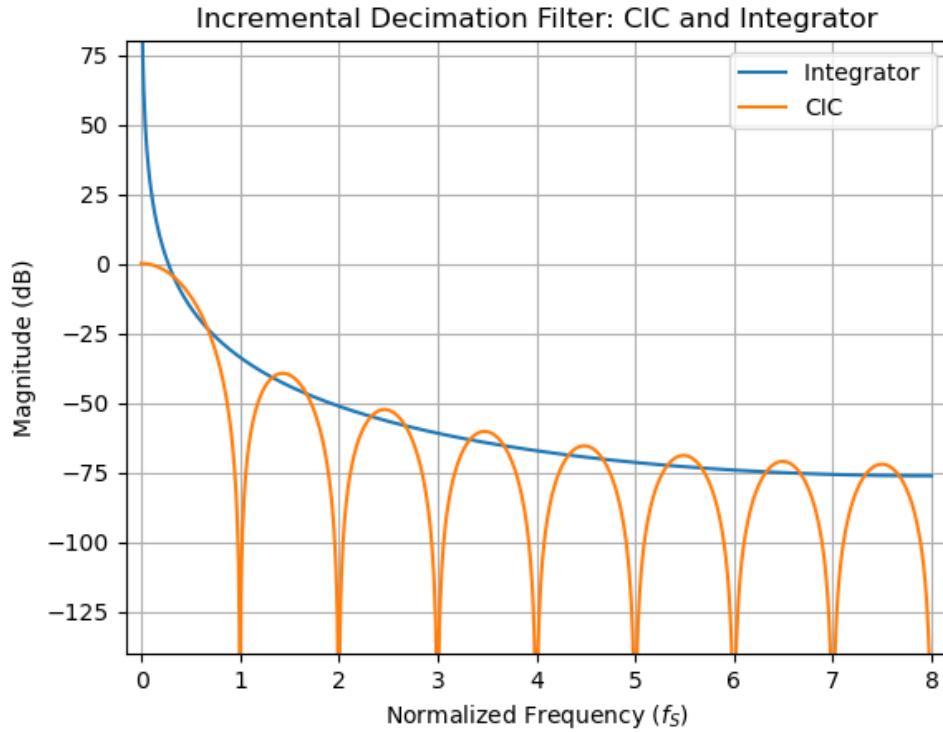


Figure 11 Decimation Filter Frequency Response: CIC vs Integrator

6.2.3.1 Integrator

The transfer function equation of an integrator filter is as follows

$$H(z) = \frac{1}{(1 - z^{-1})^N} = \frac{z^N}{(z - 1)^N}$$

N represents the number of stages of the integrator filter, and z is $e^{\frac{(2\pi f)}{F_S}}$.

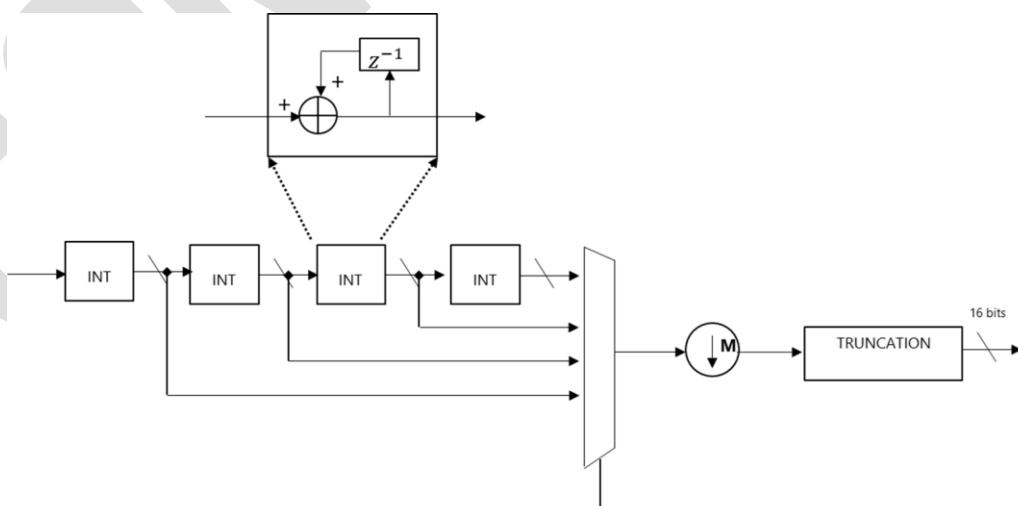


Figure 12 Decimation Filter : Integrator

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The resolution is determined by the integrator of the filter, and the maximum bit vector size is determined by the magnitude of the accumulated value until one sample is output during the filter's decimation. In NMS4110, the bit size is fixed since the integrator must also be compatible with the CIC filter. Each stage produces an output in 46 digits, which can be selected through the mux. M stands for the oversampling rate, which compensates for the excessive accumulation from the integration process. The output is later truncated to meet the resolution criteria.

Table 12 Decimation Filter Gain : Integrator

	GAIN(M : OSR)
STAGE 1	M
STAGE 2	$\frac{M(M + 1)}{2}$
STAGE 3	$\frac{M(M + 1)(M + 2)}{6}$
STAGE 4	$\frac{M(M + 1)(M + 2)(M + 3)}{24}$

The stage configuration of the integrator filter can be adjusted through register settings.

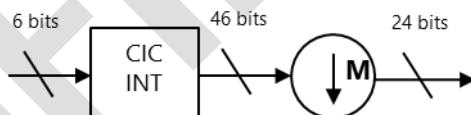


Figure 13 Decimation filter: integrator stage1

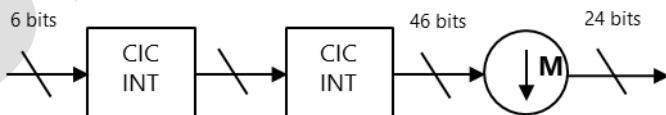


Figure 14 Decimation filter: integrator stage2

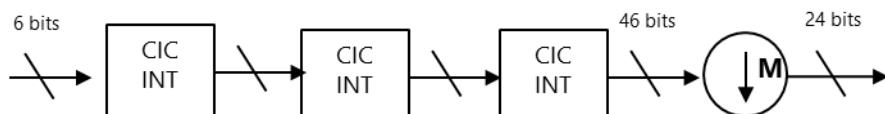


Figure 15 Decimation filter: integrator stage3

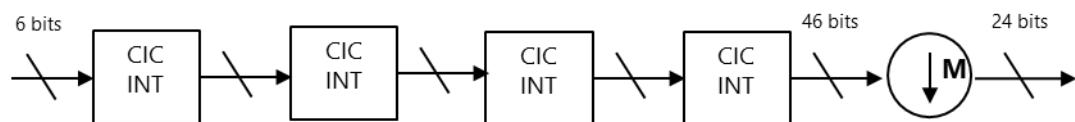


Figure 16 Decimation filter: integrator stage4

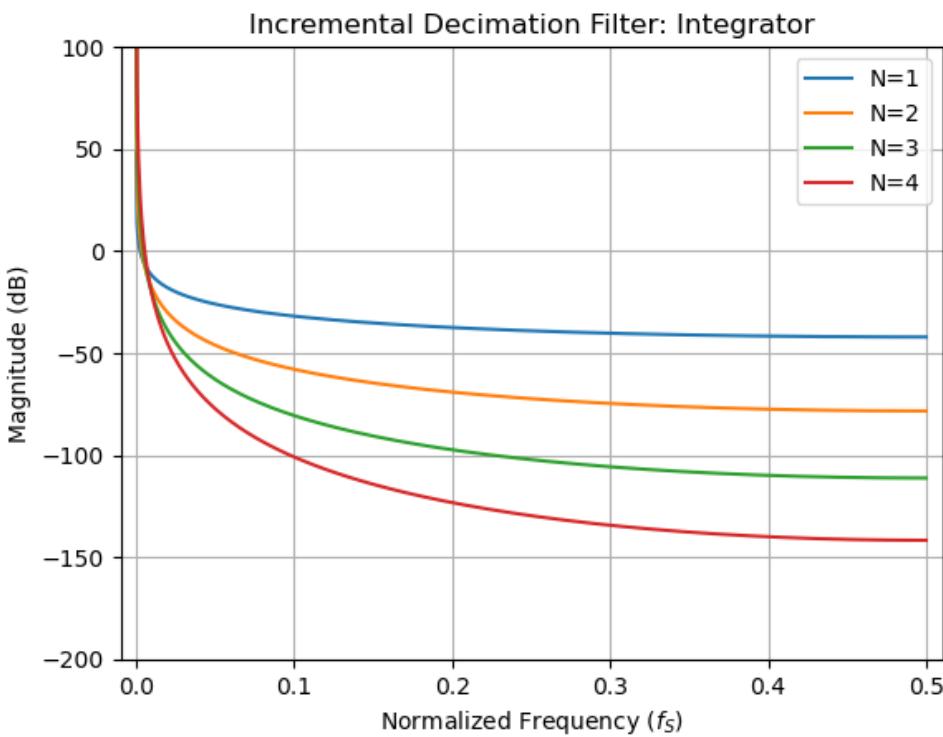


Figure 17 Frequency Response of Decimation Filter

$$f_S = \frac{\text{input } f}{F_s} \text{ where } F_s = 800\text{kHz}$$

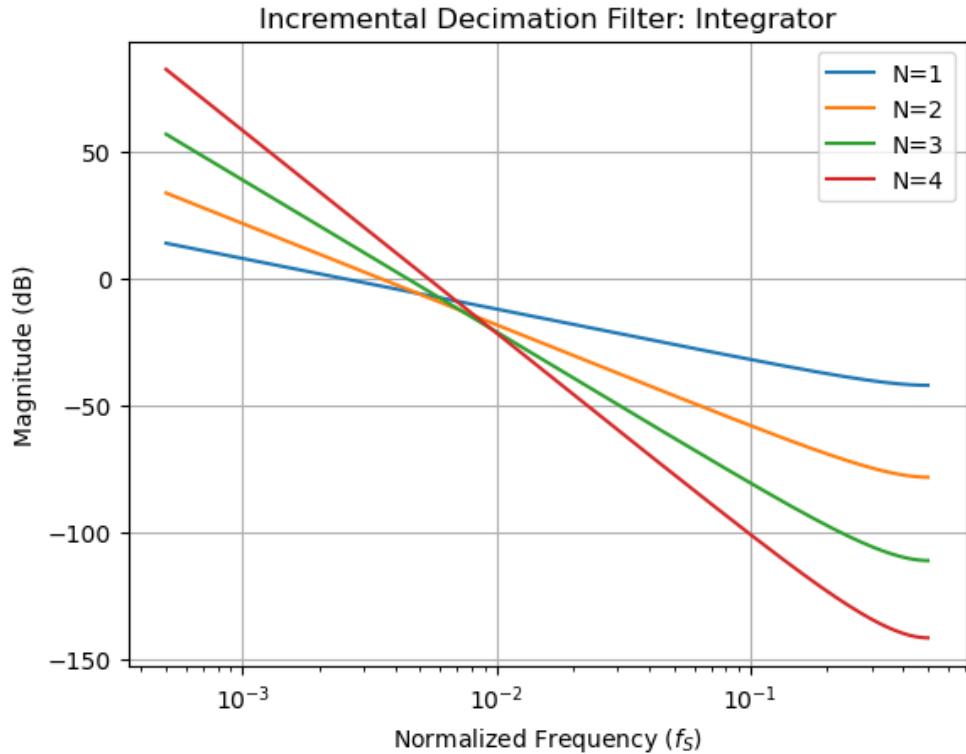


Figure 18 Frequency Response of Decimation Filter: log scale

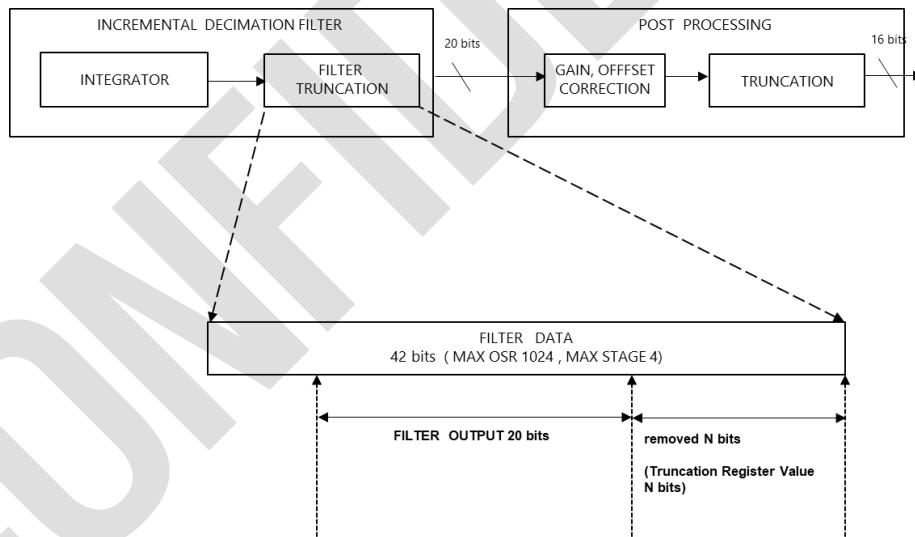


Figure 19 Incremental Decimation Filter Truncation

Refer to Sec. 7 for an example of filter settings.

6.2.3.2 CIC

The CIC (Cascaded Integrator and Comb) filter can be expressed by the following equation.

$$H(z) = \sum_{k=0}^{(RM-1)N} C_k z^{-k} = \left[\sum_{k=0}^{RM-1} z^{-k} \right]^N = \frac{(1 - z^{-RM})^N}{(1 - z^{-1})^N} = H_I^N(z) H_C^N(z)$$

C_k is an arbitrary constant that satisfies the equation, N represents the number of stages of the CIC filter, R is the decimation rate, and M denotes the delay order. As can be seen from the equation, it essentially takes the form of an FIR filter and is specifically implemented in a cascade of an integrator $H_I^N(z)$ and a differentiator $H_C^N(z)$. Particularly in a decimation filter, $H_C^N(z)$ is purely expressed as z^{RM} , which allows processing after decimation through the Noble identity. Therefore, when implemented by applying the Noble identity, it can be simplified to the form shown in Figure 20

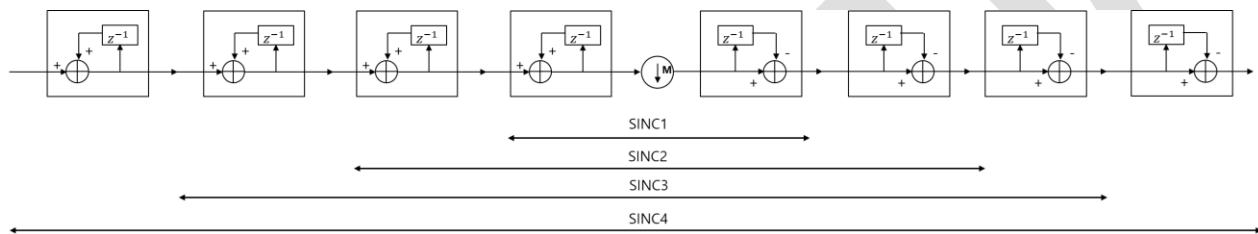


Figure 20 CIC Decimation Filter

The resolution is determined by the integrator of the CIC filter, and the maximum bit vector size is determined by the magnitude of the accumulated value until one sample is output during the CIC filter's decimation. In the CIC equation, the maximum gain G_{max} from the integrator can be calculated, and the maximum output bit vector size can be determined from the following relation using the input bit vector size B_{in} and the logarithmic value of the maximum gain B_{in} .

$$G_{max} = (RM)^N$$

$$B_{max} = [N \log_2(RM) + B_{in}]$$

You can select the sinc order through register settings. To achieve a 1:1 ratio between OSR and ODR, SINC1 should be selected. Choosing SINC2/3/4/5 allows for more noise reduction, but with each increase in the number of stages, a delay equivalent to the OSR occurs. Figure 18 displays the magnitude response according to the number of stages. As shown in the figure, increasing the number of stages effectively reduces high-frequency noise. The input frequency is scaled by $F_s \times OSR$, where $F_s = 800\text{kHz}$ and $OSR = 16$. N indicates the number of stages.

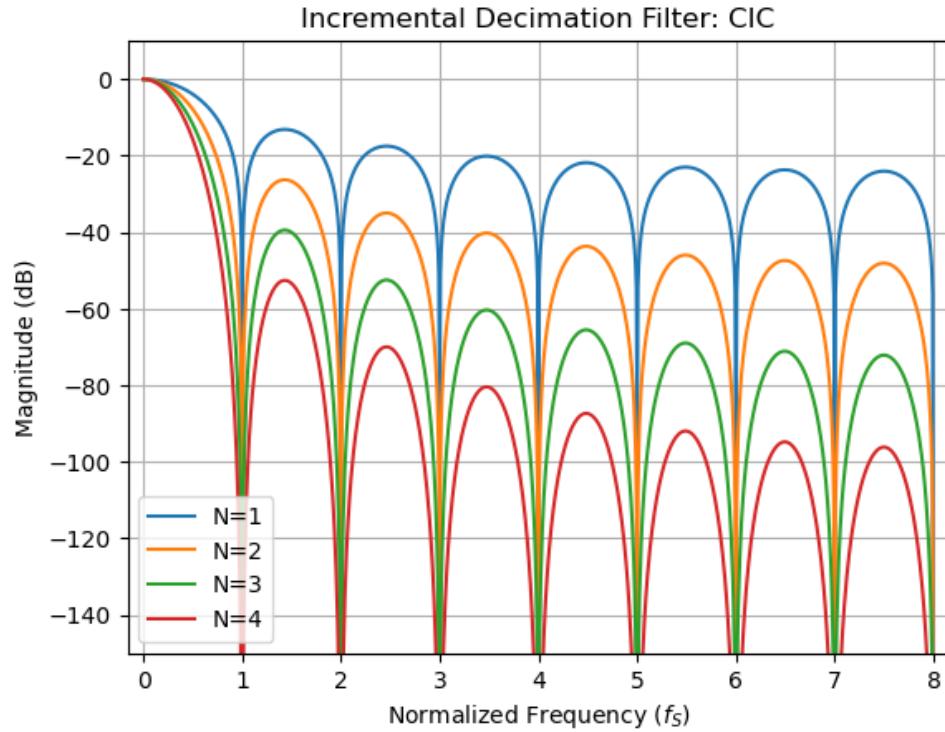


Figure 21 Frequency Response of CIC Decimation Filter

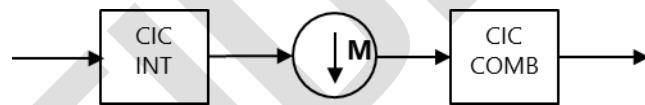


Figure 22 Decimation filter: CIC SINC1

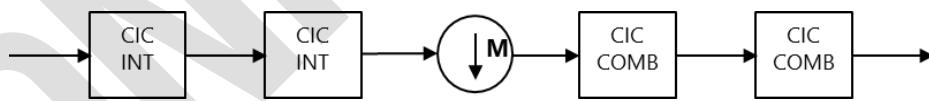


Figure 23 Decimation filter: CIC SINC2

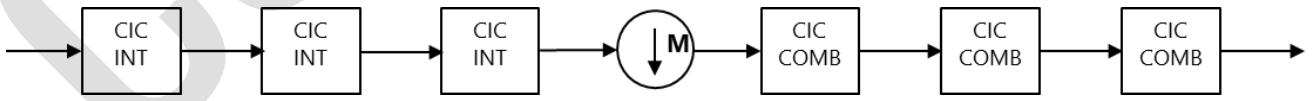


Figure 24 Decimation filter: CIC SINC3

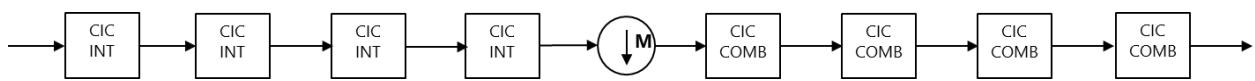


Figure 25 Decimation filter: CIC SINC4

6.2.4 Average Filter

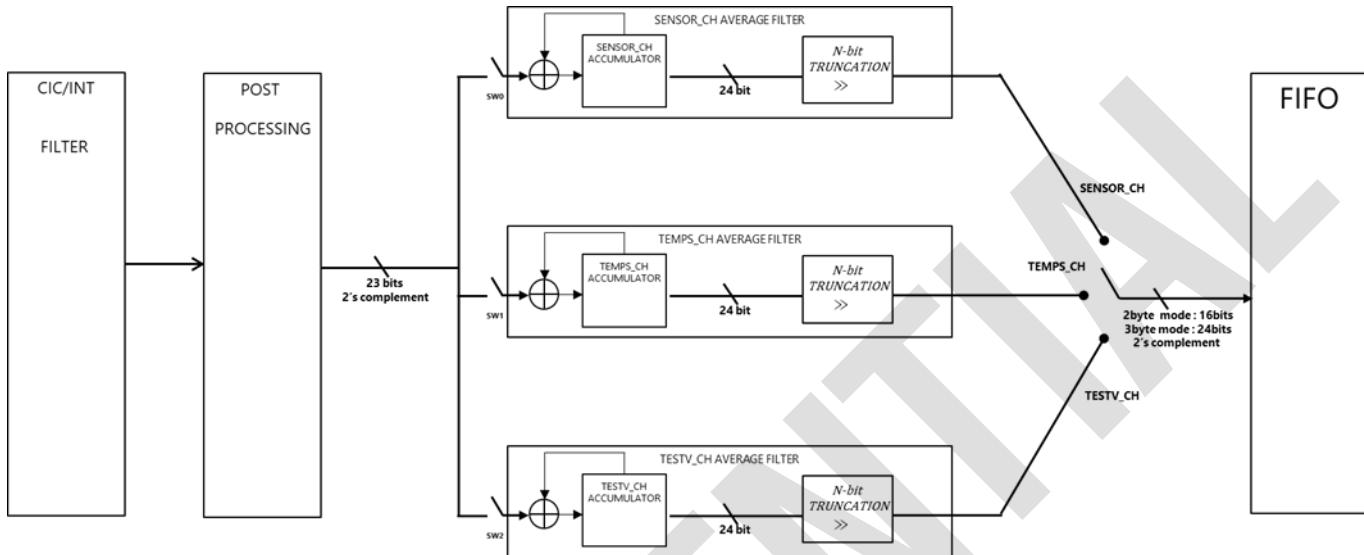


Figure 26 Average Filter Block Diagram

The Average Filter is a block that accumulates and averages the output of the decimation filter (CIC or integrator). The number of accumulations can be set using the CH_AVG_CNT register. The average of the accumulated value is calculated by applying a bit shift operation, and the number of bit shifts is set using the CH_AVG_TRNC register. The output of the accumulator is fixed at 24 bits, and the data stored in the FIFO can be in either 2-byte mode or 3-byte mode. When 2-byte mode is applied, only 16 bits are used, so the user must appropriately use the *CH_AVG_TRNC to prevent overflow. Even if overflow does not occur within the accumulator, when using 16 bits for the final output, truncation bits should be applied, considering the operating environment."

Table 13 Average Filter Register Setting

AVGSMPL (Average Sample)	*CH_AVG_CNT	*CH_AVG_TRNC
1 sample	0x0	0x0
2 sample	0x1	0x1
4 sample	0x3	0x2
8 sample	0x7	0x3
16 sample	0xF	0x4

To apply the Average Filter, the register settings provided in Table 13 must be used.

When the number of accumulations is not a power of 2 (2^n), an exact average cannot be obtained, so users should take this into account when configuring the settings.

FILTER CONTROL Register (AOM)

Address	7	6	5	4	3	2	1	0	reset										
0x0B	-	SEL_FLT	SEL_STAGE [1:0]		LOW_LATENCY	FILTER_LATENCY	DSM_INV	SIGN_CONV_TYPE	0x03										
	-	RW	RW		RW	RW	RW	RW											
Bit	Field		Type	Reset	Description														
6	SEL_FLT		R/W	0x00	filter type selection : [0] INT [1] CIC														
5:4	SEL_STAGE[1:0]		R/W	0x00	FILTER STAGE : if Filter type is selected as a CIC, this stage means the SINC order. <table border="1"> <tr><th>SEL_STAGE</th><th>Filter Stage</th></tr> <tr><td>0x0</td><td>STAGE1</td></tr> <tr><td>0x1</td><td>STAGE2</td></tr> <tr><td>0x2</td><td>STAGE3</td></tr> <tr><td>0x3</td><td>STAGE4</td></tr> </table>					SEL_STAGE	Filter Stage	0x0	STAGE1	0x1	STAGE2	0x2	STAGE3	0x3	STAGE4
SEL_STAGE	Filter Stage																		
0x0	STAGE1																		
0x1	STAGE2																		
0x2	STAGE3																		
0x3	STAGE4																		
3	LOW_LATENCY		R/W	0x00	cic filter low latency Mode [0] disable [1] enable														
2	FILTER_LATENCY		R/W	0x00	INTEGRATOR FILTER MODE Latency 0: osr + stage num 1: osr														
1	DSM_INV		R/W	0x01	sign inversion : [0] unsigned [1] signed for filter input														
0	SIGN_CONV_TYPE		R/W	0x01	[0] : 2X -1 [1] : 2X+1														

SENSOR CHANNEL DECIMATION FILTER PARAMETER1 CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset	
0x0E	SENSOR_CH_OSR[7:0]								0x00	
	RW									
Bit	Field		Type	Reset	Description					
7:0	SENSOR_CH_OSR		R/W	0x00	SENSOR_CH_OSR[10:0] : Sensor channel OSR. the setting value is limited from 8 to 1024					

SENSOR CHANNEL DECIMATION FILTER PARAMTER2 CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset
0x0F	SENSOR_CH_TRNC[4:0]						SENSOR_CH_OSR[10:8]		

	RW				RW							
Bit	Field	Type	Reset	Description								
7:3	SENSOR_CH_TRNC[4:0]	R/W	0x00	Sensor channel Decimation Filter Truncation : LSB N bits right shift								
2:0	SENSOR_CH_OSRA[10:8]	R/W	0x00	SENSOR_CH_OSRA[10:8] : Sensor channel OSR. the setting value is limited from 8 to 1024								

TEMPS CHANNEL DECIMATION FILTER PARAMETER1 CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset					
Bit	Field	Type	Reset	Description										
0x10														
TEMPS_CH_OSRA[7:0]														
RW					0x00									
Bit	Field	Type	Reset	Description										
7:0	TEMPS_CH_OSRA	R/W	0x00	TEMPS_CH_OSRA[10:0] : Temperature sensor channel OSR. the setting value is limited from 8 to 1024										

TEMPS CHANNEL DECIMATION FILTER PARAMETER2 CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset					
Bit	Field	Type	Reset	Description										
0x11														
TEMPS_CH_TRNC[4:0]														
RW					RW									
Bit	Field	Type	Reset	Description										
7:3	TEMPS_CH_TRNC[4:0]	R/W	0x00	Temperature sensor channel Decimation Filter Truncation : LSB N bits right shift										
2:0	TEMPS_CH_OSRA[10:8]	R/W	0x00	TEMPS_CH_OSRA[10:0] : Temperature sensor channel OSR. the setting value is limited from 8 to 1024										

TESTV CHANNEL DECIMATION FILTER PARAMTER1 CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset					
Bit	Field	Type	Reset	Description										
0x12														
TESTV_CH_OSRA[7:0]														
RW					0x00									
Bit	Field	Type	Reset	Description										
7:0	TESTV_CH_OSRA	R/W	0x00	TESTV_CH_OSRA[10:0] : TESTV channel OSR. the setting value is limited from 8 to 1024										

TESTV CHANNEL DECIMATION FILTER PARAMETER2 CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset					
Bit	Field	Type	Reset	Description										
0x13														
TESTV_CH_TRNC[4:0]														
RW					RW									
Bit	Field	Type	Reset	Description										
7:3	TESTV_CH_TRNC[4:0]	R/W	0x00	TESTV channel Decimation Filter Truncation : LSB N bits right shift										

2:0	TESTV_CH_OS[10:8]	R/W	0x00	TESTV_CH_OS[10:0] : TESTV channel OSR. the setting value is limited from 8 to 1024
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SENSOR CHANNEL AVERAGE FILTER PARAMETER CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset
0x15	SENSOR_CH_AVG_CNT[3:0]				-	SENSOR_CH_AVG_TRNC[2:0]			
	RW				-	RW			
Bit	Field			Type	Reset	Description			
7:4	SENSOR_CH_AVG_CNT[3:0]			R/W	0x00	Sensor channel average filter counter			
3						Reserved			
2:0	SENSOR_CH_AVG_TRNC[2:0]			R/W	0x00	Sensor channel average Filter Truncation : LSB N bits right shift			

TEMPS CHANNEL AVERAGE FILTER PARAMETER CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset
0x16	TEMPS_CH_AVG_CNT[3:0]				-	TEMPS_CH_AVG_TRNC[2:0]			
	RW				-	RW			
Bit	Field			Type	Reset	Description			
7:4	TEMPS_AVG_CNT[3:0]			R/W	0x00	Temperature sensor channel average filter counter			
3						Reserved			
2:0	TEMPS_CH_AVG_TRNC[2:0]			R/W	0x00	Temperature sensor channel average Filter Truncation : LSB N bits right shift			

TESTV CHANNEL AVERAGE FILTER PARAMETER CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset
0x17	TESTV_CH_AVG_CNT[3:0]				-	TESTV_CH_AVG_TRNC[2:0]			
	RW				-	RW			
Bit	Field			Type	Reset	Description			
7:4	TESTV_CH_AVG_CNT[3:0]			R/W	0x00	TESTV channel average filter counter			
3						Reserved			
2:0	TESTV_CH_AVG_TRNC[2:0]			R/W	0x00	TESTV channel average Filter Truncation : LSB N bits right shift			

DECIMATION FILTER TEST Register(ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x41	-	DECI_TEST_DATA[5:0]						DECI_TEST_MODE	0x00	
	-	RW						RW		
Bit	Field			Type	Reset		Description			
6:1	DECI_TEST_DATA[5:0]			R/W	0x00		sign inversion			
0	DECI_TEST_MODE			R/W	0x00		deci filter input test mode			

6.2.5 Digital Post Processing

6.2.5.1 CALIBRATION

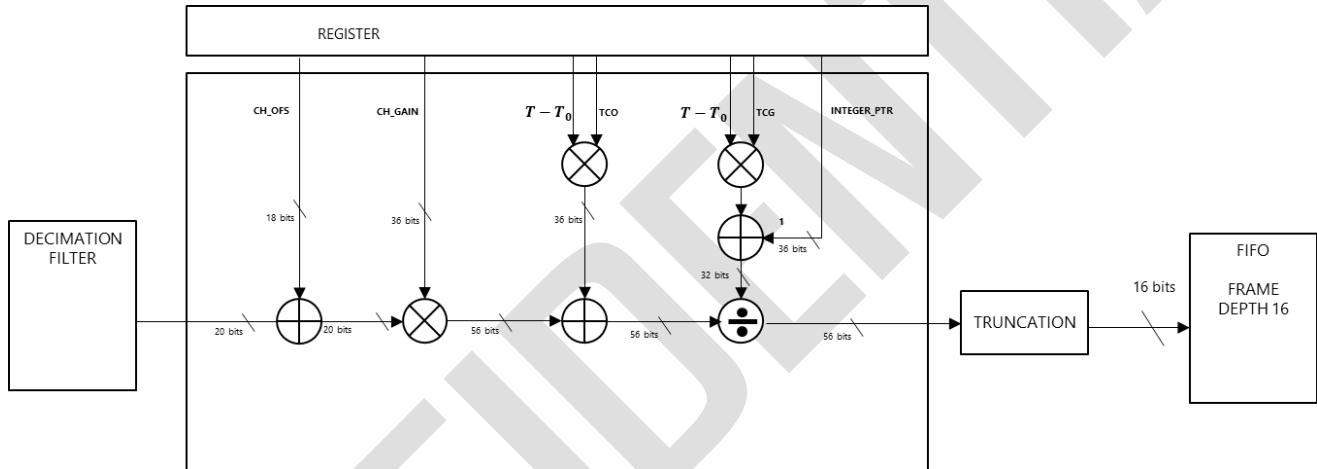


Figure 27 Calibration Block Diagram

The calibration block is used for the compensation of offset and gain. Based on the CHANNEL of the DECIMATION FILTER output, the corresponding OFFSET and GAIN registers are selected for calibration as shown below equation.

$$\text{CalibrationOut} = \frac{(CH_{OFS} + FilterOut) * (CH_{GAIN}) + \Delta T * TCO}{1 + \Delta T * TCG}$$

Refer to Sec. 7 for an example of post processing

6.2.5.2 Offset Calibration

The offset register is 16-bit and is in 2's complement format. The maximum value for offset calibration is 0x7FFF, and the minimum value is 0x8000. TEMP_OFS is applied uniformly to all channels.

6.2.5.3 Gain Calibration

The gain register is in 2's complement format and consists of 18 bits. The default setting, under the condition of CAL_INTEGER_PTR = 0x04, allocates 4 bits for the integer part and 14 bits for the fractional part. The integer and fractional allocation ratio can be adjusted through CAL_INTEGER_PTR register. In post processing, the gain register is composed of {CH_GAIN_INT[4:0], CH_GAIN_FRC[13:0]}. Depending on CAL_INTEGER_PTR setting, the position of the integer and fractional digits can be adjusted.

Table 14 shows the maximum gain according to CAL_INTEGER_PTR and CH_GAIN_INT register settings when CH_GAIN_FRC = 0x00.

Table 14 Gain Calibration Register Value (recommended setting: CAL_INTEGER_PTR=0x04)

CH*_GAIN_INT \ CAL_INTEGER_PTR	0x01	0x02	0x04	0x08	0x10	0x20
0x1	4	2	1	0.5	0.25	0.125
0x2	8	4	2	1	0.5	0.25
0x3	12	6	3	1.5	0.75	0.375
0x4	16	8	4	2	1	0.5
0x5	20	10	5	2.5	1.25	0.625
0x6	24	12	6	3	1.5	0.75
0x7	28	14	7	3.5	1.75	0.875
0x8	-32	-16	-8	-4	-2	-1
0x9	-28	-14	-7	-3.5	-1.75	-0.875
0xA	-24	-12	-6	-3	-1.5	-0.75
0xB	-20	-10	-5	-2.5	-1.25	-0.625
0xC	-16	-8	-4	-2	-1	-0.5
0xD	-12	-6	-3	-1.5	-0.75	-0.375
0xE	-8	-4	-2	-1	-0.5	-0.25
0xF	-4	-2	-1	-0.5	-0.25	-0.125

POST PROCESSING OFFSET CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset
0x1A	SENSOR_CH_OFS[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x1B	SENSOR_CH_OFS[15:8]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset

0x1C	TEMPS_CH_OFS[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x1D	TEMPS_CH_OFS[15:8]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x1E	TESTV_CH_OFS[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x1F	TESTV_CH_OFS[15:8]								0x00
	RW								

- SENSOR_CH_OFS: Sensor channel post processing OFFSET (signed)
- TEMPS_CH_OFS: Temperature Sensor channel post processing OFFSET (signed)
- TESTV_CH_OFS: TESTV channel post processing OFFSET (signed)

POST PROCESSING GAIN FRACTIONAL PART CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset
0x22	SENSOR_CH_GAIN_FRC[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x23	-	-	SENSOR_CH_GAIN_FRC[13:8]						0x00
	-	-	RW						
Address	7	6	5	4	3	2	1	0	reset
0x24	TEMPS_CH_GAIN_FRC[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x25	-	-	TEMPS_CH_GAIN_FRC[13:8]						0x00
	-	-	RW						
Address	7	6	5	4	3	2	1	0	reset
0x26	TESTV_CH_GAIN_FRC[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x27	-	-	TESTV_CH_GAIN_FRC[13:8]						0x00
	-	-	RW						

- SENSOR_CH_GAIN_FRC : Sensor channel post processing gain fractional part (signed)
- TEMPS_CH_GAIN_FRC : Temperature sensor channel post processing gain fractional part (signed)

- TESTV_CH_GAIN_FRC : TESTV channel post processing gain fractional part (signed)

POST PROCESSING GAIN INTEGER PART CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset
0x28	SENSOR_CH_GAIN_INT[3:0]				-	-	-	-	0x11
	RW				-	-	-	-	
Address	7	6	5	4	3	2	1	0	reset
0x29	TESTV_CH_GAIN_INT[3:0]				TEMPS_CH_GAIN_INT[3:0]				0x11
	RW				RW				

- SENSOR_CH_GAIN_INT : Sensor channel post processing gain integer part (signed)
- TEMPS_CH_GAIN_INT : Temperature sensor channel post processing gain integer part (signed)
- TESTV_CH_GAIN_INT : TESTV channel post processing gain integer part (signed)

GAIN FRACTIONAL PART CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset
0x2A	CAL_T0_FRC[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x2B	-	-	CAL_T0_FRC[13:8]						0x00
	-	-	RW						
Address	7	6	5	4	3	2	1	0	reset
0x2C	CAL_T_FRC[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x2D	-	-	CAL_T_FRC[13:8]						0x00
	-	-	RW						
Address	7	6	5	4	3	2	1	0	reset
0x2E	CAL_TCO_FRC[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x2F	-	-	CAL_TCO_FRC[13:8]						0x00
	-	-	RW						
Address	7	6	5	4	3	2	1	0	reset
0x30	CAL_TCG_FRC[7:0]								0x00
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x31	-	-	CAL_TCG_FRC[13:8]						0x00
	-	-	RW						

- CAL_T_FRC : T gain fractional part (signed)
- CAL_T0_FRC : T0 gain fractional part
- CAL_TCG_FRC : TCG gain fractional part
- CAL_TCO_FRC : TCO gain fractional part

GAIN INTEGER PART CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset	
0x32	CAL_T_INT[3:0]					CAL_T0_INT[3:0]				
	RW					RW				
Address	7	6	5	4	3	2	1	0	reset	
0x33	CAL_TCG_INT[3:0]					CAL_TCO_INT[3:0]				
	RW					RW				

- CAL_T_INT : T gain integer part
 - Delta_t = cal_t - cal_t0
- CAL_T0_INT : T0 gain integer part
- CAL_TCG_INT : TCG gain integer part
- CAL_TCO_INT : TCO gain integer part

GAIN INTEGER BIT POINT CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset																										
0x34	-	-	CAL_INTEGER_PTR[5:0]																																
	-	-	RW					0x04																											
Bit	Field		Type	Reset	Description																														
5:0	CAL_INTEGER_PTR[5:0]		R/W	0x04	GAIN register integer bit position <table border="1"> <tr> <td rowspan="2">CAL_INTEGER_PTR REGISTER VALUE</td><td colspan="2">GAIN = {xCH_GAIN_INT[3:0], xCH_GAIN_FRC[13:0]} (x=0 to 3)</td></tr> <tr> <td>INTEGER</td><td>FRACTIONAL</td></tr> <tr> <td>0x01</td><td>5</td><td>12</td></tr> <tr> <td>0x02</td><td>4</td><td>13</td></tr> <tr> <td>0x04</td><td>3</td><td>14</td></tr> <tr> <td>0x08</td><td>2</td><td>15</td></tr> <tr> <td>0x10</td><td>1</td><td>16</td></tr> <tr> <td>0x20</td><td>0</td><td>17</td></tr> <tr> <td>Others</td><td>Not Allowed</td><td>Not Allowed</td></tr> </table>					CAL_INTEGER_PTR REGISTER VALUE	GAIN = {xCH_GAIN_INT[3:0], xCH_GAIN_FRC[13:0]} (x=0 to 3)		INTEGER	FRACTIONAL	0x01	5	12	0x02	4	13	0x04	3	14	0x08	2	15	0x10	1	16	0x20	0	17	Others	Not Allowed	Not Allowed
CAL_INTEGER_PTR REGISTER VALUE	GAIN = {xCH_GAIN_INT[3:0], xCH_GAIN_FRC[13:0]} (x=0 to 3)																																		
	INTEGER	FRACTIONAL																																	
0x01	5	12																																	
0x02	4	13																																	
0x04	3	14																																	
0x08	2	15																																	
0x10	1	16																																	
0x20	0	17																																	
Others	Not Allowed	Not Allowed																																	

POST PROCESSING TRUNCATION BIT SHIFT CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset		
0x36	-	-	SENSOR_CH_TRNC_PP[5:0]					RW			
	-	-									
Address	7	6	5	4	3	2	1	0	reset		
0x37	-	-	TEMPS_CH_TRNC_PP[5:0]					RW			
	-	-									
Address	7	6	5	4	3	2	1	0	reset		
0x38	GAIN_MODE	-	TESTV_CH_TRNC_PP[5:0]					RW			
	RW	-									
Bit	Field	Type	Reset	Description							
7	GAIN_MODE	R/W	0x00	The temperature channel is set to bypass mode regardless of the gain mode configuration. - 0x0 : bypass mode - 0x1 : gain scaling mode							
6				Reserved							
5:0	xCH_TRNC_PP[5:0]	R/W	0x00	x Channel (x=SENSOR to TESTV) post processing output truncation n bit shift (recommend value: 0x0) o 0x0 : fractional part is removed (default set)							

6.3 DAC CIRCUIT

6.3.1 DAC

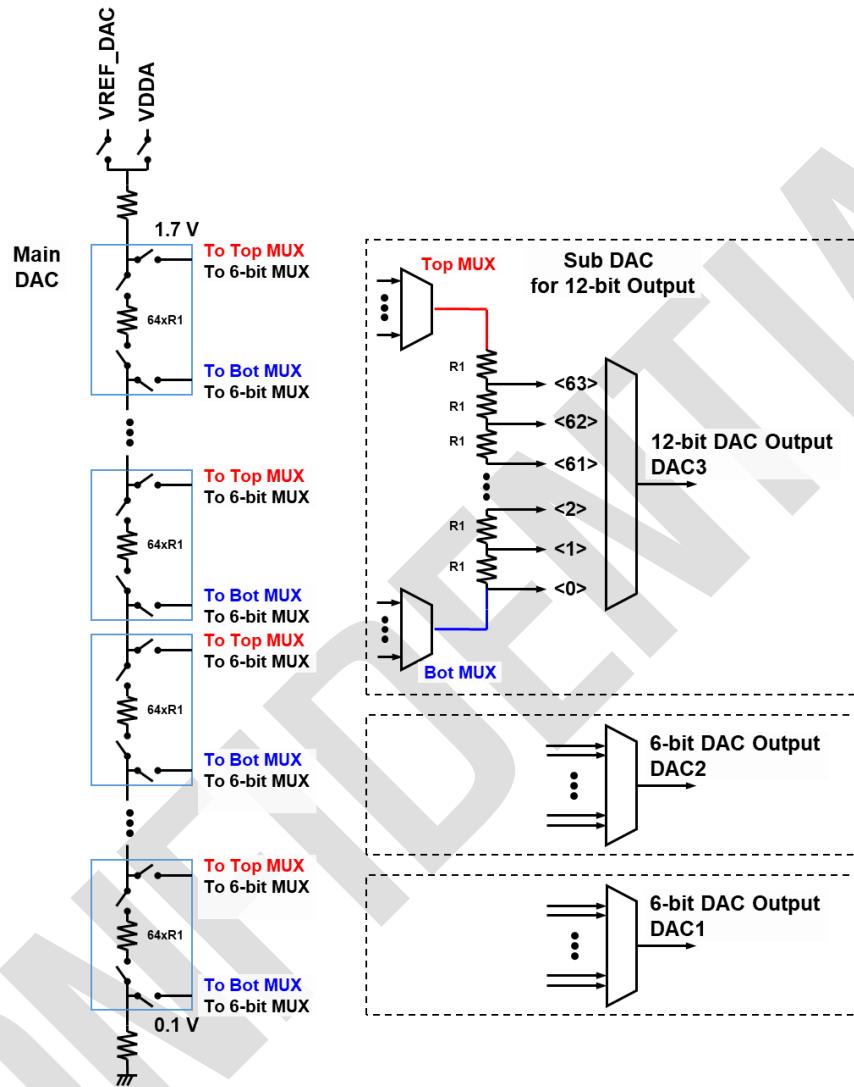


Figure 28 R-DAC Circuit Diagram, for the case of VDDA=1.8V

The R-DAC provides two 6-bit resolution outputs (VZERO0, VZERO1) and one 12-bit resolution output (VBIAS). When using a 1.8V VDDA, the main DAC divides the 0.1V to 1.7V range into 64 levels, corresponding to a 6-bit resolution. This is selected by MUX according to the DAC1 and DAC2 values, and output as a 6-bit voltage. Two adjacent nodes selected by the main DAC are connected to the top MUX and bottom MUX, respectively, and applied in series to a 64-resistor array in the subsidiary DAC, further subdividing the voltage into 64 levels. By multiplexing the nodes of the subsidiary DAC, a 12-bit output voltage is generated.

The 6-bit output voltage can be calculated as follows.

$$6-bit DAC LSB = \frac{1.7 - 0.1}{2^6 - 1} = 25.397 \text{ mV}$$

$$DAC1 Output = 0.1 + 6-bit DAC LSB \times DAC1_VZERO_0[5:0]$$

$$DAC2 Output = 0.1 + 6-bit DAC LSB \times DAC2_VZERO_1[5:0]$$

The 12-bit output voltage can be calculated as follows.

$$12-bit DAC LSB = \frac{1.7 - 0.1}{2^{12} - 1} = 39.072 \mu\text{V}$$

$$DAC3 Output = 0.1 + 12-bit DAC LSB \times DAC3_VBIAS[11:0]$$

DAC3 CONTROL1 Register(AOM)

Address	7	6	5	4	3	2	1	0	reset
0xCE	DAC3_VBIAS[7:0]								0x00
	RW								
Bit	Field								Type
7:0	DAC3_VBIAS[7:0]								R/W
	0x00								DAC3 output data (VBIAS), 12-bit control

DAC3 CONTROL2 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset			
0xCF	-	-	-	-	DAC3_VBIAS[11:8]							
	-	-	-	-	RW							
Bit	Field								Type			
3:0	DAC3_VBIAS[11:8]								R/W			
	0x00								DAC3 output data (VBIAS), 12-bit control			

DAC1 CONTROL Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xD0	-	-	DAC1_VZERO_0[5:0]							
	-	-	RW							
Bit	Field								Type	
5:0	DAC1_VZERO_0[5:0]								R/W	
	0x00								DAC1 output data (VZERO_0), 6-bit control	

DAC2 CONTROL Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xD1	-	-	DAC2_VZERO_1[5:0]						0x00	
	-	-	RW							
Bit	Field			Type	Reset	Description				
5:0	DAC2_VZERO_1[5:0]			R/W	0x00	DAC2 output data (VZERO_1), 6-bit control				

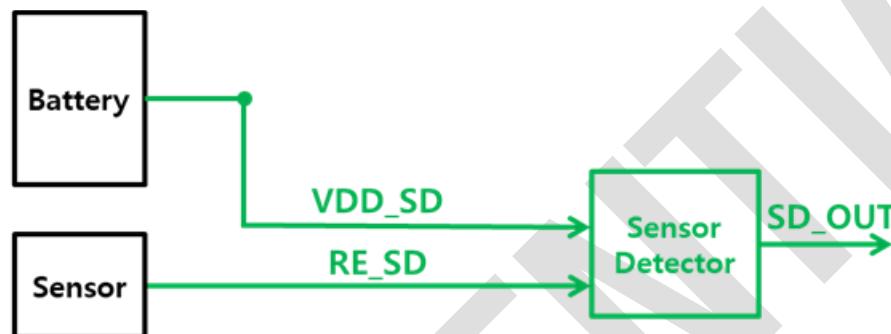
6.4 SENSOR DETECTOR

Figure 29 Sensor Detector Schematic.

Table 15 Sensor Detector Pin Description

Input	PIN name	Description
	VDD_SD	Battery Power Connected
	RE_SD	Physical contact(Ground) or No physical contact(Floating state)
Output	SD_OUT	Output

Table 16 Sensor Detector Condition Table

Condition	Input		Output
	VDD_SD	RE_SD	SD_OUT
1	Battery Power disconnected	Physical contact(Ground)	Low
2	Battery Power disconnected	No physical contact(Floating state)	Low
3	Battery Power Connected	Physical contact(Ground)	High
4	Battery Power Connected	No physical contact(Floating state)	Low

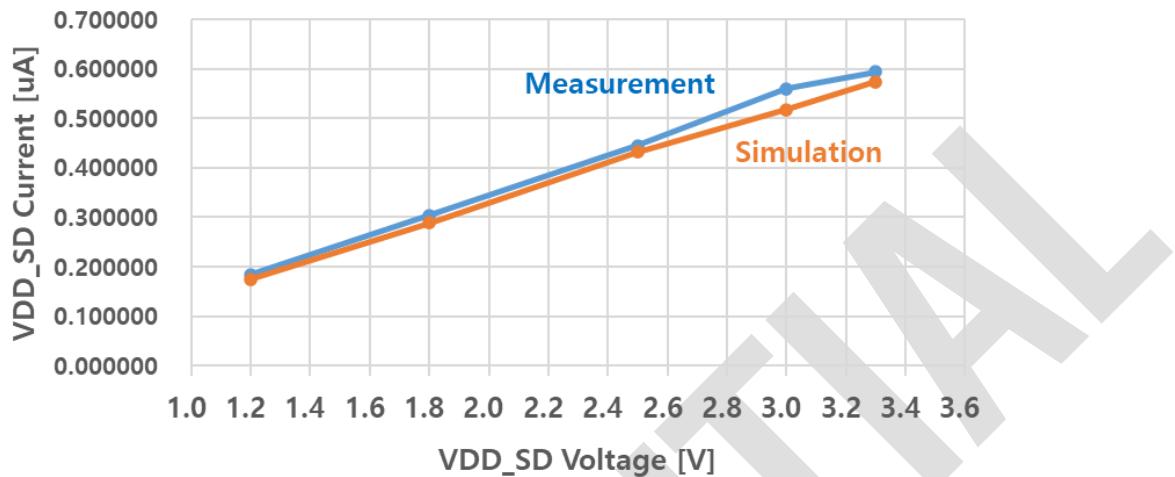


Figure 30 Current Consumption of Sensor Detector

Figure 29 shows the Sensor Detector Schematic. A 1uF capacitor should be connected externally for operation. VDD_SD is connected to the battery voltage, VBAT. When SD_RE is connected in the sequence 'Floating → GND → Floating', SD_OUT outputs 'L → H → H'.

Figure 30 shows the current consumption.

As devices become smaller, managing battery usage becomes just as important as low-power design. For example, NMS4110 or devices containing it may be stored on a shelf before sale, often paired with very small coin batteries. If there is any current consumption during storage, the battery could discharge over long storage periods, making reliable use difficult after shipping or sale.

For instance, in the case of a CR1632 battery, which has 3V and 120mAh (or 360mWh) of energy capacity, if current is consumed over a year, the minimum current consumption would be 13.69uA. If such minimal current exists, the device would be unusable when launched after a year of storage.

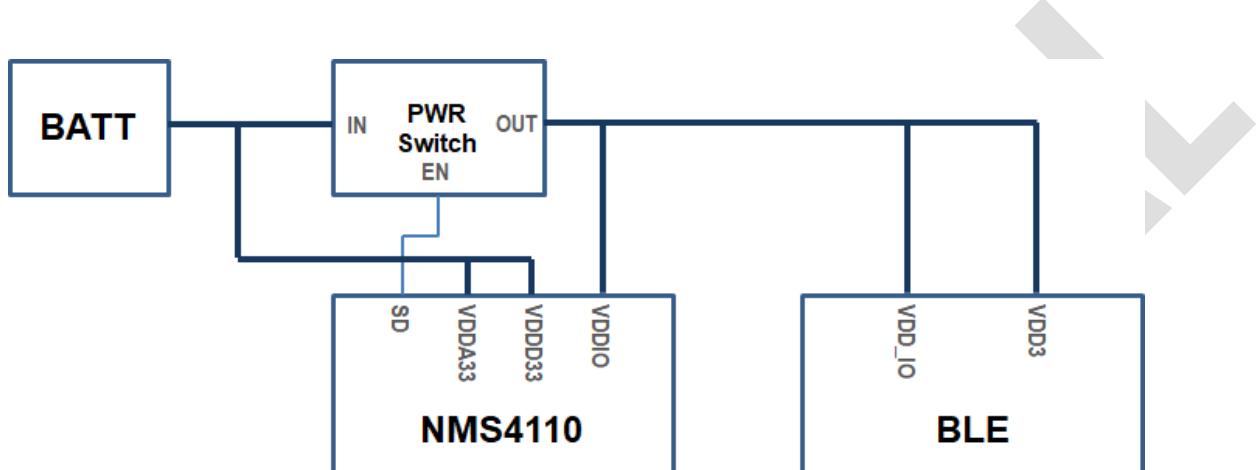
Additionally, if the device is powered on for use via Bluetooth or a physical switch, the process may become cumbersome, reducing user convenience. Moreover, if malicious reuse of devices through disassembly is allowed, leading to the circulation of faulty products, especially in medical devices, it could cause serious issues.

Therefore, the operating a Sensor Detector gives benefits as follows:

- Prevent the use of battery energy before the device is in actual use.
- Ensure that power is activated immediately after the device is used, such as when a continuous glucose monitor is attached to the skin.

- Automatically cut off power if the device is removed from the skin, either intentionally or unintentionally.
- Ensure that power does not turn on again if the removed device is reattached to the skin.

To achieve these benefits, NMS4110 presupposes the following power supply configuration.



The battery power is supplied to the NMS4110 and other devices through a power switch, which operates only when the output of the Sensor Detector is high. The output voltage of the Sensor Detector supports four different states according to the phase table.

Measure Phase	Initial	Phase 1	Phase 2	Phase 3	Phase 4
VDD_SD	Floating	3V	3V	3V	Floating
SD_RE	Floating	Floating	0V	Floating	Floating
SD_OUT	Low	Low	High	High	Low

Indicate state transition After several seconds

- Status 1: Before the device is used or when the battery is connected during assembly, the output is LOW (initial)
- Status 2: When the device is inserted for the first time, the output is HIGH
- Status 3: When the device is removed from the skin after the first attachment, the output remains HIGH
- Status 4: When the device is left unattended after removal, the output is LOW, regardless of whether the battery is connected

6.5 POWER MANAGEMENT

NMS4110 can operate between active mode for normal operation and sleep mode for low power consumption. In active mode, all power are turned on and external crystal starts oscillation, but in sleep mode, as shown in Figure 31, the separated power domain disables LDODONO, causing the on/off regions and the XTAL to stop functioning.

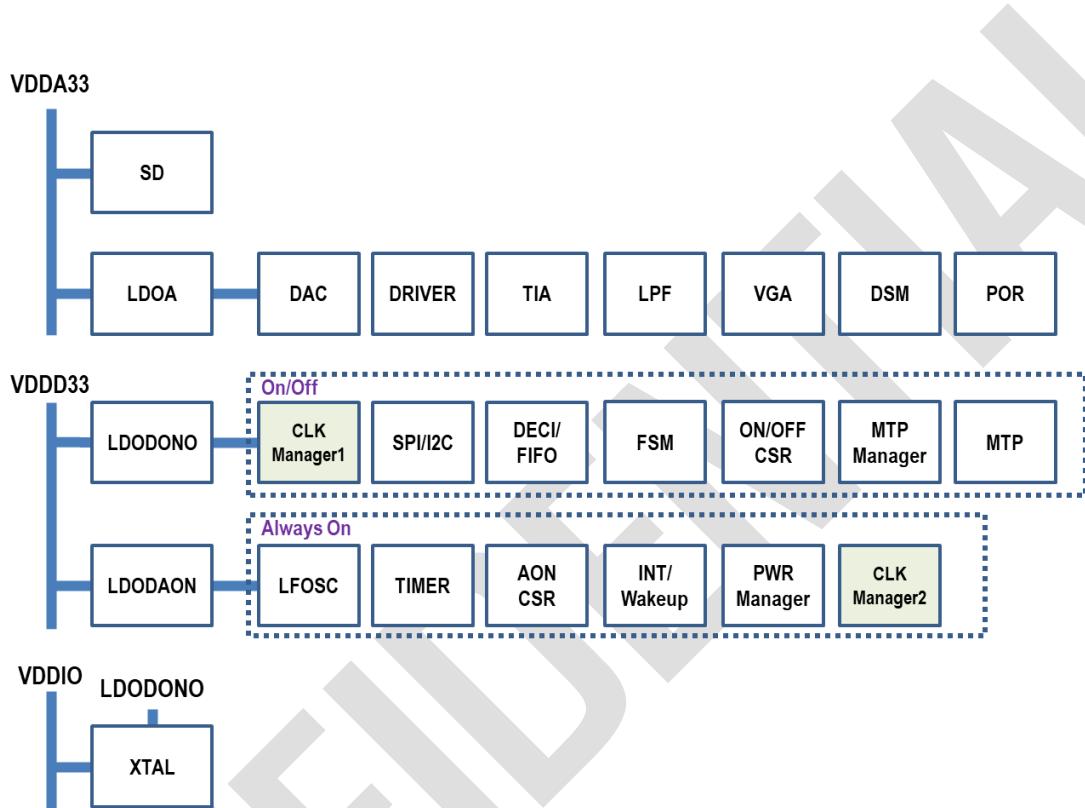


Figure 31 Power Domain

6.5.1 Power Mode Control

NMS4110 provides several methods to control the power status. There are two power states in NMS4110, active mode and sleep mode. Power down means a transition from active mode to sleep mode, and wake-up means a transition from sleep mode to active mode.

MODE (address 0x61) register is used to control the power state and supports three modes.

- 0x0: always-on mode, always turned on (power state is fixed to active mode)
- 0x1: pin-controlled mode, power state is controlled by WAKEUP
 - In case of a transition of WAKEUP from low to high, the power state is set to active mode as long as WAKEUP remains high.

- In case of a transition of WAKEUP from high to low, the power state is set to sleep mode as long as WAKEUP remains low.
- 0x2: timer-controlled mode, the power state is controlled by an internal timer and PWR_DN(address 0x61) register
 - In case of a transition of PWR_DN register from low to high, the power state is set to sleep mode by power down
 - In case of a timer hit is triggered by the end of the sleep duration, the power state is switched to active mode by wake-up

6.5.1.1 Timer

Timer is activated when the power mode is set to timer-controlled mode and uses the clock output of LFOSC, trimmed to 32KHz, as the clock input. It is controlled by the WAKEUP_PRD (addresses 0x62, 0x63, 0x64), TIMER_STOP (address 0x61), and TIMER_RST (address 0x61) registers.

- **WAKEUP_PRD:** define the timer expiration period. It can be set in 1msec units up to 4,194,303msec. Timer counts from 0, and when it reaches the set period, it signals a timer hit and resets to 0 to start counting again.
- **TIMER_STOP:** set to '1' to stop timer and reset the count value to 0. After setting to 0, the timer resumes operation.
- **TIMER_RST:** set to '1' to reset timer count value, and begin counting again.

6.5.2 CSR Back-up

NMS4110 supports a backup of the values in certain CSR registers during power down. When BACKUP_EN (address 0x61) is set to high, during the power-down process, the values written to the CSR registers are saved to nonvolatile memory. Additionally, during the wake-up process after a sleep mode, the values are restored into the CSR registers.

BACKUP CONTROL Register (AOM)

Address	7	6	5	4	3	2	1	0	reset				
0x61	-	-	BACKUP_EN	PWR_DN	TIMER_RST	TIMER_STOP	MODE[1:0]		0x00				
	-	-	RW	RW	RW	RW	RW						
Bit	Field		Type	Reset	Description								
5	BACKUP_EN		R/W	0x00	Back-up Enable before Power Down								
4	PWR_DN		R/W	0x00	System Forced Power Down (at wake-up mode 2)								
3	TIMER_RST		R/W	0x00	System Timer Reset (at wake-up mode 2)								

2	TIMER_STOP	R/W	0x00	System Timer Disable (at wake-up mode 2)
1:0	MODE[1:0]	R/W	0x00	Wake-up Mode 0: always-on, 1: PAD_WAKE Controlled, 2: timer controlled

WAKEUP PERIOD1 CONTROL Register (AOM)

Address	7	6	5	4	3	2	1	0	reset		
0x62	WAKEUP_PRD[7:0]								0xA0		
RW											
Bit	Field		Type	Reset	Description						
7:0	WAKEUP_PRD[7:0]		R/W	0xA0	wake-up triggering period bits						

WAKEUP PERIOD2 CONTROL Register (AOM)

Address	7	6	5	4	3	2	1	0	reset		
0x63	WAKEUP_PRD[15:8]								0xBB		
RW											
Bit	Field		Type	Reset	Description						
7:0	WAKEUP_PRD[15:8]		R/W	0xBB	wake-up triggering period bits						

WAKEUP PERIOD3 CONTROL Register (AOM)

Address	7	6	5	4	3	2	1	0	reset		
0x64	-	-	WAKEUP_PRD[21:16]								
RW											
Bit	Field		Type	Reset	Description						
5:0	WAKEUP_PRD[21:16]		R/W	0x0D	wake-up triggering period bits						

6.6 SERIAL INTERFACE

The serial interface, such as I2C or SPI, could be configured as shown in Table 17, Figure 32, and Figure 33.

Table 17 Serial Interface Pin Map

PIN NAME	I2C	SPI	Description
SCL	SCL	SCLK	SPI : clock I2C : clock

SDA	SDA	MISO	SPI : data out I2C : serial data
CSN		CSN	SPI : enable
MOSI		MOSI	SPI : data input

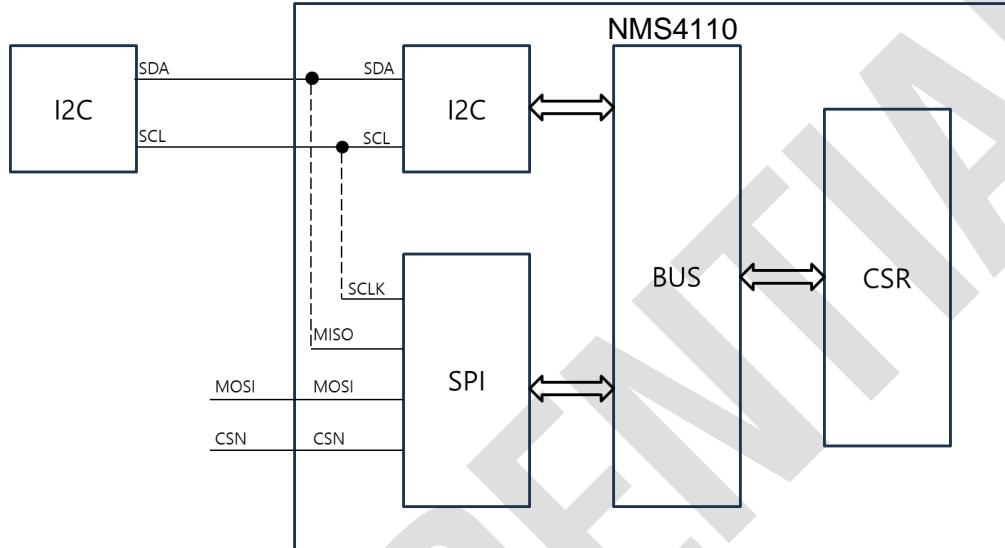


Figure 32 I2C Configuration

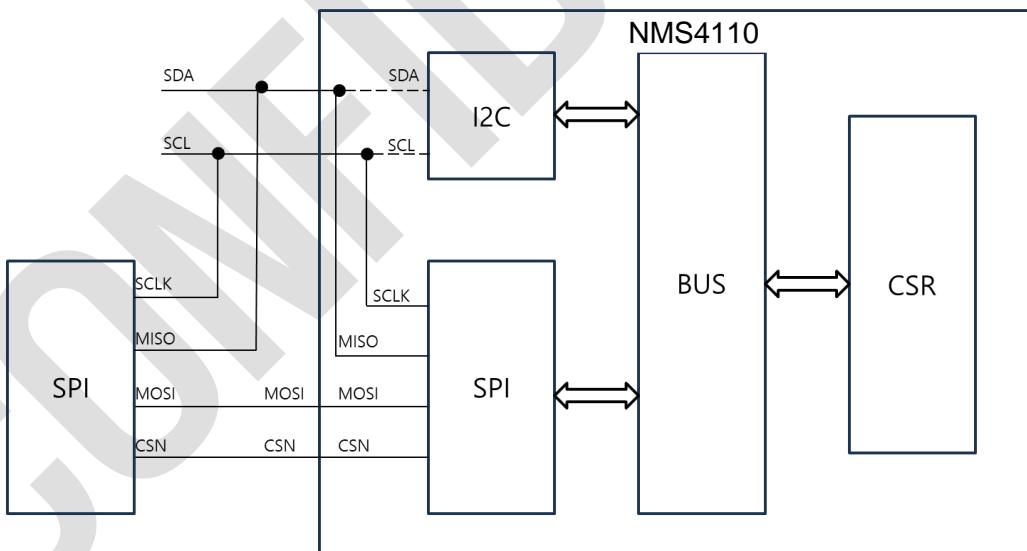


Figure 33 SPI Configuration

SPI and I2C could be used as a serial interface. After a chip reset, the first interface defines the type of the serial interface to be used for external connection. For example, if SPI is used to connect after a chip reset, I2C will not be available until the next chip reset. Conversely, if I2C is used for register access

after a chip reset, only I2C can be used as shown in Figure 34. I2C_SEL_FE would be set to low to force I2C only usage.

Address	7	6	5	4	3	2	1	0	reset
0x65	NUM_CMD_WAIT[1:0]		NUM_CLK_WAIT[1:0]		NUM_RD_WAIT[1:0]		SPI_SEL_FE	I2C_SEL_FE	0x54

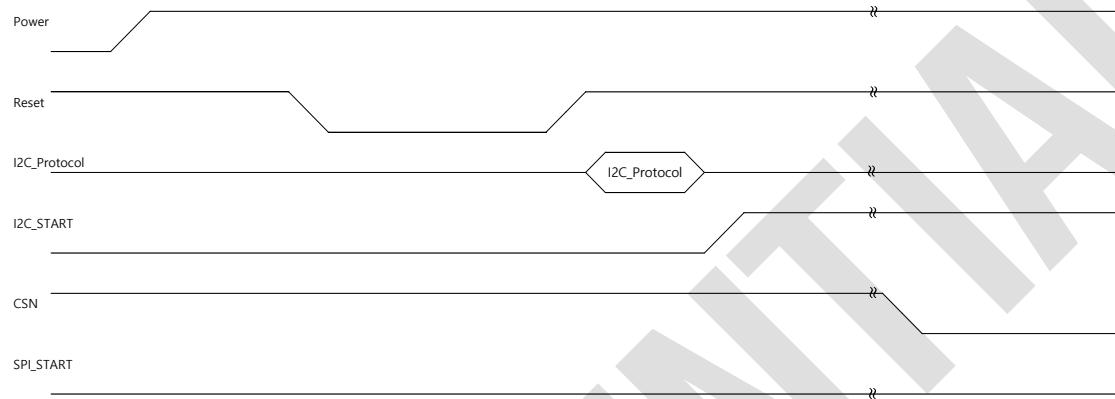


Figure 34 Serial Interface Example

6.6.1 SPI

6.6.1.1 SPI Command

Table 18 SPI Command

Command	Value	Description
REG_WR_BYTE	0x00	SPI Write
REG_RD_BYTE	0x80	SPI Read
FIFO_RX_POP	0xB0	SPI FIFO Access

6.6.1.2 SPI Write

- Command field : 0x00

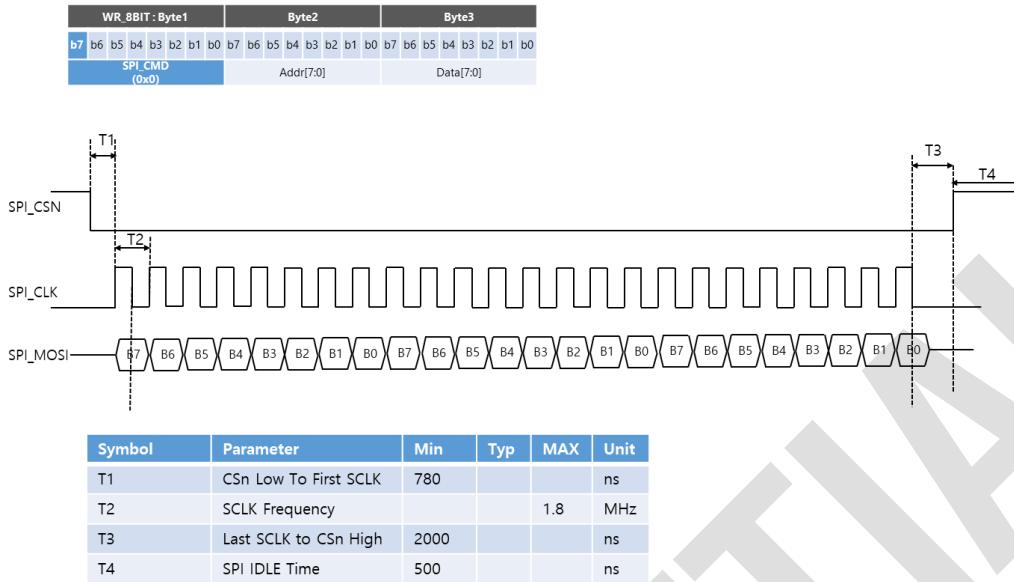


Figure 35 SPI Register Write Protocol

6.6.1.3 SPI Read

- Command field : 0x80

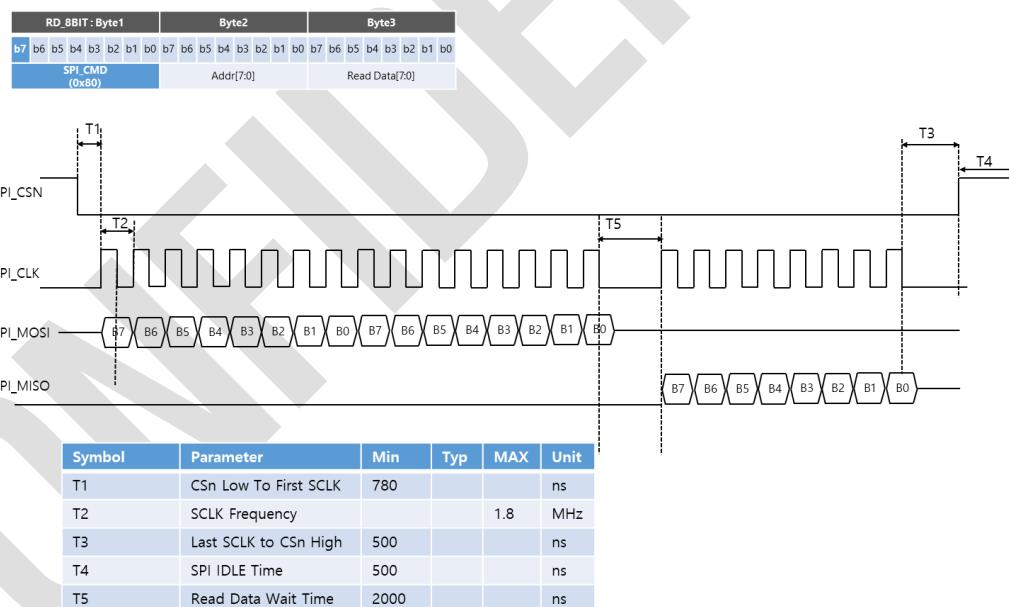


Figure 36 SPI Register Read Protocol

6.6.1.4 SPI FIFO Access

SPI supports the maximum speed of the quarter of system clock.

Figure 37 SPI FIFO Access

SPI uses an access protocol that consists of command and data sequentially.

- Command field : 0xB0
 - Data field : the data stored in FIFO, MSB first

6.6.2 I2C

- Device ID
 - ID : 011_0000
 - Write Operation : 0110_0000
 - Read Operation : 0110_0001

6.6.2.1 I2C Write

- Write Single
 - DEVICE_ID_WR – WRITE_ADDRESS – WRITE_DATA
 - EX) 01100000 – 8bit Address – WRTIE_DATA

S	DevID (7-bit)						R/W	Ack	Address (8-bit)						Ack	Data (8-bit)						Ack	P
	(msb)			...		(lsb)	0	(msb)			...			(lsb)	(msb)			...			(lsb)		

Figure 38 I2C Write Protocol

6.6.2.2 I2C Read

- Read Single
 - DEVICE_ID_WR – READ_ADDRESS – READ_DATA
 - EX) 01100001 – 8bit Address – READ_DATA

S	DevID (7-bit)					R/W	Ack	Address (8-bit)					Ack	Data (8-bit)					Ack	P
	(msb)			...		(lsb)	1	(msb)			...		(lsb)	(msb)			...		(lsb)	

Figure 39 I2C Read Protocol

6.6.2.3 I2C FIFO Access

When reading FIFO using I2C, an internal read request is automatically generated, and the data read is deleted from FIFO. For registers other than FIFO, the address automatically increments, but if the starting address is the FIFO, the address does not automatically increment and remains fixed until the I2C operation is completed.

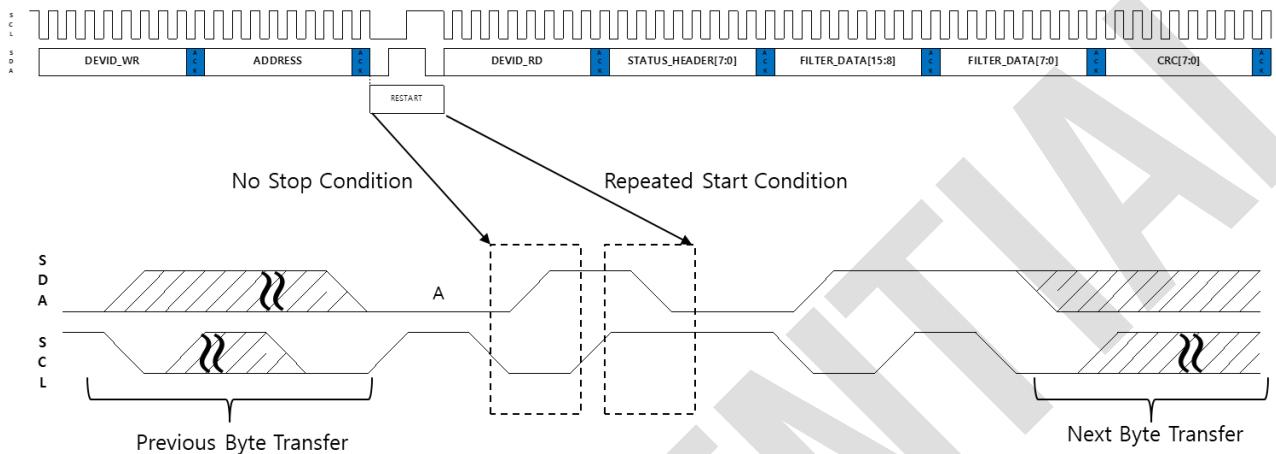


Figure 40 I2C FIFO Read Protocol

6.6.3 Serial Interface Registers

I2C MODE CONTROL Register (ONR)

Address	7	6	5	4	3	2	1	0	reset
0x51	SLV_BYT_E _ADDR _MD	SLV_DEVID[6:0]							
	RD	RW							
Bit	Field	Type	Reset	Description					
7	SLV_BYTE_ ADDR _MD	R/W	0x01	SLV_BYTE_ADDR_MD : I2C mode select 0x0 : word mode 0x1 : byte mode					
6:0	SLV_DEVID [6:0]	R/W	0x30	SLV_DEVID[6:0] : I2C Device ID (default : 0x30)					

FIFO DATA Register (ONR)

Address	7	6	5	4	3	2	1	0	reset
0x5F	FIFO_DATA[7:0]								0x00
	RO								
Bit	Field	Type	Reset	Description					

7:0	FIFO_DATA[7:0]	RO	0x00	FIFO Read Data
-----	----------------	----	------	----------------

MTP MEMORY AND SERIAL INTERFACE CONTROL Register (AOM)

Address	7	6	5	4	3	2	1	0	reset			
0x65	NUM_CMD_WAIT[1:0]		NUM_CLK_WAIT[1:0]		NUM_RD_WAIT[1:0]		SPI_SEL_FE	I2C_SEL_FE	0x54			
	RW		RW		RW		RW	RW				
Bit	Field	Type	Reset	Description								
7:6	NUM_CMD_WAIT[1:0]	R/W	0x01	Delay between Different Operation Command								
5:4	NUM_CLK_WAIT[1:0]	R/W	0x01	OSC_CLK Delay before ERASE or PROG Operation								
3:2	NUM_RD_WAIT[1:0]	R/W	0x01	Delay between READ Operation								
1	SPI_SEL_FE	R/W	0x00	Force enable I2C 0x0 : disable 0x1 : enable, If SPI_SEL_FE is enabled at the same time, I2C takes priority								
0	I2C_SEL_FE	R/W	0x00	Force enable SPI 0x0 : disable 0x1 : enable								

6.7 FIFO

FIFO is used to read out the sensed data from NMS4110 to external devices such as MCU.

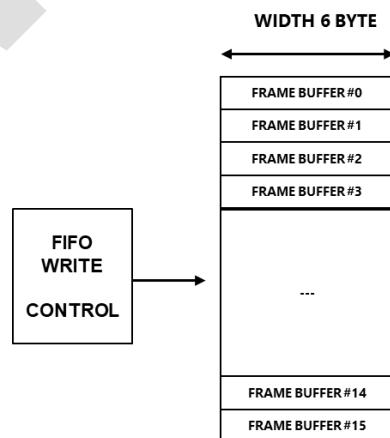


Figure 41 FIFO Block Diagram

6.7.1 FIFO SIZE

FIFO depth (or the number of words) is 16, and 1 word can store 1 frame. The length of 1 frame varies according to the settings of the FIFO_FORMAT register. The maximum size is 6 bytes (header + 3-byte data + CRC + stamp), and the minimum size is 2 bytes (2-byte data). Therefore, the maximum space is $16 \times 6 = 96$ bytes. The FIFO can only store data in frame units, regardless of the frame size. For example, if you store data in a 2-byte frame structure, only $16 \times 2 = 32$ bytes of space can be used. Although the maximum space is 96 bytes, the remaining 64 bytes cannot be utilized.

6.7.2 FIFO CONTROL

NMS4110 supports three modes for FIFO access.

- FIFO MODE: a new frame captured during FIFO full is discarded instead of storage
- STREAM MODE: a new frame captured during FIFO full is sustained and the oldest frame is discarded
- BYPASS MODE: only the latest single captured frame is kept in the FIFO

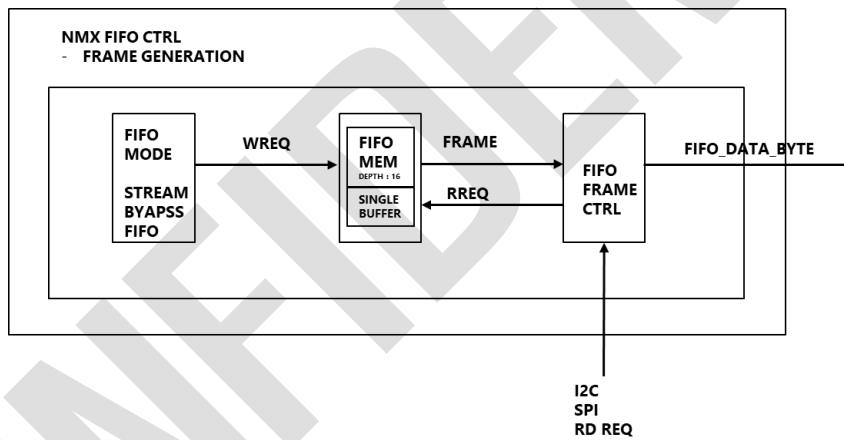


Figure 42 FIFO Block Diagram

6.7.3 FIFO Interrupt

FIFO interrupt is generated to indicate when FIFO is filled and meets certain conditions.

- **FIFO Interrupt Level** : Three types of interrupt levels are supported.
 - NEW_DATA: indicate that more than one frame is stored
 - HALF_FULL: indicate that more than the half of the number of maximum frames are stored (the number of maximum frames could be adjusted)
 - FULL: indicate that sixteen frames are stored

The number of frames to define a half level could be adjusted by register configuration.

FIFO_PTR_HALF_FULL adjusts the number of frames for FIFO_HALF_FULL. If configured as in the

following example, the FIFO_HALF_FULL interrupt is triggered only when 3 or more frames are stored in the FIFO.

Example: SEL_INT (0x3B[3:2]) = 0x1, FIFO_PTR_HALF_FULL(0x3A[5:2]) = 0x3

FIFO interrupt can be cleared using two methods described below.

- Using FIFO_CLEAR register(address 0x3A, first bit)
 - Set high to clear FIFO
 - Interrupt and all data stored in FIFO are cleared
- Reading out all data in FIFO
 - The status of FIFO can be checked using register at address 0x42
 - The interrupt status of FIFO can be checked using register at address 0x4A
 - If there are more than one frame data in FIFO, NEW_DATA bit in register at address 0x42 is set high
 - If there are sixteen frames data in FIFO, NEW_DATA and HALF_FULL bit in register at address 0x42 are set to high

6.7.4 FIFO Clear

The data captured in FIFO can be cleared by setting FIFO_CLEAR bit in register at address 0x40 to high. FIFO_CLEAR bit should be reset to low after clearing FIFO.

6.7.5 FIFO DATA FORMAT

The captured data, which is the output of Decimation Filter, can be stored in FIFO in various formats. Depending on the user's selection, the number of bytes in which the filter output is stored also varies. When reading data from the FIFO, these factors must be considered.

- FIFO_DATA_SIZE = 0x0 (DATA 2 BYTE)

FIFO_FORMAT = 0 : HEADER-DATA

STATUS HEADER				FIFO[7:0]								FIFO[7:0]											
FIFO DATA				FIFO 2 BYTE FORMAT																			
CH_NUM	0	0	0	0	DECIMATION FILTER DATA (signed)																		
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FIFO_FORMAT = 1 : HEADER-DATA-CRC

STATUS HEADER				FIFO[7:0]								FIFO[7:0]				FIFO[7:0]							
FIFO DATA				FIFO 2 BYTE FORMAT								CRC											
CH_NUM	0	0	0	0	DECIMATION FILTER DATA (signed)								CRC										
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FIFO_FORMAT = 2 : HEADER-DATA-STAMP

STATUS HEADER				FIFO[7:0]								FIFO[7:0]				FIFO[7:0]							
FIFO DATA				FIFO 2 BYTE FORMAT								STAMP											
CH_NUM	0	0	0	0	DECIMATION FILTER DATA (signed)								STAMP										
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FIFO_FORMAT = 4 : SET_MODE

FIFO[7:0]				FIFO[7:0]											
FIFO DATA				DECIMATIION FILTER DATA 16 bit (signed)											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 43 FIFO DATA 2BYTE FORMAT▪ **FIFO_DATA_SIZE = 0x1 (DATA 3 BYTE)****FIFO_FORMAT = 0 : HEADER-DATA**

STATUS HEADER				FIFO[7:0]								FIFO[7:0]				FIFO[7:0]															
FIFO DATA				FIFO 3 BYTE FORMAT																											
CH_NUM	0	0	0	0	DECIMATION FILTER OUTPUT DATA (signed)																										
7	6	5	4	3	2	1	0	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FIFO_FORMAT = 1 : HEADER-DATA-CRC

STATUS HEADER				FIFO[7:0]								FIFO[7:0]				FIFO[7:0]															
FIFO DATA				FIFO 3 BYTE FORMAT								CRC																			
CH_NUM	0	0	0	0	DECIMATION FILTER OUTPUT DATA (signed)								CRC																		
7	6	5	4	3	2	1	0	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FIFO_FORMAT = 2 : HEADER-DATA-STAMP

STATUS HEADER				FIFO[7:0]								FIFO[7:0]				FIFO[7:0]															
FIFO DATA				FIFO 3 BYTE FORMAT								STAMP																			
CH_NUM	0	0	0	0	DECIMATION FILTER OUTPUT DATA (signed)								STAMP																		
7	6	5	4	3	2	1	0	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

FIFO_FORMAT = 3 : HEADER-DATA-CRC-STAMP

STATUS HEADER				FIFO[7:0]								FIFO[7:0]				FIFO[7:0]															
FIFO DATA				FIFO 3 BYTE FORMAT								CRC				STAMP															
CH_NUM	0	0	0	0	DECIMATION FILTER OUTPUT DATA (signed)								CRC				STAMP														
7	6	5	4	3	2	1	0	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 44 FIFO DATA 3 BYTE FORMAT**6.7.6 FIFO CRC**

If secured data is needed, CRC coding can be used by setting FIFO_FORMAT register to 1 or 3. A single byte of CRC code follows the decimation output. CRC coding uses the polynomial of CRC-8-ATM

as shown below.

$$X^8 + X^2 + X + 1$$

6.7.7 FIFO SET-MODE

Example: OP_MODE = 0x0, OP_SEQ = 0x1

- OP_TEMP = 0x1, FIFO_TEMP_NULL_INSERT = 0x0



Figure 45 Continuous Conversion mode : OP_SEQ=0x1, OP_TEMP =0x1

- FIFO_FORMAT = 0x4
- FIFO_SET_CNT_SEQ = 0x0
- OP_TEMP =0x2, FIFO_TEMP_NULL_INSERT =0x0 : unallowed to use SET_MODE



Figure 46 Continuous Conversion mode : OP_SEQ=0x1, OP_TEMP =0x2

- In cycles without a TEMP Channel, a NULL value must be forcibly assigned to enable the use of FIFO SET MODE
- OP_TEMP =0x3, FIFO_TEMP_NULL_INSERT =0x1 : allowed to use SET_MODE
 - FIFO_FORMAT = 0x4
 - FIFO_SET_CNT_SEQ = 0x1
 - FIFO_TEMP_NULL_INSERT = 0x1

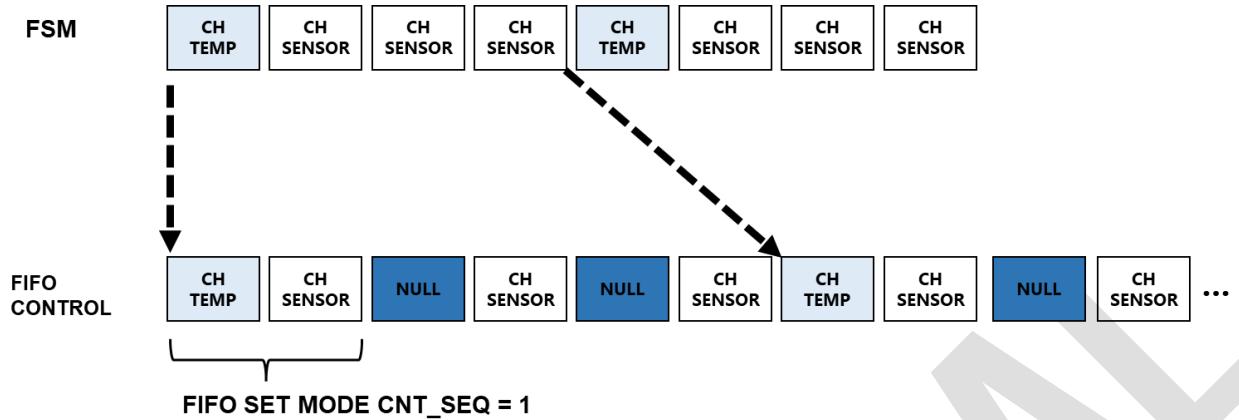


Figure 47 Continuous Conversion mode: OP_SEQ=0x1, OP_TEMP =0x3, TEMP_NULL_INSERT mode

- Example of FIFO SET MODE using the AVERAGE_FILTER

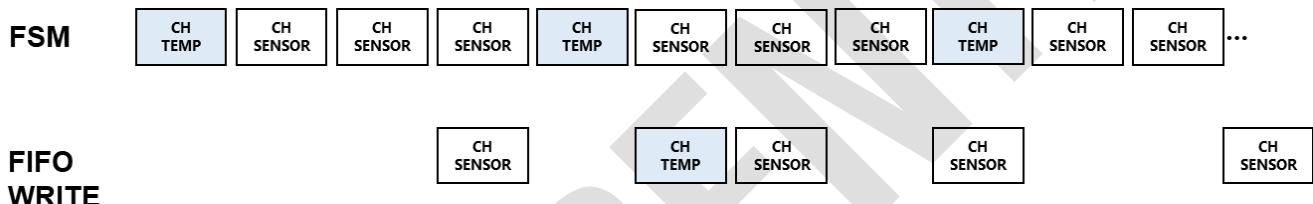


Figure 48 Continuous Conversion mode: OP_SEQ=0x1, OP_TEMP =0x3 Average Filter Mode

- OP_TEMP =0x3,
- FIFO_FORMAT = 0x4
- FIFO_TEMP_NULL_INSERT =0x0
- SENSOR_CH_AVG_CNT = 0x2
- TEMPS_CH_AVG_CNT = 0x2

In cases where the output Average of the filter is applied, the input to the FIFO may differ from the measurement sequence in the FSM due to the OP_TEMP condition. Considering such cases, NULL value insertion control should be based on the output information of the Average Filter rather than the parameters set in the FSM, and the SET_MODE configuration should take this into account.

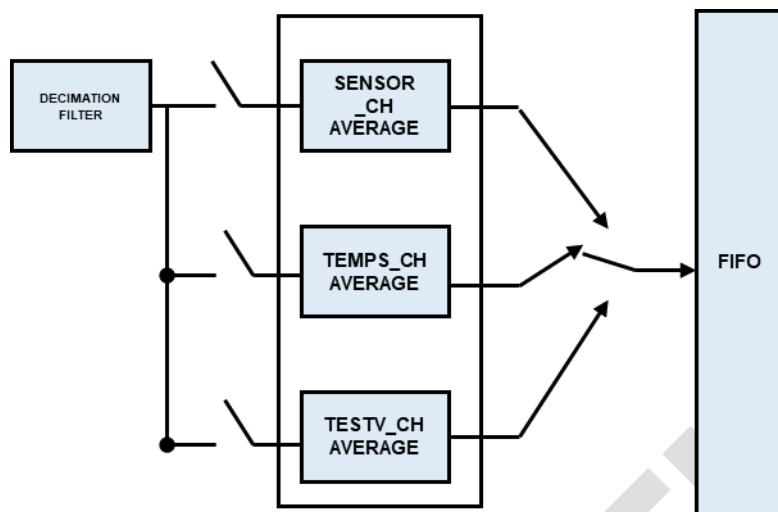


Figure 49 Average Filter Block Diagram

6.7.1 FIFO REGISTER

FIFO CONFIGURATION Register (ONM)

Address	7	6	5	4	3	2	1	0	reset				
0x39	FIFO_SET_CNT_SEQ[2:0]			FIFO_FORMAT[2:0]			FIFO_MODE[1:0]		0x00				
	RW			RW			RW						
Bit	Field			Type	Reset	Description							
7:5	FIFO_SET_CNT_SEQ[2:0]			R/W	0x00	FIFO set mode sequence number n-1 → n sequence							
4:2	FIFO_FORMAT[2:0]			R/W	0x00	0x0 : HEADER – DATA 0x1 : HEADER – DATA-CRC 0x2 : HEADER – DATA-STAMP 0x3 : HEADER – DATA-CRC-STAMP 0x4 : SET MODE (DATA 16bit)							
1:0	FIFO_MODE[1:0]			R/W	0x00	FIFO mode : 0x0:FIFO 0x1:STREAM Others : BYPASS							

FIFO SETTING Register (ONM)

Address	7	6	5	4	3	2	1	0	reset	
0x3A	-	-	FIFO_PTR_HALF_FULL[3:0]			FIFO_CLEAR		FIFO_DATA_SIZE		0x1C
	-	-	RW			RW		RW		
Bit	Field			Type	Reset	Description				
5:2	FIFO_PTR_HALF_FULL[3:0]			RW	0x07	FIFO half full interrupt pointer : 1 ~ 7				
1	FIFO_CLEAR			RW	0x00	[1] FIFO clear				

0	FIFO_DATA_SIZE	RW	0x00	[0] FILTER DATA 2BYTE [1] FILTER DATA 3 BYTE
---	----------------	----	------	--

FIFO STATUS Register (ONR)

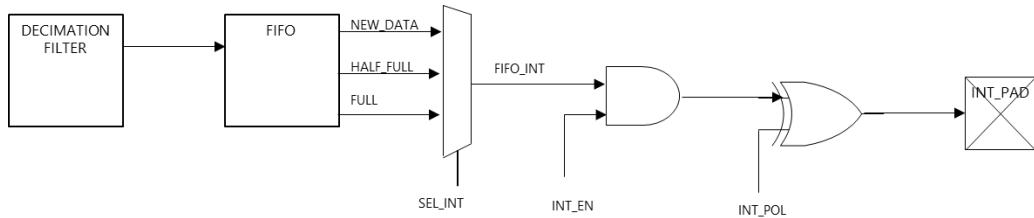
Address	7	6	5	4	3	2	1	0	reset	
0x42	-	-	-	-	-	FIFO_NEW_DATA	FIFO_HALF_FULL	FIFO_FULL	0x00	
	-	-	-	-	-	RO	RO	RO		
Bit	Field			Type		Reset	Description			
2	FIFO_NEW_DATA			RO		0x00	FIFO new data status			
1	FIFO_HALF_FULL			RO		0x00	FIFO half full status			
0	FIFO_FULL			RO		0x00	FIFO full status			

FIFO TEST MODE Register (ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x43	-	-	-	-	-	FIFO_TEMP_NULL_INSERT	FIFO_TEST_WR	FIFO_TEST_MODE	0x00	
	-	-	-	-	-	RW	AC	RW		
Bit	Field			Type	Reset	Description				
2	FIFO_TEMP_NULL_INSERT			R/W	0x00	channel 2 (TEMPERATURE CHANNEL) NULL INSERTION IN SET_MODE [0] Disable [1] enable				
1	FIFO_TEST_WR			AC	0x00	FIFO test frame write (auto Clear)				
0	FIFO_TEST_MODE			R/W	0x00	[0] NORMAL Only "1" is allowed				

FIFO_READ Register (ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x5F	FIFO_DATA[7:0]								0x00	
	RO									
Bit	Field			Type	Reset	Description				
7:0	FIFO_DATA[7:0]			RO	0x00	FIFO Read Data				

**Figure 50 FIFO Interrupt Configuration**

FIFO status signal is used as an interrupt flag. FIFO has a frame depth of 16. When 8 or more frame data are stored, a half_full interrupt is triggered, and when all 16 frames are stored, a full interrupt occurs.

6.8 CLOCK & RESET

NMS4110 provides clock source force registers that allow the clock sources to continue generating clocks regardless of the system state. These clock source forces influence the power or clock gating provided in the system. Normally, all clock source generation is automatically and internally controlled. It is not recommended to use these clock source force control registers except for testing or debugging.

CLOCK SOURCE CONTROL0 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset
0x00	CLK_FE_CSR4	CLK_FE_CSR3	CLK_FE_CSR2	CLK_FE_CSR1	CLK_FE_CAL	CLK_FE_ANA	CLK_FE_DEC2	CLK_FE_DEC1	0x00
	RW	RW	RW	RW	RW	RW	RW	RW	
Address	7	6	5	4	3	2	1	0	reset
0x01	CLK_FE_MTP	CLK_FE_FIFO2	CLK_FE_FIFO1	CLK_FE_SPI2	CLK_FE_SPI1	CLK_FE_I2C2	CLK_FE_I2C1	CLK_FE_BOOT	0x00
	RW	RW	RW	RW	RW	RW	RW	RW	
Bit	Field		Type	Reset	Description				
7	CLK_FE_CSR4		R/W	0x00	CSR4 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable				
6	CLK_FE_CSR3		R/W	0x00	CSR3 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable				
5	CLK_FE_CSR2		R/W	0x00	CSR2 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable				
4	CLK_FE_CSR1		R/W	0x00	CSR1 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable				
3	CLK_FE_CAL		R/W	0x00	digital post processing clock source force on/off control bit 0: clock source force disable 1: clock source force enable				
2	CLK_FE_ANA		R/W	0x00	Analog block clock source force on/off control bit 0: clock source force disable 1: clock source force enable				

1	CLK_FE_DEC2	R/W	0x00	decimation filter clock source force on/off control bit 0: clock source force disable 1: clock source force enable
0	CLK_FE_DEC1	R/W	0x00	decimation filter clock source force on/off control bit 0: clock source force disable 1: clock source force enable

CLOCK SOURCE CONTROL1 Register (AOM)

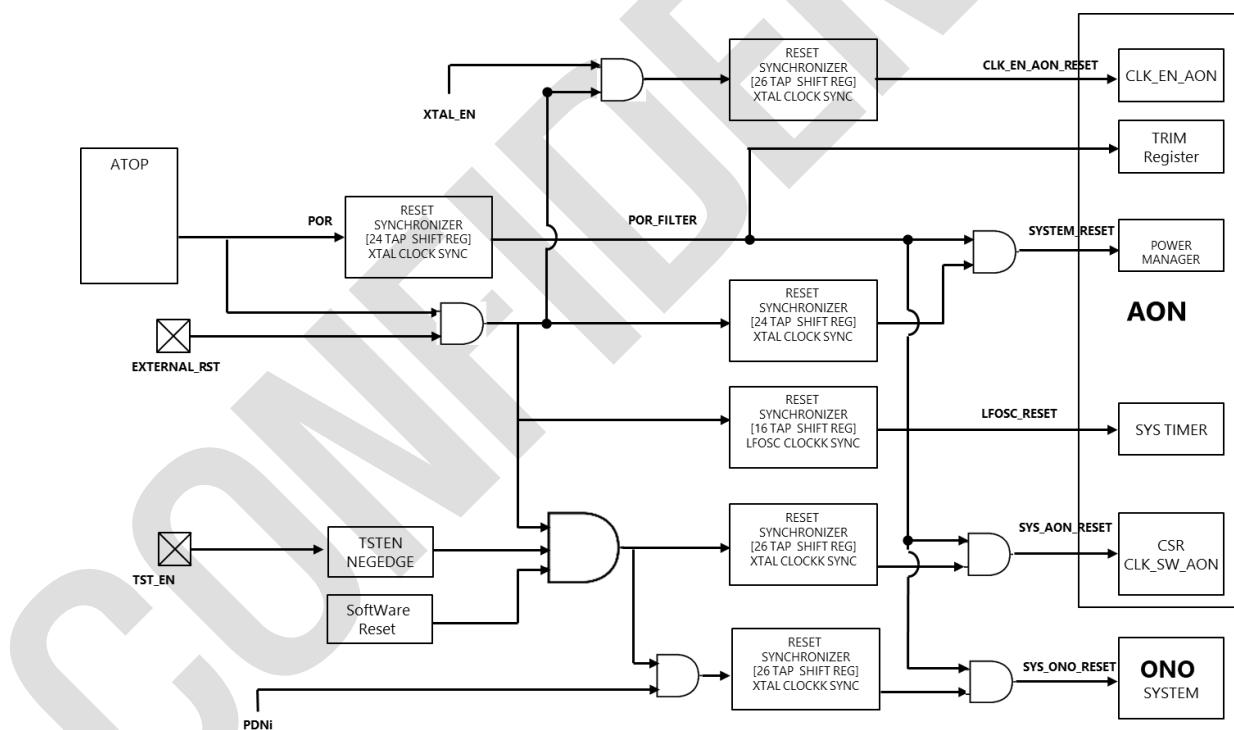
Address	7	6	5	4	3	2	1	0	reset	
0x01	CLK_FE_MTP	CLK_FE_FIFO2	CLK_FE_FIFO1	CLK_FE_SPI2	CLK_FE_SPI1	CLK_FE_I2C2	CLK_FE_I2C1	CLK_FE_BOOT	0x00	
	RW	RW	RW	RW	RW	RW	RW	RW		
Bit	Field	Type	Reset	Description						
7	CLK_FE_MTP	R/W	0x00	MTP Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable						
6	CLK_FE_FIFO2	R/W	0x00	FIFO2 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable						
5	CLK_FE_FIFO1	R/W	0x00	FIFO1 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable						
4	CLK_FE_SPI2	R/W	0x00	SPI2 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable						
3	CLK_FE_SPI1	R/W	0x00	SPI1 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable						
2	CLK_FE_I2C2	R/W	0x00	I2C2 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable						
1	CLK_FE_I2C1	R/W	0x00	I2C1 Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable						
0	CLK_FE_BOOT	R/W	0x00	BOOT Manager Block clock source force on/off control bit 0: clock source force disable 1: clock source force enable						

CLOCK SOURCE CONTROL2 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0x60	-	-	-	-	-	-	CLK_FE_RST	CLK_FE_AON	0x00	
	-	-	-	-	-	-	RW	RW		
Bit	Field	Type	Reset	Description						
1	CLK_FE_RST	R/W	0x00	RESET MANAGER clock source force on/off control bit 0: clock source force disable 1: clock source force enable						
0	CLK_FE_AON	R/W	0x00	AON DOMAIN clock source force on/off control bit 0: clock source force disable 1: clock source force enable						

ANALOG CLOCK DIVISION RATIO Register (AOM)

Address	7	6	5	4	3	2	1	0	reset																		
	-	-	-	-	-	CLK_DIV_ANA[2:0]			0x01																		
0x02	-	-	-	-	-	RW																					
Bit	Field	Type	Reset	Description																							
2:0	CLK_DIV_ANA[2:0]	R/W	0x01	the division ratio for Analog Clock Source from Main Clock <table border="1"> <tr> <th>Value</th><th>ANALOG CLOCK (CLK_ANA) Output Frequency</th></tr> <tr> <td>0</td><td>16MHz</td></tr> <tr> <td>1</td><td>8MHz</td></tr> <tr> <td>2</td><td>4MHz</td></tr> <tr> <td>3</td><td>2MHz</td></tr> <tr> <td>4</td><td>1MHz</td></tr> <tr> <td>5</td><td>500KHz</td></tr> <tr> <td>6</td><td>250KHz</td></tr> <tr> <td>7</td><td>125KHz</td></tr> </table>						Value	ANALOG CLOCK (CLK_ANA) Output Frequency	0	16MHz	1	8MHz	2	4MHz	3	2MHz	4	1MHz	5	500KHz	6	250KHz	7	125KHz
Value	ANALOG CLOCK (CLK_ANA) Output Frequency																										
0	16MHz																										
1	8MHz																										
2	4MHz																										
3	2MHz																										
4	1MHz																										
5	500KHz																										
6	250KHz																										
7	125KHz																										


Figure 51 Reset Manager Block Diagram
SOFTWARE RESET Register (ONR)

Address	7	6	5	4	3	2	1	0	reset
0x3C	SW_RST[7:0]								0x00

					RW		
Bit	Field	Type	Reset	Description			
7:0	SW_RST[7:0]	R/W	0x00	0xA5 : software reset code To execute the software reset command, users must set the CLK_FE_RST register value as 0x1			

6.9 INTERRUPT

The Interrupt block collects interrupts generated from each block, outputs them through the pad, and displays their status.

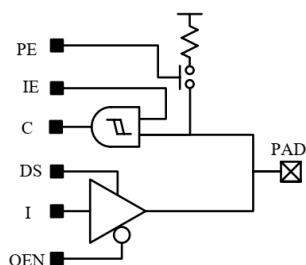
INTERRUPT CONTROL Register (ONR)

Address	7	6	5	4	3	2	1	0	reset		
0x3B	-	TEST_POWER_EN	FAST_EP_EN	E32B_EN	SEL_INT[1:0]	INT_EN	INT_POL	0x00			
	-	RW	RW	RW	RW	RW	RW				
Bit	Field		Type	Reset	Description						
6	TEST_POWER_EN		R/W	0x00	MTP Power Test Enable						
5	FAST_EP_EN		R/W	0x00	MTP Memory Fast Erase & Program Enable						
4	E32B_EN		R/W	0x00	MTP Memory Erase 32 Bit Enable						
3:2	SEL_INT[1:0]		R/W	0x00	FIFO interrupt type selection 0x0: new data (An interrupt occurs after one frame is stored) 0x1: half full (An interrupt occurs after 8 frames are stored.) 0x2: full (An interrupt occurs after 16 frames are stored.)						
1	INT_EN		R/W	0x00	FIFO Interrupt Enable 0x0: disable 0x1: enable						
0	INT_POL		R/W	0x00	Interrupt Polarity Select 0x0: active high, 0x1: active low						

INTERRUPT STATUS Register (ONR)

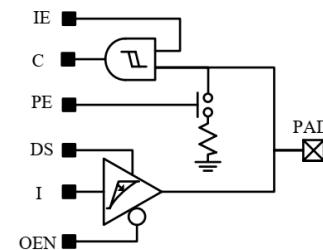
Address	7	6	5	4	3	2	1	0	reset			
0x4A	STATUS[6:0]						INT	0x00				
	RO_RF											
Bit	Field		Type	Reset	Description							
7:1	STATUS[6:0]		RO_RF	0x00	STATUS[0] : FIFO new data interrupt indication STATUS[1] : FIFO half full interrupt indication STATUS[2] : FIFO full interrupt indication STATUS[3] : boot done interrupt indication STATUS[4] : ISP done interrupt indication STATUS[5] : program error interrupt indication STATUS[6] : boot watchdog-timer out interrupt indication							
0	INT		RO	0x00	Interrupt indication							

6.10 GPIO



Truth Table

INPUT						OUTPUT	
DS	OEN	I	PAD	PE	IE	PAD	C
0/1	0	0	-	0/1	0	0	0
0/1	0	0	-	0/1	1	0	0
0/1	0	1	-	0/1	0	1	0
0/1	0	1	-	0/1	1	1	1
0/1	1	0/1	0	0/1	0	-	0
0/1	1	0/1	0	0/1	1	-	0
0/1	1	0/1	1	0/1	0	-	0
0/1	1	0/1	1	0/1	1	-	1
0/1	1	0/1	Z	0	0	-	0
0/1	1	0/1	Z	0	1	-	X
0/1	1	0/1	Z	1	0	H	0
0/1	1	0/1	Z	1	1	H	H



Truth Table

INPUT						OUTPUT	
DS	OEN	I	PAD	PE	IE	PAD	C
0/1	0	0	-	0/1	0	0	0
0/1	0	0	-	0/1	1	0	0
0/1	0	1	-	0/1	0	1	0
0/1	0	1	-	0/1	1	1	1
0/1	1	0/1	0	0/1	0	-	0
0/1	1	0/1	0	0/1	1	-	0
0/1	1	0/1	1	0/1	0	-	0
0/1	1	0/1	1	0/1	1	-	1
0/1	1	0/1	Z	0	0	-	0
0/1	1	0/1	Z	0	1	-	X
0/1	1	0/1	Z	1	0	L	0
0/1	1	0/1	Z	1	1	L	L

Figure 52 PULL-UP GPIO

Figure 53 PULL-DOWN GPIO

INT/RESET PAD Control Register (ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x4B	-	-	-	-	-	INT_OEN	INT_DS	RESET_PE	0x00	
	-	-	-	-	-	RW	RW	RW		
Bit	Field			Type	Reset		Description			
2	INT_OEN			R/W	0x00		Interrupt pad output enable negated			
1	INT_DS			R/W	0x00		Interrupt pad driving strength			
0	RESET_PE			R/W	0x00		Reset pad pull-up enable			

SDA PAD Control Register (ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x4C	-	-	-	SDA_IE	SDA_PE	SDA_OEN	SDA_I	SDA_DS	0x14	
	-	-	-	RW	RW	RW	RW	RW		
Bit	Field			Type	Reset		Description			
4	SDA_IE			R/W	0x01		SDA pad input enable			
3	SDA_PE			R/W	0x00		SDA pad pull-up enable			
2	SDA_OEN			R/W	0x01		SDA pad output enable negated			

1	SDA_I	R/W	0x00	SDA pad output value
0	SDA_DS	R/W	0x00	SDA pad driving strength

SCL PAD Control Register (ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x4D	-	-	-	SCL_IE	SCL_PE	SCL_OEN	SCL_I	SCL_DS	0x14	
	-	-	-	RW	RW	RW	RW	RW		
Bit	Field		Type		Reset		Description			
4	SCL_IE		R/W		0x01		SCL pad input enable			
3	SCL_PE		R/W		0x00		SCL pad pull-up enable			
2	SCL_OEN		R/W		0x01		SCL pad output enable negated			
1	SCL_I		R/W		0x00		SCL pad output value			
0	SCL_DS		R/W		0x00		SCL pad driving strength			

CSN PAD Control Register (ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x4E	-	-	-	CSN_IE	CSN_PE	CSN_OEN	CSN_I	CSN_DS	0x14	
	-	-	-	RW	RW	RW	RW	RW		
Bit	Field		Type		Reset		Description			
4	CSN_IE		R/W		0x01		CSN pad input enable			
3	CSN_PE		R/W		0x00		CSN pad pull-up enable			
2	CSN_OEN		R/W		0x01		CSN pad output enable negated			
1	CSN_I		R/W		0x00		CSN pad output value			
0	CSN_DS		R/W		0x00		CSN pad driving strength			

MOSI PAD Control Register (ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x4F	-	-	-	MOSI_IE	MOSI_PE	MOSI_OEN	MOSI_I	MOSI_DS	0x14	
	-	-	-	RW	RW	RW	RW	RW		
Bit	Field		Type		Reset		Description			
4	MOSI_IE		R/W		0x01		MOSI pad input enable			
3	MOSI_PE		R/W		0x00		MOSI pad pull-down enable			
2	MOSI_OEN		R/W		0x01		MOSI pad output enable negated			
1	MOSI_I		R/W		0x00		MOSI pad output value			
0	MOSI_DS		R/W		0x00		MOSI pad driving strength			

DTEST0 PAD Control Register (ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x50	-	-	-	DTEST0_IE	DTEST0_PE	DTEST0_OEN	DTEST0_I	DTEST0_DS	0x14	
	-	-	-	RW	RW	RW	RW	RW		
Bit	Field		Type	Reset		Description				
4	DTEST0_IE		R/W	0x01		DTEST0 pad input enable				
3	DTEST0_PE		R/W	0x00		DTEST0 pad pull-down enable				
2	DTEST0_OEN		R/W	0x01		DTEST0 pad output enable negated				
1	DTEST0_I		R/W	0x00		DTEST0 pad output value				
0	DTEST0_DS		R/W	0x00		DTEST0 pad driving strength				

6.11 ISP INTERFACE

NMS4110 includes 128 bytes of MTP memory, configured as 16-bit x 64. This memory is used to store values that are set before booting, with some CSR (AOM, ONM) registers allocated (refer to the memory map). The memory can be accessed for erase, program, and read operations through the ISP (In System Programming) feature.

To activate the ISP interface and enter memory programming mode, a specific sequence of signals must be input to the chip. This sequence involves setting the chip's TST_EN pin to high, DTEST0 (TST_CMD) pin to low, performing a reset, and then waiting for at least 52 cycles of the main clock.

ISP interface operates by requesting commands and receiving acknowledgments. Values needed for commands and requests are written to registers, and acknowledgments are confirmed by reading register values. The following registers are used for this operation: ISP_RDATA (address 0x54, 0x55), ISP_WDATA (address 0x56, 0x57), ISP_ADDR (address 0x58), ISP_CMD (address 0x59), ISP_STATUS (address 0x5A), ISP_REQ (address 0x5B), and ISP_ERR_CNT (address 0x5C).

6.11.1 Command for ISP

The commands that can be written to the ISP_CMD register for ISP operation are as follows.

- 0x00: ENABLE_IP: enable MTP
- 0x01: DISABLE_IP: disable MTP
- 0x02: WORD_ERASE: erase a single word
- 0x03: WORD_PROG: program a single word
- 0x04: WORD_READ: read a single word
- 0x05: WORD_COMPARE: compare a single word

6.11.2 ISP Operation Sequence

ISP interface operates in the sequence of command request, command execution, and command acknowledgment.

- **Command request**
 - Write command code in ISP_CMD register
 - Write MTP address and data related with command
- **Command execution**
 - Set ISP_REQ bit high for executing ISP command (ISP_REQ bit is automatically cleared to low)
- **Command acknowledges**
 - Check ISP_STATUS bit by polling to determine if the command is completed (ISP_STATUS bit is automatically cleared to low when it is read)
 - Check ISP_RDATA or ISP_ERR_CNT depending on the command

6.11.3 ISP Interface Commands

The following are several commands used to control the operation of MTP via the ISP interface:

- **ENABLE_IP**

ENABLE_IP command is required to activate MTP, and it must be executed before any other command can function. This command can be used following the sequence outlined below:

- Write 0x00 in ISP_CMD register
- Write 0x01 in ISP_REQ register

ISP Command Register (ISP_CMD)

Address	7	6	5	4	3	2	1	0	reset				
0x59	-	-	-	-	-	ISP_CMD[2:0]							
	-	-	-	-	-	RW							
Bit	Field		Type	Reset	Description								
2:0	ISP_CMD[2:0]		R/W	0x00	0: EN_IP, 1: DISABLE_IP, 2: WORD_ERASE, 3: WORD_PROG, 4: WORD_READ, 5: WORD_COMPARE								

ISP Command Run Request Register (ISP_REQ)

Address	7	6	5	4	3	2	1	0	reset
0x5B	-	-	-	-	-	-	-	ISP_REQ	
	-	-	-	-	-	-	-	AC	
Bit	Field		Type	Reset	Description				

0	ISP_REQ	AC	0x00	ISP Command Start Request
---	---------	----	------	---------------------------

▪ **DISABLE_IP**

The DISABLE_IP command is necessary to deactivate the MTP and reset all associated control signals. It should be executed according to the following sequence:

- Write 0x01 in ISP_CMD register
- Write 0x01 in ISP_REQ register

▪ **WORD_ERASE**

The WORD_ERASE command is utilized to erase a specific word in the MTP, selected by its address. The execution sequence is outlined below:

- Write 0x02 in ISP_CMD register
- Write the destination address in ISP_ADDR register
- Write 0x01 in ISP_REQ register
- Confirm ISP_STATUS register is high by reading it after 3.2 msec

ISP Status Register (ISP_STATUS)

Address	7	6	5	4	3	2	1	0	reset	
0x5A	-	-	-	-	-	-	-	ISP_STATUS	0x00	
	-	-	-	-	-	-	-	RO_RF		
Bit		Field		Type		Reset		Description		
0		ISP_STATUS		RO_RF		0x00		ISP Command Done		

▪ **WORD_PROG**

The WORD_PROG command is utilized to program a specific word in the MTP, selected by its address. The execution sequence is outlined below:

- Write 0x03 in ISP_CMD register
- Write the destination address in ISP_ADDR register
- Write the data to be programmed into MTP in ISP_WDATA0 and ISP_WDATA1 registers
- Write 0x01 in ISP_REQ register
- Confirm ISP_STATUS register is high by reading it after 3.2 msec

ISP Write Data 0 Register (ISP_WDATA0)

Address	7	6	5	4	3	2	1	0	reset	
0x56	ISP_WDATA0[7:0]								0x00	
	RW									
Bit		Field		Type		Reset		Description		
7:0		ISP_WDATA0[7:0]		RW		0x00		Memory Write Data(LSB, even address)		

ISP Write Data 1 Register (ISP_WDATA1)

Address	7	6	5	4	3	2	1	0	reset
0x57	ISP_WDATA1[7:0]								0x00
Bit	Field								Type
7:0	ISP_WDATA1[7:0]								RW
Bit	Field								Reset
7:0	ISP_WDATA1[7:0]								0x00
Bit	Field								Description
7:0	ISP_WDATA1[7:0]								Memory Write Data(MSB, odd address)

ISP Address Register (ISP_ADDR)

Address	7	6	5	4	3	2	1	0	reset
0x58	ISP_ADDR[7:0]								0x00
Bit	Field								Type
7:0	ISP_ADDR[7:0]								RW
Bit	Field								Reset
7:0	ISP_ADDR[7:0]								0x00
Bit	Field								Description
7:0	ISP_ADDR[7:0]								Access Memory Address

- **WORD_READ**

The WORD_READ command is utilized to read out a specific word in the MTP, selected by its address. The execution sequence is outlined below:

- Write 0x04 in ISP_CMD register
- Write the destination address in ISP_ADDR register
- Write 0x01 in ISP_REQ register
- Confirm ISP_STATUS register is high by reading it after 6.3 usec
- Read out ISP_RDATA0 and ISP_RDATA1 register

ISP Read Data 0 Register (ISP_RDATA0)

Address	7	6	5	4	3	2	1	0	reset
0x54	ISP_RDATA0[7:0]								0x00
Bit	Field								Type
7:0	ISP_RDATA0[7:0]								RO
Bit	Field								Reset
7:0	ISP_RDATA0[7:0]								0x00
Bit	Field								Description
7:0	ISP_RDATA0[7:0]								Memory Read Data(LSB, even address)

ISP Read Data 1 Register (ISP_RDATA1)

Address	7	6	5	4	3	2	1	0	reset
0x55	ISP_RDATA1[7:0]								0x00
Bit	Field								Type
7:0	ISP_RDATA1[7:0]								RO
Bit	Field								Reset
7:0	ISP_RDATA1[7:0]								0x00
Bit	Field								Description
7:0	ISP_RDATA1[7:0]								Memory Read Data(MSB, odd address)

▪ WORD_COMPARE

The WORD_COMPARE command is utilized to compare a specific word in the MTP, selected by its address, with a reference. The execution sequence is outlined below:

- Write 0x05 in ISP_CMD register
- Write the destination address in ISP_ADDR register
- Write the reference to be compared in ISP_WDATA0 and ISP_WDATA1 register
- Write 0x01 in ISP_REQ register
- Confirm ISP_STATUS register is high by reading it after 6.3 usec
- Check ISP_ERR_CNT register to check mismatch

ISP Error Counter Register (ISP_ERR_CNT)

Address	7	6	5	4	3	2	1	0	reset	
0x5C	ISP_ERR_CNT[7:0]								0x00	
	RO									
Bit	Field		Type	Reset		Description				
7:0	ISP_ERR_CNT[7:0]		RO	0x00		ISP compare error count				

6.11.4 ISP Check Pattern

The NMS4110 uses the memory address 0x3F as a designated area to verify if the user has programmed it. During boot, the specific pattern 0xFFA1 must be written to this location for the system to proceed with reading values from memory.

7

OPERATION CONFIGURATION

7.1 TARGET(NMS4110) INTERFACE

The NMS4110 can configure the interface using the CSN, MOSI, SDA, SCL, DTEST0, INT, RESET, WAKEUP, and TSTEN pins. Refer to the Pin Description for the location of these pins.

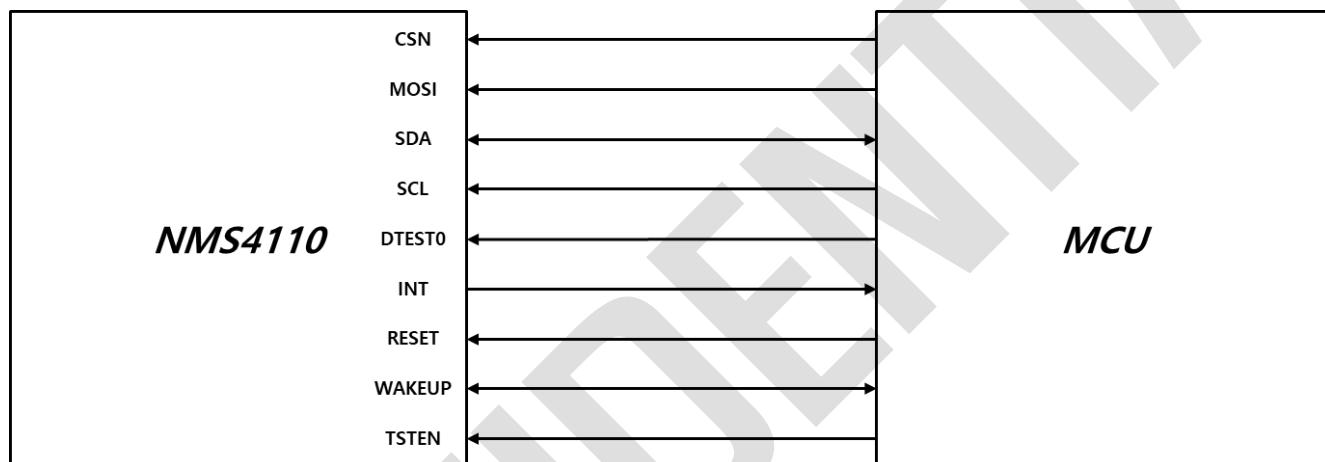


Table 19 TARGET INTERFACE Pin Map

PIN NAME	I2C	SPI	ISP	POWER MODE	INTERRUPT	RESET	Description
CSN		CSN					SPI : enable
MOSI		MOSI					SPI : data input
SDA	SDA	MISO					SPI : data out I2C : serial data
SCL	SCL	SCLK					SPI : clock I2C : clock
DTEST0			DTEST0				ISP : Test mode entry
INT					INTERRUPT		INT : Output Interrupt signal
RESET						RESET	Hardware reset
WAKEUP				WAKEUP			PM : WAKEUP signal inout

TSTEN			TEST Enable				ISP : Test mode entry
Reference	I2C	SPI	ISP INTERFACE	POWER MANAGEMENT	INTERRUPT FIFO Interrupt	Reset	

7.2 DAC SETUP

NMS4110 includes DAC1, DAC2, and DAC3. DAC1 and DAC2 have an LSB of 25mV and are used for internal reference voltage settings, while DAC3 has an LSB of 390.63μV and is intended for driving external circuits.

DAC3 can be set using the following pseudo code

PSEUDO CODE VARIABLE : SET_DAC3_BIAS_VOLTAGE

VARIABLE	REGISTER	Description
voltage		Input voltage value

SET_DAC3_BIAS_VOLTAGE : START

```

void SET_DAC3_BIAS_VOLTAGE (double voltage)           // voltage unit : mV input range -800 ~ +800mV
{
    double DAC3_1LSB = 1600.0/4096.0 ;               // reference 0.9V
    double V ;
    integer dac_code ;
    byte   dac_lsb  ;
    byte   dac_msb  ;

    if ( voltage < 800 )  V = voltage ;
    else                  V = 799.9 ;      // voltage limit
    endif

    dac_code = int ((V + 800)/DAC3_1LSB );
    dac_lsb = dac_code & 0xFF ;
    dac_msb = (dac_code >> 8) & 0x0F ;

    WRITE_REGISTER (0xCE, dac_lsb) ;      // register DAC3_VBIAS[7:0]
    WRITE_REGISTER (0xCF, dac_msb) ;      // register DAC3_VBIAS[11:8]
}
SET_DAC3_BIAS_VOLTAGE : END

```

DAC3 CONTROL1 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset
0xCE	DAC3_VBIAS[7:0]								0x00
	RW								
Bit	Field								Type
7:0	DAC3_VBIAS[7:0]								R/W
	0x00								DAC3 output data (VBIAS), 12-bit control

DAC3 CONTROL2 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset				
0xCF	-	-	-	-	DAC3_VBIAS[11:8]								0x00
	-	-	-	-	RW								
Bit	Field								Type				
3:0	DAC3_VBIAS[11:8]								R/W				
	0x00								DAC3 output data (VBIAS), 12-bit control				

7.3 ADC SETUP

To operate the ADC, the following registers must be enabled:

- ENB_ACTRL
- ENB_BIAS_GLOBAL
- ENB_DSM
- ENB_MUXBUF

These registers need to be enabled to ensure the proper functioning of the DSM.

After that, operations can be performed using the registers listed below

- CLK_DIV_ANA[2:0]
- SENSOR_CH_OSRA[7:0]
- SENSOR_CH_OSRA[10:8]
- SENSOR_CH_TRNC[4:0]
- TEMPS_CH_OSRA[7:0]
- TEMPS_CH_OSRA[10:8]
- TEMPS_CH_TRNC[4:0]
- TESTV_CH_OSRA[7:0]
- TESTV_CH_OSRA[10:8]
- TESTV_CH_TRNC[4:0]

ADC can be set using the following pseudo code

PSEUDO CODE VARIABLE : SET_CH(OSR)

VARIABLE	REGISTER	Description
OSR	*CH_OSR Register	Filter OSR Value
channel		Select channel variable

SET_CH_OSR : START

```
define SENSOR_CH 1
define TEMPS_CH 2
define TESTV_CH 3

void SET_CH_OSR (integer OSR, byte channel )
{
    byte rdata ;
    byte wdata ;
    byte OSR_LSB ;
    byte OSR_MSB ;
    OSR_LSB = OSR & 0xFF ;
    OSR_MSB = (OSR >> 8) & 0x07 ;

    Switch(channel)
    {
        case SENSOR_CH :
            rdata = 오류! 참조 원본을 찾을 수 없습니다. (0x0F) & 0xF8;
            wdata = rdata | OSR_MSB;
            오류! 참조 원본을 찾을 수 없습니다. (0x0E, OSR_LSB);
            오류! 참조 원본을 찾을 수 없습니다. (0x0F, wdata);

        case TEMPS_CH :
            rdata = 오류! 참조 원본을 찾을 수 없습니다. (0x11) & 0xF8;
            wdata = rdata | OSR_MSB;
            오류! 참조 원본을 찾을 수 없습니다. (0x10, OSR_LSB);
            write_register (0x11, wdata);

        case TESTV_CH :
            rdata = 오류! 참조 원본을 찾을 수 없습니다. (0x13) & 0xF8;
```

```
wdata = rdata | OSR_MSB;  
오류! 참조 원본을 찾을 수 없습니다. (0x12, OSR_LSB);  
오류! 참조 원본을 찾을 수 없습니다. (0x13, wdata);  
}  
}  
SET_CH_OSRA : END
```

PSEUDO CODE VARIABLE : SET_AVG_FILTER

VARIABLE	REGISTER	Description
AVGSMPL	*CH_AVG Register	Average filter CNT, TRNC Value
channel		Select channel variable

```
SET_AVG_FILTER : START  
define SENSOR_CH 1  
define TEMPS_CH 2  
define TESTV_CH 3  
void SET_AVG_FILTER ( byte channel , byte AVGSMPL)  
{  
    byte wdata ;  
    switch (AVGSMPL)  
    {  
        case 1 : wdata = 0x00 ;  
        case 2 : wdata = 0x11 ;  
        case 4 : wdata = 0x32 ;  
        case 8 : wdata = 0x73 ;  
        case 16 : wdata = 0xF4 ;  
    }  
    switch (channel )  
    {  
        case SENSOR_CH : 오류! 참조 원본을 찾을 수 없습니다. (0x15, wdata );  
        case TEMPS_CH : 오류! 참조 원본을 찾을 수 없습니다. (0x16, wdata ) ;  
        case TESTV_CH : 오류! 참조 원본을 찾을 수 없습니다. (0x17, wdata ) ;  
    }  
}  
SET_AVG_FILTER : END
```

NMS4110 supports a wide range of ADC output data rates (ODR), adjustable by configuring CLK_ANA_DIV[2:0], SET_FOS_CLKN[7:0], OSR[10:0], and AVGSMPL. The recommended ODR spans from 48.8 SPS to 100k SPS, depending on the specific settings. The sampling rate and conversion rate can be expressed as equation below:

$$F_{CLK_ANA} = F_S * \left(\frac{1}{2^{CLK_ANA_DIV}} \right)$$

$$F_{EOC} = \frac{F_{CLK_ANA}}{2 * SET_FOS_CLKN}$$

$$ODR = \frac{F_{EOC}}{OSR * AVG_{SMPL}}$$

ODR can be set using the following pseudo code

PSEUDO CODE VARIABLE : SET_AVG_FILTER		
VARIABLE	REGISTER	Description
OSR	*CH_OSR Register	Filter OSR value
ODR		Return Variable

```

GET_ODR_FROM_OSР : START
double GET_ODR_FROM_OSР (integer OSР )
{
    double ODR ;
    double TEOC ;
    TEOC = GET_TIME_ADC_EOC_PERIOD () ; // UINT : ms
    ODR = 1000/(TEOC * OSР * AVGsmpl ) ;
    return ODR ; // UNIT Hz
}
GET_ODR_FROM_OSР : END

```

PSEUDO CODE VARIABLE : SET_AVG_FILTER		
VARIABLE	REGISTER	Description
TEOC		Return variable

```

GET_TIME_ADC_EOC_PERIOD : START
double GET_TIME_ADC_EOC_PERIOD ( ) // TEOC Unit msec
{
    double TCLK_ANA;

```

```

double TEOC;
byte CLK_DIV_ANA ;           //register

CLK_DIV_ANA = 오류! 참조 원본을 찾을 수 없습니다. (0x02) & 0x0F ;

SET_FOS_CLKN = 오류! 참조 원본을 찾을 수 없습니다. (0x86) ;

TCLK_ANA = 62.5*pow (2, CLK_DIV_ANA) ;           // TCLK_ANA unit ns 62.5*2 = 125ns
TEOC = TCLK_ANA *10;                            // TEOC = 125ns*10 = 1.25us
TEOC = TEOC /1000000 ;                          // unit conversion : ms   TEOC = 0.00125 ms

return TEOC ;
}

GET_TIME_ADC_EOC_PERIOD : END

```

ANALOG CLOCK DIVISION RATIO Register (AOM)

Address	7	6	5	4	3	2	1	0	reset																		
0x02	-	-	-	-	-	CLK_DIV_ANA[2:0]																					
	-	-	-	-	-	RW																					
Bit	Field		Type	Reset	Description																						
2:0	CLK_DIV_ANA[2:0]		R/W	0x01	the division ratio for Analog Clock Source from Main Clock <table border="1"> <tr> <th>Value</th><th>ANALOG CLOCK (CLK_ANA) Output Frequency</th></tr> <tr> <td>0</td><td>16MHz</td></tr> <tr> <td>1</td><td>8MHz</td></tr> <tr> <td>2</td><td>4MHz</td></tr> <tr> <td>3</td><td>2MHz</td></tr> <tr> <td>4</td><td>1MHz</td></tr> <tr> <td>5</td><td>500KHz</td></tr> <tr> <td>6</td><td>250KHz</td></tr> <tr> <td>7</td><td>125KHz</td></tr> </table>					Value	ANALOG CLOCK (CLK_ANA) Output Frequency	0	16MHz	1	8MHz	2	4MHz	3	2MHz	4	1MHz	5	500KHz	6	250KHz	7	125KHz
Value	ANALOG CLOCK (CLK_ANA) Output Frequency																										
0	16MHz																										
1	8MHz																										
2	4MHz																										
3	2MHz																										
4	1MHz																										
5	500KHz																										
6	250KHz																										
7	125KHz																										

Fos CLOCK RATE CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset	
0x86	SET_FOS_CLKN[7:0]								0x05	
	RW									
Bit	Field		Type	Reset	Description					
7:0	SET_FOS_CLKN[7:0]		R/W	0x05	Control of Fos clock rate in analog controller Input clock is divided by (2xSET_FOS_CLKN) to generate CLK_SH					

SENSOR CHANNEL DECIMATION FILTER PARAMETER1 CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset			
0x0E	SENSOR_CH_OS[7:0]								0x00			
	RW											
Bit	Field								Type	Reset	Description	
7:0	SENSOR_CH_OS[7:0]		R/W	0x00	SENSOR_CH_OS[10:0] : Sensor channel OSR. the setting value is limited from 8 to 1024							

SENSOR CHANNEL DECIMATION FILTER PARAMTER2 CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset			
0x0F	SENSOR_CH_TRNC[4:0]								0x00			
	RW								RW			
Bit	Field								Type	Reset	Description	
7:3	SENSOR_CH_TRNC[4:0]		R/W	0x00	Sensor channel Decimation Filter Truncation : LSB N bits right shift							
2:0	SENSOR_CH_OS[10:8]		R/W	0x00	SENSOR_CH_OS[10:0] : Sensor channel OSR. the setting value is limited from 8 to 1024							

TEMPS CHANNEL DECIMATION FILTER PARAMETER1 CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset			
0x10	TEMPS_CH_OS[7:0]								0x00			
	RW								RW			
Bit	Field								Type	Reset	Description	
7:0	TEMPS_CH_OS[7:0]		R/W	0x00	TEMPS_CH_OS[10:0] : Temperature sensor channel OSR. the setting value is limited from 8 to 1024							

TEMPS CHANNEL DECIMATION FILTER PARAMTER2 CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset			
0x11	TEMPS_CH_TRNC[4:0]								0x00			
	RW								RW			
Bit	Field								Type	Reset	Description	
7:3	TEMPS_CH_TRNC[4:0]		R/W	0x00	Temperature sensor channel Decimation Filter Truncation : LSB N bits right shift							
2:0	TEMPS_CH_OS[10:8]		R/W	0x00	TEMPS_CH_OS[10:0] : Temperature sensor channel OSR. the setting value is limited from 8 to 1024							

TESTV CHANNEL DECIMATION FILTER PARAMTER1 CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset		
0x12	TESTV_CH_OS[7:0]								0x00		
	RW								RW		
Bit	Field								Type	Reset	Description

Bit	Field	Type	Reset	Description				
7:0	TESTV_CH_OSR	R/W	0x00	TESTV_CH_OS[10:0] : TESTV channel OSR. the setting value is limited from 8 to 1024				

TESTV CHANNEL DECIMATION FILTER PARAMETER2 CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset					
0x13	TESTV_CH_TRNC[4:0]					TESTV_CH_OS[10:8]			0x00					
	RW					RW								
Bit	Field		Type	Reset	Description									
7:3	TESTV_CH_TRNC[4:0]		R/W	0x00	TESTV channel Decimation Filter Truncation : LSB N bits right shift									
2:0	TESTV_CH_OS[10:8]		R/W	0x00	TESTV_CH_OS[10:0] : TESTV channel OSR. the setting value is limited from 8 to 1024									

SENSOR CHANNEL AVERAGE FILTER PARAMETER CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset			
0x15	SENSOR_CH_AVG_CNT[3:0]					-	SENSOR_CH_AVG_TRNC[2:0]					
	RW					-	RW					
Bit	Field		Type	Reset	Description							
7:4	SENSOR_CH_AVG_CNT[3:0]		R/W	0x00	Sensor channel average filter counter							
3					Reserved							
2:0	SENSOR_CH_AVG_TRNC[2:0]		R/W	0x00	Sensor channel average Filter Truncation : LSB N bits right shift							

TEMPS CHANNEL AVERAGE FILTER PARAMETER CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset			
0x16	TEMPS_CH_AVG_CNT[3:0]					-	TEMPS_CH_AVG_TRNC[2:0]					
	RW					-	RW					
Bit	Field		Type	Reset	Description							
7:4	TEMPS_AVG_CNT[3:0]		R/W	0x00	Temperature sensor channel average filter counter							
3					Reserved							
2:0	TEMPS_CH_AVG_TRNC[2:0]		R/W	0x00	Temperature sensor channel average Filter Truncation : LSB N bits right shift							

TESTV CHANNEL AVERAGE FILTER PARAMETER CONTROL Register(ONM)

Address	7	6	5	4	3	2	1	0	reset
---------	---	---	---	---	---	---	---	---	-------

0x17	TESTV_CH_AVG_CNT[3:0]			-	TESTV_CH_AVG_TRNC[2:0]	0x00	
	RW			-	RW		
Bit	Field	Type	Reset	Description			
7:4	TESTV_CH_AVG_CNT[3:0]	R/W	0x00	TESTV channel average filter counter			
3				Reserved			
2:0	TESTV_CH_AVG_TRNC[2:0]	R/W	0x00	TESTV channel average Filter Truncation : LSB N bits right shift			

7.4 DIGITAL FILTER SETUP

OSR is configured for processing DSM output samples and can be set between 8 and 1024. After Decimation Filter, the results can be adjusted for gain and offset in Post Processing block. There are two types of digital filters available for decimation, and the user can configure only one of them for use. Digital Filter introduces latency depending on OSR, which the user should consider when configuring the filter.

7.4.1 FILTER LATENCY

The Digital Filter introduces latency proportional to the OSR. In the integrator filter, as the stage increases, the latency difference is up to 3 DSM samples, while in the CIC filter, the latency is $OSR * (\text{STAGE}-1)$ DSM samples. When the FILTER_LATENCY register is set to high, the system enters low latency mode, which eliminates the latency but results in reduced accuracy.

7.4.1.1 Integrator

Table 20 Decimation Filter Latency : integrator

FILTER_STAGE	Filter Latency = 0	Filter Latency = 1
STAGE 1	OSR	OSR
STAGE 2	$OSR + 1$	OSR
STAGE 3	$OSR + 2$	OSR
STAGE 4	$OSR + 3$	OSR

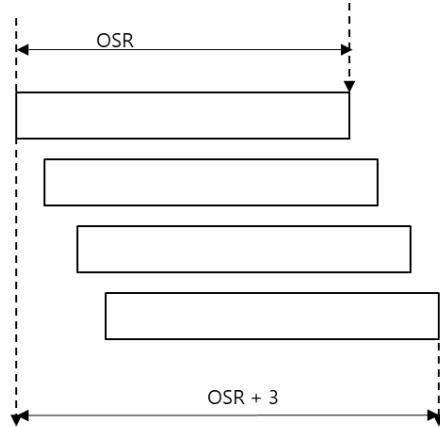


Figure 54 Decimation Filter Latency : Integrator (FILTER_LATENCY = 0, SEL_STAGE = 3).

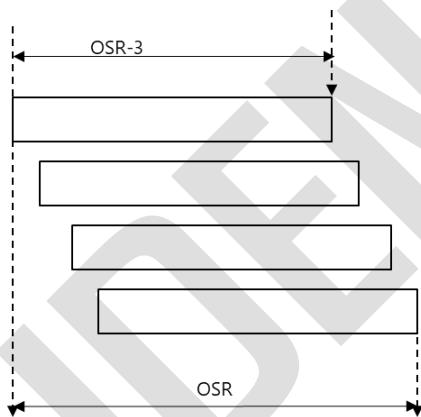


Figure 55 Decimation Filter Latency: Integrator Low latency mode (FILTER_LATENCY = 1, SEL_STAGE = 3).

Figure 54 and Figure 55 illustrate the differences in the FILTER_LATENCY register settings for the integrator filter. Since the number of SAMPLES input into the Digital Filter changes, the difference in FILTER GAIN corresponds to the number of SAMPLES.

7.4.1.2 CIC

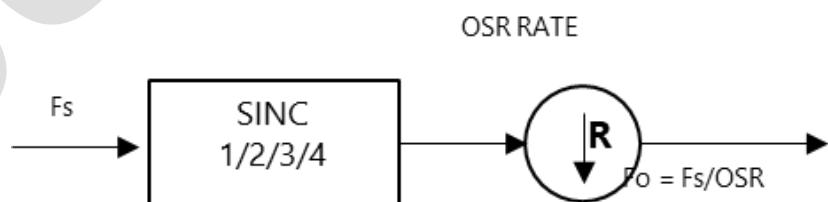


Figure 56 Block Diagram of Decimation and Digital Filter

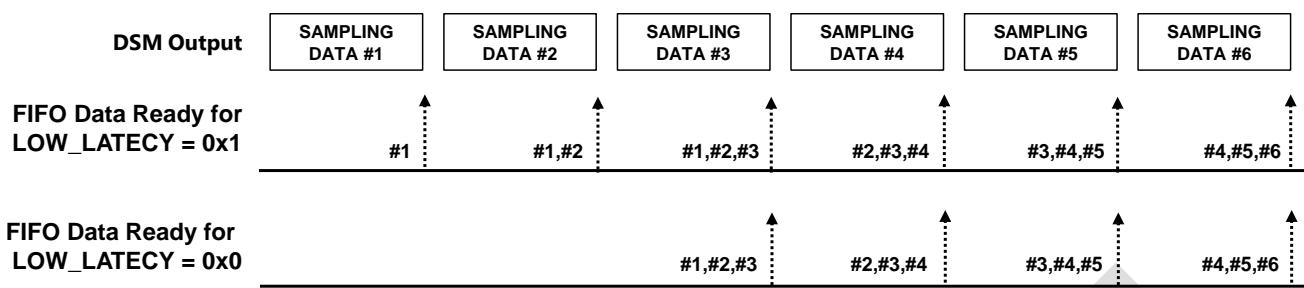


Figure 57 Diagram of ODR (Output Data Rate) in Case of CIC Decimation(SYNC3)

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7.4.2 Filter Bit Truncation & Output path

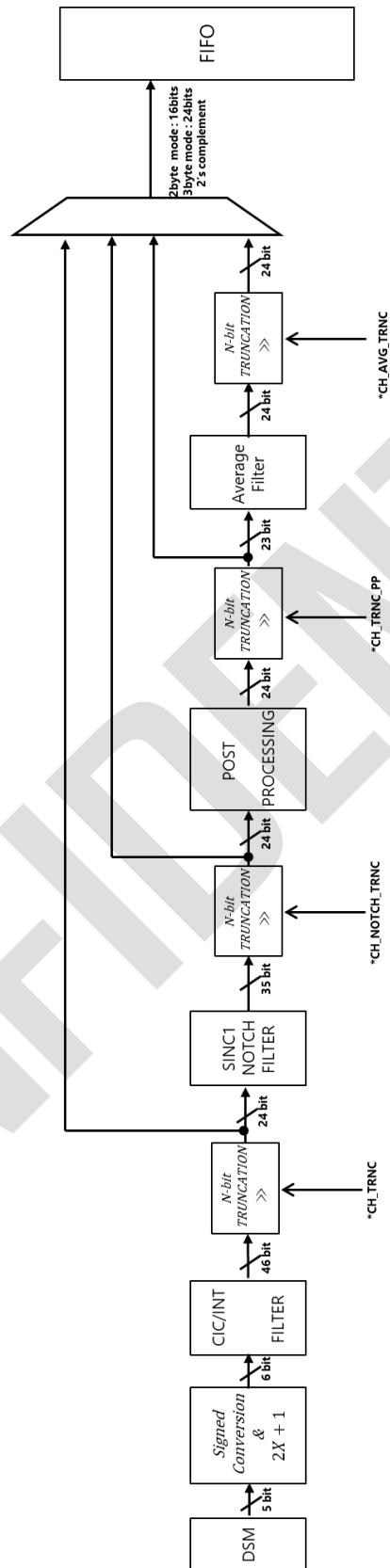
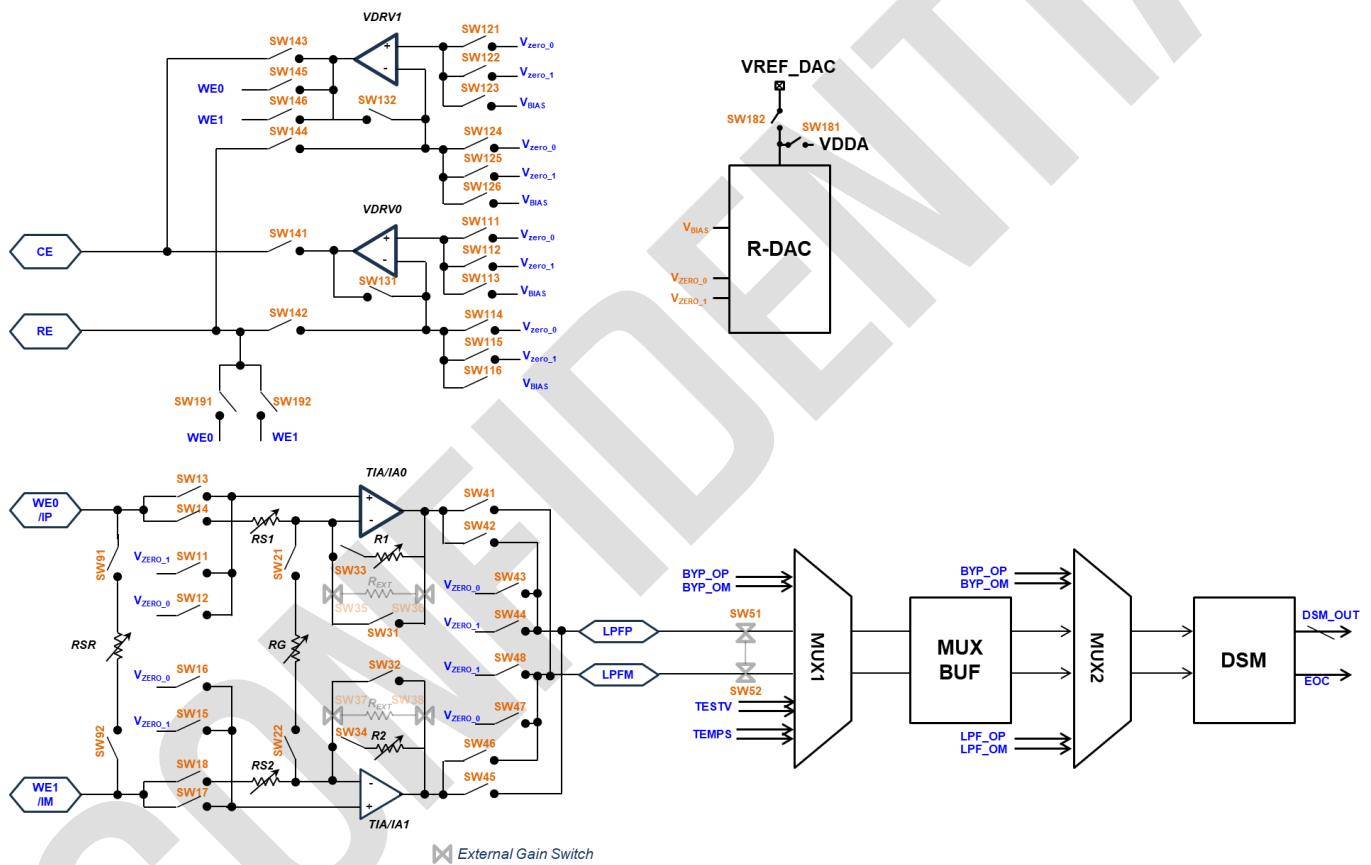


Figure 58 Filter Bit Truncation Block Diagram

Table 21 FIFO Input Mux Selection

Filter Output Mux Selection	GAIN_MODE	*CH_AVG_CNT	*CH_AVG_TRNC
CIC/INT-FIFO	0x0	0x0	0x0
POST_PROCESSING -FIFO	0x1	0x0	0x0
AVERAGE - FIFO	Don't Care	Not Equal to "0x0"	Don't Care

7.5 SWITCH CONFIGURATION

**Figure 59 Diagram of Switch Matrix**

The External Gain Switch is a switch that connects to external resistors or capacitors on the chip. SW51_SW52 can be connected to PAD LPFP and PAD LPFM. SW35_SW36 controls PAD TIA01 and PAD TIA00, while SW37_SW38 controls PAD TIA10 and PAD TIA11.

7.5.1 2-TERMINAL MODE

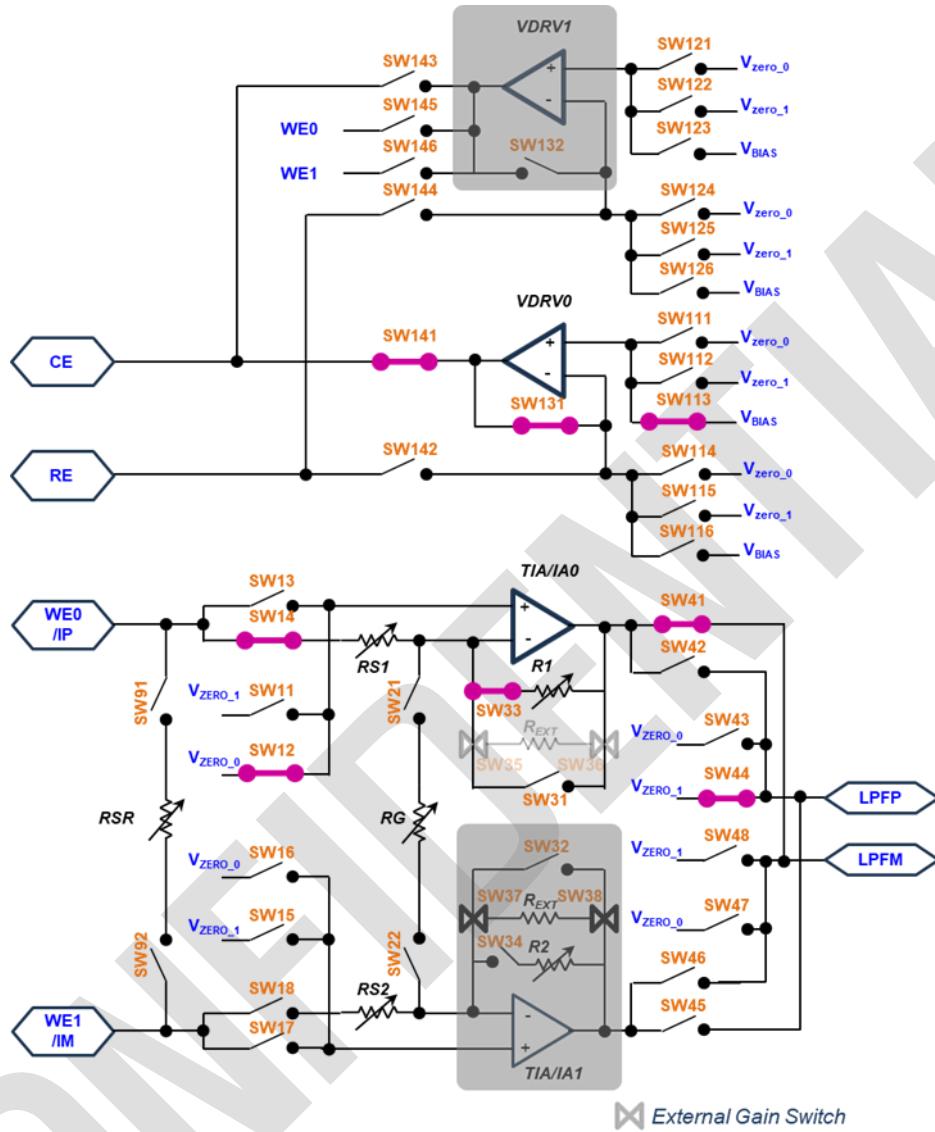


Figure 60 2-Terminal WE0 Switch Configuration

Switch On: SW12, SW14, SW33, SW41, SW44, SW113, SW131, SW141

Table 22 Register Setting for Switch Control: 2-Terminal Single Channel, WE0

Address(Hex)	Data (Hex)	Description
0xD2	0x50	On : SW12, SW14
0xD3	0x40	ON : SW33
0xD4	0x24	ON : SW41, SW44
0xD5	0x00	OFF
0xD6	0x04	ON : SW113
0xD7	0x50	ON: SW131, SW141
0xD8	0x00	OFF
0xD9	0x00	OFF
0xD0	0x20	DAC1_VZERO_0 : 0.9V
0xD1	0x20	DAC2_VZERO_1 : 0.9V
0xC8	0xA8	Enable : ENB_TIA0, ENB_VDRV0 ENB_DAC, ENB_ACTRL, ENB_BIAS_GLOBAL

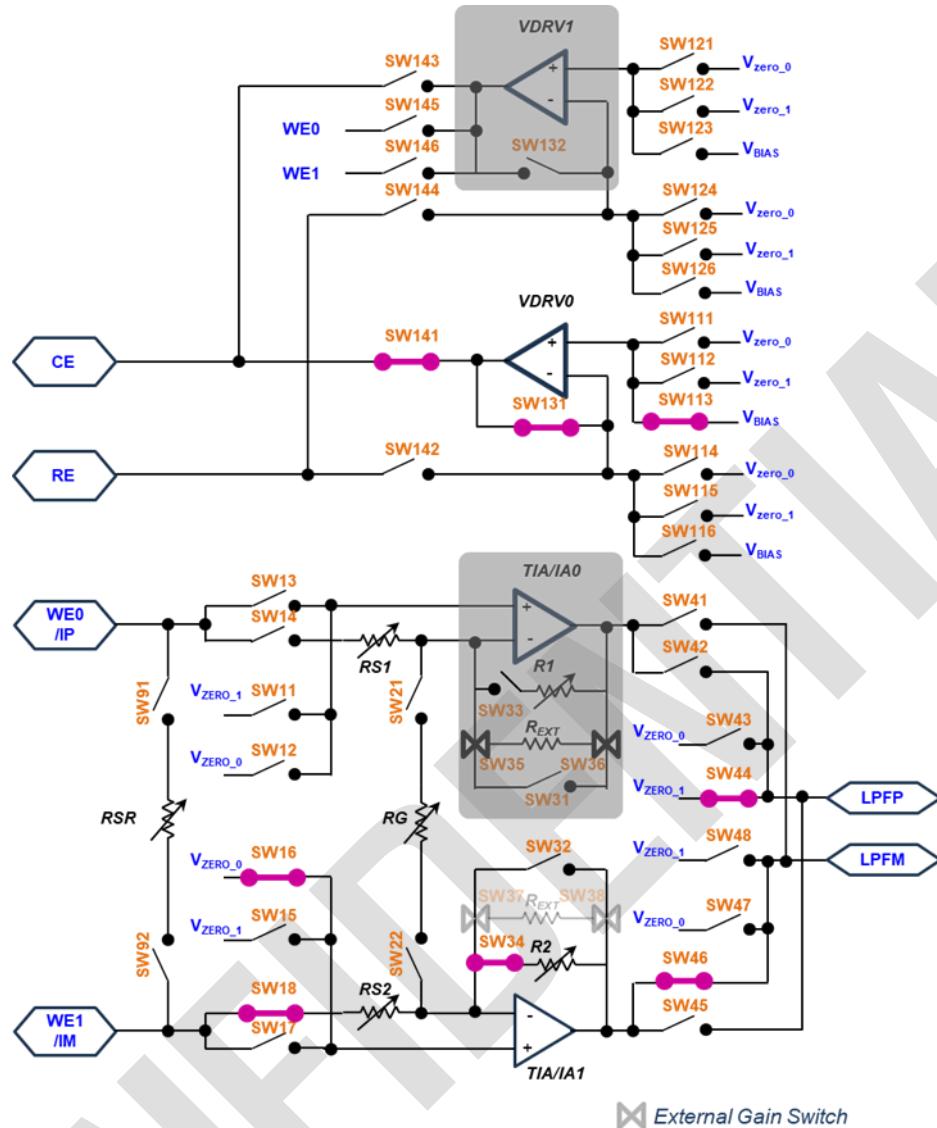


Figure 61 2-Terminal WE1 Switch Configuration

Switch On: SW16, SW18, SW34, SW44, SW46, SW113, SW131, SW141

Table 23 Register Setting for Switch Control: 2-Terminal Single Channel, WE1

Address(Hex)	Data (Hex)	Description
0xD2	0x00	OFF
0xD3	0x85	ON : SW16, SW18, SW34
0xD4	0xA0	ON : SW44, SW46
0xD5	0x00	OFF
0xD6	0x04	ON : SW113
0xD7	0x50	ON: SW131, SW141
0xD8	0x00	OFF
0xD9	0x00	OFF
0xD0	0x20	DAC1_VZERO_0 : 0.9V
0xD1	0x20	DAC2_VZERO_1 : 0.9V
0xC8	0x68	Enable : ENB_TIA1, ENB_VDRV0 ENB_DAC, ENB_ACTRL, ENB_BIAS_GLOBAL

7.5.2 3-Terminal MODE

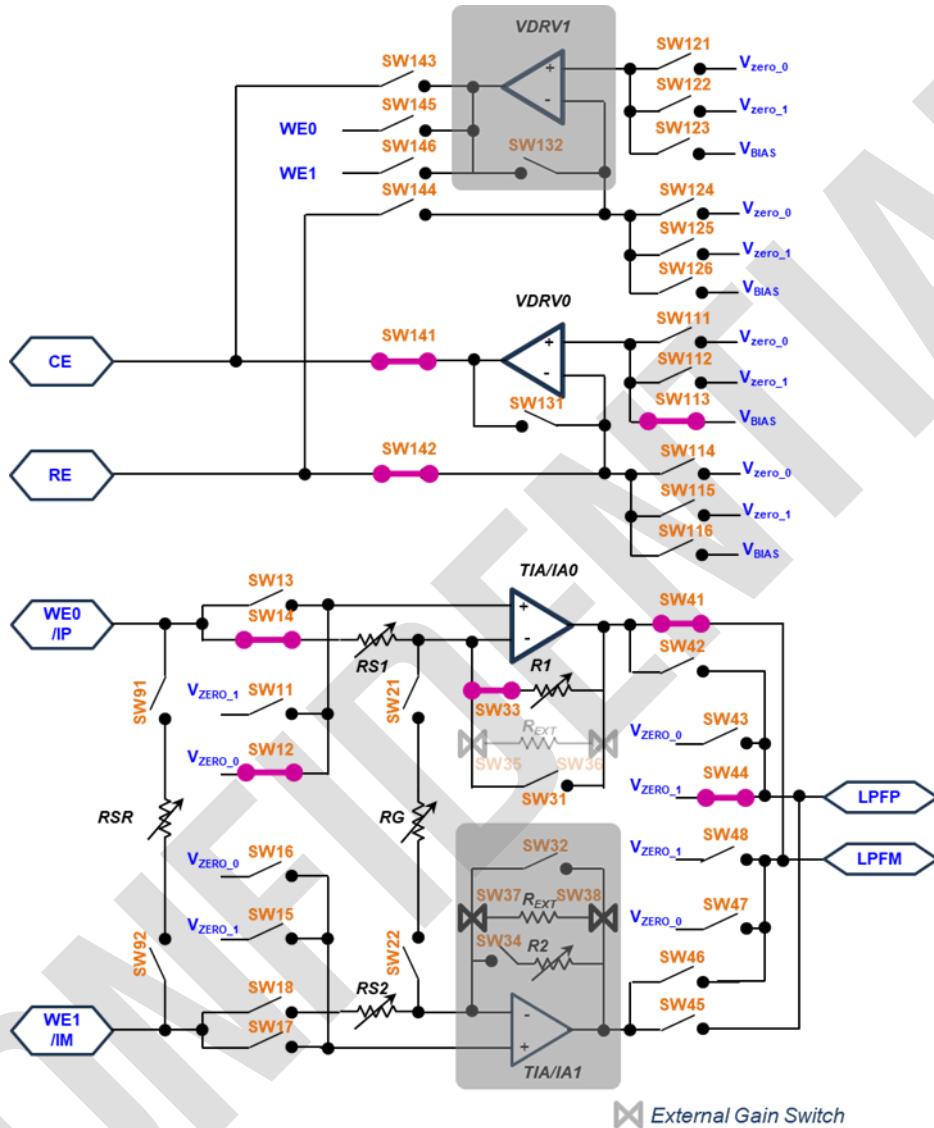


Figure 62 3-Terminal WE0 Switch Configuration

Switch On: SW12, SW14, SW33, SW41, SW44, SW113, SW141, SW142,

Table 24 Register Setting for Switch Control : 3-Terminal Single Channel WE0

Address(Hex)	Data (Hex)	Description
0xD2	0x50	On : SW12, SW14
0xD3	0x40	ON : SW33
0xD4	0x24	ON : SW41, SW44

0xD5	0x00	OFF
0xD6	0x04	ON : SW113
0xD7	0xC0	ON: SW141, SW142
0xD8	0x00	Others OFF
0xD9	0x00	Others OFF
0xD0	0x20	DAC1_VZERO_0 : 0.9V
0xD1	0x20	DAC2_VZERO_1 : 0.9V
0xC8	0xA8	Enable : ENB_TIA0, ENB_VDRV0 ENB_DAC, ENB_ACTRL, ENB_BIAS_GLOBAL

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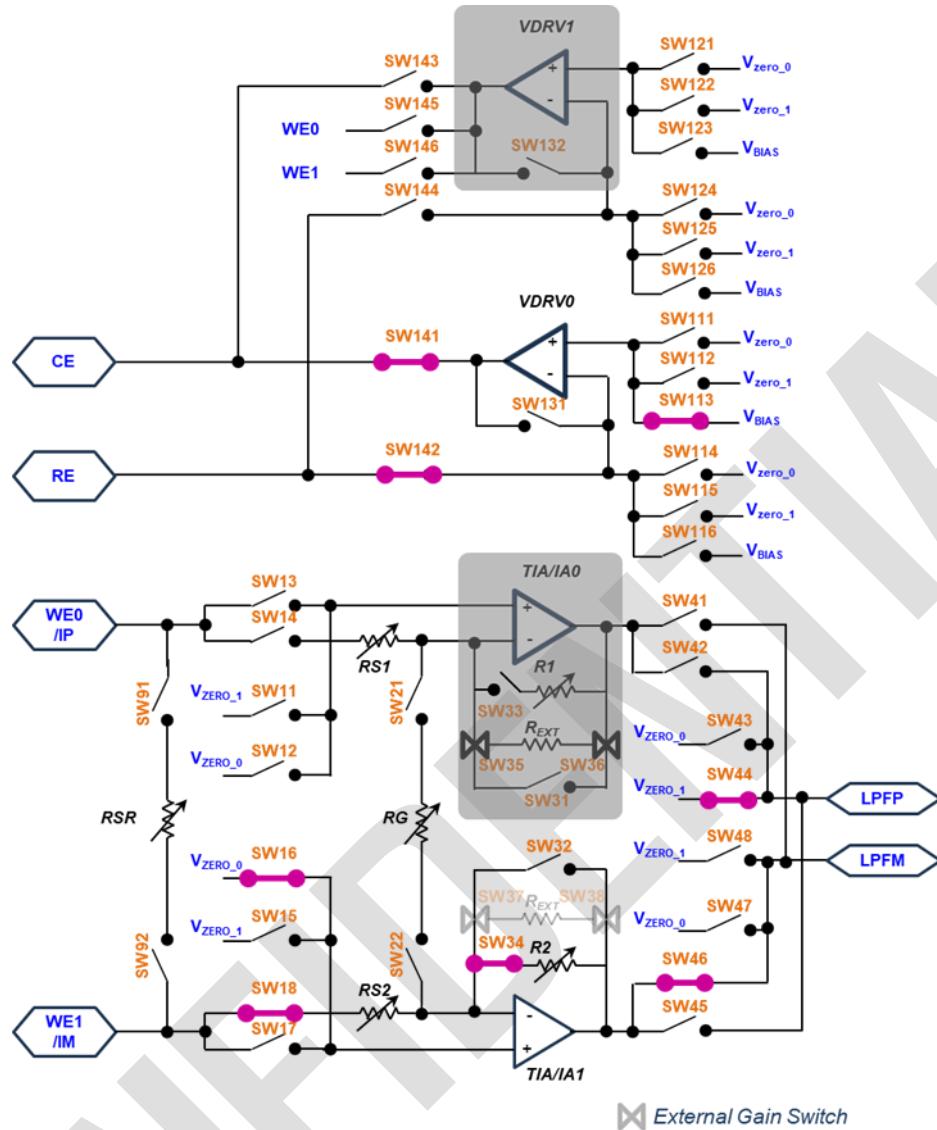


Figure 63 3-Terminal WE1 Switch Configuration

Switch On: SW16, SW18, SW34, SW44, SW46, SW113, SW141, SW142

Table 25 Register Setting for Switch Control : 3-Terminal Single Channel WE1

Address(Hex)	Data (Hex)	Description
0xD2	0x00	Others OFF
0xD3	0x85	ON : SW16, SW18, SW34
0xD4	0xA0	ON : SW44, SW46
0xD5	0x00	OFF
0xD6	0x04	ON : SW113
0xD7	0xC0	ON: SW141, SW142
0xD8	0x00	Others OFF
0xD9	0x00	Others OFF
0xD0	0x20	DAC1_VZERO_0 : 0.9V
0xD1	0x20	DAC2_VZERO_1 : 0.9V
0xC8	0x68	Enable : ENB_TIA1, ENB_VDRV0 ENB_DAC, ENB_ACTRL, ENB_BIAS_GLOBAL

7.5.3 4-TERMINAL MODE

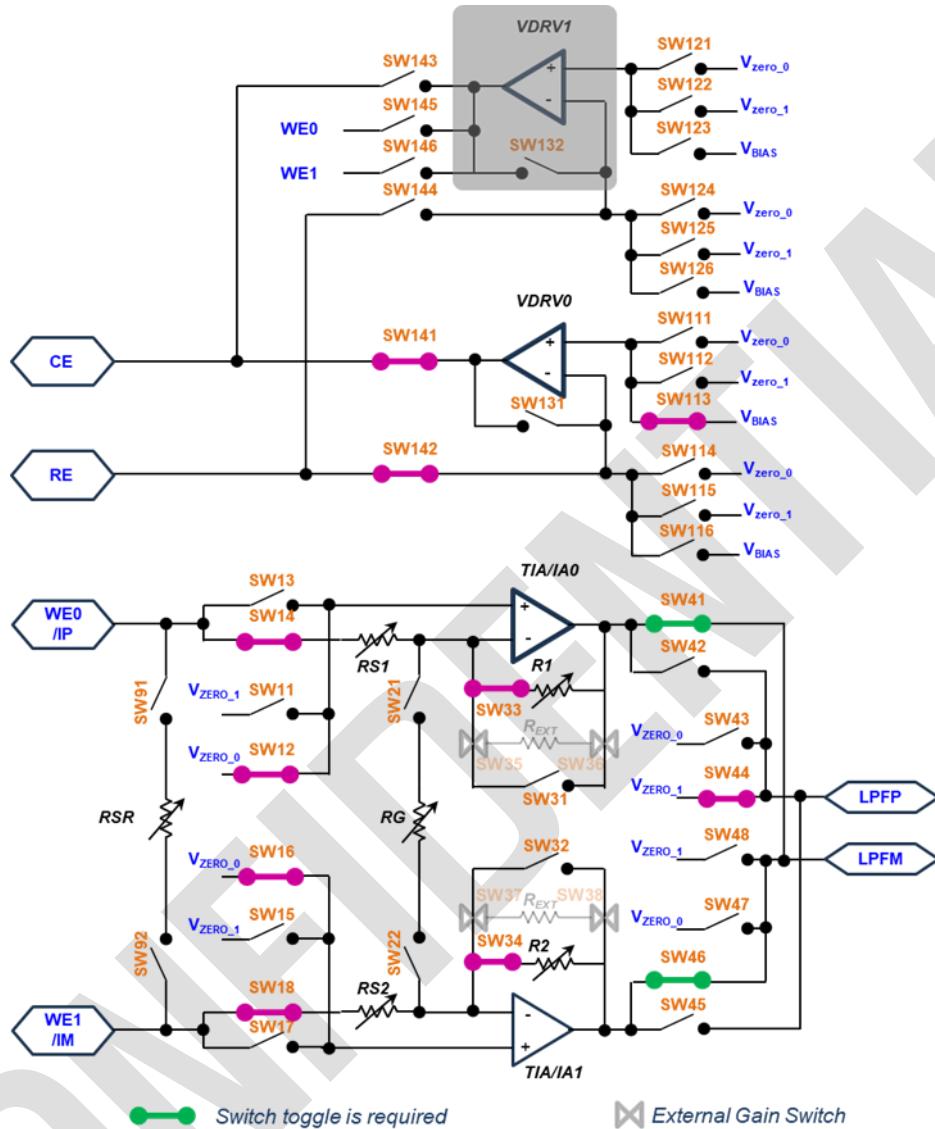


Figure 64 4-Terminal Switch Configuration

- Switch On (common) : SW12, SW14, SW16, SW18, SW33, SW34, SW44, SW113, SW141, SW142
- Switch WE0 : ON SW41 , OFF SW46
- Switch WE1 : ON SW46 , OFF SW41

Table 26 Register Setting for Switch Control : 4-terminal (Biopotentiostat)

Address(Hex)	Data (Hex)	Description
0xD2	0x50	ON: SW12, SW14
0xD3	0xC5	ON: SW16, SW18, SW33, SW34

0xD4	0x20	ON : SW44
0xD5	0x00	OFF
0xD6	0x04	ON : SW113
0xD7	0xC0	ON : SW142, SW141,
0xD8	0x00	OFF
0xD9	0x00	OFF
0xD0	0x20	DAC1_VZERO_0 : 0.9V
0xD1	0x20	DAC2_VZERO_1 : 0.9V
0xC8	0x28	Enable : ENB_TIA0, ENB_TIA1, ENB_VDRV0 ENB_DAC, ENB_ACTRL, ENB_BIAS_GLOBAL

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7.5.4 IA MODE

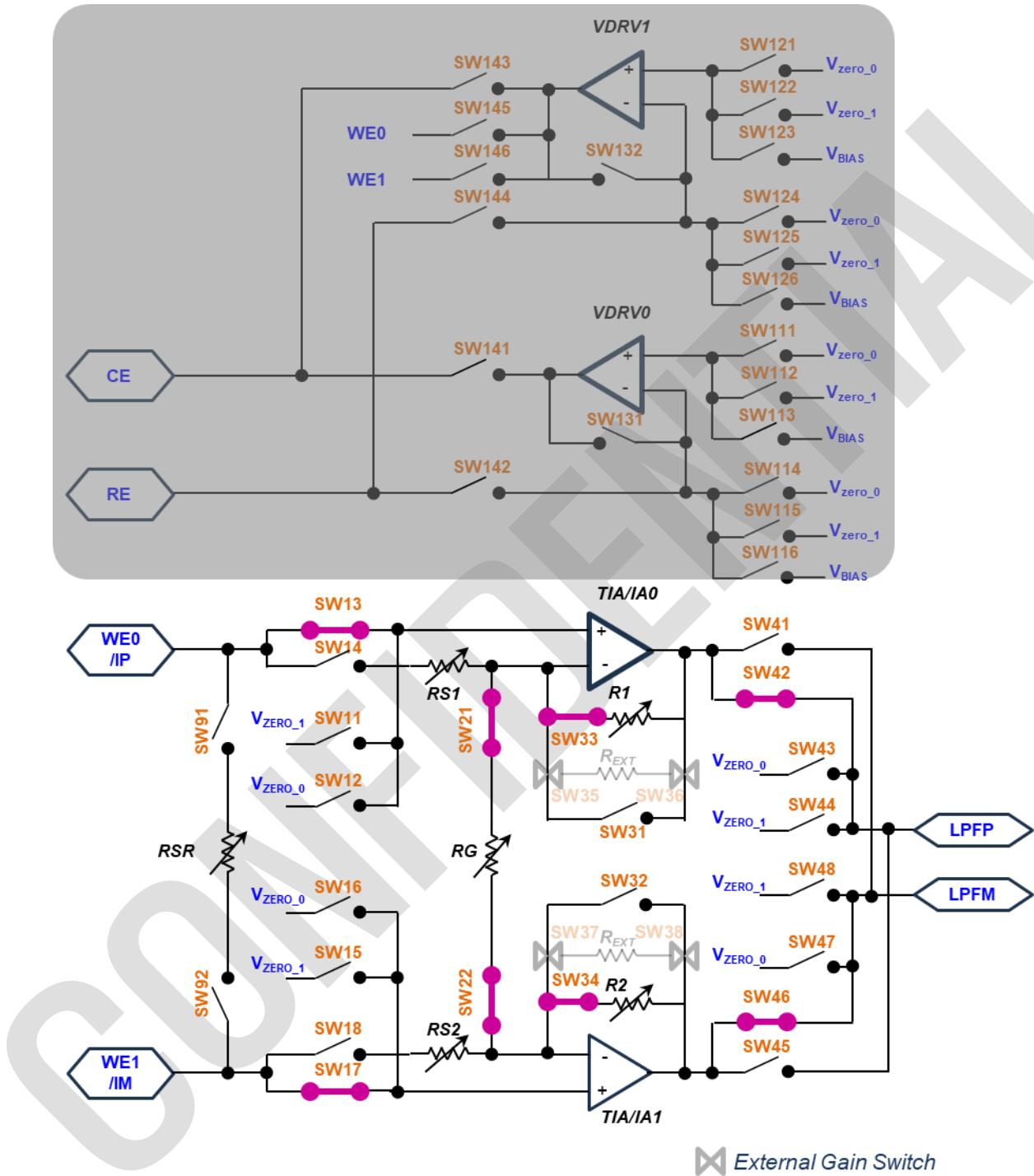


Figure 65 IA MODE Switch Configuration

Switch On : SW13, SW17, SW21_SW22, SW33, SW34, SW42, SW46

Table 27 Register Setting for Switch Control : IA (Instrumental Amplifier) Mode

Address(Hex)	Data (Hex)	Description
0xD2	0x20	ON : SW13
0xD3	0xCA	ON : SW17, SW21_22, SW33, SW34
0xD4	0x88	ON : SW42, SW46
0xD5	0x00	OFF
0xD6	0x00	OFF
0xD7	0x00	OFF
0xD8	0x00	OFF
0xD9	0x00	OFF
0xC8	0x38	Enable : ENB_TIA0, ENB_TIA1, ENB_DAC, ENB_ACTRL, ENB_BIAS_GLOBAL
0xD2	0x20	ON : SW13
0xD3	0xCA	ON : SW17, SW21_22, SW33, SW34

SWITCH CONTROL0 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xD2	CSW15	CSW14	CSW13	CSW12	CSW11	CSW82	CSW81	CSW91_92	0x00	
	RW	RW	RW	RW	RW	RW	RW	RW		
Bit	Field	Type	Type	Reset	Description					
7	CSW15	R/W	R/W	0x00	V_ZERO_1 - Positive input of TIA1					
6	CSW14	R/W	R/W	0x00	Control TIA0 operation mode					
5	CSW13	R/W	R/W	0x00	Control TIA0 operation mode					
4	CSW12	R/W	R/W	0x00	V_ZERO_0 - Positive input of TIA0					
3	CSW11	R/W	R/W	0x00	V_ZERO_1 - Positive input of TIA0					
2	CSW82	R/W	R/W	0x00	Control bypass of TIA1					
1	CSW81	R/W	R/W	0x00	Control bypass of TIA0					
0	CSW91_92	R/W	R/W	0x00	Control SENSR connection. 0: open 1: using SENSR					

SWITCH CONTROL1 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xD3	CSW34	CSW33	CSW32	CSW31	CSW21_22	CSW18	CSW17	CSW16	0x00	
	RW	RW	RW	RW	RW	RW	RW	RW		
Bit	Field	Type	Type	Reset	Description					
7	CSW34	R/W	R/W	0x00	Control TIA1 operation mode					
6	CSW33	R/W	R/W	0x00	Control TIA0 operation mode					
5	CSW32	R/W	R/W	0x00	Control TIA1 unity-gain mode					
4	CSW31	R/W	R/W	0x00	Control TIA0 unity-gain mode					
3	CSW21_22	R/W	R/W	0x00	Control RG connection 0: open 1: Connection to RG					
2	CSW18	R/W	R/W	0x00	Control TIA1 operation mode					
1	CSW17	R/W	R/W	0x00	Control TIA1 operation mode					
0	CSW16	R/W	R/W	0x00	V_ZERO_0 - Positive input of TIA1					

SWITCH CONTROL2 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset
0xD4	CSW46	CSW45	CSW44	CSW43	CSW42	CSW41	CSW37_38	CSW35_36	0x00
	RW	RW							

Bit	Field	Type	Reset	Description
7	CSW46	R/W	0x00	TIA1 - Negative input of LPF
6	CSW45	R/W	0x00	TIA1 - Positive input of LPF
5	CSW44	R/W	0x00	V_ZERO_1 - Positive input of LPF
4	CSW43	R/W	0x00	V_ZERO_0 - Positive input of LPF
3	CSW42	R/W	0x00	TIA0 - Positive input of LPF
2	CSW41	R/W	0x00	TIA0 - Negative input of LPF
1	CSW37_38	R/W	0x00	Control external TIA1 C1 connection
0	CSW35_36	R/W	0x00	Control external TIA0 C1 connection

SWITCH CONTROL3 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xD5	-	-	-	-	-	CSW51_52	CSW48	CSW47	0x00	
	-	-	-	-	-	RW	RW	RW		
Bit	Field		Type		Reset		Description			
2	CSW51_52		R/W		0x00		Control external cap connections of LPF			
1	CSW48		R/W		0x00		V_ZERO_1 - Negative input of LPF			
0	CSW47		R/W		0x00		V_ZERO_0 - Nagative input of LPF			

SWITCH CONTROL4 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xD6	CSW122		CSW121	CSW116	CSW115	CSW114	CSW113	CSW112	CSW111	
	RW		RW	RW	RW	RW	RW	RW	0x00	
Bit	Field		Type		Reset		Description			
7	CSW122		R/W		0x00		V_ZERO_1 - Positive input of VDRV1			
6	CSW121		R/W		0x00		V_ZERO_0 - Positive input of VDRV1			
5	CSW116		R/W		0x00		V_BIAS - Negative input of VDRV0			
4	CSW115		R/W		0x00		V_ZERO_1 - Negative input of VDRV0			
3	CSW114		R/W		0x00		V_ZERO_0 - Negative input of VDRV0			
2	CSW113		R/W		0x00		V_BIAS - Positive input of VDRV0			
1	CSW112		R/W		0x00		V_ZERO_1 - Positive input of VDRV0			
0	CSW111		R/W		0x00		V_ZERO_0 - Positive input of VDRV0			

SWITCH CONTROL5 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xD7	CSW142	CSW141	CSW132	CSW131	CSW126	CSW125	CSW124	CSW123	0x00	
	RW	RW								
Bit	Field		Type		Reset		Description			
7	CSW142		R/W		0x00		Control VDRV0 - RE connection			
6	CSW141		R/W		0x00		Control VDRV0 output connection			
5	CSW132		R/W		0x00		Control VDRV1 unity-gain configuration			
4	CSW131		R/W		0x00		Control VDRV0 unity-gain configuration			
3	CSW126		R/W		0x00		V_BIAS - Negative input of VDRV1			
2	CSW125		R/W		0x00		V_ZERO_1 - Negative input of VDRV1			
1	CSW124		R/W		0x00		V_ZERO_0 - Negative input of VDRV1			
0	CSW123		R/W		0x00		V_BIAS - Positive input of VDRV1			

SWITCH CONTROL6 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xD8	-	-	CSW192	CSW191	CSW146	CSW145	CSW144	CSW143	0x00	
	-	-	RW	RW	RW	RW	RW	RW		
Bit	Field		Type		Reset		Description			
5	CSW192		R/W		0x00		Control RE - WE1 connection			
4	CSW191		R/W		0x00		Control RE - WE0 connection			
3	CSW146		R/W		0x00		Control VDRV1 output - WE1 connection			
2	CSW145		R/W		0x00		Control VDRV1 output - WE0 connection			
1	CSW144		R/W		0x00		Control VDRV1 - RE connection			
0	CSW143		R/W		0x00		Control VDRV1 output connection			

SWITCH CONTROL7 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xD9	-	-	-	CSW181_182	CSW196	CSW195	CSW194	CSW193	0x00	
	-	-	-	RW	RW	RW	RW	RW		
Bit	Field		Type		Reset		Description			
4	CSW181_182		R/W		0x00		Select DAC reference 0: VDDA 1: VREF_DAC			
3	CSW196		R/W		0x00		Control RE - VSSA connection			
2	CSW195		R/W		0x00		Control RE - VDDA connection			
1	CSW194		R/W		0x00		Control CE - VSSA connection			

0	CSW193	R/W	0x00	Control CE - VDDA connection
---	--------	-----	------	------------------------------

7.6 OPERATION CONTROL

7.6.1 Reset

7.6.1.1 Hardware Reset

~~RESET pin을 통해 reset 신호를 인가 하면 TRIM_* register를 제외 한 나머지 register들이 reset 된다.~~

When a reset signal is applied through the RESET pin, all registers except the TRIM_* registers are reset.

7.6.1.2 Software Reset

Writing 0xA5 to the register at address 0x3C resets all registers and functions, excluding the TRIM_* registers. To initiate a software reset, set the CLK_FE_RST register to 0x1.

7.6.2 Interrupt Setting

7.6.2.1 Hardware Interrupt Setting

Refer to Sec.6.9

7.6.2.2 FIFO Interrupt Setting

Refer to Sec.6.7.3

7.6.3 Gain Setting

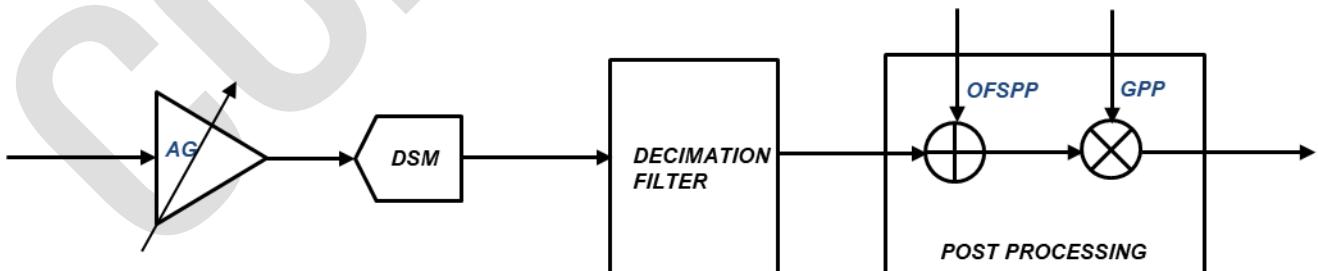


Figure 66 NMS4110 Gain Chain Diagram

Figure 66 provides a simplified schematic of NMS4110 calibration process. Gain adjustment is achieved through two components: analog gain and digital gain.

7.6.3.1 Analog Gain

Table 28 provides an overview of the optimal GAIN setting codes for the current ranges applied to the sensor, with the ETC column detailing the recommended BOOST settings.

Table 28 Analog Gain R1,R2 & TIA BST@@@@

R1 or R2	gain avg	current range	etc	R1 or R2	gain avg	current range	etc
0	-241.179			14	-30255.1	~25uA	
1	-423.761	~1mA	bst3	15	-32262.1	~23uA	
2	-680.8	~500uA	bst2	16	-40285.4	~20uA	
3	-1188.67	~200uA		17	-48309.5	~15uA	
4	-2195.16	~175uA		18	-64356.8	~10uA	
5	-3197.63	~150uA	bst1	19	-85419.7	~9uA	
6	-4196.1	~125uA		20	-96452.1	~8uA	
7	-6194.99	~100uA		21	-100465	~7uA	
8	-8197.55	~80uA		22	-120524	~6uA	
9	-10201.6	~70uA		23	-128547	~5uA	
10	-12207.5	~60uA		24	-160642	~4uA	
11	-16217.2	~40uA		25	-196749	~3uA	
12	-20228.1	~35uA		26	-256926	~2uA	
13	-24239.4	~30uA		27	-513613	~1uA	

Analog gain can be set using the following pseudo code

PSEUDO CODE VARIABLE : SET_RESISTOR_Rn		
VARIABLE	REGISTER	Description
AG	SEL_Rn Register	Resistor value
Rn		Select R1 or R2

```

SET_RESISTOR_Rn : START
define R1    0
define R2    1
void SET_RESISTOR_Rn (byte AG, integer Rn )
{
    byte    rdata ;
    byte    wdata ;

```

```

switch(Rn)
{
    case R1
        rdata = 오류! 참조 원본을 찾을 수 없습니다. (0xCB) & 0x07 ;
        wdata = (AG << 3) | rdata ;
        오류! 참조 원본을 찾을 수 없습니다. (0xCB, wdata) ;

    case R2
        rdata = 오류! 참조 원본을 찾을 수 없습니다. (0xCC) & 0xE0 ;
        wdata = AG | rdata ;
        오류! 참조 원본을 찾을 수 없습니다. (0xCC, wdata) ;
    }
}
SET_RESISTOR_Rn : END

```

PSEUDO CODE VARIABLE : SET_TIA_BST

VARIABLE	REGISTER	Description
TIA_BST	TIA_BST Register	Adjust TIA driving boost
Rn		Select R1 or R2

```

SET_TIA_BST :
define R1      0
define R2      1
void SET_TIA_BST (byte TIA_BST, integer Rn)
{
    byte    rdata ;
    byte    wdata ;

    switch(Rn)
    {
        case R1
            rdata = 오류! 참조 원본을 찾을 수 없습니다. (0xDB) & 0xFC ;
            wdata = TIA_BST | rdata ;
            오류! 참조 원본을 찾을 수 없습니다. (0xDB, wdata) ;

        case R2
            rdata = 오류! 참조 원본을 찾을 수 없습니다. (0xDB) & 0xCF ;
            wdata = (TIA_BST << 4) | rdata ;
    }
}

```

```

        오류! 참조 원본을 찾을 수 없습니다. (0xDB, wdata) ;

    }

SET_TIA_BST : END

```

TIA COMPONENT CONTROL1 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset					
0xCB	SEL_R1[4:0]					SEL_RS2[2:0]			0x00					
	RW					RW								
Bit	Field	Type	Reset	Description										
7:3	SEL_R1[4:0]	R/W	0x00	configure R1 value for TIA0										
2:0	SEL_RS2[2:0]	R/W	0x00	configure RS2 value for TIA1										

TIA COMPONENT CONTROL2 Register (AOM)

Address	7	6	5	4	3	2	1	0	reset						
0xCC	SEL_C1[2:0]				SEL_R2[4:0]				0x20						
	RW				RW										
Bit	Field	Type	Reset	Description											
7:3	SEL_C1[2:0]	R/W	0x00	configure C1 in parallel with R1											
2:0	SEL_R2[4:0]	R/W	0x00	configure R2 value for TIA1											

TIA_BST CONTROL Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0xDB	-	TIA1_BST_ACT	TIA1_BST[1:0]			-	TIA0_BST_ACT	TIA0_BST[1:0]		0x00
	-	RW	RW			-	RW	RW		
Bit	Field	Type	Reset	Description						
6	TIA1_BST_AC	R/W	0x00	Activation(1) of RX TIA1 driving boost						
5:4	TIA1_BST[1:0]	R/W	0x00	Adjust RX TIA1 driving boost.0: x1, 1: x2, 2: x4, 3: x8						
2	TIA0_BST_AC	R/W	0x00	Activation(1) of RX TIA0 driving boost						
1:0	TIA0_BST[1:0]	R/W	0x00	Adjust RX TIA0 driving boost.0: x1, 1: x2, 2: x4, 3: x8						

7.6.3.2 DIGITAL Gain

Digital gain is governed by the OSR. To avoid overflow during filter operations, truncation and

scaling adjustments are required. The equation below provides the method to calculate bit truncation and post-processing block parameters to prevent overflow in the CIC filter based on the OSR configuration.

$$CicFilterGain = OSR^{STAGE}$$

$$CicFilterBitWidth = (\log_2 OSR) * STAGE + 6$$

$$CicFilterTruncation = \lfloor CicFilterBitWidth \rfloor - 16$$

$$PostProcessingInputGain = \frac{CicFilterGain}{2^{CicFilterTruncation}}$$

$$PostProcessingGain = \frac{1024}{PostProcessingInputGain}$$

In the above equation, CIC Filter Truncation is applied to the *CH_TRNC register. The Post Processing Gain can be determined using the following pseudo code.

PSEUDO CODE VARIABLE : CIC FILTER		
VARIABLE	REGISTER	Description
OSR	*CH_OSR Register	Filter OSR Value
FS	SEL_FLT Register	
FLT _{TRNC}	*CH_TRNC Register	
G _{PP}		Post Processing Gain

```

GET_CIC_FILTER_TRUNCATION : START
FLTTRNC GET_CIC_FILTER_TRUNCATION (integer OSR, integer FS) // 
{
    double cic_filter_bit_width ;
    byte FLTTRNC ;
    cic_filter_bit_width = LOG2(OSR) * FS + 6 ;
    FLTTRNC = int (cic_filter_bit_width) - 16 ;

    if ( FLTTRNC < 0 )
        FLTTRNC = 0 ;
    endif

    return FLTTRNC ;
}

GET_CIC_FILTER_TRUNCATION : END

```

```
GET_CIC_FILTER_PROCESSING_GAIN : START
[GPP , FLTTRNC] GET_CIC_FILTER_PROCESSING_GAIN (integer OSR, integer FS ) // {
{
    double cic_filter_gain ;
    double GPP ;
    double post_processing_gain ;
    double post_processing_input_gain ;
    integer cic_filter_truncation ;

    cic_filter_gain = pow (OSR, FS) ;
    FLTTRNC = GET_CIC_FILTER_TRUNCATION (OSR, FS) ;
    post_processing_input_gain = cic_filter_gain/pow(2, FLTTRNC) ;
    post_processing_gain = 1024/post_processing_input_gain ;
    GPP = post_processing_gain ;
    return [GPP , FLTTRNC] ;
}
GET_CIC_FILTER_PROCESSING_GAIN : END
```

```
SET_POST_PROCESSING_GAIN : START
define SENSOR_CH 1
define TEMPS_CH 2
define TESTV_CH 3
void SET_POST_PROCESSING_GAIN ( byte channel, double GPP)
{
    double pp_gain ;
    int32_t pp_gain_fixed ;
    integer CIP ; //CAL_INT_PTR
    integer k ;
    byte GAIN_INT;
    integer GAIN_FRC;
    byte gain_frc_msb;
    byte gain_frc_lsb;
    byte rdata ;
    byte wdata ;

    CIP = 0x04 ;
    k = 14 ;
    pp_gain = GPP ;
    if ( pp_gain > 32.0 ) pp_gain = 32.0 ; // max value limit

    if ( pp_gain < 0.9 ) { CIP = 0x20 ; k=17 ;}
```

```
else if ( pp_gain < 1.5 ) { CIP = 0x10 ; k=16 ;}
else if ( pp_gain < 3.0 ) { CIP = 0x08 ; k=15 ;}
else if ( pp_gain < 7.0 ) { CIP = 0x04 ; k=14 ;}
else if ( pp_gain < 14.0 ) { CIP = 0x02 ; k=13 ;}
else { CIP = 0x01 ; k=12 ;}

pp_gain_fixed = (int) (pp_gain * pow(2.0,k));

GAIN_INT = (pp_gain_fixed >> 14) & 0x0F ;
GAIN_FRC = pp_gain_fixed & 0x3FFF ;
gain_frc_lsb = GAIN_FRC & 0xFF ;
gain_frc_msb = (GAIN_FRC >> 8 ) & 0x3F ;
```

오류! 참조 원본을 찾을 수 없습니다. (0x34, CIP);

```
switch ( channel )
{
    case SENSOR_CH :
        rdata = 오류! 참조 원본을 찾을 수 없습니다. (0x28) & 0x0F ;
        wdata = rdata | (GAIN_INT << 4);
        오류! 참조 원본을 찾을 수 없습니다. (0x28, wdata );
        오류! 참조 원본을 찾을 수 없습니다. (0x22, gain_frc_lsb );
        오류! 참조 원본을 찾을 수 없습니다. (0x23, gain_frc_msb );
        break;
    case TEMPS_CH:
        rdata = 오류! 참조 원본을 찾을 수 없습니다. (0x29) & 0xF0 ;
        wdata = rdata | GAIN_INT ;
        오류! 참조 원본을 찾을 수 없습니다. (0x29, wdata );
        오류! 참조 원본을 찾을 수 없습니다. (0x24, gain_frc_lsb );
        오류! 참조 원본을 찾을 수 없습니다. (0x25, gain_frc_msb );
        break;
    case TESTV_CH :
        rdata = 오류! 참조 원본을 찾을 수 없습니다. (0x29) & 0x0F ;
        wdata = rdata | (GAIN_INT << 4);
        오류! 참조 원본을 찾을 수 없습니다. (0x29, wdata );
        오류! 참조 원본을 찾을 수 없습니다. (0x26, gain_frc_lsb );
        오류! 참조 원본을 찾을 수 없습니다. (0x27, gain_frc_msb );
```

```

        break;
    default : ;
}
}

SET_POST_PROCESSING_GAIN : END

```

7.6.4 Conversion Start/Stop

Writing 0x1 to the 0th bit of address 0x40 initiates the conversion start, while writing 0x0 stops the conversion.

DSM START Register (ONR)

Address	7	6	5	4	3	2	1	0	reset	
0x40	-	-	-	-	-	-	-	START	0x00	
	-	-	-	-	-	-	-	RW		
Bit	Field		Type		Reset		Description			
0	START		R/W		0x00		DSM START 0x1 : conversion start 0x0 : conversion stop			

7.6.5 OP MODE

DSM in NMS4110 operates in three different modes.

DSM RESET PERIOD Register (AOM)

Address	7	6	5	4	3	2	1	0	reset		
0x03	T_RST_DSM[7:0]							0x13			
	RW										
Bit	Field		Type	Reset	Description						
7:0	T_RST_DSM[7:0]		R/W	0x13	Initial DSM RST(reset) period. Mark (a) in operation timing diagram.: Nx16 CLK_ANA cycle max = 255*16*125ns = 0.51ms @ CLK_ANA 8MHz						

SENSOR_CH_DUMMY, TEMPS_CH_DUMMY, TESTV_CH_DUMMY, CH3_DUMMY

Address	7	6	5	4	3	2	1	0	reset
0x05	SENSOR_CH_DUMMY[7:0]								0x01

	RW								
Address	7	6	5	4	3	2	1	0	reset
0x06	TEMPS_CH_DUMMY[7:0]								0x01
	RW								
Address	7	6	5	4	3	2	1	0	reset
0x07	TESTV_CH_DUMMY[7:0]								0x01
	RW								

- **SENSOR_CH_DUMMY** : The number of data points to discard from sensor channel for stabilization and accuracy improvement.
- **TEMPS_CH_DUMMY**: The number of data points to discard from temperature sensor channel for stabilization and accuracy improvement.
- **TESTV_CH_DUMMY** : The number of data points to discard from TESTV channel for stabilization and accuracy improvement.

OPERATION CONTROL Register (ONM)

Address	7	6	5	4	3	2	1	0	reset						
0x08	OP_SEQ[3:0]				OP_MODE[1:0]		T_SOC[1:0]		0x00						
	RW				RW		RW								
Bit Field Type Reset Description															
7:4	OP_SEQ[3:0]	R/W	0x00	Control operation channels in sequence. 1: Sensor 2: Temperature sensor 3: TESTV Others are not allowed											
3:2	OP_MODE[1:0]	R/W	0x00	Control operation mode 0: Continuous(cyclic) conversion mode 1: Single conversion mode 1 2: Single conversion mode 2											
1:0	T_SOC[1:0]	R/W	0x00	SOC high duration : 1 ~ 4 CLK_ANA cycle											

Table 29 Operating Modes & Sequences

Mode Name	OP_MODE[1:0]	OP_SEQ[3:0]	Operation Sequence & Description	Comment
Continuous (Cyclic)	0 (b00)	0	(Not used)	*Based on the OP_TEMP value, the TEMP measurement cycle is determined. In other words, a measurement is taken once every OP_TEMP cycles. * OP_TEMP = 0: TEMP measurement is disabled. * OP_TEMP = 1: TEMP measurement occurs every 1 cycle. * OP_TEMP = 3: TEMP measurement occurs every 3 cycles.
		1	(OP_TEMP=0) SENSOR_CH-> SENSOR_CH-> ... (OP_TEMP=1) TEMPS_CH -> SENSOR_CH -> TEMPS_CH -> SENSOR_CH -> ...	
		2	(OP_TEMP=x) TEMPS_CH -> TEMPS_CH -> ...	
		3~15	(Not used)	
		0	(Not used)	
Single-1	1 (b01)	0	(Not used)	* After N measurements, ENB = 1. * N: register setting (example) If N = 1, perform 1 measurement and 1 SOC. If N = 4, perform 3 measurements and 4 SOCs.
		1	SENSOR_CH	
		2	TEMPS_CH	
		3	TESTV	
		4~15	(Not used)	
Mode Name	OP_MODE[1:0]	OP_SEQ[3:0]	Operation Sequence & Description	Comment
Single-2	2 (b10)	0	(Reserved)	* Perform 1 SOC and continue operation. * Analog and decimation: Continuous operation. * To turn off the operation, set START from 1 to 0.
		1	SENSOR_CH	
		2	TEMPS_CH	
		3	TESTV	
		4~15	(Reserved)	
(Reserved)	3 (b11)	-	(Reserved)	

Address	7	6	5	4	3	2	1	0	reset	
0x09	OP_TEMP[7:0]								0x00	
	RW									
Bit	Field		Type		Reset		Description			
7:0	OP_TEMP[7:0]		R/W		0x00		TEMP channel cycle			

7.6.5.1 CONTINUOUS

Once ADC conversion is completed based on the configured OSR, the DSM resets and continues data conversion. Temperature values are automatically captured at intervals specified by the OP_TEMP[7:0] register and sent to the FIFO.

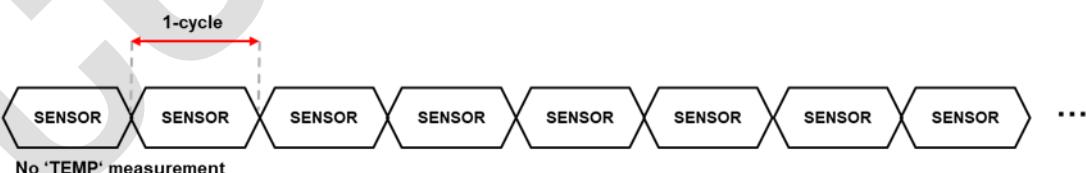


Figure 67 Operation Example-1: Continuous Mode, OP_MODE=0, OP_SEQUENCE=1, OP_TEMP=0.

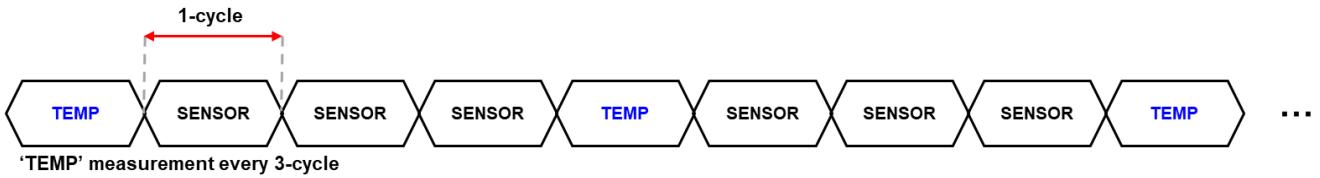


Figure 68 Operation Example-2: Continuous Mode, OP_MODE=0, OP_SEQUENCE=1, OP_TEMP=3.

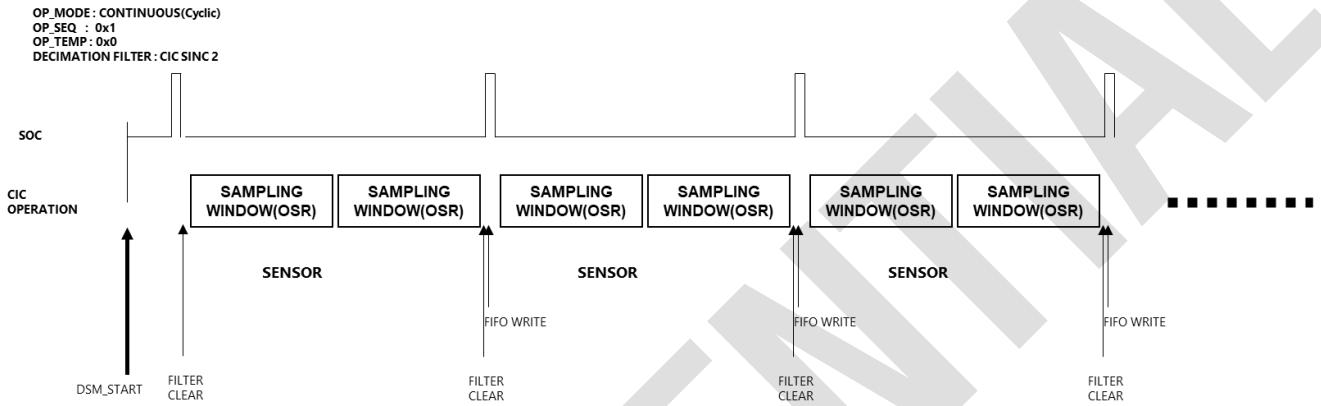


Figure 69 Operation Example: Continuous Mode, OP_MODE=0, OP_SEQ=1, OP_TEMP=0. CIC SINC2

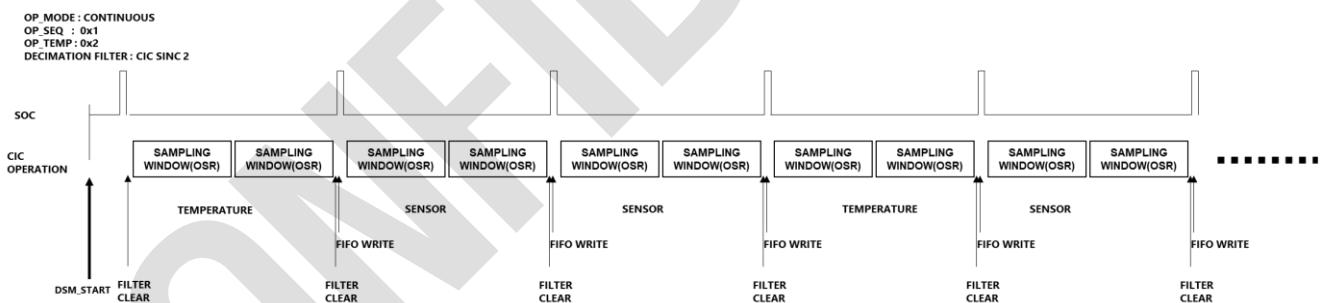


Figure 70 Operation Example: Continuous Mode, OP_MODE=0, OP_SEQ=1, OP_TEMP=2. CIC SINC2

7.6.5.2 SINGLE1

ADC conversion occurs for a specified number of times, which can be set using the SINGLE1_CNT_SEQ register. After each conversion sequence, the DSM is reset.



Figure 71 Operation Example-3: SINGLE1 Mode, OP_MODE=1, OP_SEQUENCE=1, OP_TEMP=x

Figure 72 illustrates the case where OP_MODE is set to SINGLE1, SINGLE1_CNT_SEQ[7:0] is set to '1', and SEL_STAGE[1:0] is set to '1'. In this case, one ADC conversion occurs, and the operation is completed.

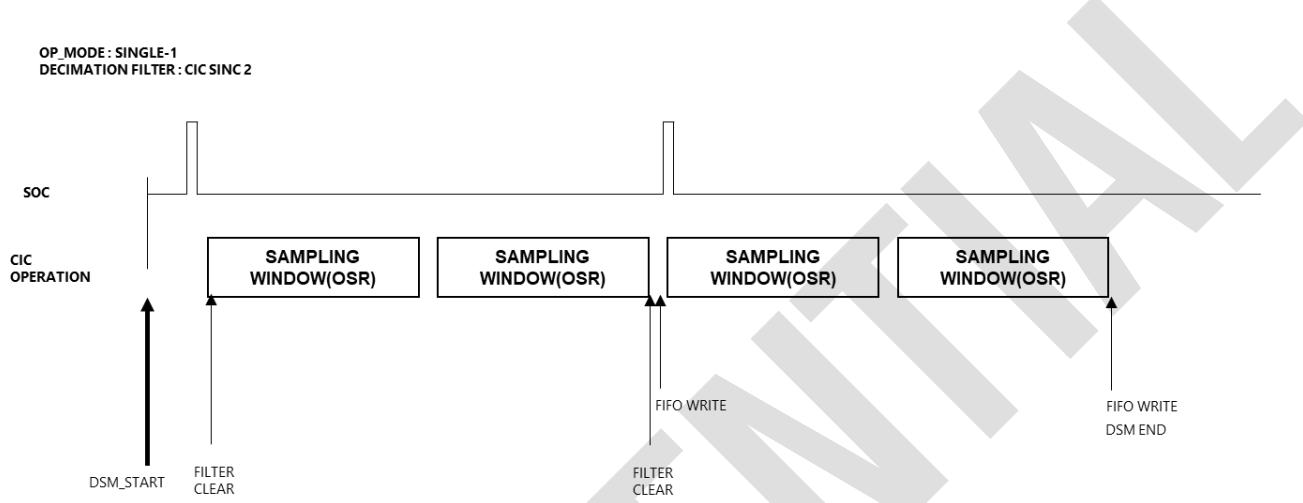


Figure 72 OPMode- SINGLE1 : A Control Timing Diagram of CIC Filter, SINGLE1_CNT_SEQ=2

Figure 72 depicts the CIC Filter timing diagram with OP_MODE set to SINGLE1 and FILTER_LATENCY set to '0'. With SINGLE1_CNT_SEQ[7:0] set to '2' and SEL_STAGE set to '1', two ADC conversions occur. Upon completion of the first operation, the DSM is reset by the SOC."

SINLGE1 MODE SEQUENCE Register (AOM)

Address	7	6	5	4	3	2	1	0	reset	
0x0A	SINGLE1_CNT_SEQ[7:0]								0x01	
	RW									
Bit	Field			Type	Reset	Description				
7:0	SINGLE1_CNT_SEQ[7:0]			R/W	0x01	SINGLE1 Mode iteration : N time measure (1 ~ 255)				

7.6.5.3 SINGLE2

SINGLE2 mode is selected by setting 0x2 in P_MODE[1:0] register.

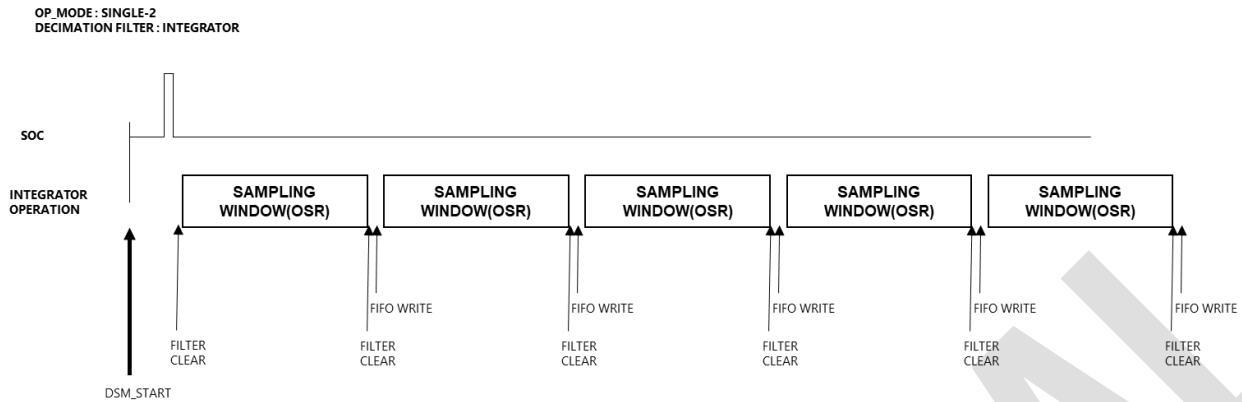


Figure 73 OPMODE- SINGLE2 : A Control Timing Diagram of Integrator Filter

Figure 73 shows the timing diagram of the integrator filter when OP_MODE is set to SINGLE2. Initially, the DSM is reset by the SOC signal, and ADC conversions occur at OSR sample intervals. If DSM is not stopped, ADC conversions will continue indefinitely.

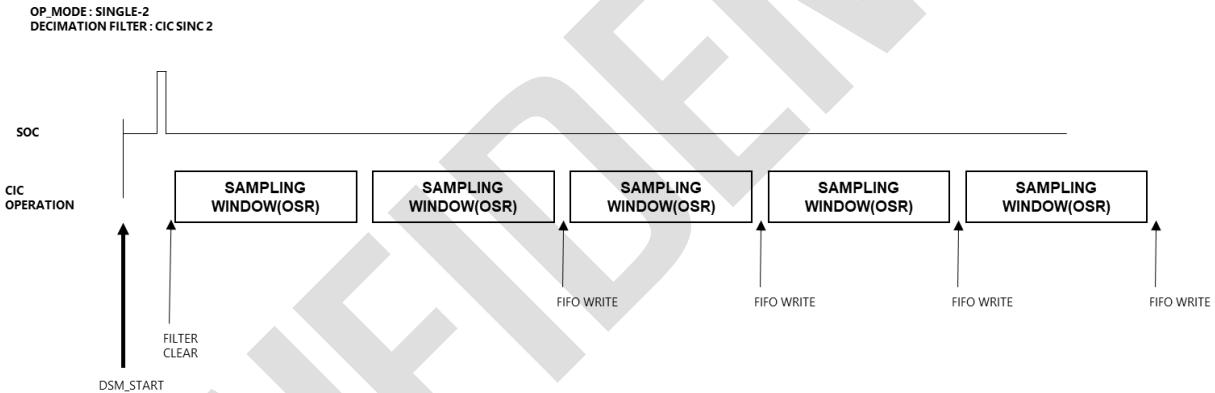


Figure 74 OPMODE- SINGLE2 : A Control Timing Diagram of CIC Filter

Figure 74 illustrates the CIC Filter timing diagram when OP_MODE is set to SINGLE2 and the FILTER_LATENCY register is set to '0'. Initially, the DSM is reset by the SOC signal, and after the initial latency, ADC conversions occur at OSR sample intervals. If DSM is not stopped, ADC conversions will continue indefinitely.

8 APPLICATION

8.1 Cyclic Voltammetry Mode

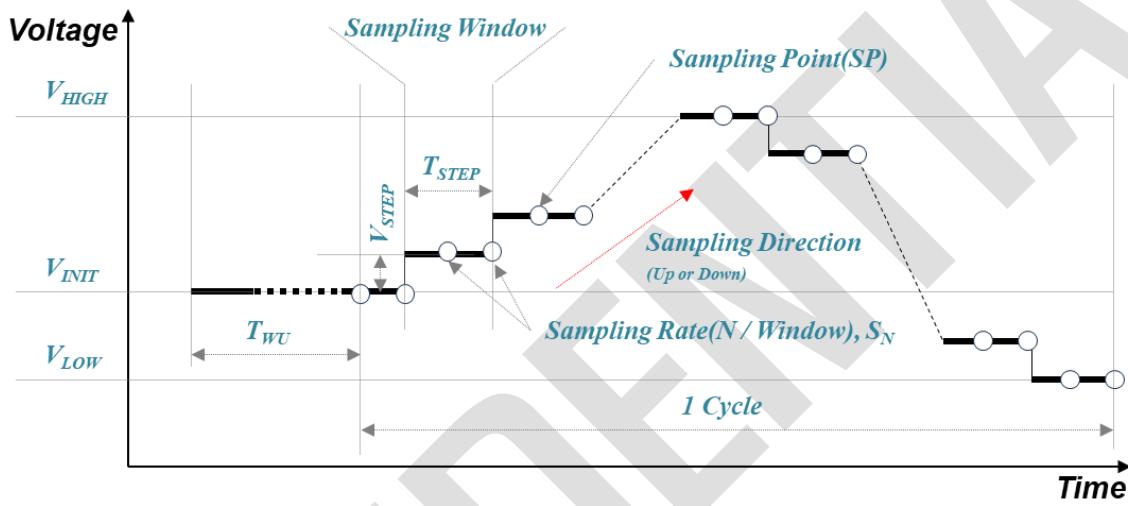


Figure 75 CV SCAN WAVE Timing Diagram

8.2 Difference Puls Voltammetry Mode

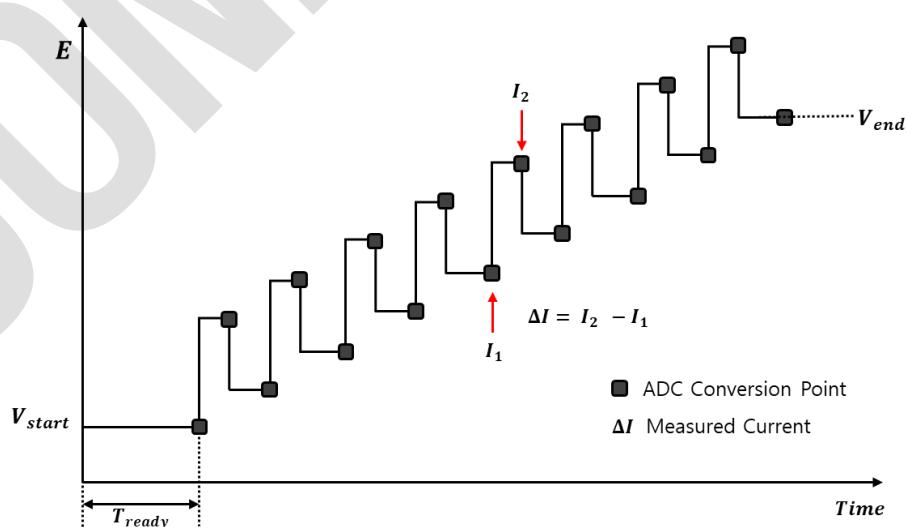


Figure 76 DPV Wave

8.3 Chronoamperometry Mode

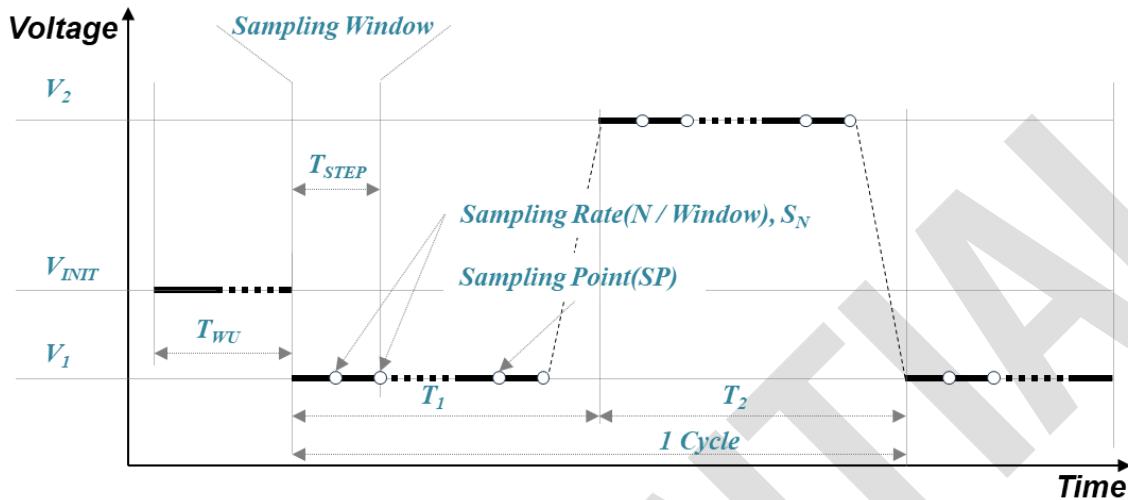


Figure 77 CA wave timing Diagram

8.4 Multistep Amperometry Mode

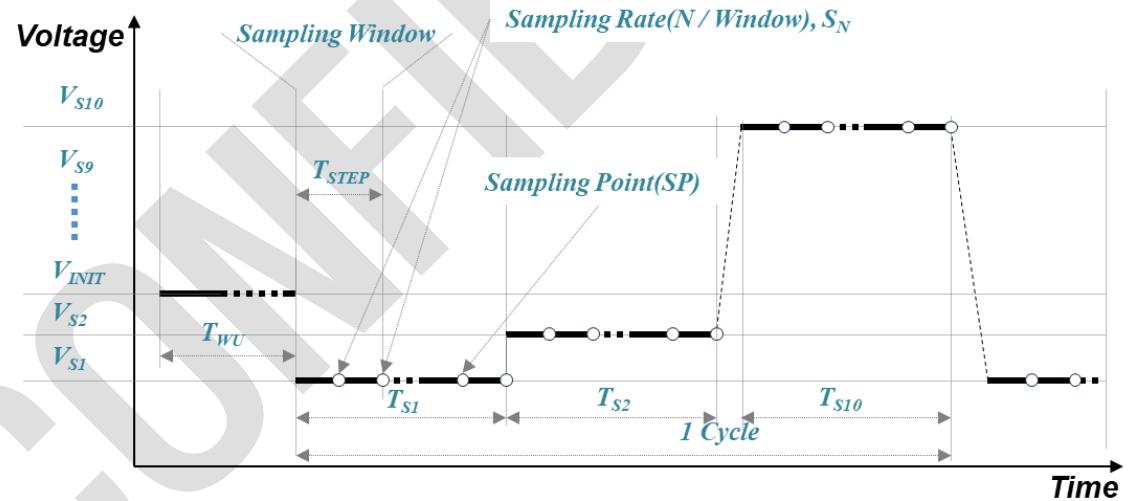


Figure 78 MA Wave Timing Diagram

9 APPENDIX

9.1 MEMORY MAP

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x00	CLK_FE_MTP	CLK_FE_FIFO2	CLK_FE_FIFO1	CLK_FE_SPI2	CLK_FE_SPI1	CLK_FE_I2C2	CLK_FE_I2C1	CLK_FE_BOOT	CLK_FE_CSR4	CLK_FE_CSR3	CLK_FE_CSR2	CLK_FE_CSR1	CLK_FE_CAL	CLK_FE_ANA	CLK_FE_DEC2	CLK_FE_DEC1	0x0000
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x01	T_RST_DSM[7:0]								-	-	-	-	-	CLK_DIV_ANA[2:0]			0x1301
	RW								-	-	-	-	-	RW			
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x02	SENSOR_CH_DUMMY[7:0]								-	-	-	-	-	-	-	-	0x0101
	RW								-	-	-	-	-	-	-	-	
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x03	TESTV_CH_DUMMY[7:0]								TEMPS_CH_DUMMY[7:0]								0x0101
	RW								RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x04	OP_TEMP[7:0]								OP_SEQ[3:0]				OP_MODE[1:0]		T_SOC[1:0]		0x0000
	RW								RW				RW		RW		

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x05	-	SEL_FLT	SEL_STAGE[1:0]	LOW_LATENCY	FILTER_LATENCY	DSM_INV	SIGN_CONV_TYPE	SINGLE1_CNT_SEQ[7:0]								0x0301	
	-	RW	RW	RW	RW	RW	RW	RW									
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x06	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0x0000	
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-		
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x07	SENSOR_CH_TRNC[4:0]					SENSOR_CH_OSR[10:8]			SENSOR_CH_OSR[7:0]								0x0000
	RW					RW			RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x08	TEMPS_CH_TRNC[4:0]					TEMPS_CH_OSR[10:8]			TEMPS_CH_OSR[7:0]								0x0000
	RW					RW			RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x09	TESTV_CH_TRNC[4:0]					TESTV_CH_OSR[10:8]			TESTV_CH_OSR[7:0]								0x0000
	RW					RW			RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x0A	SENSOR_CH_AVG_CNT[3:0]					-	SENSOR_CH_AVG_TRNC[2:0]			-	-	-	-	-	-	-	0x0000
	RW					-	RW			-	-	-	-	-	-	-	
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x0B	TESTV_CH_AVG_CNT[3:0]					-	TESTV_CH_AVG_TRNC[2:0]			TEMPS_CH_AVG_CNT[3:0]				-	TEMPS_CH_AVG_TRNC[2:0]		0x0000
	RW					-	RW			RW				-	RW		
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x0C	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0x0000
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x0D	SENSOR_CH_OFS[15:8]								SENSOR_CH_OFS[7:0]								0x0000
	RW								RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x0E	TEMPS_CH_OFS[15:8]								TEMPS_CH_OFS[7:0]								0x0000
	RW								RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x0F	TESTV_CH_OFS[15:8]								TESTV_CH_OFS[7:0]								0x0000
	RW								RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0x0000
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x11	-	-	SENSOR_CH_GAIN_FRC[13:8]						SENSOR_CH_GAIN_FRC[7:0]								0x0000
	-	-	RW						RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x12	-	-	TEMPS_CH_GAIN_FRC[13:8]						TEMPS_CH_GAIN_FRC[7:0]								0x0000
	-	-	RW						RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x13	-	-	TESTV_CH_GAIN_FRC[13:8]						TESTV_CH_GAIN_FRC[7:0]								0x0000
	-	-	RW						RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x14	TESTV_CH_GAIN_INT[3:0]				TEMPS_CH_GAIN_INT[3:0]				SENSOR_CH_GAIN_INT[3:0]				-	-	-	-	0x1111
	RW				RW				RW				-	-	-	-	

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x15	-	-	CAL_T0_FRC[13:8]						CAL_T0_FRC[7:0]								0x0000
	-	-	RW						RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x16	-	-	CAL_T_FRC[13:8]						CAL_T_FRC[7:0]								0x0000
	-	-	RW						RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x17	-	-	CAL_TCO_FRC[13:8]						CAL_TCO_FRC[7:0]								0x0000
	-	-	RW						RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x18	-	-	CAL_TCG_FRC[13:8]						CAL_TCG_FRC[7:0]								0x0000
	-	-	RW						RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x19	CAL_TCG_INT[3:0]				CAL_TCO_INT[3:0]				CAL_T_INT[3:0]				CAL_T0_INT[3:0]				0x1111
	RW				RW				RW				RW				
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x1A	-	-	-	-	-	-	-	-	-	-	-	CAL_INTEGER_PTR[5:0]					0x0004
	-	-	-	-	-	-	-	-	-	-	-	RW					
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x1B	-	-	TEMPS_CH_TRNC_PP[5:0]						-	-	SENSOR_CH_TRNC_PP[5:0]						0x0000
	-	-	RW						-	-	RW						
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x1C	FIFO_SET_CNT_SEQ[2:0]			FIFO_FORMAT[2:0]			FIFO_MODE[1:0]		GAIN_MODE		-	TESTV_CH_TRNC_PP[5:0]					0x0000
	RW			RW			RW		RW		-	RW					

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x1D	-	TEST_POWER_EN	FAST_EP_EN	E32B_EN	SEL_INT[1:0]		INT_EN	INT_POL	-	-	FIFO_PTR_HALF_FULL[3:0]			FIFO_CLEAR	FIFO_DATA_SIZE	0x001C	
	-	RW	RW	RW	RW		RW	RW	-	-	RW			RW	RW		
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x1E	-	-	BACKUP_EN	PWR_DN	TIMER_RST	TIMER_STOP	MODE[1:0]		-	-	-	-	-	-	CLK_FE_RST	CLK_FE_AON	0x0000
	-	-	RW	RW	RW	RW	RW		-	-	-	-	-	-	RW	RW	
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x1F	WAKEUP_PRD[15:8]								WAKEUP_PRD[7:0]								0xBBA0
	RW								RW								
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x20	NUM_CMD_WAIT[1:0]		NUM_CLK_WAIT[1:0]		NUM_RD_WAIT[1:0]		SPI_SEL_FE	I2C_SEL_FE	-	-	WAKEUP_PRD[21:16]					0x540D	
	RW		RW		RW		RW	RW	-	-	RW						
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x21	-	-	-	-	ENB_TESTV	ENB_TEMPS	ENB_DSM	ENB_MUXBUF	-	CUR_TEMPS	CUR_MUXBUF[1:0]		CUR_DSM_VADC_BUF[1:0]	CUR_DSM[1:0]		0x0F2A	
	-	-	-	-	RW	RW	RW	RW	-	RW	RW		RW	RW			
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x22	-	-	DSM_GM1_CTRL[1:0]		DSM_GAIN[1:0]		DSM_BUFI[1:0]		DSM_REFI[1:0]		DSM_DSMI[1:0]		DSM_BYP_VREF	SEL_DUTY_R[2:0]			0x2150
	-	-	RW		RW		RW		RW		RW		RW	RW			
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x23	-	-	-	DEM_ST_POINT[4:0]					-	DEM_MODE[2:0]			CLK_CMP_WIDTH[3:0]				0x0022
	-	-	-	RW					-	RW			RW				
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x24	DSM_CHOP_POSITION[7:0]								SET_FOS_CLKN[7:0]								0x0005
	RW								RW								

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x25	-	-	-	SEL_DSM_DV[4:0]					-	-	-	-	-	-	-	SEL_DSM_CHOP	0x1701	
	-	-	-	RW					-	-	-	-	-	-	-	RW		
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x26	-	-	-	TESTV_DV[4:0]					-	-	-	SEL_DSM_VOCM[1:0]	SEL_DSM_BGR[1:0]	SEL_PSEUDO_R	0x0800			
	-	-	-	RW					-	-	-	RW			RW			
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x27	-	-	TEMPS_DEM_MODE[1:0]		TEMPS_DEM_N1[3:0]					-	-	-	TESTV_VREF[4:0]					0x3010
	-	-	RW		RW					-	-	-	RW					
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x28	TRIM_BGR_A_I[7:0]								TRIM_BGR_A_V[7:0]								0x0000	
	RW								RW									
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x29	TRIM_BGR_D_I[7:0]								TRIM_BGR_D_V[7:0]								0x0000	
	RW								RW									
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x2A	TRIM_LFOSC1_32K[7:0]								STB_SEL_LDO_DONO	STB_SEL_LDO_DAON	STB_SEL_LDO_A	BYPASS_LDO_DONO	BYPASS_LDO_DAON	BYPASS_LDO_A	BGR_D_EXT_V_MODE	BGR_A_EXT_V_MODE	0x0000	
	RW								RW	RW	RW	RW	RW	RW	RW	RW		
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x2B	-	-	-	-	-	ENB_LDODONO	ENB_LDOA	ENB_BGR_A	-	-	-	-	CUR_TIA_VDRV[3:0]				0x0005	
	-	-	-	-	-	RW		RW	RW	-	-	-	RW					
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x2C	-	-	-	-	-	ENB_LFOSC1_32K	ENB_TIA1	ENB_TIA0	ENB_VDRV1	ENB_VDRV0	ENB_TIA_VDRV_BIAS	ENB_DAC	ENB_ACTRL	ENB_BIAS_GLOBAL	0x01FF			
	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW	RW	RW			

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x2D	SEL_R1[4:0]					SEL_RS2[2:0]			-	-	SEL_RS1[2:0]			SEL_RG[2:0]			0x0000	
	RW					RW			-	-	RW			RW				
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x2E	SEL_SENSR[2:0]			LPF_R[1:0]		SEL_C2[2:0]			SEL_C1[2:0]			SEL_R2[4:0]					0x2120	
	RW			RW		RW			RW			RW						
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x2F	-	-	-	-	DAC3_VBIAS[11:8]				DAC3_VBIAS[7:0]								0x0000	
	-	-	-	-	RW				RW									
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x30	-	-	DAC2_VZERO_1[5:0]					-	-	DAC1_VZERO_0[5:0]					RW			0x0000
	-	-	RW					-	-	RW					RW			
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x31	CSW34	CSW33	CSW32	CSW31	CSW21_22	CSW18	CSW17	CSW16	CSW15	CSW14	CSW13	CSW12	CSW11	CSW82	CSW81	CSW91_92	0x0000	
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x32	-	-	-	-	-	CSW51_52	CSW48	CSW47	CSW46	CSW45	CSW44	CSW43	CSW42	CSW41	CSW37_38	CSW35_36	0x0000	
	-	-	-	-	-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x33	CSW142	CSW141	CSW132	CSW131	CSW126	CSW125	CSW124	CSW123	CSW122	CSW121	CSW116	CSW115	CSW114	CSW113	CSW112	CSW111	0x0000	
	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset	
0x34	-	-	-	CSW181_182	CSW196	CSW195	CSW194	CSW193	-	-	CSW192	CSW191	CSW146	CSW145	CSW144	CSW143	0x0000	
	-	-	-	RW	RW	RW	RW	RW	-	-	RW	RW	RW	RW	RW	RW		

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	reset
0x35	-	TIA1_BST_ACT	TIA1_BST[1:0]	-	TIA0_BST_ACT	TIA0_BST[1:0]	-	VDRV1_BST_ACT	VDRV1_BST[1:0]	-	VDRV0_BST_ACT	VDRV0_BST[1:0]	0x0000				
	-	RW	RW	-	RW	RW	-	RW	RW	-	RW	RW		RW	RW		