FAET630004: AI-Core and RISC Architecture **(Due: 5/7/20)**

Homework Assignment #2

Instructor: Chixiao Chen *Name:* , *FudanID:*

- This HW counts 15% of your final score, please treat it carefully.
- Please submit the electronic copy via mail: faet_english@126.com before 03/23/2019 11:59pm.
- It is encouraged to use LaTeX to edit it, the source code of the assignment is available via: https://www.overleaf.com/read/qnqfpcmqvchp
- You can also open it by Office Word, and save it as a .doc file for easy editing. Also, you can print it out, complete it and scan it by your cellphone.
- The assignment needs verilog/SV simulation. It is suggested to use Vivado from Xilinx to complete the simulation. If you do not want to install a local verilog simulator, please use an online tool: https://www.edaplayground.com/, you need register for save.
- You can answer the assignment either in Chinese or English

Problem 1: Implement a matrix multiplier on a RISC Core

(8+7=15 points)

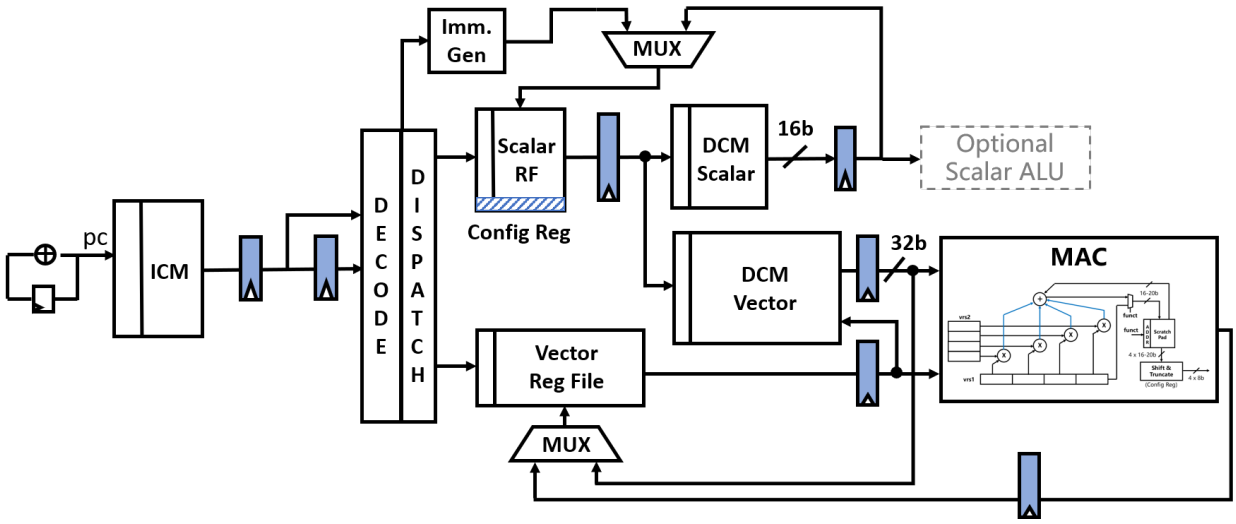
Using the following ISA and hardware architecture to compute $\mathbf{A} \cdot \mathbf{B} + \mathbf{C}$, where $\mathbf{A}$, $\mathbf{B}$ and $\mathbf{C}$ are 8×8 matrices. Each element in them are signed integers with 8b length.

Base: Scalar Instruction

```
LOAD    rd  ,  rs    , imm5b
Store   /   ,  rs1   , rs2
MOV     rd  ,  imm8b , funct1b
```

Extension: Vector Instruction

```
Vload   vrd3b , rs    , imm5b
Vstore  imm5b , rs    , vrs3b
VMAC    vrd3b , vrs13b , vrs23b , funct4b
```



(a) Write the entire assembly code for computation. (hints: 8 indexed vector register file is not sufficient for 8x8 matrix.)

(b) Propose a superscalar strategy (maximum 2 instruction per fetch), and calculate how many cycles needed. Compare the utilization ratio with and without the superscalar strategy.