FAET630004: AI-Core and RISC Architecture **(Due: 4/2/20)**

Homework Assignment #1

Instructor: Chixiao Chen *Name:* , *FudanID:*

- This HW counts 15% of your final score, please treat it carefully.
- Please submit the electronic copy via mail: faet_english@126.com before 03/23/2019 11:59pm.
- It is encouraged to use LaTeX to edit it, the source code of the assignment is available via: https://www.overleaf.com/read/gmxszwbypznk
- You can also open it by Office Word, and save it as a .doc file for easy editing. Also, you can print it out, complete it and scan it by your cellphone.
- The assignment needs verilog/SV simulation. It is suggested to use Vivado from Xilinx to complete the simulation. If you do not want to install a local verilog simulator, please use an online tool: https://www.edaplayground.com/, you need register for save.
- For students who prefer C rather than Verilog, a C-based hardware description method is also recommended. It is called high level synthesis (HLS) supported by Vivado as well. A HLS tutorial can be found via: https://www.bilibili.com/video/BV11b411e7m3. Also, an HLS example of RISC RISC is available by: https://gitlab.cs.washington.edu/cse599s/hls-tutorials/tree/master/part3.
- You can answer the assignment either in Chinese or English

Problem 1: Implement a simple RISC Core

(2+5+8=15 points)

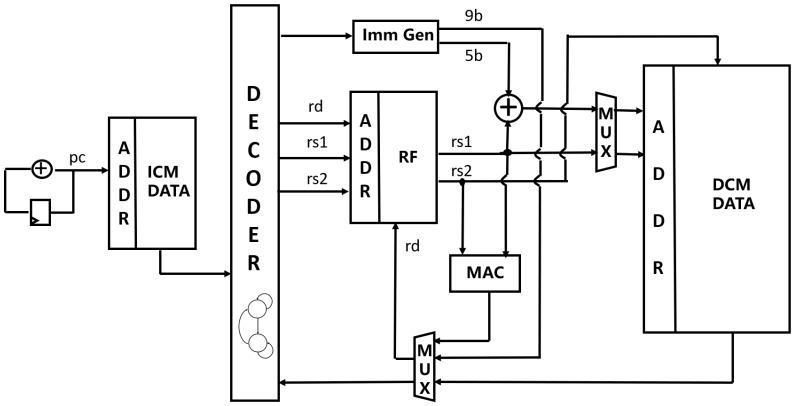
On class, we define an extremely simple RISC ISA and its hardware organization, which are both shown below. For this homework assignment, we need to design/implement/simulate this core.

极简指令集（RISC）Load/Store 架构			
opcode	目标 Reg	源寄存器/立即数	说明
Load	rd	rs+imm(5b)	//在 rst imm 地址→rd
Store	/	rs(地址)/rs(DATA)	//rs(DAI)→Mem index =rs(地址)
MOV	rd	imm(9b)	//赋值→rd
MAC	rd rd	rs1,rs2,funct=0 rs1,/,funct=1	//乘加 //初始赋值清除

(a) Which HDL you want to use ?

(b) For Verilog-players, please write an top-level structural verilog file to decribe the system.
For C-players, please complete a header filer and .cc file , compatible to Vivado HLS, to describe the system.
(Hint: Plz submit your script as well)

(c) For Verilog-players, please write an testbench verilog file to simulate the system. It should complete a



4-MAC (neuron) computing.
For C-players, please complete a _test.cc file , compatible to Vivado HLS, to simulate the system. It should complete a 4-MAC (neuron) computing.
(Hint: Plz submit your script and simulated waveform, highlight the final results and compare it with the theoretical value.)