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3D-TTP: Efficient Transient Temperature-Aware Power Budgeting for 3D-Stacked Processor-Memory Systems

Sobhan Niknam*,Yixian Shen*, Anuj Pathania, Andy D Pimentel

Parallel Computing Systems

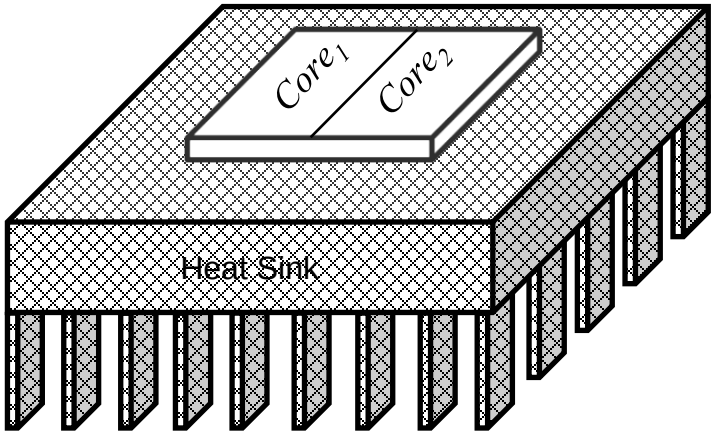
Universiteit van Amsterdam

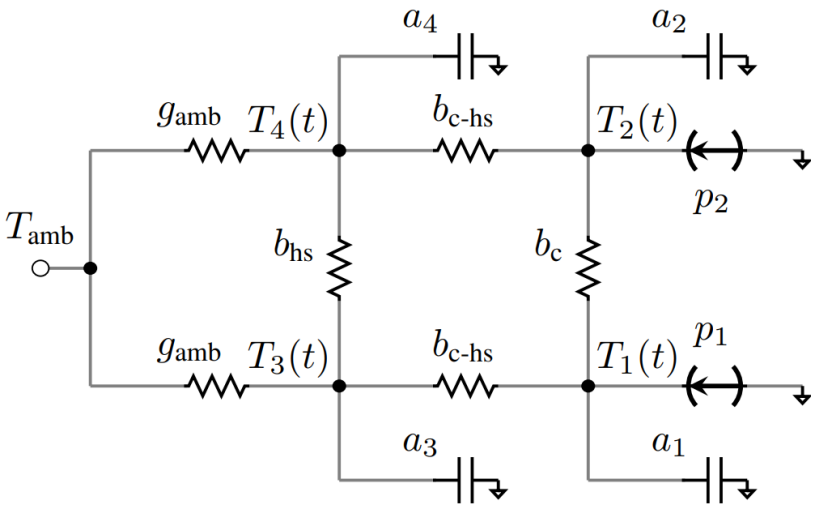
Outline

- ***Research background***
- Dynamic Thermal management
- The key designs of our approach
- Experimental results
- Conclusion

R-C thermal model

- Thermal behavior is dual to electronic circuit.





R-C thermal model

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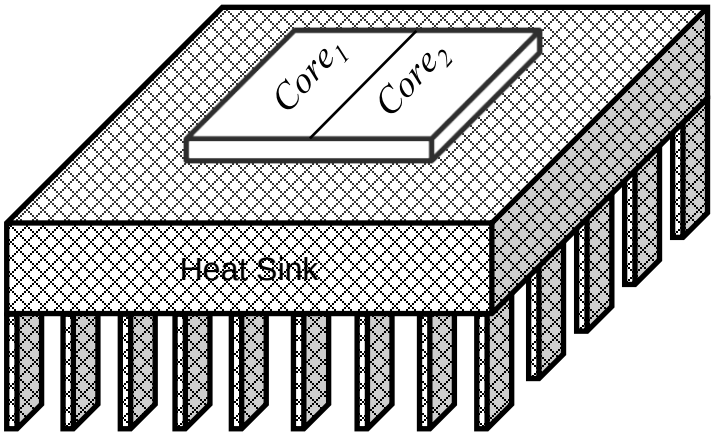
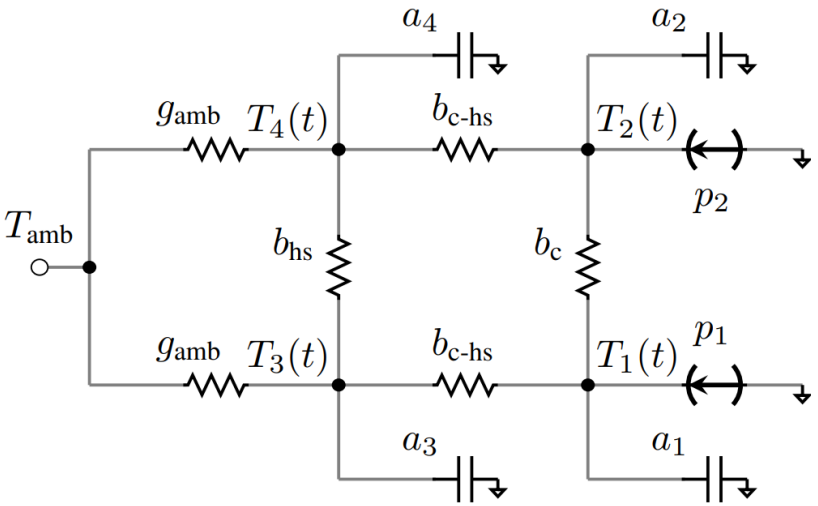
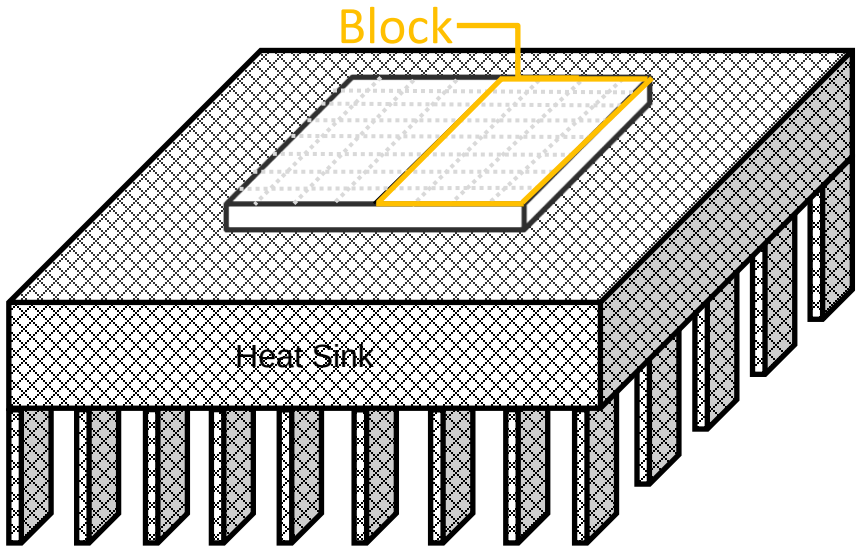




$$\mathbf{A}\mathbf{T}' + \mathbf{B}\mathbf{T} = \mathbf{P} + T_{\text{amb}}\mathbf{G}$$

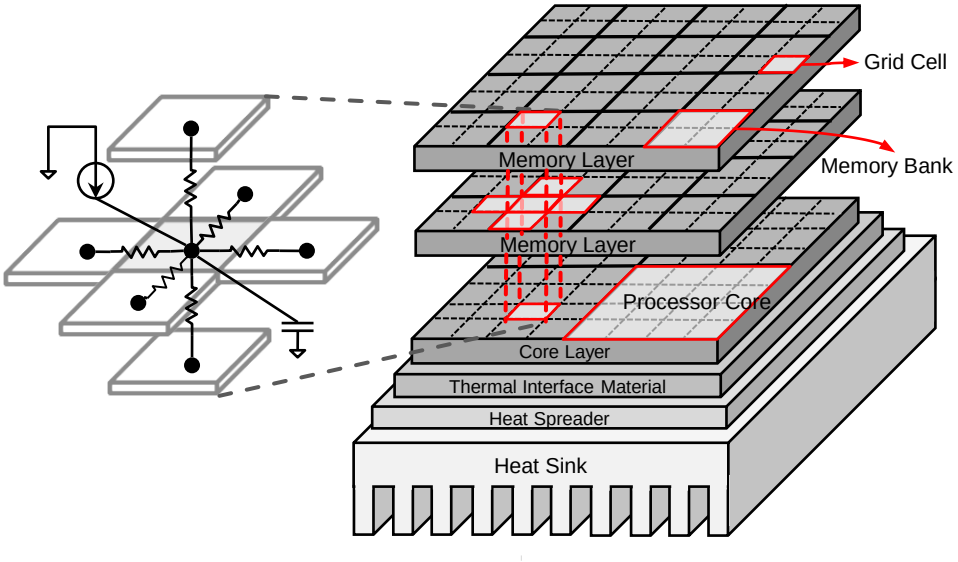
Block Mode vs Grid Mode in HotSpot

- Block Mode: Thermal resistance and specific heat of each layer (i.e., silicon, TIM, package) is uniform.



3D-stacked Processors

- Core and Memory stacked together



- Through-Silicon Vias (TSVs) are composed of uniform material
- Non-uniform Thermal Conducting Sheets

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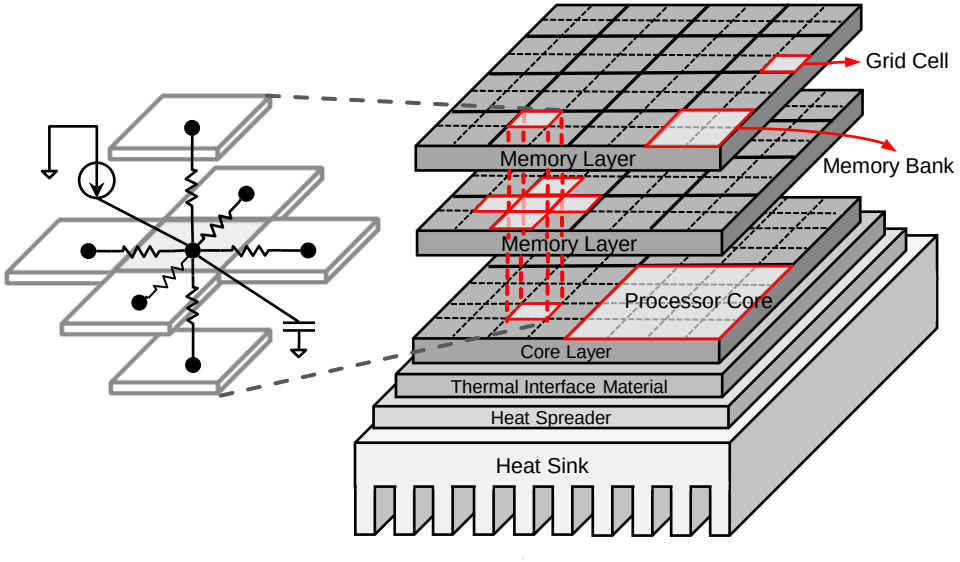
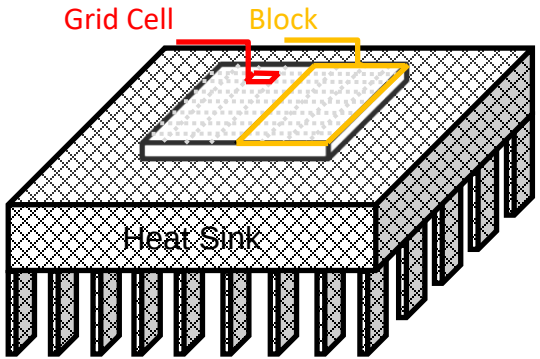
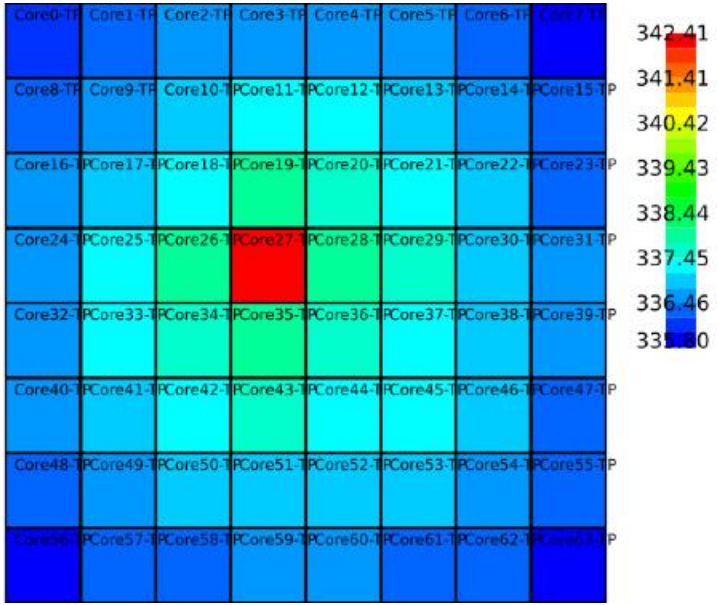


- Through-Silicon Vias (TSVs) are composed of uniform material
- Non-uniform Thermal Conducting Sheets

3D-stacked processors require the grid model for thermal modelling.

Block Mode vs Grid Mode in HotSpot





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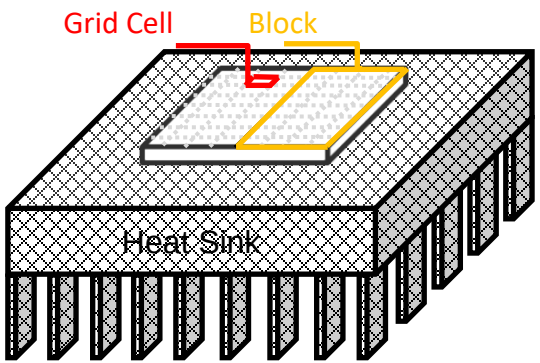
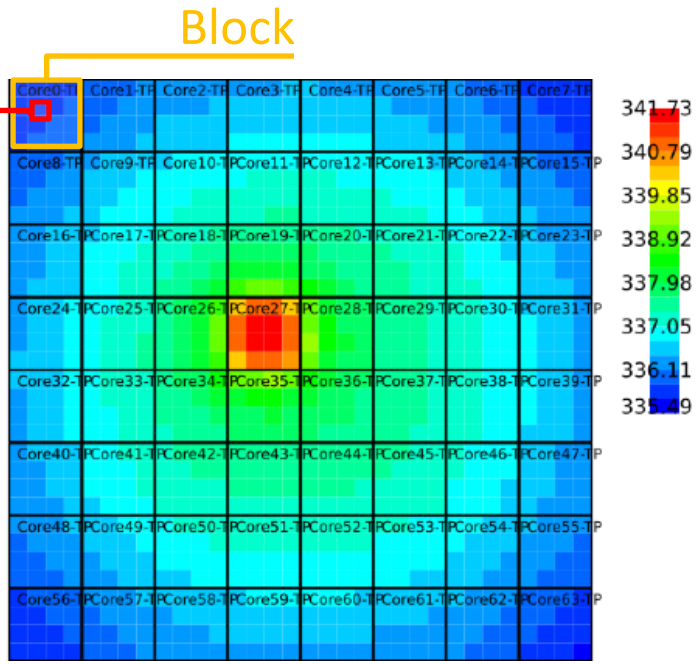
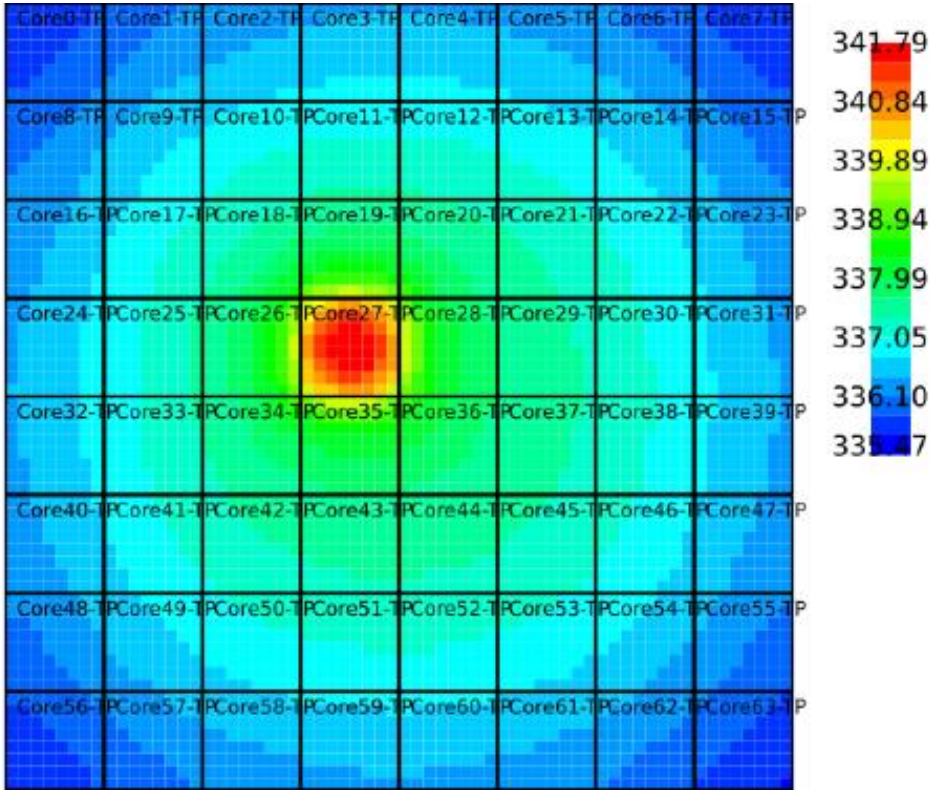


N_g=16



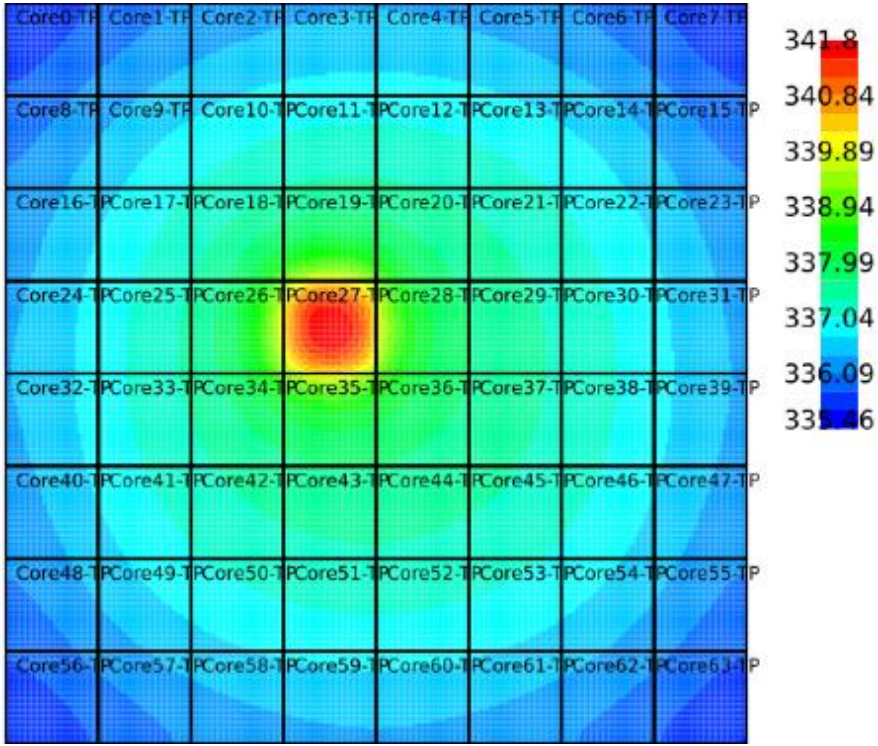
Block Mode vs Grid Mode in HotSpot

N_g=64



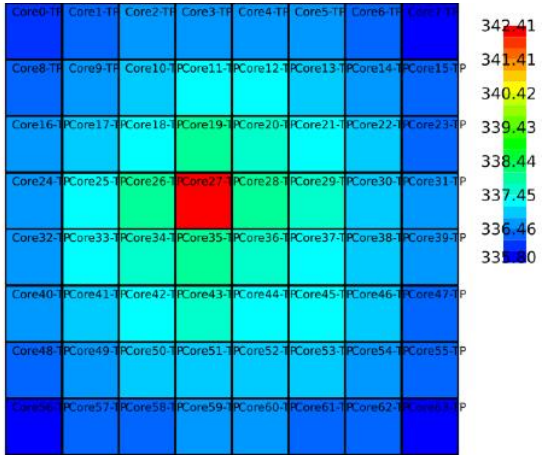
Block Mode vs Grid Mode in HotSpot

N_g=256

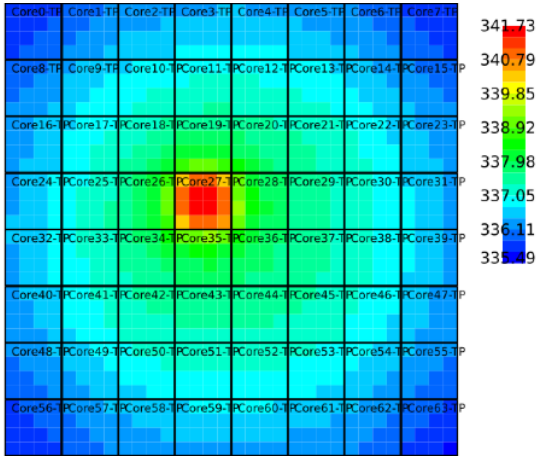


Block Mode vs Grid Mode in HotSpot

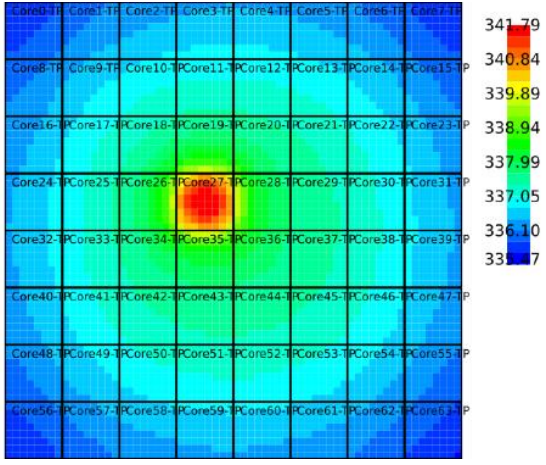
N_g=1



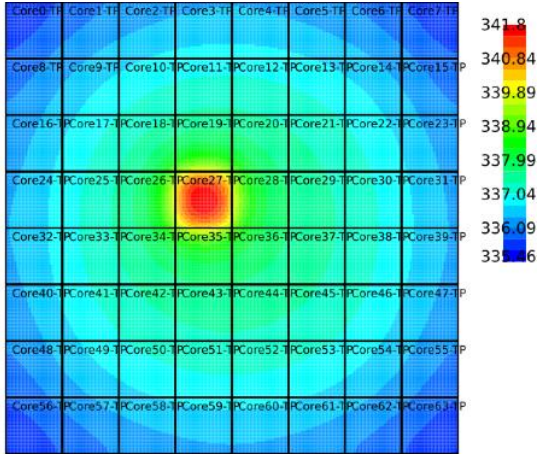
N_g=16



N_g=64



N_g=256



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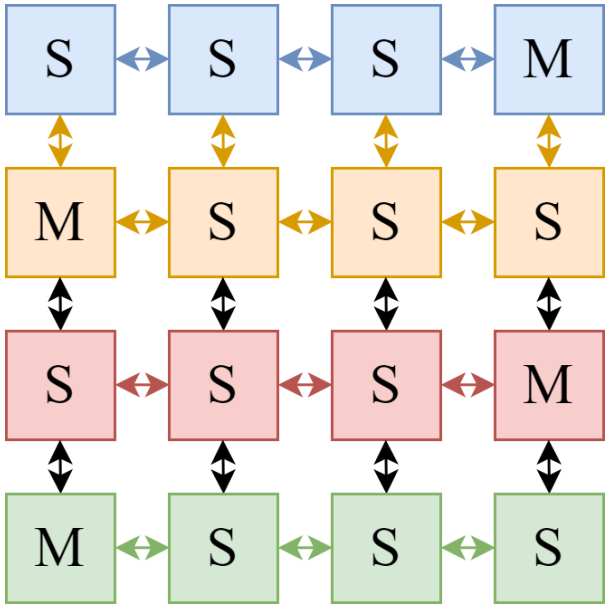
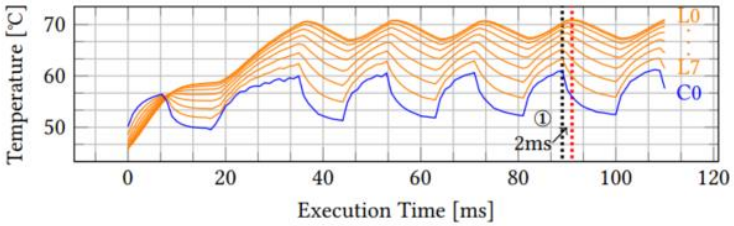
A motivational example

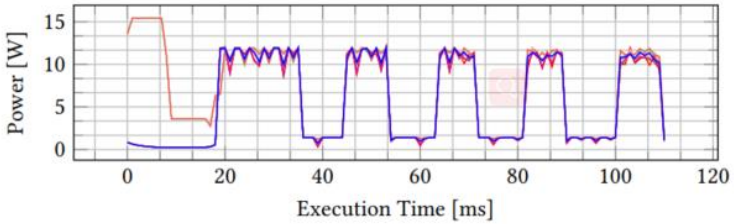
- Experimental platform: simulated 9-layer 16-core 3D-stacked system
- Experimental configuration
- Thermal threshold 70(℃)



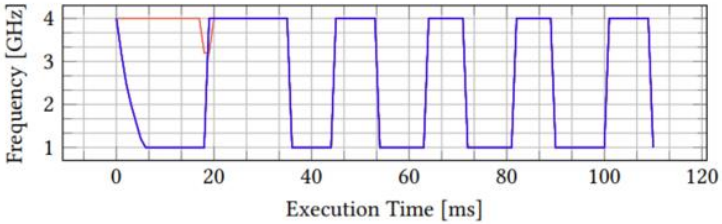
A motivational example



(a) Peak Temperature per Layer



(b) Power Consumption per Core



(c) Frequency per Core

- DTM Passively reduces the frequency of cores
- Thermal transfer takes time from the bottom layer to the top layer

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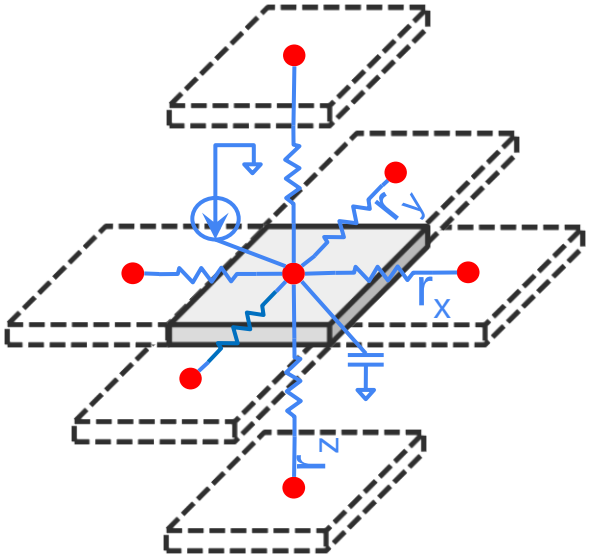
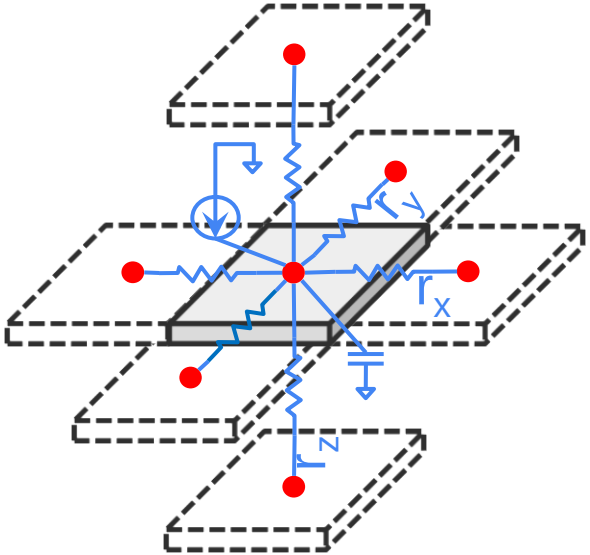
Grid Model Challenges in Power Budgeting



$$\mathbf{A}\mathbf{T}' + \mathbf{B}\mathbf{T} = \mathbf{P} + T_{\text{amb}}\mathbf{G}$$

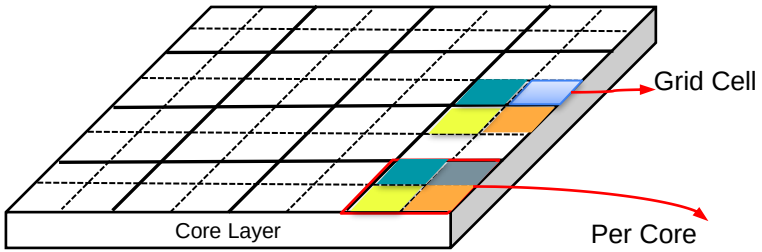
- The data structure of block model is not applicable
- DVFS operates per-core, not per-grid

Power Budgeting Solutions for 3D-stacked Processors.



- Establish a data structure to track **per-grid-node thermal RC values** instead of per-layer RC
- Ingest per-block thermal resistance, specific heat conductance, and geometric data from the .flp file
- Calculate per-grid-node thermal RC based on the provided block-level thermal properties
- Solve the **heterogeneous** RC network

Power Budgeting Solutions for 3D Processors.



- New data structure for tracking **per-grid-node thermal RC values**

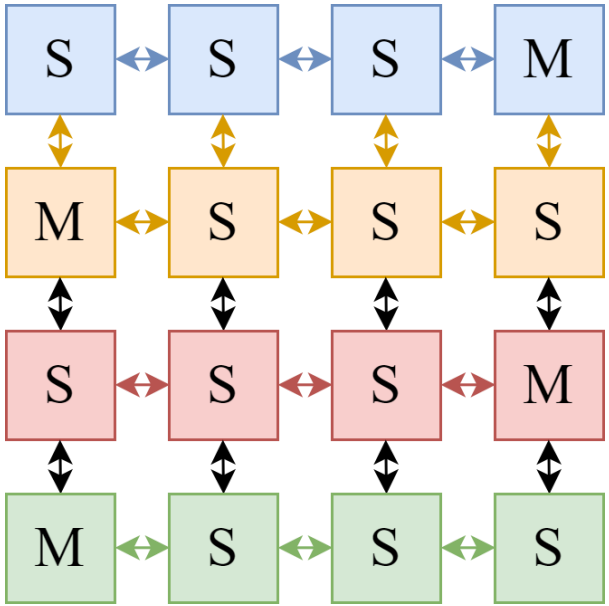
$$\mathbf{AT'_g + BT_g = P_g + } T_{amb}\mathbf{G}$$

- All grid nodes belonged to a certain block should have the same power budget

$$\mathbf{P_g = Occupancy \times P_b}$$

Case Study

- Experimental platform: simulated 9-layer 16-core 3D-stacked system
- Experimental configuration
- Thermal threshold 70(℃)



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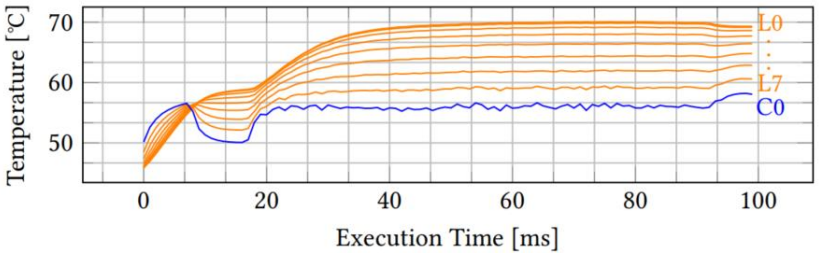

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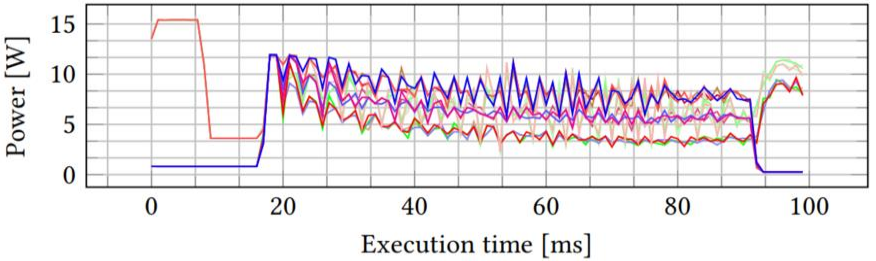
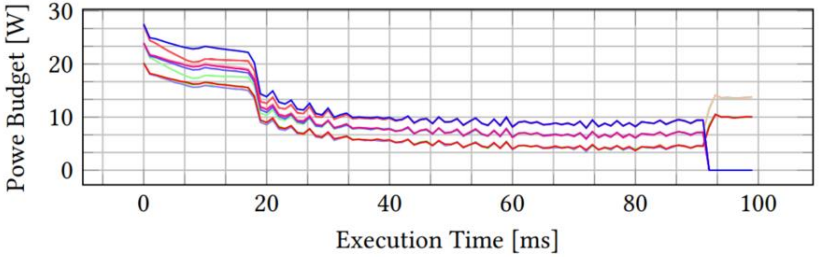
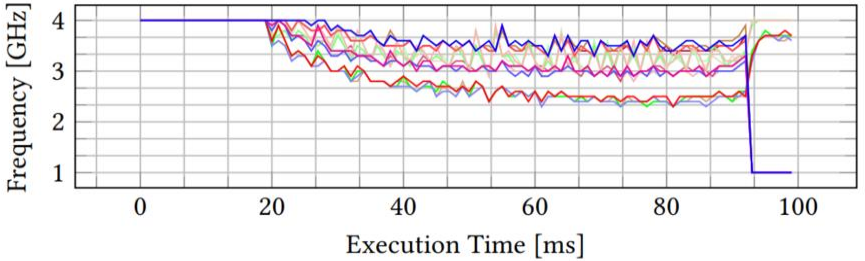


(c) Power Consumption per Core

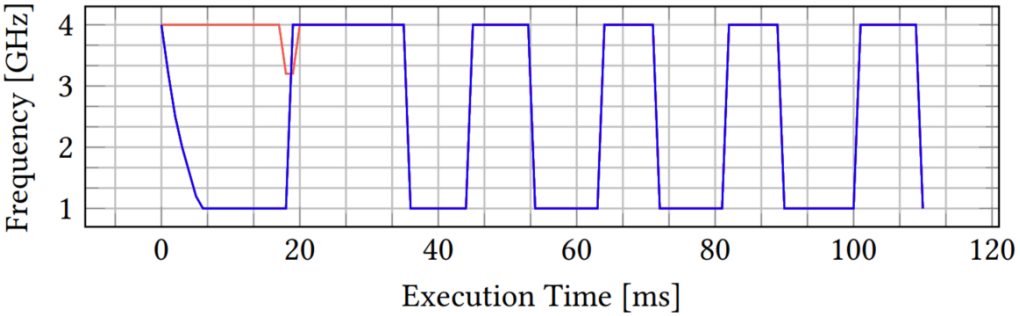


(b) Power Budget per Core

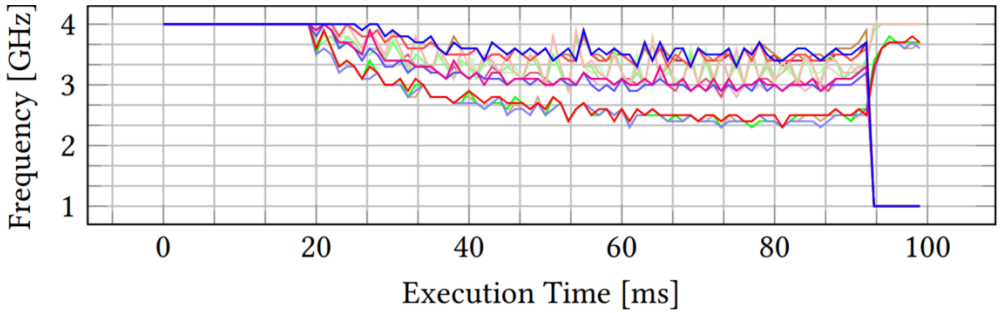


(d) Frequency per Core

Case Study



(c) Frequency per Core



(d) Frequency per Core

- 10% faster due to less performance loss compared with DTM

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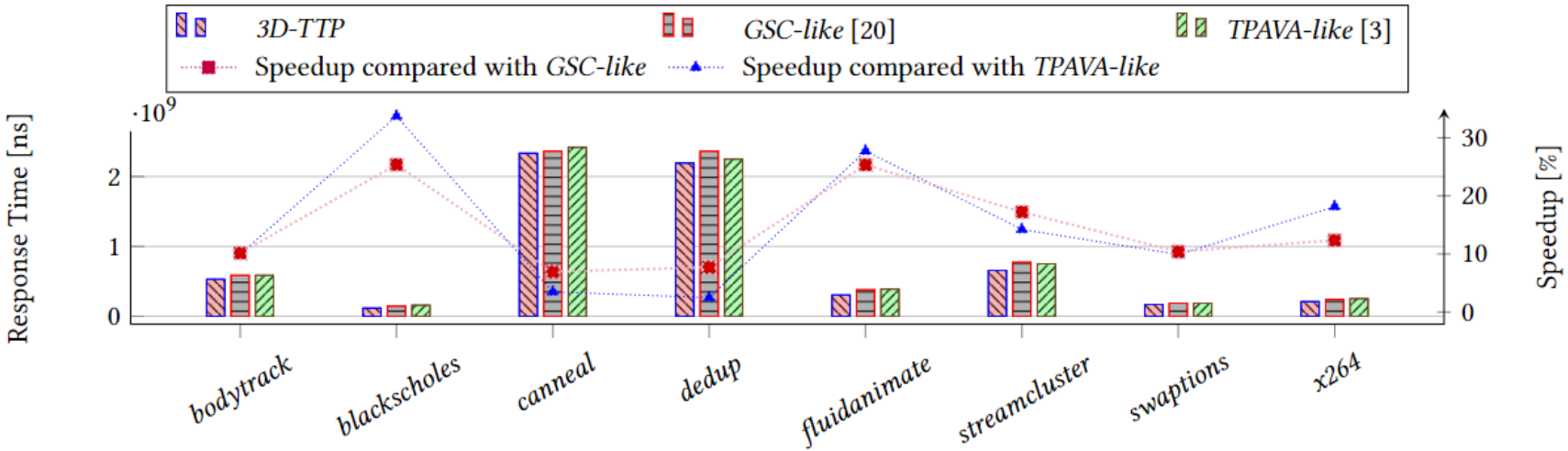
The experimental configuration

Table 1: Parameters for the simulated 3D-stacked system.

Core Parameters	
Number of Cores	16, 1 layer
Core Model	x86, 4.0 GHz, 22 nm, out-of-order
Core Area	2.89 mm^2
L1 I/D cache	32/32 KB, 4/4-way,64 B block
L2 cache	private,512 KB, 8-way, 64 B block
L3 cache	512 KB, 16-way, 64B-block
Memory Parameters	
3D-stacked Memory	8 G, 8 layers, 16 channels, 128 banks
Memory Bank Area	2.89 mm^2
Memory Bandwidth	25.6 GB/s

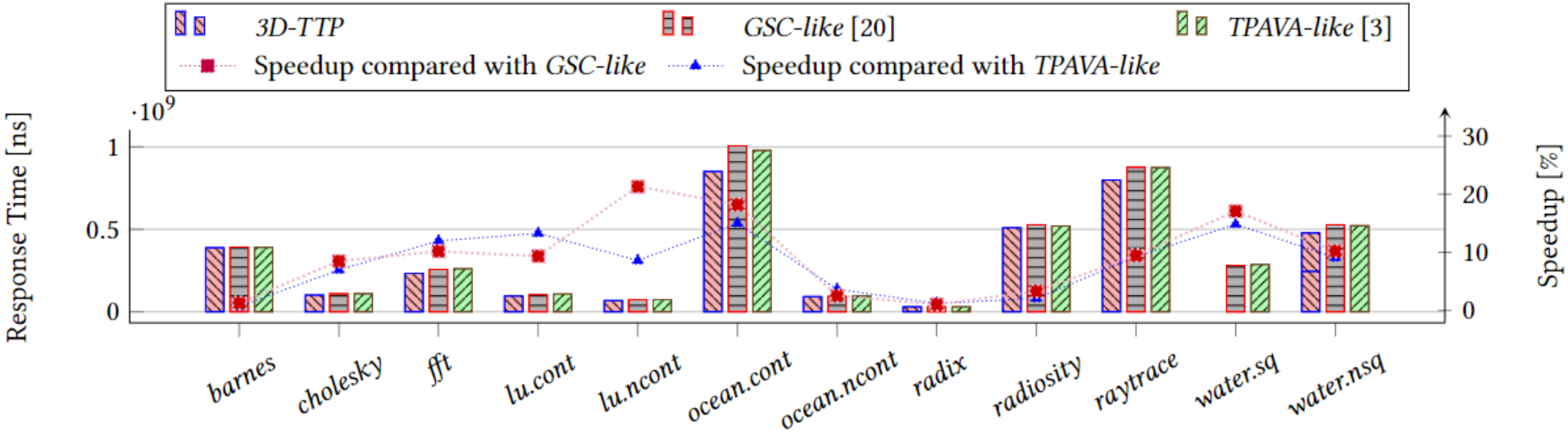
The experimental results

- Comparison on PARSEC benchmark suite



The experimental results

- Comparison on SPLASH-2 benchmark suite



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The conclusion.

- Developed ***a linear algebra-based method*** for power budgeting in 3D systems.
- Introduced ***a transient temperature-aware power budgeting*** technique.
- Employed ***a grid-level RC-thermal model*** for accurate power budgeting in 3D systems.
- Integrated and evaluated 3D-TTP with the CoMeT thermal simulator using SPLASH and PARSEC benchmarks.

Thanks for your attention

y.shen@uva.nl

Questions