2021秋 数字逻辑与部件设计

Lab1说明文档

朱奕新19307090029

设计思路

程序的思路如下：

- 运用两个四位的输入，计算出一个八位的结果。
- 取此结果的低四位，转化为七位二进制码。
- 用约束文件绑定变量与实验板部件。

设计方法

以下列出了本程序实现的主要部分，完整的可运行的实现请见实际代码。

- 各个变量的声明

```
    output reg[6:0] r;
    output reg[3:0] AN;
    reg[7:0] F;
    input[3:0] A,B;
    input[1:0] op;
```

- 计算八位结果F，直接使用数据流建模的方法算出结果

```
always@(A,B,op)
begin
    AN = 4'b1110;
    case(op)
        2'b00:  F = A + B;
        2'b01:  F = A - B;
        2'b10:  F =  ~ A ;
        2'b11:  F = A * B;
    endcase
end
```

- 取此结果的低四位，转化为七位二进制码

```
always@(F)
begin
    case (F[3:0])
        4'h0: r = 7'b1000000;
```

```
        4'h1: r = 7'b1111001;
        4'h2: r = 7'b0100100;
        4'h3: r = 7'b0110000;
        4'h4: r = 7'b0011001;
        4'h5: r = 7'b0010010;
        4'h6: r = 7'b0000010;
        4'h7: r = 7'b1111000;
        4'h8: r = 7'b0000000;
        4'h9: r = 7'b0010000;
        4'hA: r = 7'b0001000;
        4'hB: r = 7'b0000011;
        4'hC : r = 7'b1000110;
        4'hD: r = 7'b0100001;
        4'hE: r = 7'b0000110;
        4'hF : r = 7'b0001110;
        default: r = 7'b1000000;
    endcase
 end
```

- 约束文件

```
set_property PACKAGE_PIN R15 [get_ports {A[3]}]
set_property PACKAGE_PIN M13 [get_ports {A[2]}]
set_property PACKAGE_PIN L16 [get_ports {A[1]}]
set_property PACKAGE_PIN J15 [get_ports {A[0]}]
set_property PACKAGE_PIN J14 [get_ports {AN[3]}]
set_property PACKAGE_PIN T9 [get_ports {AN[2]}]
set_property PACKAGE_PIN J18 [get_ports {AN[1]}]
set_property PACKAGE_PIN J17 [get_ports {AN[0]}]
set_property PACKAGE_PIN R13 [get_ports {B[3]}]
set_property PACKAGE_PIN U18 [get_ports {B[2]}]
set_property PACKAGE_PIN T18 [get_ports {B[1]}]
set_property PACKAGE_PIN R17 [get_ports {B[0]}]
set_property PACKAGE_PIN U8 [get_ports {op[1]}]
set_property PACKAGE_PIN T8 [get_ports {op[0]}]
set_property PACKAGE_PIN L18 [get_ports {r[6]}]
set_property PACKAGE_PIN T11 [get_ports {r[5]}]
set_property PACKAGE_PIN P15 [get_ports {r[4]}]
set_property PACKAGE_PIN K13 [get_ports {r[3]}]
set_property PACKAGE_PIN K16 [get_ports {r[2]}]
set_property PACKAGE_PIN R10 [get_ports {r[1]}]
set_property PACKAGE_PIN T10 [get_ports {r[0]}]
```

仿真结果

测试了4+3，4-3，~4，4*3*，*2*3，以及2+3这几组数据进行测试。 测试模块代码

```
module test;
    wire[6:0] r1;
```

```
    wire[3:0] an1;
    wire[7:0] f1;
    reg[3:0] A1,B1;
    reg[1:0] op1;
    parameter stoptime = 800;

calculater testfun(r1,an1,f1,A1,B1,op1);
initial #stoptime $finish;
initial begin
    A1 = 4; B1 = 3; op1 = 0;
    #100 op1 = 1;
    #100 op1 = 2;
    #100 op1 = 3;
    #100 A1 = 2;
    #100 op1 = 0;
 end
endmodule
```