ICD Final Report

Group ID: G_18

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RTL Report

Testbench	Pass (Pass/Fail)
Clock Cycle	10 (ns)
Total Time	11330 (ns)

Synthesis Report

Testbench	Pass (Pass/Fail)
No Latch	Pass (Pass/Fail)
Clock Cycle	10 (ns)
Cell Area(A)	271984.582(um^2)
Total Time(T)	11330 (ns)

Cell Area: Please report **Total cell area**

APR Report

Testbench	Pass (Pass/Fail)
No Error(x)	Pass (Pass/Fail)
Clock Cycle	10 (ns)
Cell Area(A)	340063.906(um^2)
Total Time(T)	11330 (ns)
$A*T^2$	43,653,629,542,923.4(ns^2*um^2)

Cell Area: Please report **Total area of Core**

Synthesis: No latch

```
Inferred memory devices in process
        in routine core line 956 in file
                '/home/raid7_2/userb08/b08179/Final/01_RTL/core.v'.
=================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=================================================================================
| display_counter_reg | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|        a_reg        | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|    op_ready_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|      state_reg      | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|      state_reg      | Flip-flop |   4   |  Y  | N  | N  | Y  | N  | N  | N  |
|        b_reg        | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|    in_ready_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
| image_register_reg  | Flip-flop |  2048 |  Y  | N  | Y  | N  | N  | N  | N  |
|     shift_x_reg     | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|     shift_y_reg     | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|  kernel_adjust_reg  | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     counter_reg     | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
|        c_reg        | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
|  kernel_pos_y_reg   | Flip-flop |  45   |  Y  | N  | Y  | N  | N  | N  | N  |
|  kernel_pos_x_reg   | Flip-flop |  45   |  Y  | N  | Y  | N  | N  | N  | N  |
|    out_valid_reg    | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|    out_data_reg     | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
|   sort_col_p2_reg   | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
|   sort_col_p4_reg   | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
|   sort_col_p6_reg   | Flip-flop |   8   |  Y  | N  | Y  | N  | N  | N  | N  |
|   med_counter_reg   | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     pos1_x_reg      | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|     pos1_y_reg      | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|     pos2_x_reg      | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|     pos2_y_reg      | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|     pos3_x_reg      | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|     pos3_y_reg      | Flip-flop |   4   |  Y  | N  | Y  | N  | N  | N  | N  |
|      pos_x_reg      | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|      pos_y_reg      | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
=================================================================================
```

```
Statistics for MUX_OPs
=======================================================
| block name/line   | Inputs | Outputs | # sel inputs |
=======================================================
|      core/632     |  256   |    8    |       8      |
|      core/632     |  256   |    8    |       8      |
|      core/633     |  256   |    8    |       8      |
|      core/633     |  256   |    8    |       8      |
|      core/634     |  256   |    8    |       8      |
|      core/634     |  256   |    8    |       8      |
|      core/635     |  256   |    8    |       8      |
|      core/635     |  256   |    8    |       8      |
|      core/639     |  256   |    8    |       8      |
|      core/948     |  256   |    8    |       8      |
=======================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb08/b08179/Final/01_RTL/core.db:core'
Loaded 1 design.
Current design is 'core'.
core
```

APR: NanoRoute Innovus Result