APRIL 2023, 4 BY ACKYE

Smart ZYNQ (SP&SL version) Project 1 Light up an LED with ZYNQ's PL resources (full graphic)

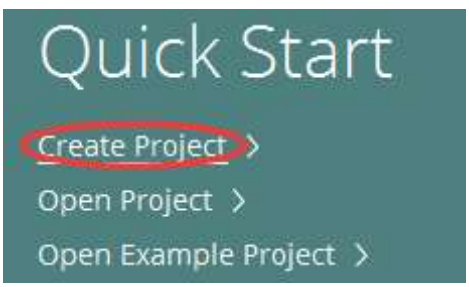
Programmer's first program is helloword, in the FPGA field, the meaning of lighting an LED light is equivalent to helloword, you can understand the complete process of the project from creation to operation in the process, below I use graphics to detail the operation of each step.

(Note: The content of this section applies to the boards of Smart ZYNQ SP and SL Edition, if it is Smart ZYNQ Standard Edition, please refer to the corresponding board directory)

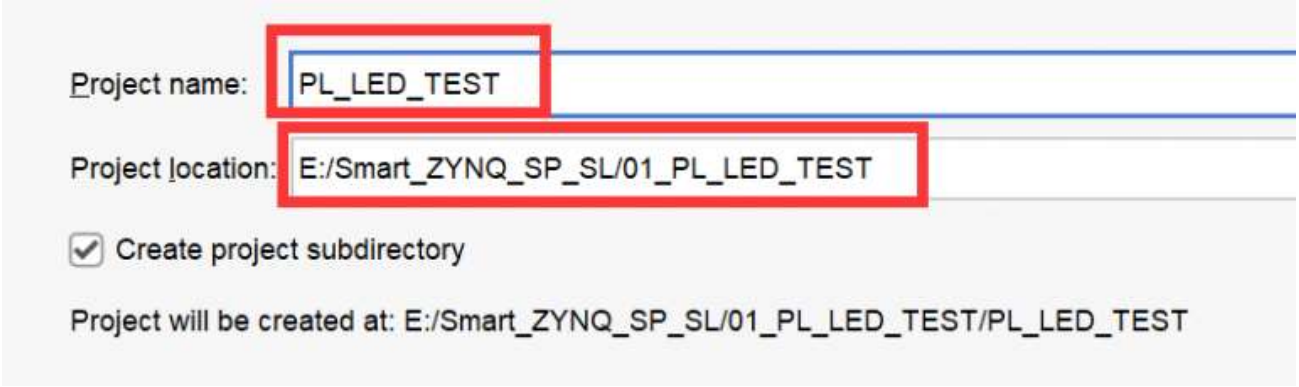
This article is demonstrated on vivado2018.3, please research for other versions

1. Specific steps

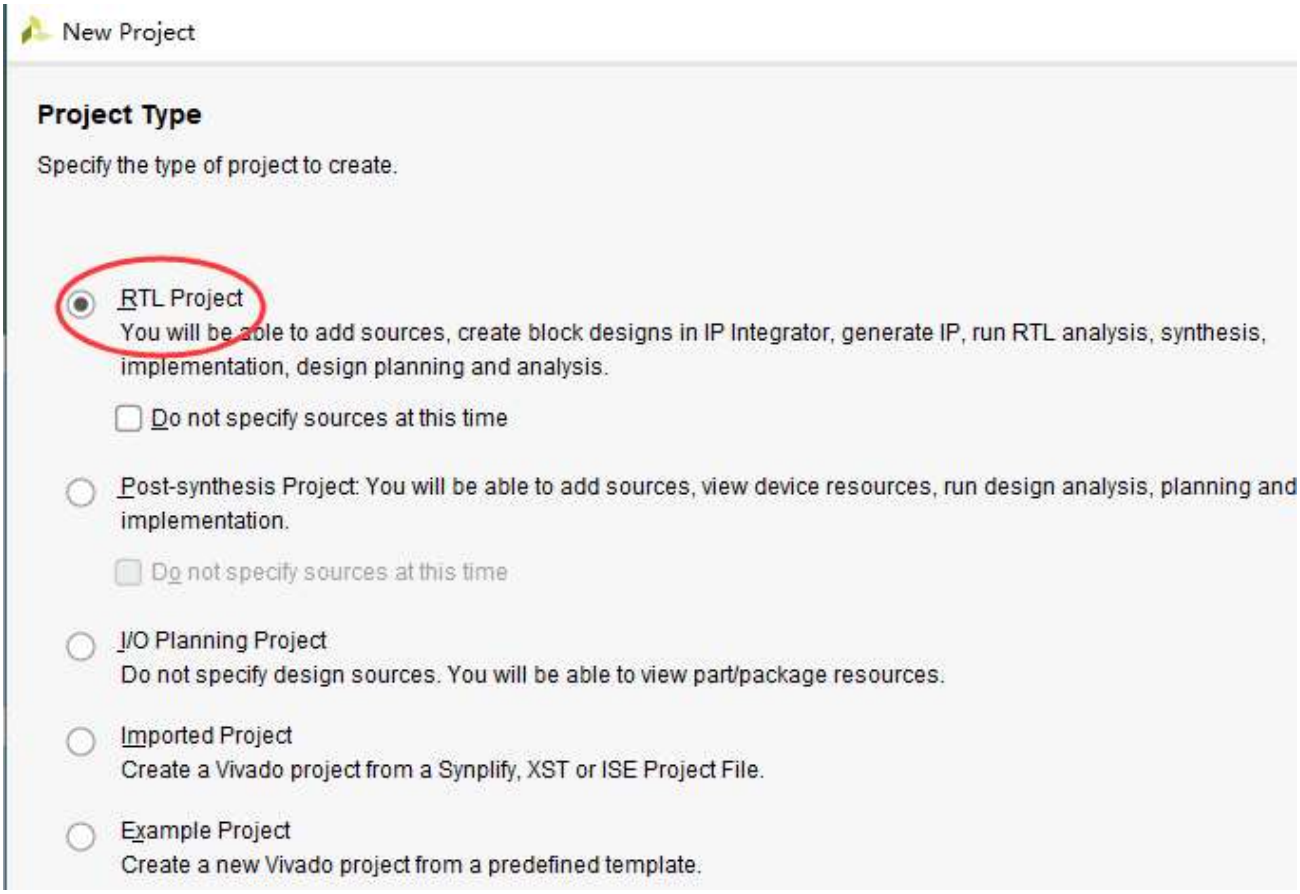
1) Specific steps to create a VIVADO project, open the software and select Create Project, as shown in the following figure



2) Click NEXT and enter the project name in the second dialog box "Project name" that appears; Select the save path in Project location; Check "Create project subdirectory" and click "Next" **Note, all paths cannot appear Chinese name**



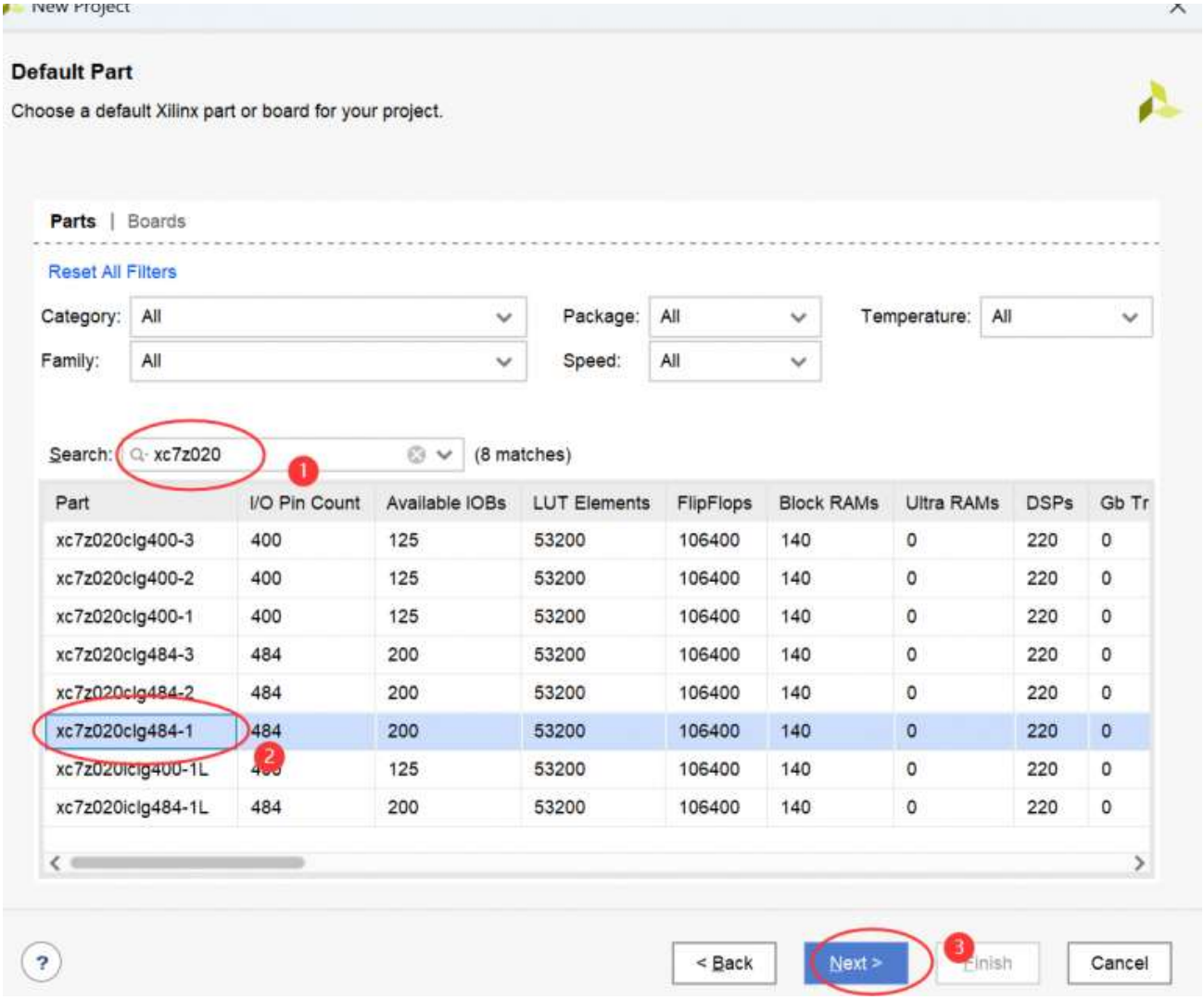
3) Click the RTL PROJECT option and click NEXT



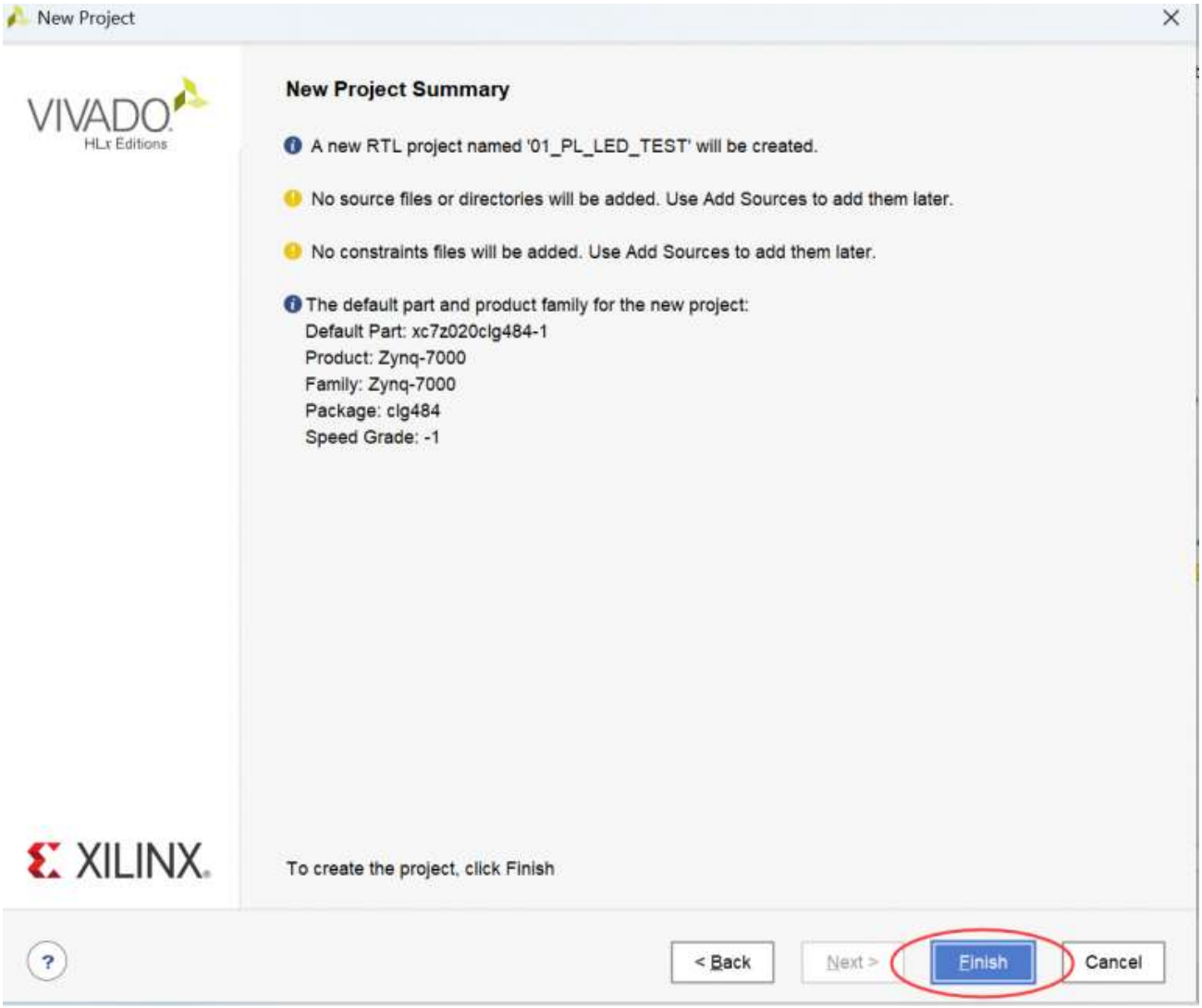
4) Step <>: The Add Sources option is left blank, NEXT

5) Step <>: The Add Constraints option is left blank, NEXT

6) Select the chip model The chip model of the board is XC7Z010 and the package is CLG484, so we choose xc7z020CLG484-1 for the model

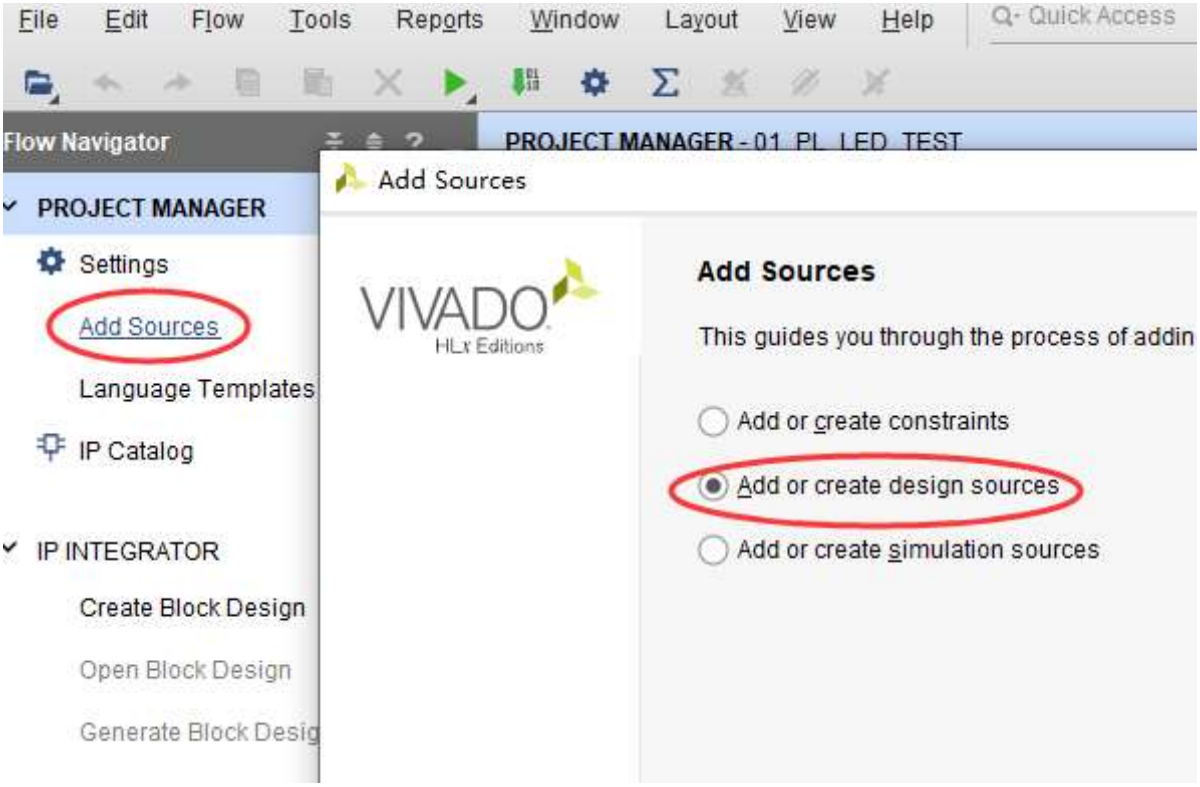


7）确认所选信息 点击“Finish”，完成vivado的工程创建

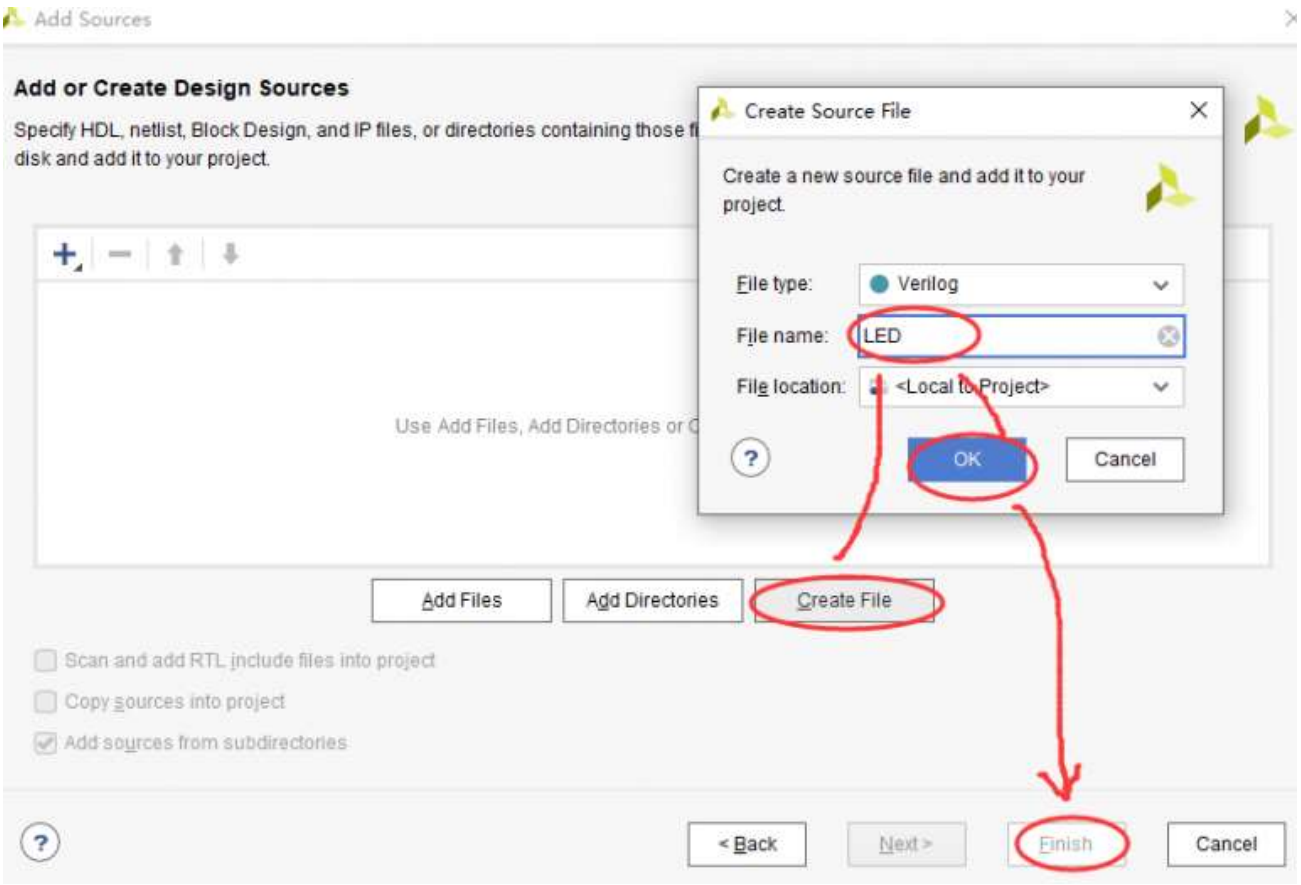


2 ADD VERILOG FILES

1) Click Add Sources on the left side of the main interface, click the Add or create design sources option in the checkbox and click NEXT

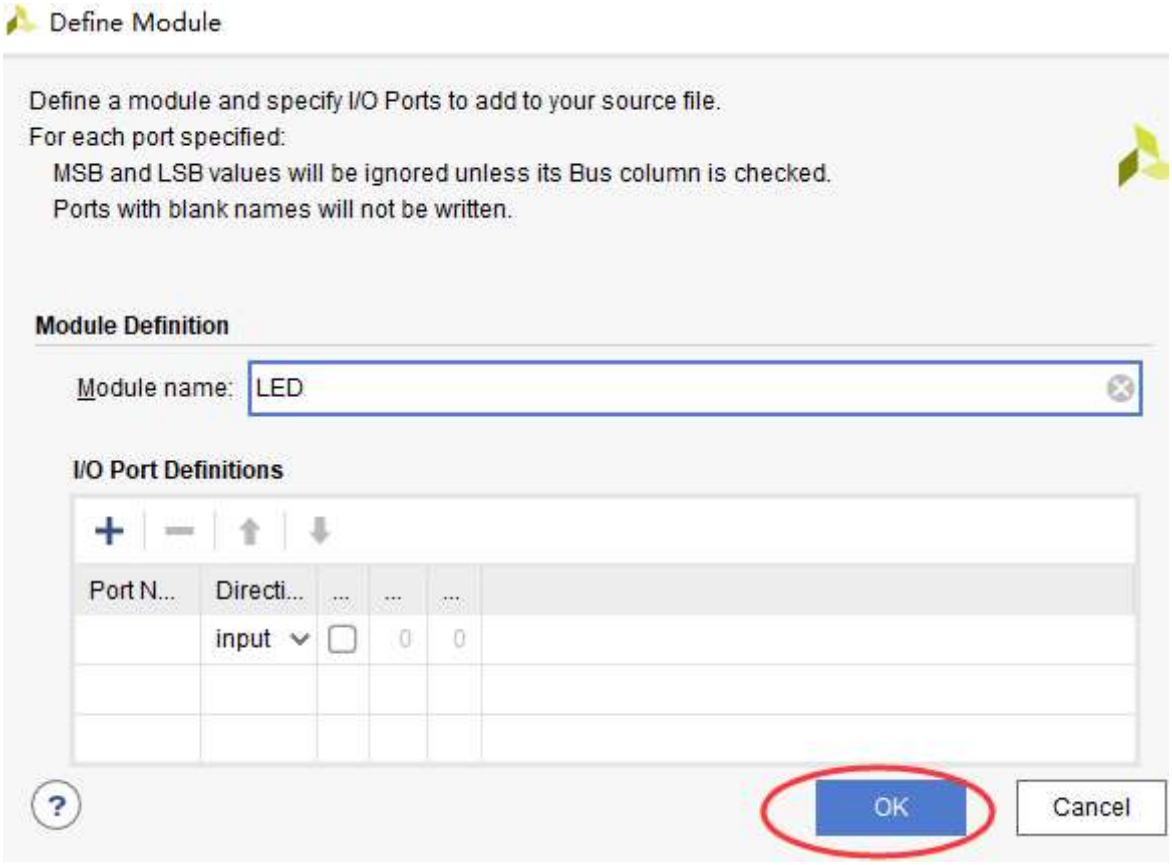


2) In the Add Sources that appears, select Create a new file Create FILE as below screenshot shown, and in the pop-up window, select the category as Verilog, fill in the name of the file in the FILE name, here with LED instead, click OK and click FINISH



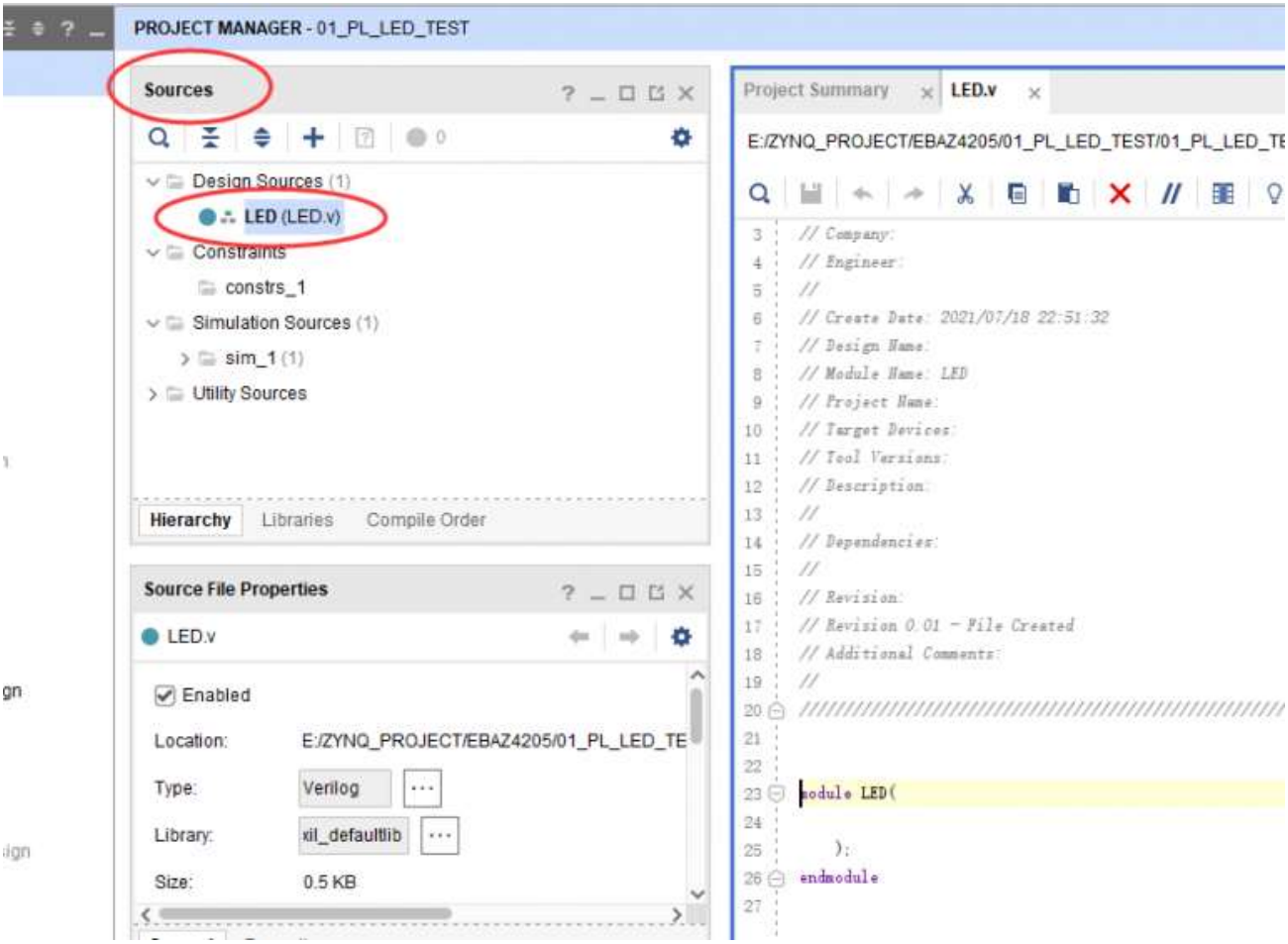
3) In the pop-up window, you can fill in the input and output signals of the module, because this part of the work can be completed in the code, so click OK directly here to complete

the creation of the VERILOG file



3. WRITE THE CODE FOR VERILOG

1) Double click to open the LED.V file just created and write the code of the LED inside

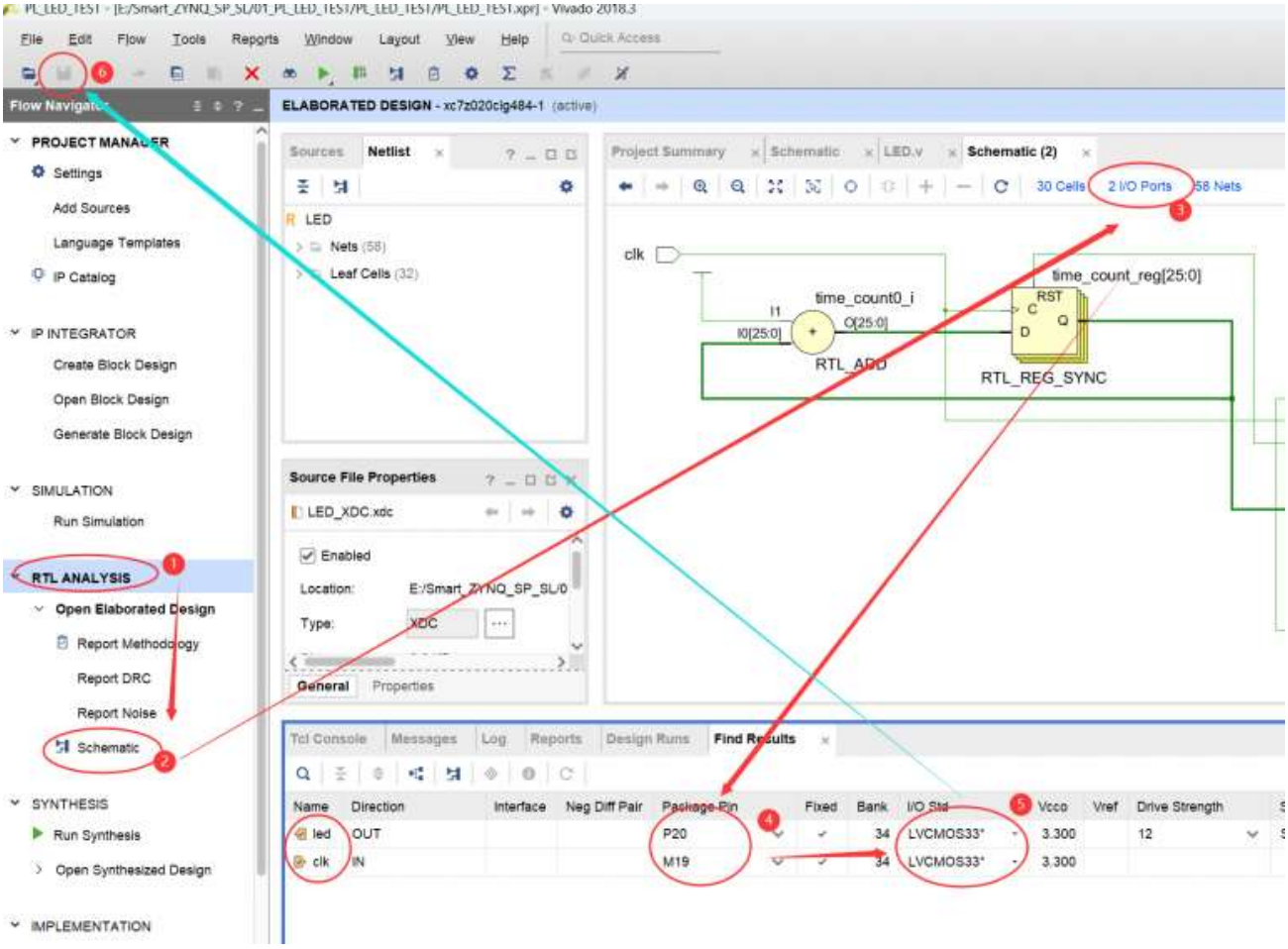


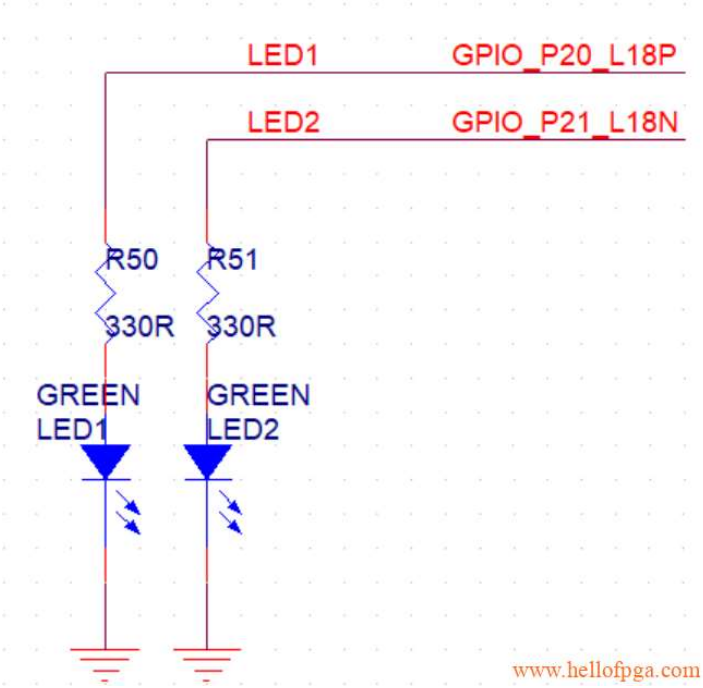

```
`timescale 1ns / 1ps
module LED(
    input clk,
    output led
);
parameter T1MS = 26'd50_000_000 ; //50M晶振时钟
reg [25:0]time_count=26'd0;//时钟计数器
reg led_r=1'b0;
always@(posedge clk)
    if(time_count>=T1MS)begin
        time_count<=26'd0;
        led_r<=~led_r;
    end
    else time_count<=time_count+1'b1;
assign led=led_r;
endmodule
```

After writing the code, compile the code

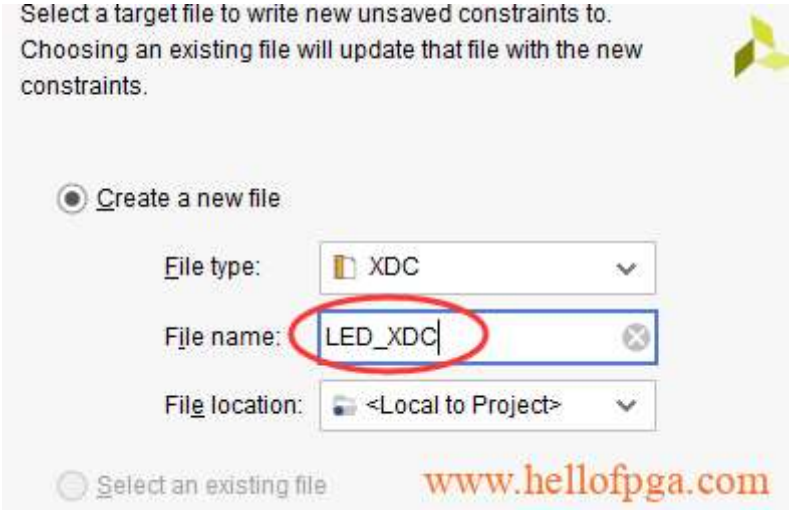
1. Next, RTL analysis, and complete the setting of the IO port (there are two ways, one is to use the graphical interface, the other is to write the constraint file to set, the two ways have the same result and eventually generate the same constraint file - this article is introduced in the graphical interface)

2. Graphical interface pin settings 1) Modify the IO interface in the Package pin first, CLK is connected to the M19 pin of the chip on the board, and the LED is connected to the P20 pin of the chip 2) Fill in the IO interface and pin electrical properties in the right side of the blue window I/O std, here is 3.3V Select LVCOMS3V3

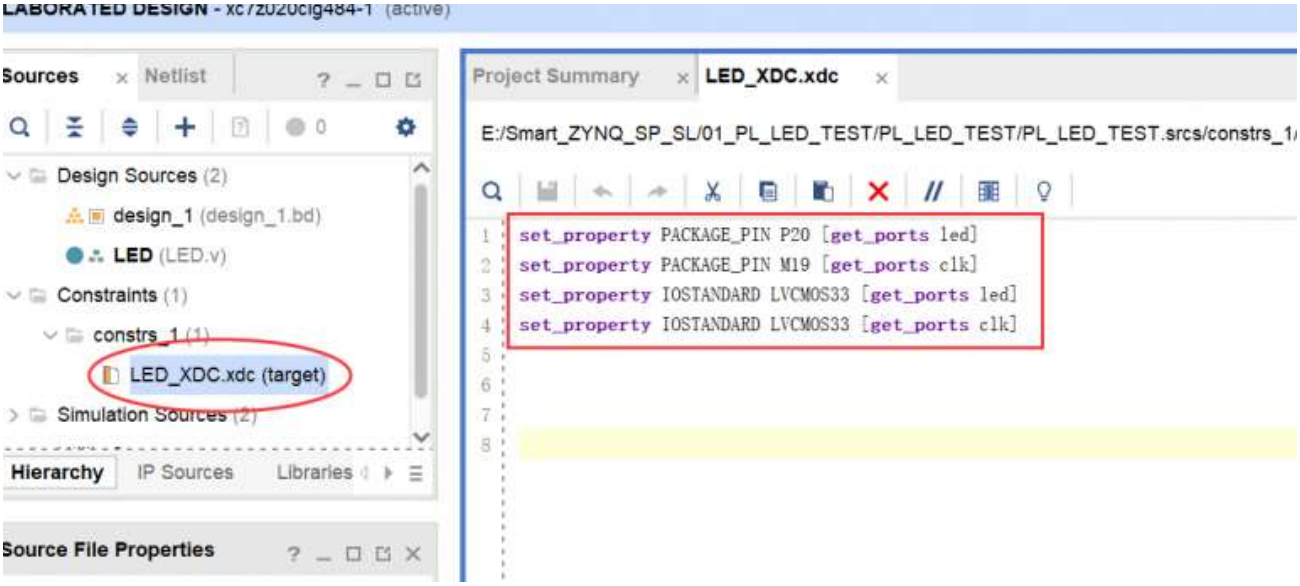




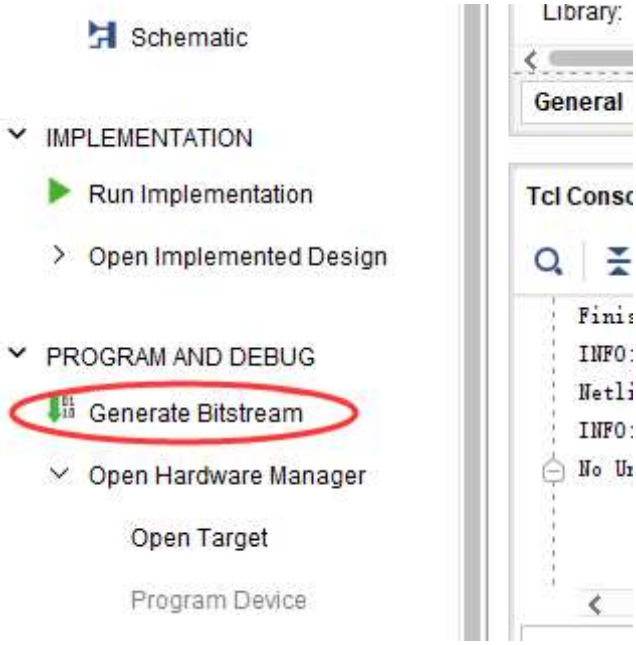
3. Select Save, the first time you save, you will be asked to fill in the name of the constraint file, and the information defined by the pin will be saved to the constraint file



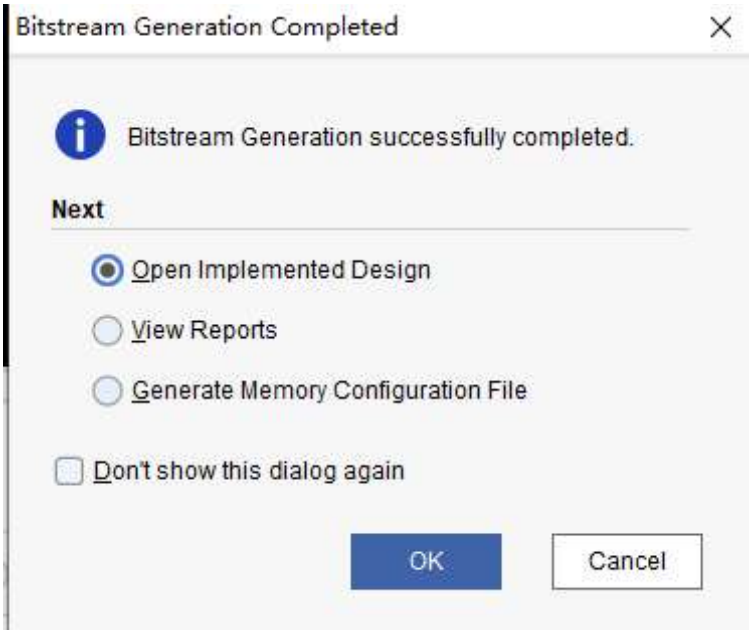
4. After that, there will be an additional constraint file in the project, and the pin definition we just added will be added in the constraint file (we can also directly add and modify the constraint file to achieve the pin definition, so that there is no need for the previous operation)



5. After saving, click Generate Bitstream to synthesize and generate a Bit file

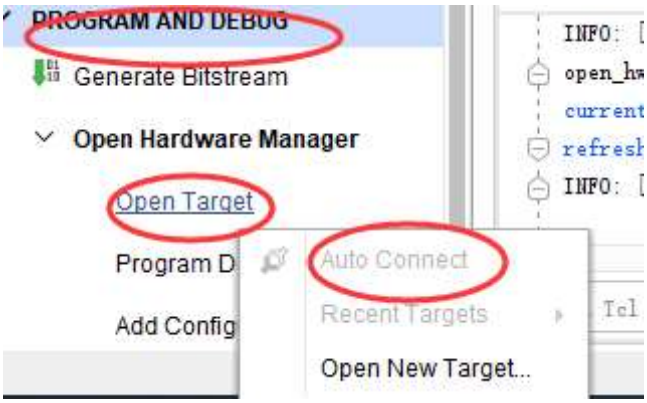


After success, the following dialog box will appear, click OK to confirm

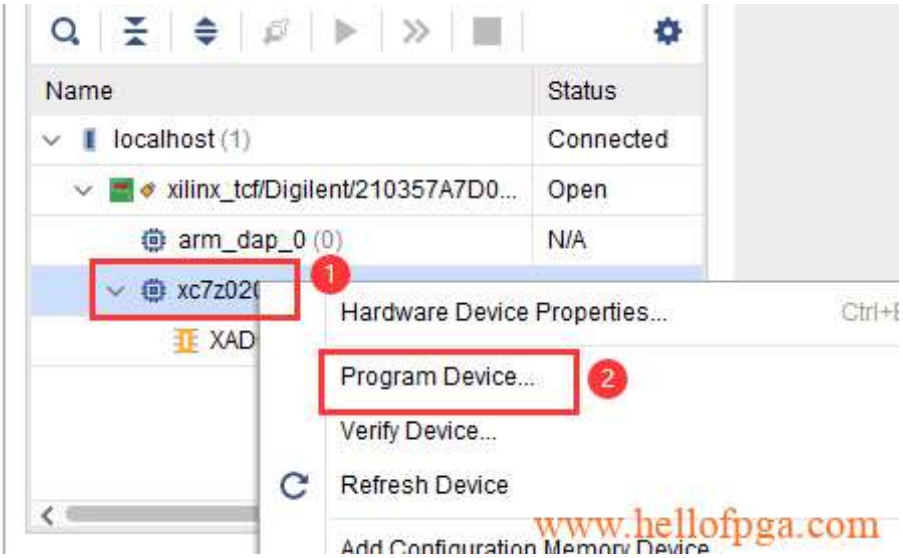


Use the TYPE C data cable to connect the JTAG port of the board to the computer, after powering the board, click Auto Connect under OPEN TARGET in PROGRAM AND DEBUG to connect the board

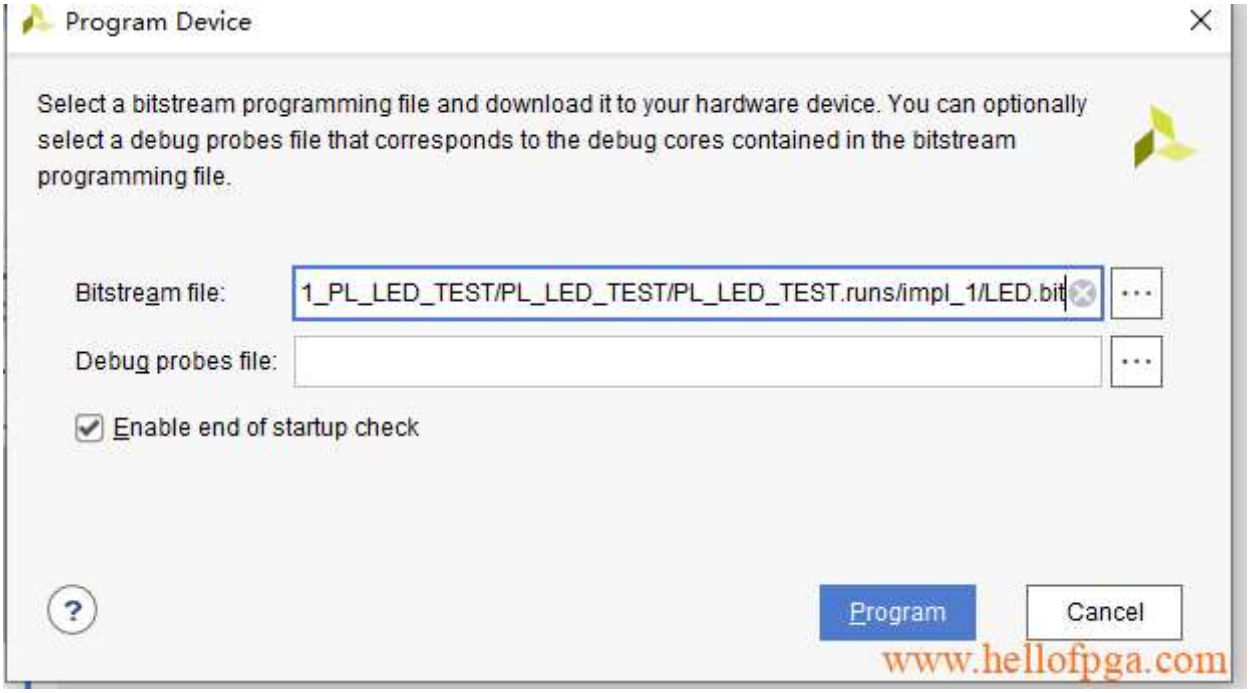
If the connection is normal, the device will be displayed in the right hardware bar, as shown in the following figure



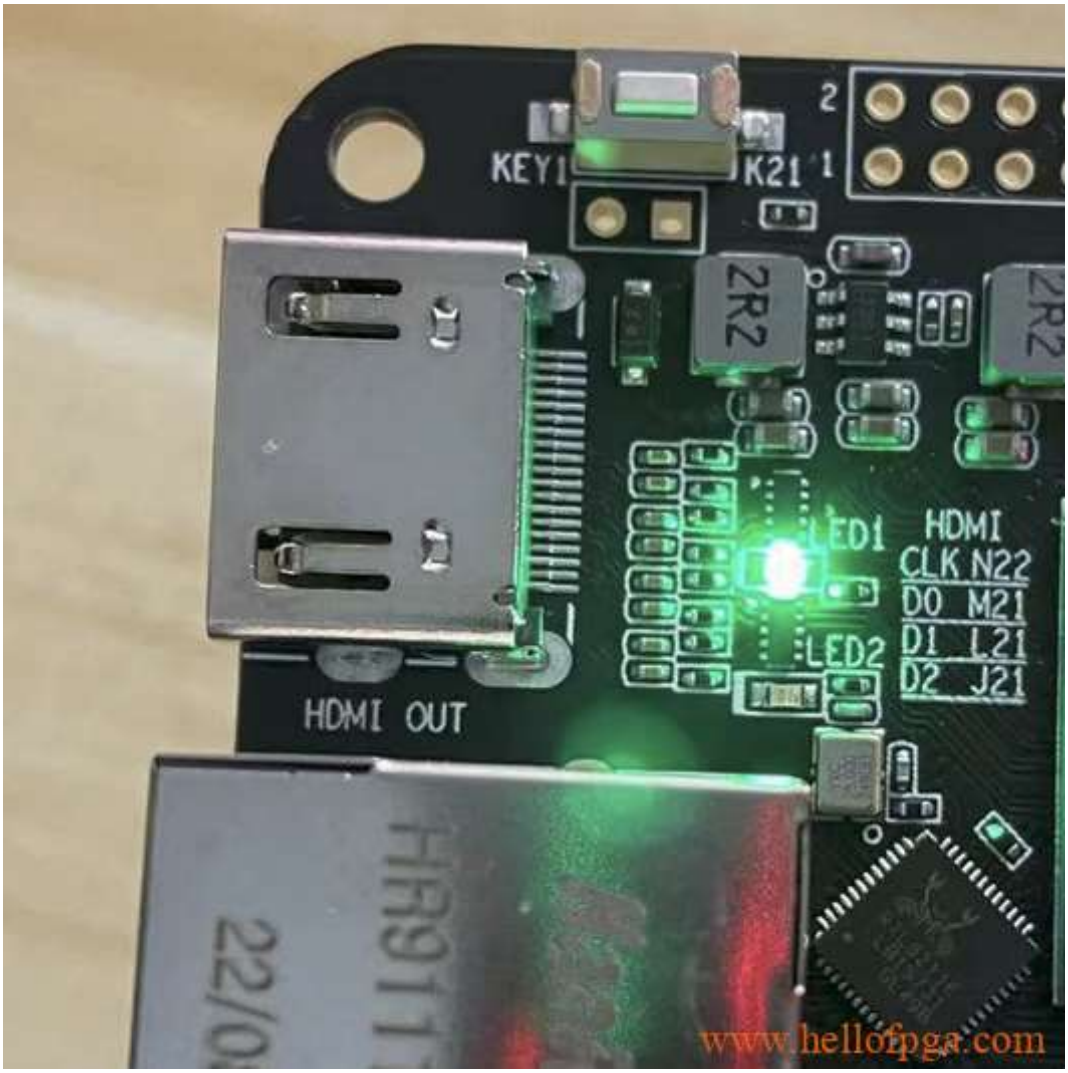
Next, download the bit file, right-click on the device and select Program Device



The generated BIT file will appear by default, if not, you need to add the path manually, click PROGRAM to download



After downloading, the board starts to run according to our code The LED light of the P20 starts to flash at 1S interval (at the same time, after the program download is completed, only the DONE light next to the chip also lights up, indicating that the chip is working normally)



The above is the completion and realization process of a project

Full project download:

01_PL_LED_TEST_XC7Z020 **Download**

SMART ZYNQ SP & SL