APRIL 2023, 4 BY ACKYE

Smart ZYNQ (SP version) data summary

Contains the schematic of Smart Zynq (SP version), precautions, and schematics of the interposer board for subsequent updates

First of all, thank you for your attention and support, if you have any questions, you can search for users in the salted fish APP: Super Electrician, or Taobao store hellofpga

NOTE ALL THE INFORMATION ON THIS SITE IS BASED ON VIVADO2018.3 VERSION, IF YOU ARE NOT FAMILIAR WITH THE DEVELOPMENT PROCESS, THE VERSION IS AS CONSISTENT AS POSSIBLE

In addition, this page is the information of the SP version, if it is a motherboard of Smart ZYNQ Standard Edition or SL Edition, please see the corresponding content

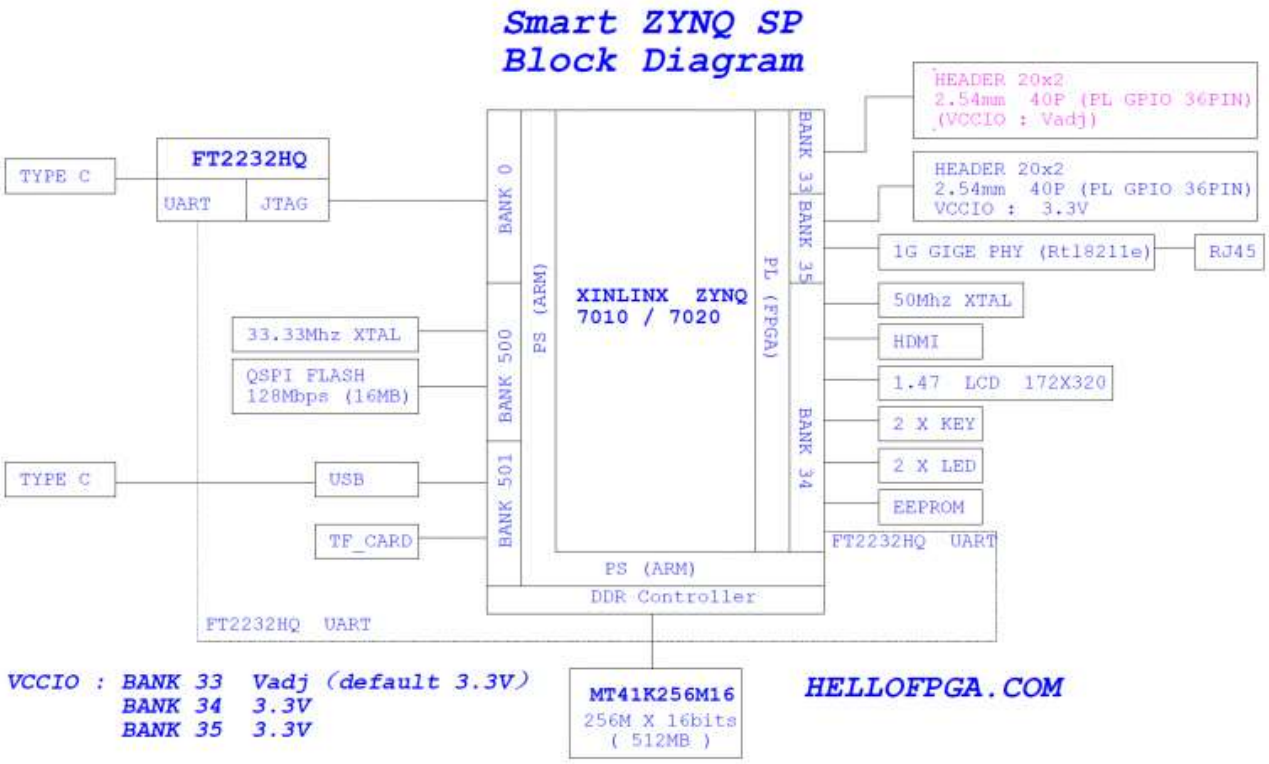
Motherboard information

Motherboard model	Smart Zynq SP	Smart Zynq SL	same
Main control chip	XC7Z020	XC7Z020	√
DDR memory	256M x 16bit （512MB）	256M x 16bit （512MB）	√
FLASH	128Mbits （16MB）	128Mbits （16MB）	√
EEPROM	24C02 2kbits	24C02 2kbits	√
clock	PS end: 33.33M active crystal amplium PL end: 50M active crystal oscillator	PS end: 33.33M active crystal amplium PL end: 50M active crystal oscillator	√
Number of board layers	8 floors	8 floors	√

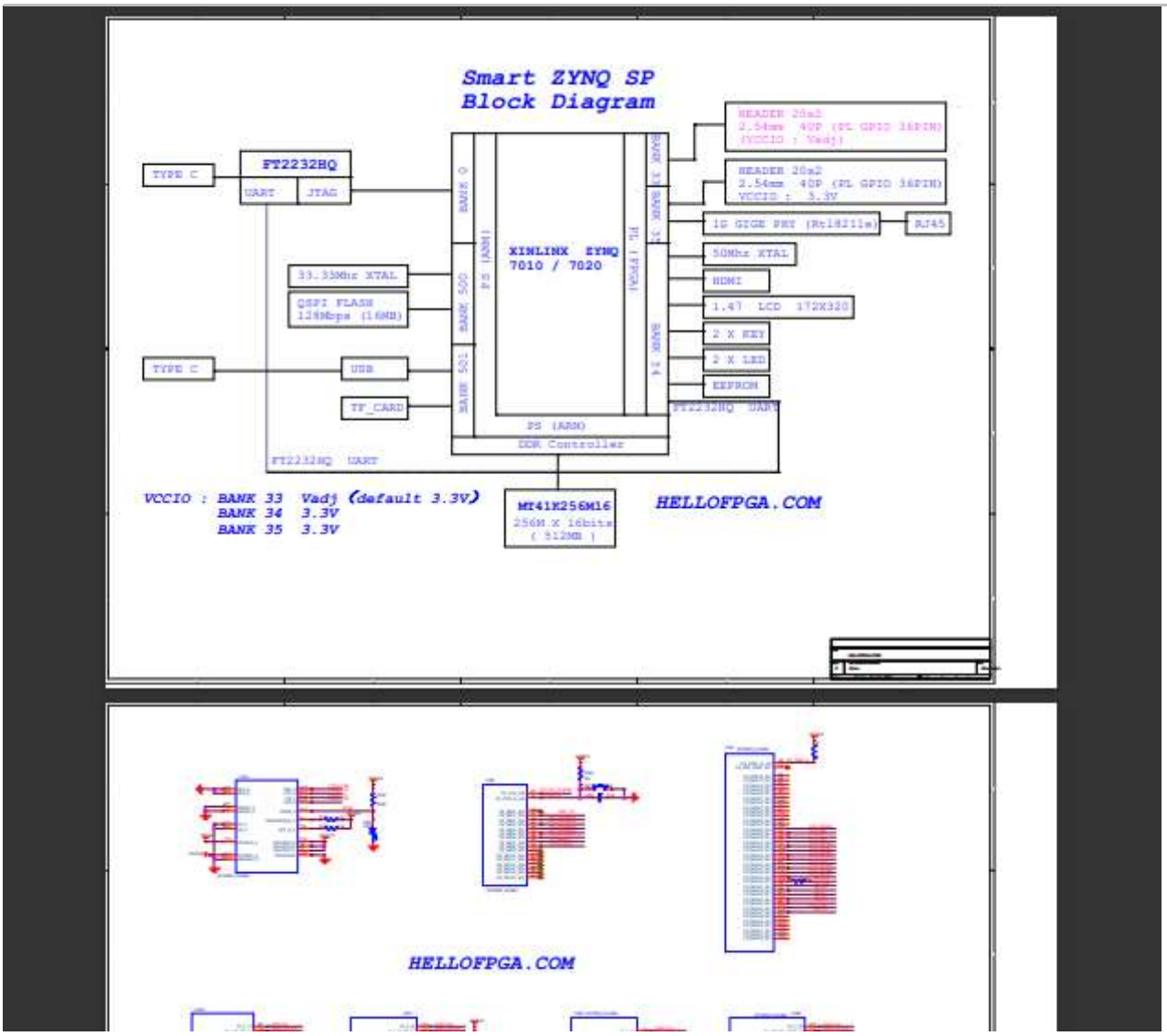
TF card slot	All the way TF card slot	All the way TF card slot	√
Network capabilities	Gigabit network X1 (connected to PL terminal, PS can also be used)	Gigabit network X1 (connected to PL terminal, PS can also be used)	√
HDMI interface	With one HDMI output (IO analog)	With one HDMI output (IO analog)	√
keystroke	Programmable button (PL side) x2 RST reset button x1	Programmable button (PL side) x2 RST reset button x1	√
LED indicator	Programmable LED X2 DONE Indicator X1 Power Indicator X1	Programmable LED X2 DONE Indicator X1 Power Indicator X1	√
Start the option DIP switch	A two-way DIP switch is responsible for the selection of the start-up method	A two-way DIP switch is responsible for the selection of the start-up method	√
The pin header is led out	68 programmable GPIOs (all led out by PL, PS can be mapped by EMIO) All pins are pinned out in pairs (equal length within the differential line) with a pin spacing of 2.54mm	68 programmable GPIOs (all led out by PL, PS can be mapped by EMIO) All pins are pinned out in pairs (equal length within the differential line) with a pin spacing of 2.54mm	√
Whether the BANK voltage is adjustable	In the GPIO, the bank voltage on one side of the lead is adjustable	In the GPIO, the bank voltage on one side of the lead is adjustable	√
Serial	Comes with a serial port TYPE C interface	Comes with a serial port TYPE C interface	√
USB	The board comes with USB function and can be used as a USB HOST, or USB SLAVE	**No USB function**	×

LCD	The board comes with a 1.47-inch SPI LCD screen, which is connected to PL testing (PS can also be used)	**Does not have an on-board LCD function**	×
JTAG downloader	**Boards are part of the Xilinx JTAG downloader and require no additional configuration**	**Without an onboard downloader, an external downloader is required**	×
Resource rollups	TYPE C: JTAG + UART (powered) TYPE C: USB **SLAVE USB** **A : USB HOST** **LCD : 1.47" COLOR** TF: TF CARD SLOT (BOOTABLE) RJ45 : Gigabit Ethernet HDMI : HDMI OUT 40PIN Pin header X2 (68 PL GPIO) programmable LED X2 programmable button X2 POR reset button X1 ZYNQ 7020 chip 512MB DDR 2Kbits EEPROM 16MB FLASH (bootable) crystal oscillator 33.33M (PS) 50M (PL) one bank voltage adjustable	TYPE C : UART (POWERED) TF : TF CARD SLOT (BOOTABLE) RJ45 : Gigabit Ethernet hdmi : hdmi out 40PIN Pin header X2 (68 PL GPIOS) PROGRAMMABLE LED X2 PROGRAMMABLE BUTTON X2 POR reset button X1 ZYNQ 7020 chip 512MB DDR 2Kbits EEPROM 16MB FLASH (bootable) one bank voltage adjustable crystal oscillator 33.33M (PS) 50M (**Note: (SL model requires additional downloader).**	×

SP and SL versions of the same resource programs are fully compatible, and the pin and GPIO line order are also exactly the same, except for the functions that the SL version does not have such as USB HOST, USB SLAVE and on-board LCD

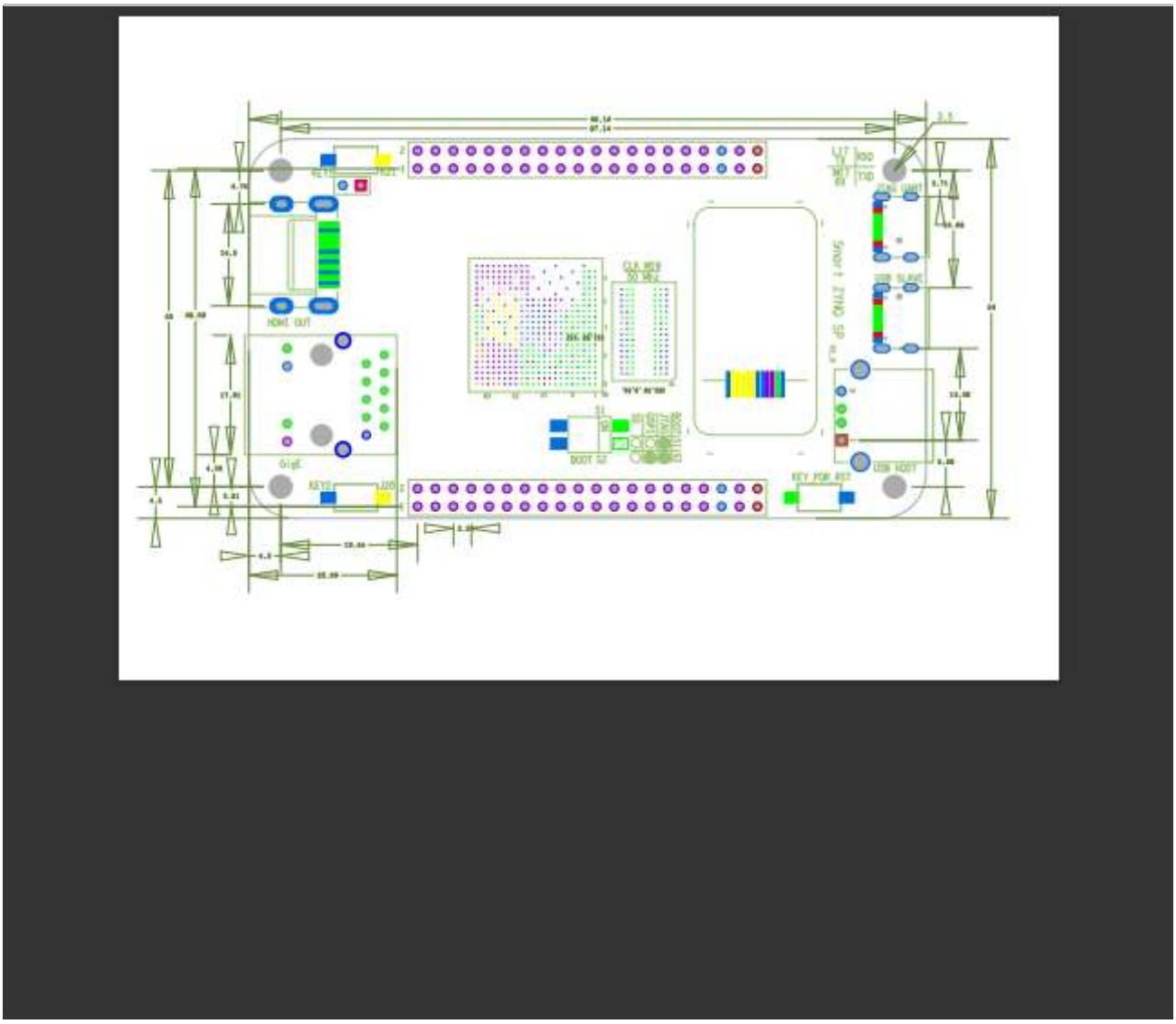


The board schematic is as follows: (Last updated May 2023, 5)



Smart_zynq_sp_v1_0_20230501 **Download**

Dimensional drawing



Smart_ZYNQ_SP_V1_SIZE_20230502 **Download**

Pin length report of the pin row on the board: (Remarks Differential line is made of equal length in the group, and no equal length is made outside the group, if there are requirements for equal length during the design of the bottom board, please refer to the following length report)

Smart_ZYNQ_SP_IO_length_20230705 **Download**

Data sheet for all functional ICs on the board:

smart_zynq_datasheet download

PL resources for the 7010 and 7020 are shown in the figure below

Table 1: **Zynq-7000 and Zynq-7000S SoCs *(Cont'd)***

	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Block RAM (# 36 Kb Blocks)	1.8 Mb (50)	2.5 Mb (72)	3.8 Mb (107)	2.1 Mb (60)	3.3 Mb (95)	4.9 Mb (140)	9.3 Mb (265)	17.6 Mb (500)	19.2 Mb (545)	26.5 Mb (755)
	DSP Slices (18x25 MACCs)	66	120	170	80	160	220	400	900	900	2,020
	Peak DSP Performance (Symmetric FIR)	73 GMACs	131 GMACs	187 GMACs	100 GMACs	200 GMACs	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express (Root Complex or Endpoint)[3]		Gen2 x4			Gen2 x4		Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[2]	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication									

Notes:

1. Restrictions apply for CLG225 package. Refer to the UG585, *Zynq-7000 SoC Technical Reference Manual* (TRM) for details.
2. Security is shared by the Processing System and the Programmable Logic.
3. Refer to PG054, *7 Series FPGAs Integrated Block for PCI Express* for PCI Express support in specific devices.

Notes

1) The silkscreen mark of Uart on the board of Smart ZYNQ SP and SL version V1.0 is inverted, TX–>L17, RX–>M17 (when you use it, please refer to the schematic)

2) USB SLAVE and USB HOST on the Smart ZYNQ SP board share ZYNQ's USB resources, so only one function can be used at the same time (USB HOST and USB SLAVE cannot be connected to external devices at the same time)

3) The two TYPE C interfaces on the board can supply power to the board, and the VCC port on the board pin header can also be connected to 5V to power the board, and the USB and external power supply do not conflict with each other (USB has diodes for anti-backcurrent protection)

4) Some notebooks and old computers USB port output power is less than 5V 500ma, if the board due to power supply problems caused by unstable function, please try to replace the data cable, or replace the USB port and try again, you can also provide 5V power supply for the board through the external adapter board (VCC pin of the pin header)

5) The VCC port on the pin header can be used as a power input or as a power output

- When used as input, it can be connected to an external 5V power supply (that is, through the adapter board, or the bottom plate to power the board, **such as the power supply effect is not good with DuPont line**)
- As an output (no external 5V power supply, only via USB) can output a voltage of 4.5-4.7V (that is, the motherboard supplies power to the adapter board)

6) The POR RST on the board is the reset button for the entire hardware (priority is higher than any program, as long as this button is pressed, the whole system will restart according to the BOOT boot mode)

8) Regarding the voltage of BANK33, the BANK 33 voltage can be adjusted by adjusting the two 0805-sized resistors on the back (the silk screen on the board is marked as RA RB) (the factory default is 3.3V)

9) BANK35 Because various peripherals on the board are connected, the BANK35 voltage is not adjustable and fixed at 3.3V

10) If you need to draw the upper expansion board, please pay attention to the height of the RJ45 interface and reserve the slot of RJ45, otherwise the upper expansion board will not be inserted

Introduction to the demo program pre-downloaded with the board (boot mode, select QSPI FLASH and then power on)

- HDMI output 720p test color stripes
- 1.4 inch screen output test color stripes
- UART sends "hello world" at one-second intervals
- The LED light lights up back and forth in the form of a running light after power-on (once any of the keys KEY1 KEY2 are pressed, the running light stops, and the program switches to the light in the corresponding button direction to light up)
- USB slave interface with data cable and computer connection You can see a ram-mapped 255MB virtual U disk (because it is RAM-mapped, so the power failure data will be lost, please do not store important data, only for testing)

TF firmware available for testing

(How to use: Download and unzip the file, copy the contents to the root directory of the FAT32 format TF card, and insert it into the motherboard, set the DIP switch to SD boot, and press the POR on the board to reset the keyboard)

1. Full functional test

- All GPIOs (pin headers) flash **the running light**
- HDMI output 720p test color stripes
- 1.4 inch screen output color pictures
- UART sends "hello world" at one-second intervals
- The LED light lights up back and forth in the form of a running light after power-on (once any of the keys KEY1 KEY2 are pressed, the running light stops, and the program switches to the light in the corresponding button direction to light up)
- USB slave interface with data cable and computer connection You can see a ram-mapped 255MB virtual U disk (because it is RAM-mapped, so the power failure data will be lost, please do not store important data, only for testing)

ALL_TEST_20230430 **Download**

2. Network and USB HOST test firmware (linux entry account root password root)

NET_USB_LINUX_20230430 **Download**

- Log in to Linux through the command line with a serial port, then plug in the network cable to connect to the router, and test the network function through ping
- Insert the FAT32 format U disk and use the command line related commands to access the U disk **(SL version does not have this function).**
- In terms of operation, you can refer to the operation demonstrated at the bottom of the following two projects: ZYNQ linux development chapter 8 Petalinux Gigabit Ethernet function test (Smart ZYNQ SP&SL version) and project Smart ZYNQ (SP) Project 27 PS-based USB slave function test (that is, the functional test of ZYNQ analog U disk).

Some graphic routines that have been collated (constantly being updated)

When ZYNQ is encountered, the SDK debug fails to report an error solution

There are several ways to add reset signals to the PL part of the ZYNQ board

Vivado 2018.3 download and install

Verilog quick to get started with notes

A note on the 7020 chip grinding code

Smart ZYNQ (SP&SL version) Project 1 Light up an LED with ZYNQ's PL resources (full graphic)

Smart ZYNQ (SP&SL Version) Project II Design flow lights with ZYNQ's PL (FPGA).

Smart ZYNQ (SP&SL version) Project 3 Provide a clock for PL logic through the PS part (common method when doing engineering)

Smart ZYNQ (SP&SL VERSION) Project 4 PL partial button function demonstration (IO input function)

Smart ZYNQ (SP&SL Edition) Project V HDMI function demonstration based on ZYNQ PL resources

Smart ZYNQ (SP&SL Edition) Project 6 Use ZYNQ's PS to light up the LED light connected to the PL end AXI_GPIO_IP method (full picture and text)

Smart ZYNQ (SP&SL Version) Project 7 Use ZYNQ's PS to light up the LED light EMIO method connected to the PL end (Recommended use)

Smart ZYNQ (SP&SL version) Project VIII solidifies the program to QSPI FLASH

Smart ZYNQ (SP&SL Edition) Project IX Place the program on the TF card and perform a TF card startup demonstration

Smart ZYNQ (SP&SL VERSION) Project X Vivado's built-in simulation feature demo

Smart ZYNQ (SP&SL Edition) Project XI FPGA Hardware Debug ILA Demonstration Feature

Smart ZYNQ (SP&SL version) Project XII PWM demo based on ZYNQ FPGA resources

Smart ZYNQ (SP&SL version) Engineering XIII Testing of PL-based PLL clock modules

Smart ZYNQ (SP&SL VERSION) Project 14 The use of block RAM IP cores based on the PL side

Smart ZYNQ (SP&SL VERSION) Project XV ZYNQ side PS accesses the reg register on the PL side to realize PS and PL data interaction

Smart ZYNQ (SP&SL Edition) Project XVI Demonstration of UART functionality in the PS part based on ZYNQ

Smart ZYNQ (SP&SL Edition) Engineering XVII Gigabit Network Module Preliminary Test (Based on PS EMIO)

Smart ZYNQ (SP&SL version) Engineering XVIII is based on timer interrupts on the PS side

Smart ZYNQ (SP&SL Edition) Project XIX Demonstration of the GPIO (EMIO) input function based on the PS side

Smart ZYNQ (SP&SL version) works twenty based on external interrupt testing on the PS side

Smart ZYNQ (SP&SL Edition) Engineering XXI PL-based VIO online debugging functional test

(Project 800 RGB480X<> screen module temporarily sorted)

Smart ZYNQ (SP&SL Edition) Project XXIII Use the VDMA module to cache images and display them on HDMI (a) 800X600 resolution test

Smart ZYNQ (SP&SL Edition) Project XXIV Use the VDMA module to cache images and display them on HDMI (2) Use always crossover to adapt to more resolutions

Smart ZYNQ (SP&SL Version) Project XXV Use the VDMA module to cache the image and display it on HDMI (3) Display the BMP format picture on the TF card

Smart ZYNQ (SP Version) Project XXVI Drives color LCD with the hardware SPI resources of ZYNQ PS (**SL version does not have this feature).**

Smart ZYNQ(SP) Engineering XXVII PS-based USB slave functional test (i.e. functional test of ZYNQ analog USB stick) (**SL version does not have this function).**

(Project 28 Temporarily sorted out)

Smart ZYNQ (SP&SL version) Project 29 calls on-chip XADC resources on the PS side to read the chip's power and temperature information in real time

Smart ZYNQ (SP&SL Edition) Project Thirty The on-chip XADC resource is called on the PL side to read the level voltage of the ADC pin

The following is the graphic tutorial material of the Linux section (continuously updated)

ZYNQ Linux Development Chapter 1 Installation of Ubuntu and the virtual machine VMware

ZYNQ Linux Development Chapter 2 Shared folder settings under Ubuntu (optional)

ZYNQ Linux Development Chapter 3 Installation of the Petalinux Development Environment

ZYNQ Linux Development Chapter 4 Designing a Linux boot image for ZYNQ - QSPI Flash Boot (Smart ZYNQ SP&SL version)

ZYNQ Linux Development Chapter 5 Petalinux Designing Zynq's Linux Boot Image - TF Card Boot (Smart ZYNQ SP&SL Edition)

ZYNQ Linux Development Chapter 6 GPIO (EMIO mode) input and output experiment under Petalinux - sysfs method (Smart ZYNQ SP&SL Edition)

ZYNQ Linux Development Chapter 7 Input and Output Experiment II of GPIO (EMIO Method) under Petalinux - Invoke by Writing Applications (Smart ZYNQ SP&SL Edition)

ZYNQ Linux Development Chapter 8 Testing Petalinux Gigabit Ethernet Functionality (Smart ZYNQ SP&SL Edition)

ZYNQ Linux Development Chapter 9 Petalinux USB HOST Experiment (Smart ZYNQ SP Edition). **(SL version does not come with this feature).**

ZYNQ linux开发 章节十 Petalinux 板载LCD 显示linux命令行实验（Smart ZYNQ SP 版） **(SL版不带此功能)**

SMART ZYNQ SP & SL