Accusilicon PM33
Ultra-Low Phase Jitter PLL and Super DIR Module for High Performance Audiophile Application

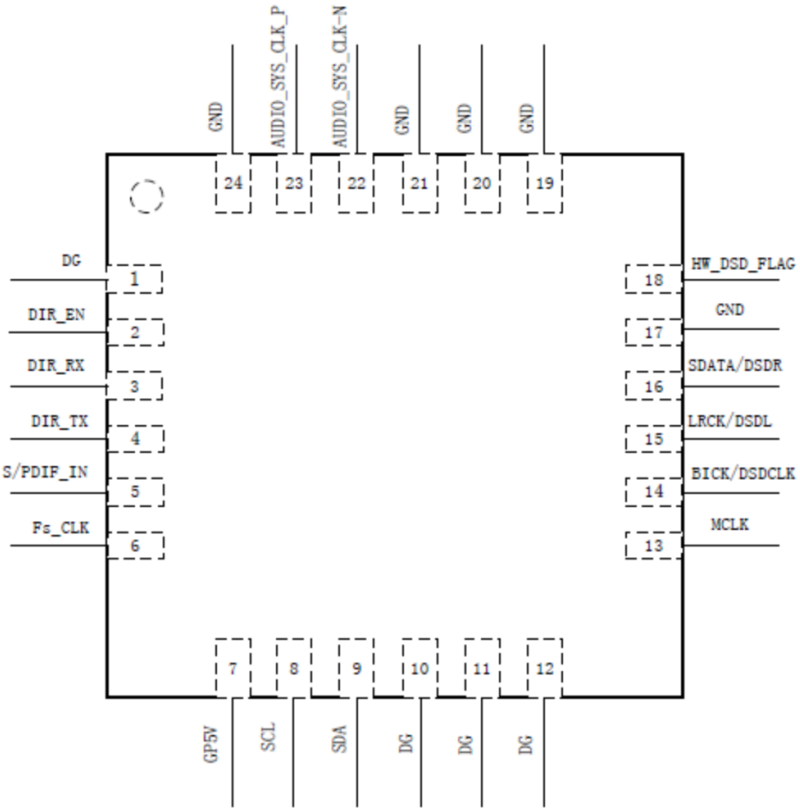
Features

- Support both High Performance Audio DIR Mode and Ultra Low Phase Jitter PLL Mode
- Generates any combination of output frequencies range from any input frequency in PLL mode; LVDS: up to 393.216 MHz, LVCMOS: up to 196.608 MHz
- Input Clock frequency (fs) range, LVCMOS: 44.1 kHz to 1.536 MHz
- Ultra-Low Phase Jitter :
  150 fs typ (10Hz-1MHz) @ f0=196.608 MHz
  100 fs typ (12 kHz–20 MHz) @ f0=196.608 MHz
- Configurable outputs compatible with LVDS and LVCMOS in PLL mode
- Programmable jitter attenuation bandwidth from 0.1 Hz to 100 Hz in PLL mode
- More than 60dB Jitter rejection > 10 Hz ; More than 80dB Jitter rejection > 40 Hz
- +/-500 ppm pulling range (APR) in PLL mode
- Less than +/- 1ppm clock accuracy @ audio clock generator mode
- Fast lock feature for low nominal bandwidths
- S/PDIF audio stream input and I2S audio stream output in Audio DIR mode
- Support up to 24Bit/384 kHz Super S/PDIF audio stream input
- Support both PCM and DSD(DSD Over PCM) audio file format in DIR mode
- Serial interface I2C
- +5V Power Supply Only
- 40mmx 40 mm 24 pin SMD Package for Audiophile Application

Application

- High Quality Audiophile Application
- Test and Measurement Instrument
- Broadcast Audio
- Audio Clock Generator
- Audio Clock Recovery

Pin Assignment



Top View

No	Pin Name	Description
1	DG	Ground
2	DIR_EN	DIR Enable
3	DIR_RX	DIR data receive
4	DIR_TX	DIR data transmit
5	S/PDIF_IN	S/PDIF audio stream input
6	Fs_Clk	Fs clock input
7	GP5V	+5V Power Supply
8	SCL	Serial clock input for I2C
9	SDA	Serial data interface for I2C

10	DG	Ground
11	DG	Ground
12	DG	Ground
13	MCLK	Audio master clock output
14	BICK/DSDCLK	I2S BICK/DSDCLK
15	LRCK/DSDL	I2S LRCK/DSDL
16	SDATA/DSDR	I2S SDATA/DSDR
17	GND	Ground
18	HW_DSD_FLAG	DSD audio format flag
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	AUDIO_SYS_CLK_N	Audio system clock output LVDS_N
23	AUDIO_SYS_CLK_P	Audio system clock output LVDS_P / LVCMOS
24	GND	Ground

Typical Operating Characteristics

Input Clock Speciation –Single-Ended AC Coupled

Parameter	Description	Min	Typical	Max	Unit
Fs_Clk	Input Frequency Range LVCMOS	44.1		1536	kHz
	Input Voltage Swing		3.3		V
DC	Duty Cycle	40		60	%
Cin	Capacitance		5		pf

LVDS Output Clock Speciation

Parameter	Description	Min	Typical	Max	Unit
AUDIO_SYS_CLK_P/N	Output Frequency Range LVDS	44.1		393216	kHz
	Output Voltage Swing	400	450	500	mVpp_se
D	Duty Cycle	45		55	%
TR	Rise Time		200		ps
Z	Differential Output Impedance		100		Ω

LVCOMS Output Clock Speciation

Parameter	Description	Min	Typical	Max	Unit
AUDIO_SYS_CLK_P	Output Frequency Range LVCOMS	44.1		196608	kHz
D	Duty Cycle	45		55	%
VH	Voltage High	2.8			V
VL	Voltage Low			0.5	V
TR	Rise Time		500		ps

Performance Characteristics

Parameter	Description	Min	Typical	Max	Unit
F-BW	PLL Loop Bandwidth	0.1		100	Hz
	Pull-in Range		+/-500		ppm
	PLL Lock Time	5	700		ms
Residual	RMS Phase Jitter (10Hz-1MHz) @ f0=196.608MHz		150		fs
	RMS Phase Jitter (12kHz~20MHz) @ f0=196.608MHz		100		fs
Reject	>1 Hz Jitter Rejection (F-BW is 0.1Hz, same as below)		30		dB
	>10 Hz Jitter Rejection		60		dB
	>40 Hz Jitter Rejection		80		dB
	>100 Hz Jitter Rejection		90		dB
	>400 Hz Jitter Rejection		100		dB

Absolute Maximum Ratings

Parameter	Description	Min	Typical	Max	Unit
GP5V	Supply Voltage	4.5	5	5.5	V
Fs_Clk	Input Voltage		3.3		V
AUDIO_SYS_CLK_P	Outout Voltage		3.3		V
AUDIO_SYS_CLK_N	Outout Voltage		3.3		V
TA	Operating Temperature	-10		60	°C
TS	Storage Temperature	-45		125	°C

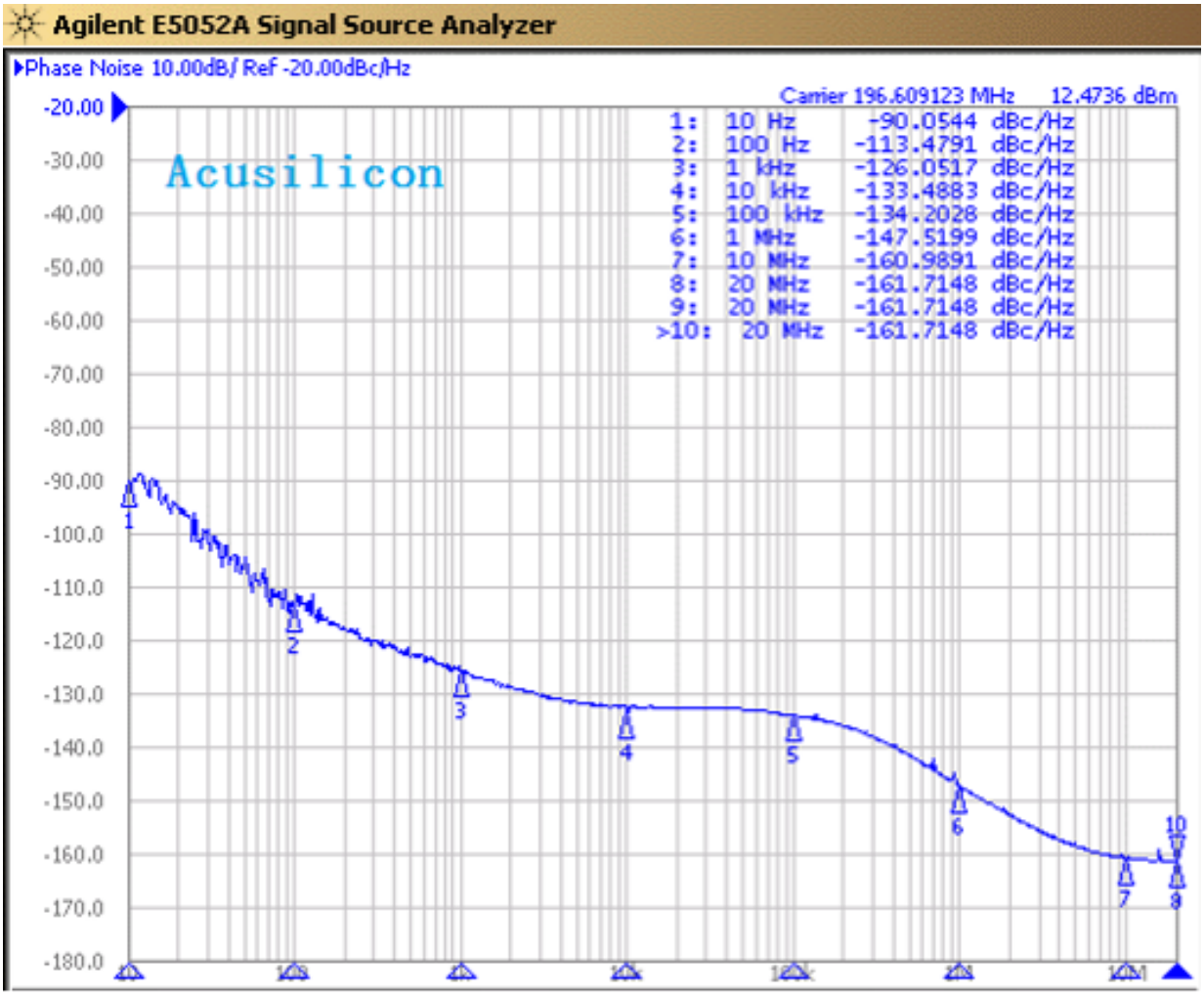
Absolute Phase Noise f0 = 196.608 MHz @ Clock Generator Mode

Parameter	Description	Min	Typical	Max	Unit
PN	1 Hz				dBc
	10 Hz		-90		dBc
	100 Hz		-113		dBc
	1 kHz		-126		dBc
	10 kHz		-133		dBc
	100kHz		-134		dBc
	1 MHz		-147		dBc

Absolute Phase Noise f0 = 196.608 MHz @ PLL Mode (Input fs = 44.1 kHz/ 0.1Hz Bandwidth)

Parameter	Description	Min	Typical	Max	Unit
PN	1 Hz		-50		dBc
	10 Hz		-75		dBc
	100 Hz		-105		dBc
	1 kHz		-121		dBc
	10 kHz		-127		dBc
	100kHz		-131		dBc
	1 MHz		-142		dBc

Typical Clock output Phase Noise Performance @ Clock Generator Mode



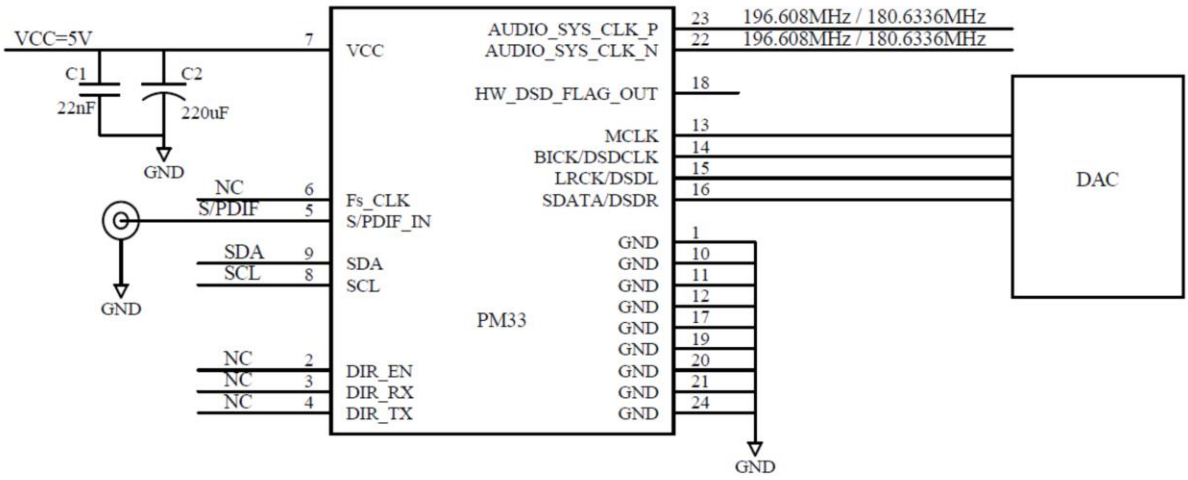
Output = 196.608MHz 3.3V LVCOMS

10Hz to 1MHz Phase Jitter @ f0=196.608MHz: 149fs

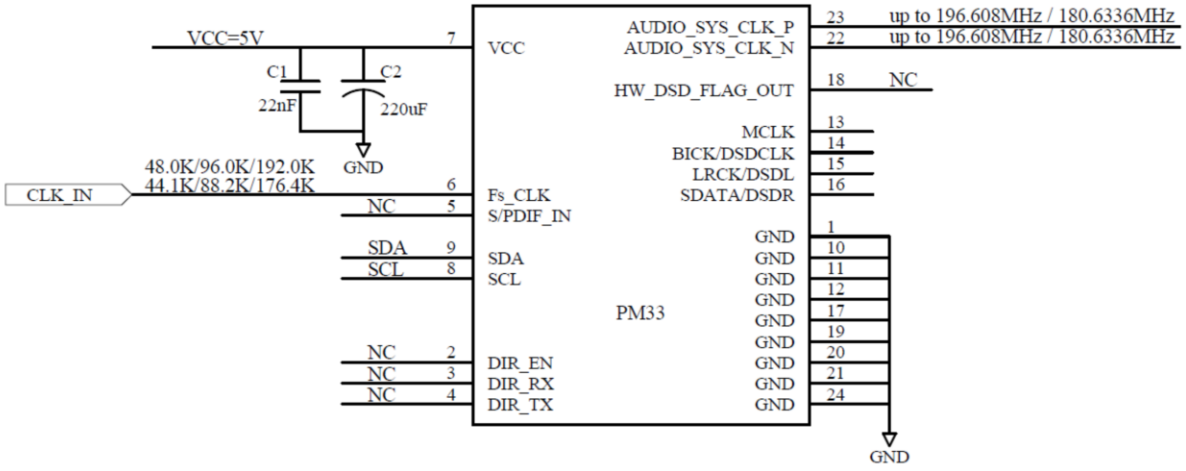
100Hz to 1MHz Phase Jitter @ f0=196.608MHz: 126fs

Typical Application

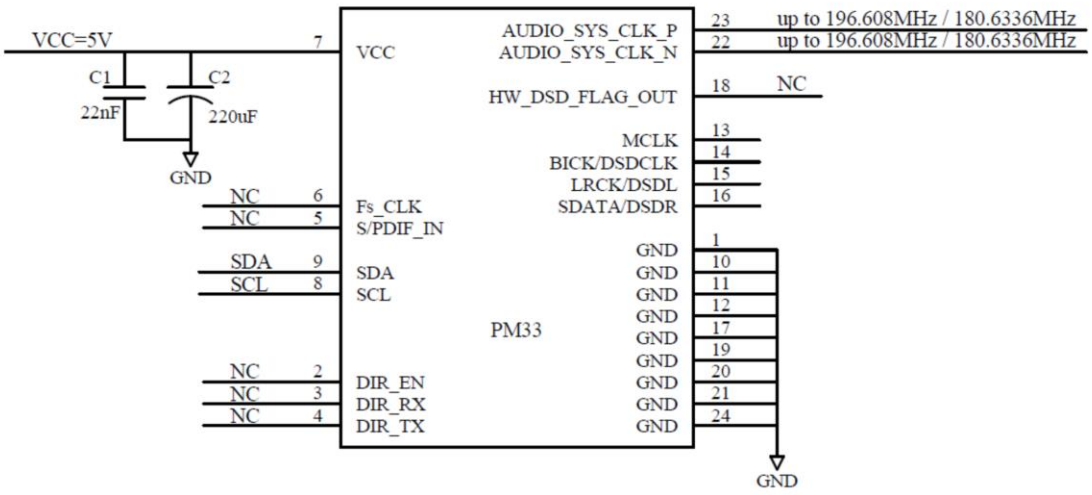
TYPICAL APPLICATION of S/PDIF MODE



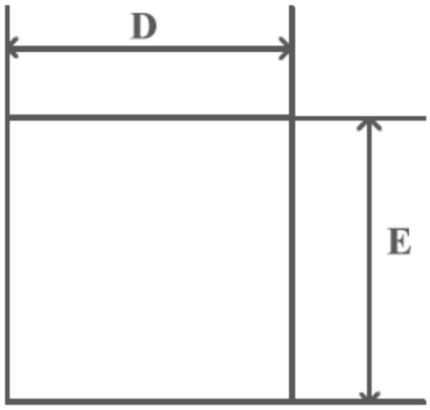
TYPICAL APPLICATION of PLL MODE



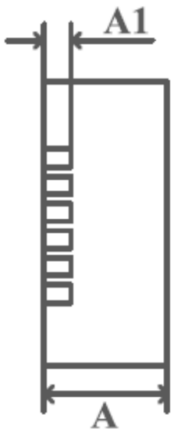
TYPICAL APPLICATION of CLOCK GENERATOR MODE



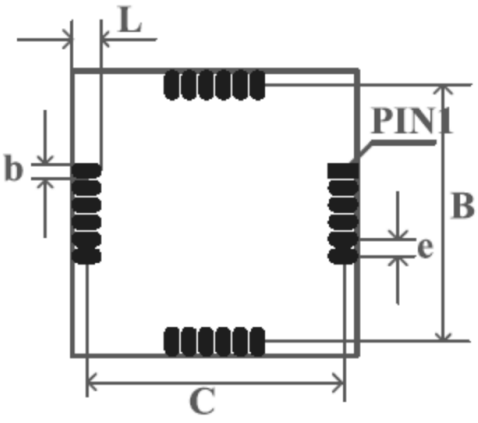
Package Outlines



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters	
	Min	Max
A	8.5	8.7
A1	1.55	1.65
B	36	
C	36	
D	40	
E	40	
e	3	
b	2	2.2
L	5	6

PCB Land Pattern