

# The ZedBoard Development Platform for Embedded Systems

A Theme Based Project Report submitted in partial fulfilment of  
the academic requirement for the award of the degree of

**BACHELOR OF ENGINEERING**

In

**ELECTRONICS AND COMMUNICATION ENGINEERING**

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*2021-2025*



## Department of Electronics and Communication Engineering

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#### CERTIFICATE

This is to certify that the theme-based project work title: "The ZedBoard Development Platform for Embedded Systems"

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students of the Electronics and Communication Engineering Department, Vasavi College of Engineering in partial fulfilment of the requirement for the award of the degree of Bachelor of Engineering in Electronics and Communication Engineering is a record of the bonafide work carried out by them during the academic year 2024-2025. The result embodied in this theme-based project report has not been submitted to any other university or institute for the award of any degree.

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## **DECLARATION**

This is to state that the work presented in this theme-based project report titled “The ZedBoard Development Platform for Embedded Systems” is a record of work done by us in the Department of Electronics and Communication Engineering, Vasavi College of Engineering, Hyderabad. No part of the thesis is copied from books/journals/internet and wherever the portion is taken, the same has been duly referred to in the text. The report is based on the project work done entirely by us and not copied from any other source. I hereby declare that the matter embedded in this thesis has not been submitted by me in full or partial thereof for the award of any degree/diploma of any other institution or university previously.

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## ABSTRACT

The ZedBoard development board is a flexible platform that combines software and hardware features to speed up embedded system development and prototyping. By integrating Xilinx's Zynq-7000 All Programmable System-on-Chip (SoC), the Zed Board enables both enthusiasts and engineers to investigate the combination of conventional processing units with programmable logic.

From Internet of Things (IoT) devices to industrial automation, this abstracted environment offers a platform

for creativity in a wide range of applications. The ZedBoard's extensive range of interfaces and peripherals, such as HDMI, USB, and Ethernet, increases its usefulness in a variety of applications, and its interoperability with industry-standard development tools promotes a smooth integration into Current workflows.

The ZedBoard is a conduct for revolutionary exploration in the field of embedded systems development because it strikes a balance between accessibility and intricacy. Its ability to connect hardware and software allows artists to more effectively realise their ideas, pushing the boundaries of technical innovation.

Our Main Aim is to design a zed board from the scratch and understand the Allegro  
Allegro is the software we are using to design the zed board.

In between we are using capture cis for schematics Padstack Editor for pads and PCB editor for footprints

Generating a expected 3D model of zed board

Generating Gerbers files for the board using allegro

## CHAPTER-1: INTRODUCTION

### 1.1 Project Description:

The ZedBoard is a popular development board that integrates the Xilinx Zynq-7000 All Programmable System-on-Chip (SoC), combining the flexibility of a software-programmable processor with the parallel processing power of an FPGA (Field-Programmable Gate Array). This unique architecture allows for the implementation of custom hardware accelerators and real-time processing capabilities, making it ideal for a wide range of embedded applications.

Incorporating the ZedBoard into the project enhances its capabilities, providing developers with a robust platform for prototyping and deploying advanced embedded systems solutions. With its rich set of interfaces including HDMI, USB, Ethernet, and more, the ZedBoard offers unparalleled flexibility for connecting peripherals and expanding functionality. By leveraging the features of the ZedBoard and Allegro PCB Editor, the project aims to create a cutting-edge development board that pushes the boundaries of embedded systems innovation.

### 1.2 Aim of the project:

Design and manufacture an zedboard (Zynq Evaluation & Development Board) with comprehensive capabilities, ensuring functionality and efficiency.

### 1.3 Objective of the project:

The objective of the "Design of ZedBoard Development Board using Allegro" project is to create an optimized and reliable PCB layout for the ZedBoard, leveraging the advanced capabilities of Allegro PCB Editor.

The following could be the goals of a project centred around the ZedBoard Development Board:

- Enhanced Performance: Designing the PCB layout to ensure optimal signal integrity, power distribution, and thermal management, thereby enhancing the overall performance of the ZedBoard.
- Component Placement: Strategically placing components on the board to minimize signal interference, reduce trace lengths, and optimize the use of available space.
- Routing: Implementing efficient routing techniques to maintain signal integrity, reduce electromagnetic interference, and ensure compatibility with industry standards.
- Design Validation: Performing thorough design validation and testing to ensure that the PCB layout meets the required specifications and standards.
- Documentation: Creating comprehensive documentation of the PCB layout, including schematics, layout files, and design notes, to facilitate future modifications and troubleshooting.

**Outreach to Education:** Encourage the use of the ZedBoard in learning environments by developing This goal is to equip the upcoming generation of inventors and engineers with the abilities and know-how required to be successful in their chosen fields. **Application-Specific Development:** Promote the creation of creative projects and programmes that make use of the ZedBoard's capabilities in a range of fields, including industrial automation, robotics, signal processing, and the Internet of Things. In order to achieve this goal, it will be necessary to present case studies of accomplished projects, offer advice and assistance to developers, and foster teamwork on innovative and engaging platform applications. **Market Adoption and Expansion:** By focusing on new markets, sectors, and user groups, ZedBoard can increase its reach and adoption. This could entail product positioning, marketing campaigns, and strategic alliances to draw attention to the ZedBoard's distinctive value proposition and draw in new users and clients.

By focusing on the ZedBoard Development Board, a project can equip users and developers with the resources and tools they need to succeed, foster innovation and creativity in the area, and contribute to the further evolution and improvement of embedded systems development.

## **1.4 Software Used:**

### **1. ALLEGRO PCBDESIGNER**

Cadence Design Systems created Allegro PCB Designer, a feature-rich printed circuit board (PCB) design programme. Engineers and PCB designers use it extensively while creating, routing, and analysing intricate PCB layouts for a range of electrical systems and gadgets. The following are some of Allegro PCB Designer's main attributes and capabilities:

**Schematic Capture:** To develop and modify schematic diagrams for their electronic circuits, designers can utilise Allegro PCB Designer's robust schematic capture feature. For a smooth workflow, it facilitates netlist generation, hierarchical design, and connection with other EDA tools.

**PCB Layout Design:** With the software's sophisticated PCB layout design features, designers may arrange parts, route traces, specify power and signal planes, and control design limitations.

Design constraints, such as manufacturing, timing, and electrical ones, can be defined and managed by designers with the aid of Allegro PCB Designer's powerful constraint management features. It enables constraint-driven design to guarantee that the finished PCB layout satisfies all requirements.

**Signal Integrity Analysis:** With the software's integrated features, designers may assess and enhance the electrical performance of their PCB designs. This covers functions like timing analysis, crosstalk analysis, impedance computation, and high-speed signal simulation.

**Power Integrity Analysis:** Another feature that Allegro PCB Designer offers is the ability to analyse and optimise the power distribution network of PCB designs.



**Fig 1: Allegro PCB Editor**

## CHAPTER-2: LITERATURE REVIEW

### INTRODUCTION

In the modern world, the power requirement is increasing exponentially. This creates space for research in circuitry where high current and high voltage can be handled efficiently without much interference, maintaining the reliability, precision, and reduction in the losses. EMI (Electromagnetic Interference) and EBG (Electromagnetic Bandgap) are important aspects. This is studied by PEEC (partial element equivalent circuit) technique, here spate layers are used for shielding that is not economically fusible. Which can be replaced by an external metallic enclose that helps in EMI and EBG shielding. In synchronous buck converter is studied using an electrothermal circuit design. Which uses the thermoelectric cooler to reduce the temperature by 3-5 degree C for the same electro thermal trace.

#### i. OVERVIEW: subheading considerations in footprints

Designing the schematic and producing netlist is pre place and route task. The next most important step is termed as place i.e. placing the footprints.

1. Placement of footprints is done in a way such that minimum path resistance and length is achieved between two connecting points on a PCB. For this rotating the footprint and flipping are done to adjust or move it to another side of the board respectively.
2. One important point to be taken care of is separating the components or spreading them on the basis of the number of ground planes present on the board. To assure proper grounding and isolation between ground planes.
3. When high voltage components and high current carrying components are placed, make sure to leave enough clearance between them for proper isolation in case of high voltage components and to have enough space for wide traces in case of high current carrying components. Also done to make sure proper cooling in case of high current-carrying components.

#### ii. THERMAL CONSIDERATION

Thermal relief and proper heat sinking techniques in PCB designing.

1. When in a footprint the pad that is used to connect the components to the PCB by soldering if it doesn't require high current to flow through that connection. In such cases, the pad is connected to a plane using a thin cross-shaped connection the techniques are Copper thickness of the PCB is increased to increase the cross-sectional area of the conductor usually measured in ounces of copper deposited.

## CHAPTER-3: METHODOLOGY

### 3.1 Working:

The ZedBoard development board operates as a versatile platform for prototyping and developing embedded systems, leveraging the power of the Xilinx Zynq-7000 All Programmable System-on-Chip (SoC). Here's an overview of how the ZedBoard works:

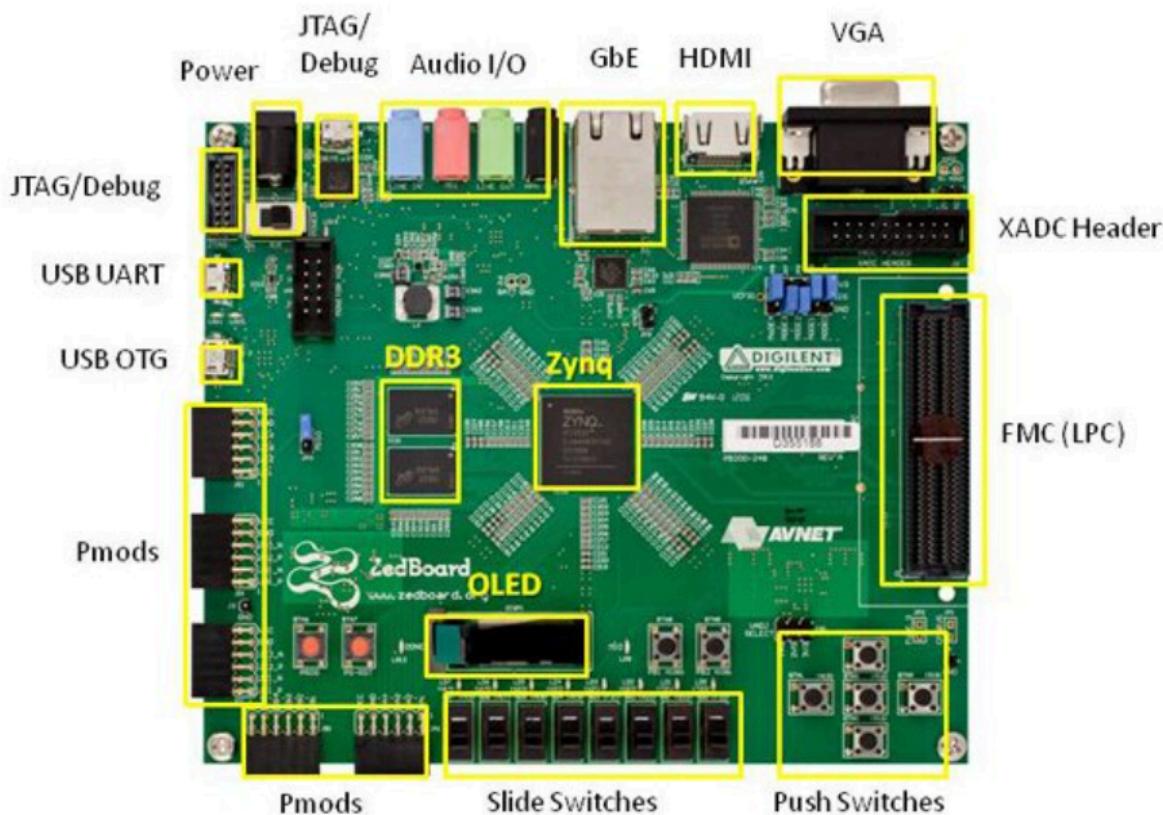
1. Hardware Configuration: The ZedBoard consists of a combination of hardware components, including the Zynq-7000 SoC, various onboard peripherals (such as HDMI, USB, Ethernet, audio, and GPIO), memory modules (typically DDR3 SDRAM), and expansion connectors (such as PMOD, FMC, and Arduino-compatible headers). These components are interconnected on a printed circuit board (PCB) and provide the foundation for building embedded systems.
2. Zynq-7000 SoC: At the core of the ZedBoard is the Zynq-7000 SoC, which integrates dual-core ARM Cortex-A9 processors with programmable logic (FPGA fabric) in a single chip. This unique architecture allows developers to combine the processing power of the ARM cores with the flexibility and customization of the FPGA fabric to implement a wide range of applications.
3. Developers can utilize software development tools like Xilinx Vivado Design Suite and SDK to program the ZedBoard. Vivado is for FPGA design, synthesis, and implementation, while SDK is for writing and debugging software for ARM Cortex-A9 processors.
4. FPGA Programming: The FPGA fabric on the Zynq-7000 SoC can be programmed using hardware description languages (HDL) such as Verilog or VHDL. Developers can design custom hardware accelerators, interfaces, or processing pipelines in the FPGA fabric to offload tasks from the ARM processors and improve system performance.
5. Software Execution: Once the FPGA fabric is programmed and the software application is developed, the ZedBoard can execute the application by running it on the ARM Cortex-A9 processors. The ARM

processors handle tasks such as running the operating system (e.g., Linux), managing system resources, and executing high-level software algorithms.

6. Integration and Expansion: The ZedBoard offers various expansion interfaces, such as PMOD, FMC, and Arduino-compatible headers, allowing developers to connect additional peripherals, sensors, or expansion modules to extend the capabilities of the board. This enables the development of complex embedded systems that require multiple I/O interfaces and processing resources.

7. Testing and Debugging: Throughout the development process, developers can use built-in debugging tools and instrumentation features to test and debug their hardware and software designs. This includes features such as JTAG debugging, logic analyzer, and software debugging tools provided by the SDK.

Overall, the ZedBoard development board provides a flexible and powerful platform for prototyping and developing embedded systems, enabling developers to leverage the integration of ARM processors and FPGA fabric to implement custom solutions for a wide range of applications. Whether for IoT devices, robotics, signal processing, or industrial automation, the ZedBoard offers the versatility and scalability needed to bring innovative ideas to life.



**Fig 2.1 SD card and QSPI Flash reside on back side of the board**

### **3.2 *Flowchart:***

Schematic Design: Create the schematic for the ZedBoard, including all components, connections, and signal routing.

1. Component Placement: Place components on the PCB layout according to the schematic and the physical constraints of the board.
  2. Routing: Route traces between components following best practices for signal integrity, power distribution, and EMI/EMC considerations.
  3. Routing: Route traces between components following best practices for signal integrity, power distribution, and EMI/EMC considerations
  4. Power Plane Design: Design power and ground planes to ensure proper power distribution and signal integrity. Signal Integrity Analysis: Perform signal integrity analysis to ensure that signal quality meets the required specifications.
  5. Design for Manufacturability (DFM): Check the design for manufacturability to ensure that it can be produced using the chosen fabrication process.
  6. Design for Assembly (DFA): Optimize the design for ease of assembly, considering component placement, orientation, and solderability
  7. Design for Testability (DFT): Include test points and features to facilitate testing and debugging of the Board
  8. Thermal Analysis: Perform thermal analysis to ensure that the board can dissipate heat effectively.
  - Final Design Check: Perform a final design check to ensure that all requirements have been met and that the design is ready for manufacturing.
  9. Final Design Check: Perform a final design check to ensure that all requirements have been met and that the design is ready for manufacturing
  10. Gerber File Generation: Generate Gerber files for the PCB fabrication process.
  11. Manufacturing: Send the Gerber files to a PCB manufacturer for fabrication.
  12. Assembly: Assemble the PCB with components according to the assembly drawings and bill of materials.
  13. Testing: Test the assembled PCB to ensure that it functions correctly and meets all specifications.
- Documentation

## Chapter 4. Design and Implementation

### Flow Of Solution

The project was completed in three phases step

**Step1:CREACTION OF PADS IN-PADSTACK EDITOR**

**Step 2:CREACTION OF FOOTPRINT IN PCB EDITOR**

**Step 3: LINKING SCHEMATIC (CAPTURE CIS) with pcb Editor**

**Step 4:CREACTION OF SCHEMATIC DIAGRAM**

**Step 5: PCB ROUTING**

**Step 6: linking step file**

This is used for calculation of tracewidth this plays an major role in EMI&EMC effects

$$W = \frac{\Delta T \times K \times I}{\Delta T_{\max} \times \sqrt[3]{\Delta T_{\max}}},$$

where

W is the trace width

T is the temperature rise

K is a constant

I is the current

## 4.1 Creation of Pads using Padstack editor

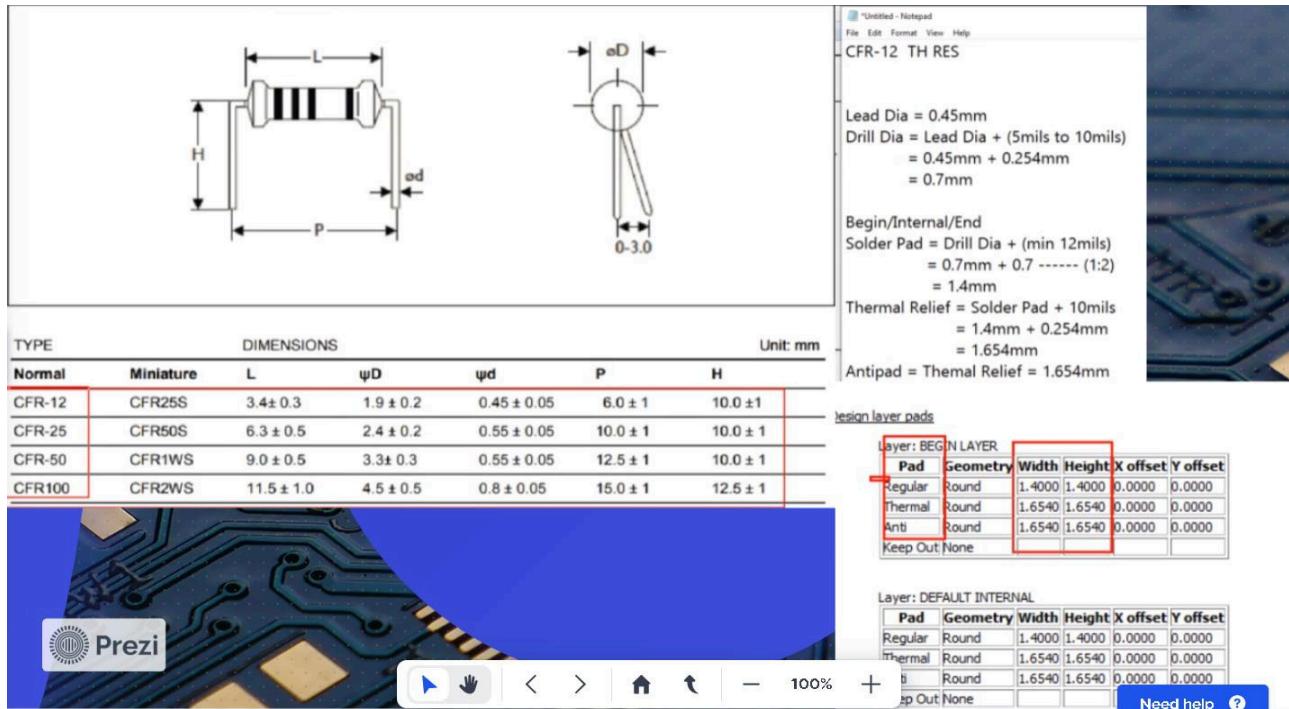
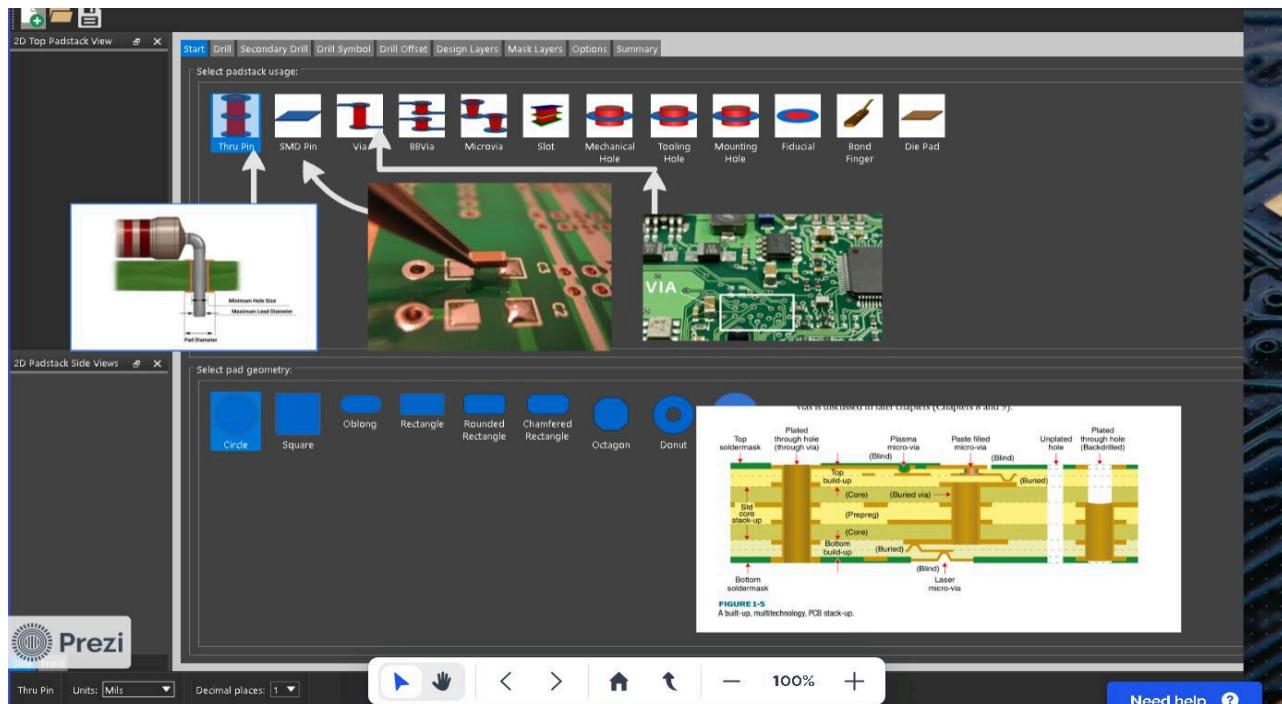
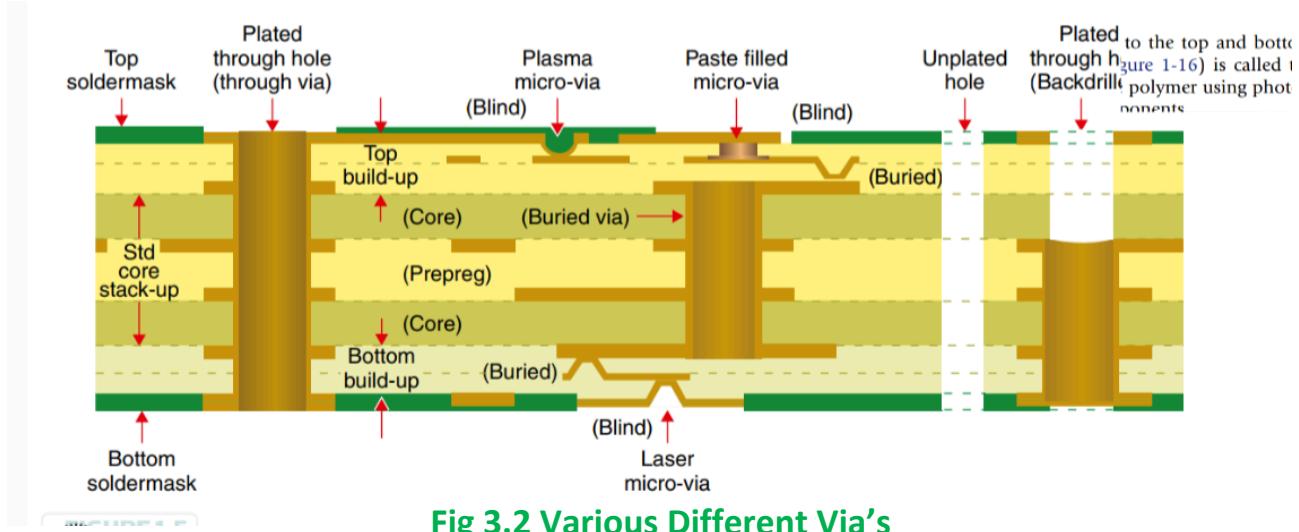


Fig 3.1 Creation of Pads using Padstack editor



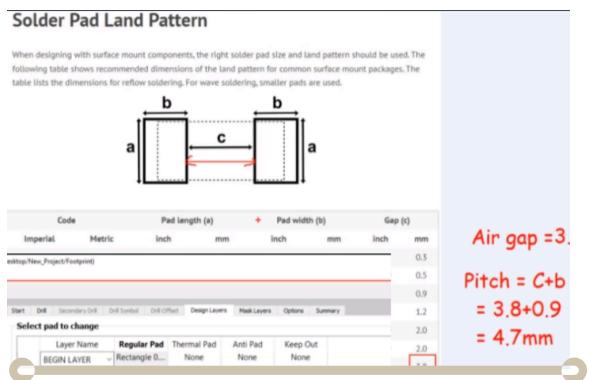
**Fig 3.2 Various Different Via's**

- 1) select thruhole, for select the default pad \*(circle, rectangle, square, any polygon)
- 2) as it is thruhole, drill diameter, drill symbol, is required
- 3) in design layer > give begin layer and end layer, default layer according to data sheet and antipad and thermal pad must be greater than regular pad
- 4) consider lead dia = 0.55 mm  
drill dia =  $0.55 + 0.254 = 0.804$  mm
- 5) begin layer =  $2 * (0.804) = 1.608$   
default layer =  $2 * (0.804) = 1.608$   
end layer =  $2 * (0.804) = 1.608$
- 6) thermal pad, antipad =  $1.608 + 0.254 = 1.862$
- 7) solder mask top, bottom =  $1.608 + 0.1524 = 1.7604$

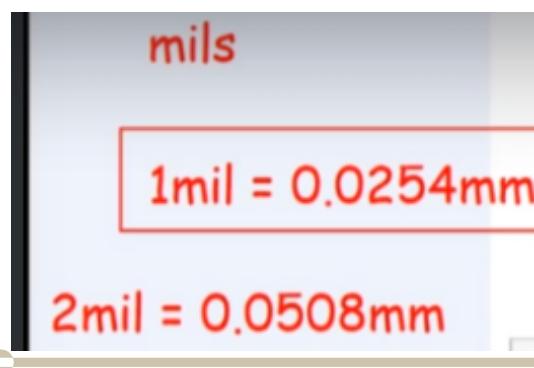
\*select padstack usage > default pad geometry > convert units into mils

\*if you are creating smd pad

you have no drill diameter > so go to design layer > set begin layer according to the datasheet  
according to ipc 27 standards maintain proper soldering mask, soldering top layer, pastemask top based on requirement, give thermal, antipad



**Fig 3.3 Calculation of Pad length**



**Fig 3.4 Conversion of mils to mm**

## 4.2 Creation of Footprint using pcb Editor

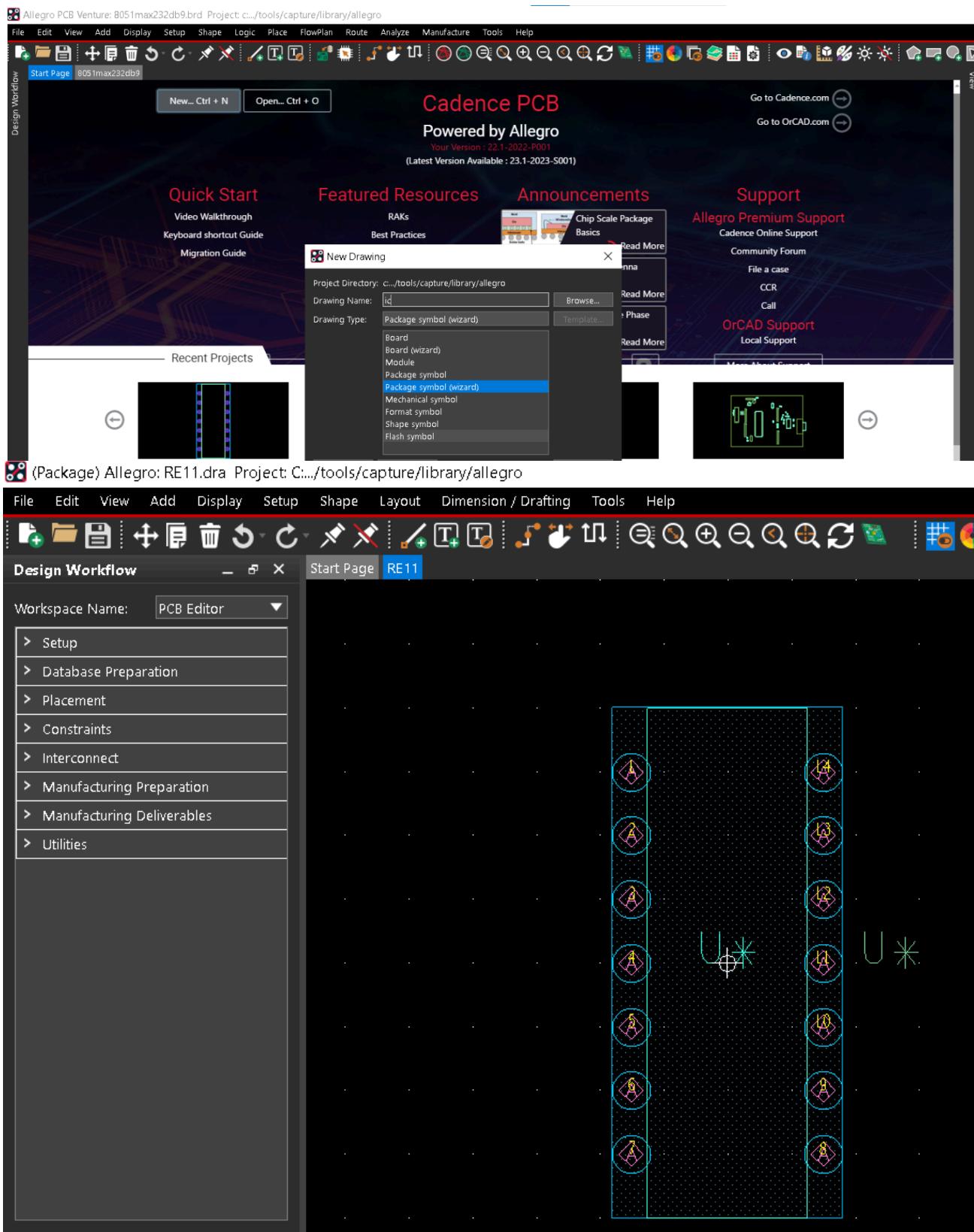
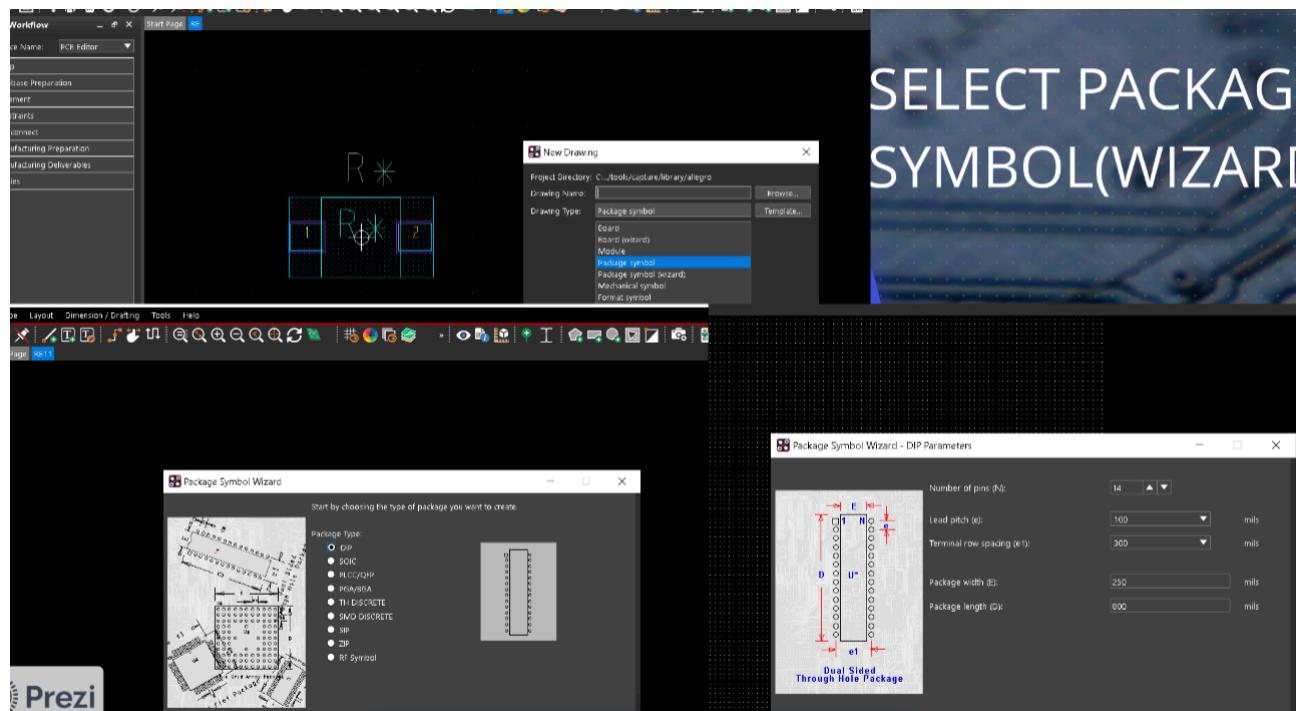


Fig 3.5.1 Creation of Footprint using pcb Editor



**Fig 3.5.2 Selecting the Drawing type in PCB Editor**

- new > board name > drawing type (package symbol (wizard))>
- select package type > load the default template of grid  
mostly mm is better option than mils > give the package length and width according to data sheet > terminal spacing > load the pad for pin 1 and for all the pins then basic footprint for the component was created
- change according to requirement before changing, follow the below steps:
  - once the pad is created according to datasheet to make footprint open allegro pcb editor > setup > design parameter > check all tick boxes > grid also > first change mils to millimeter in design > size = anything  
left x lower y is -500, -500  
width and height should be 1000, 1000. now open grid > non-etch, etch is set in accordance

## 4.3 Linking Schematic(Capture CIS) with Pcb Editor

This include both step 3,4

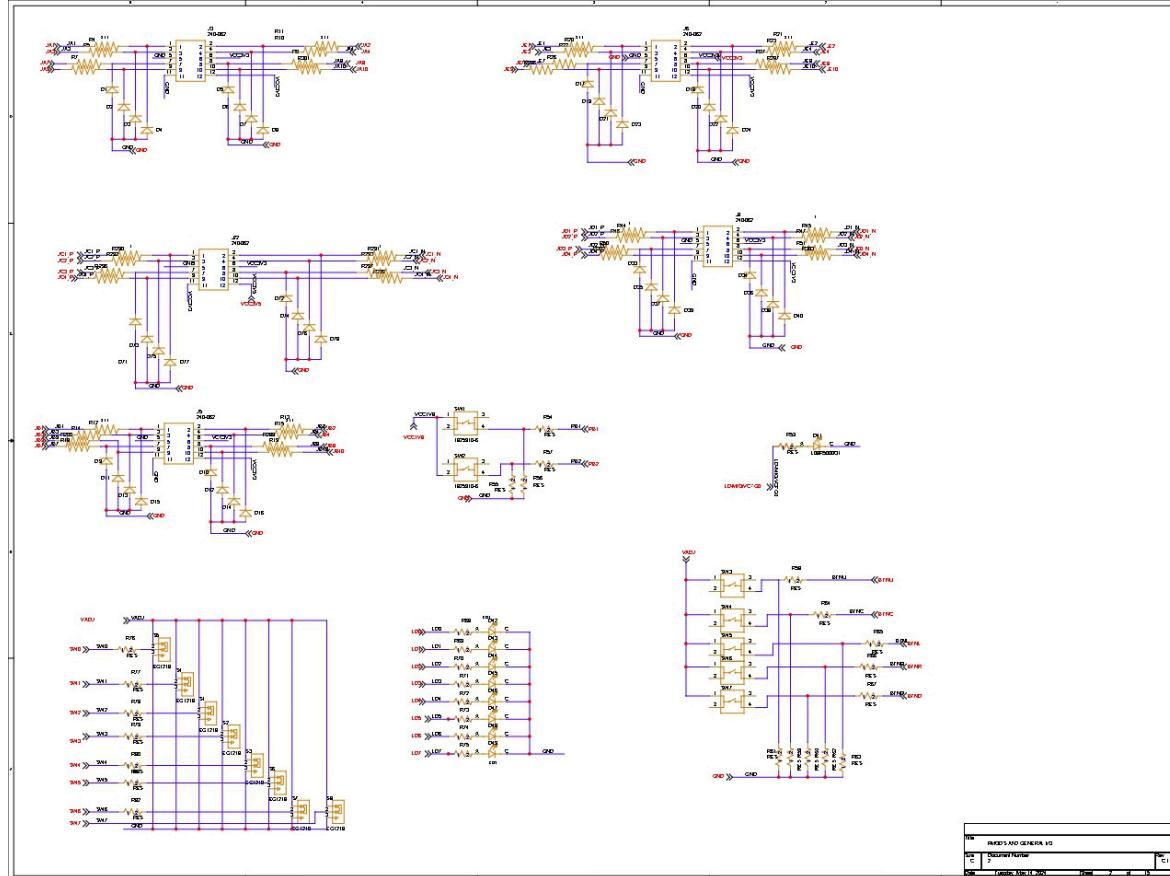
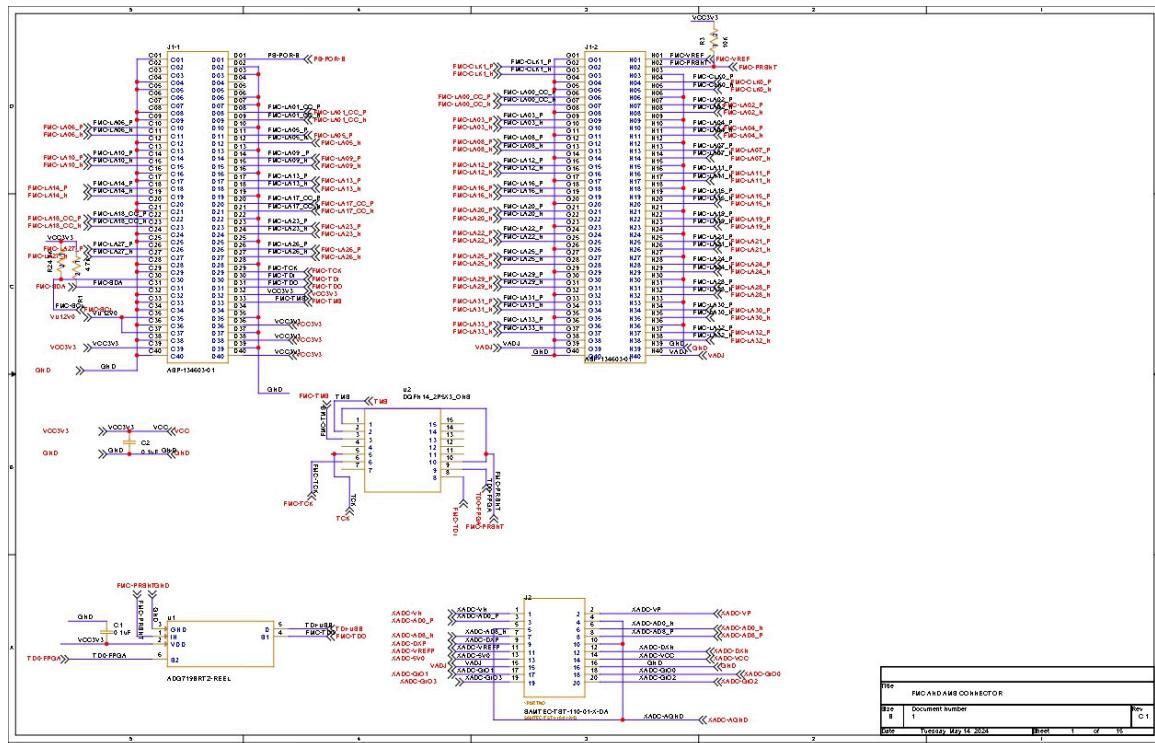
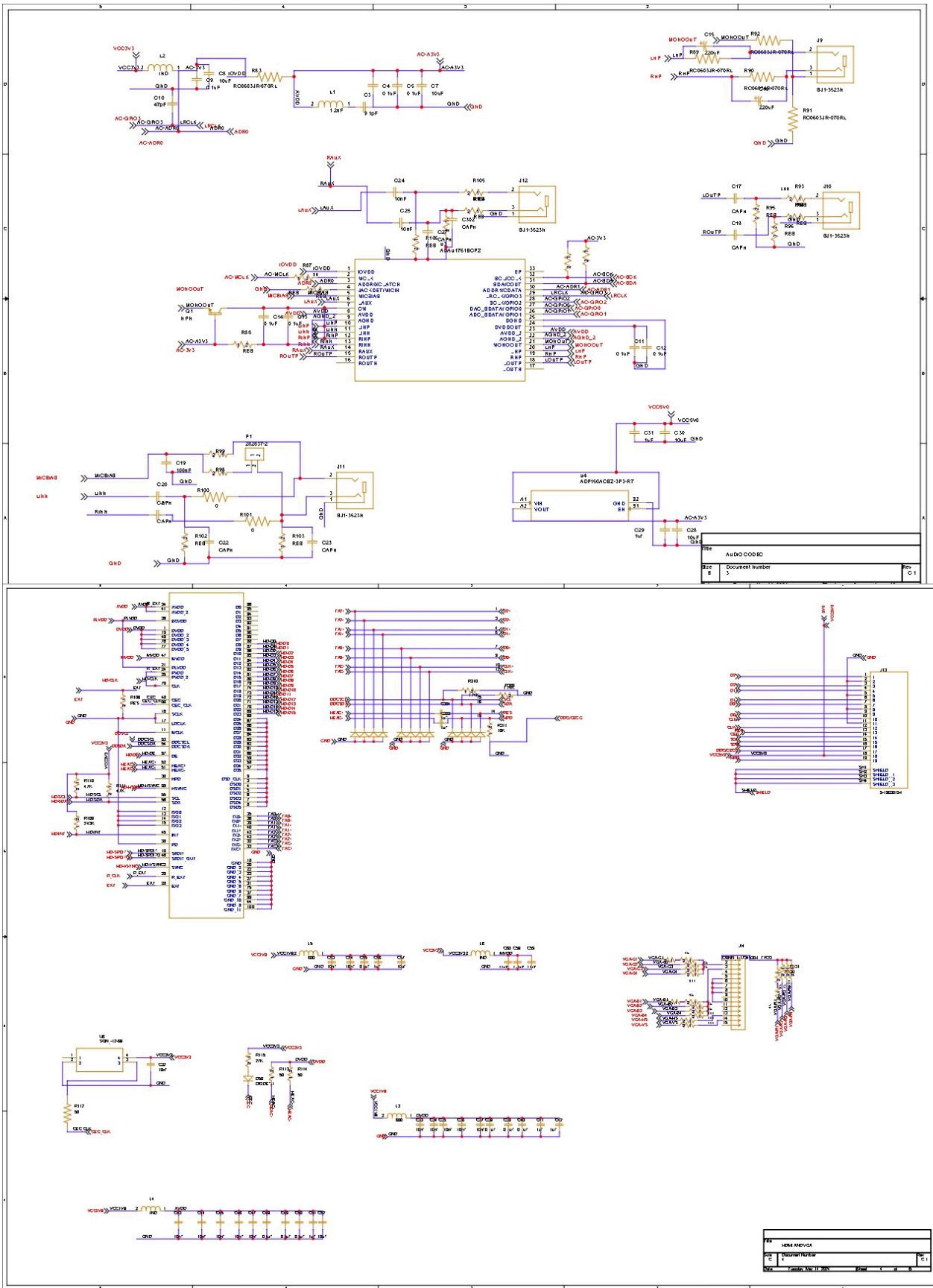
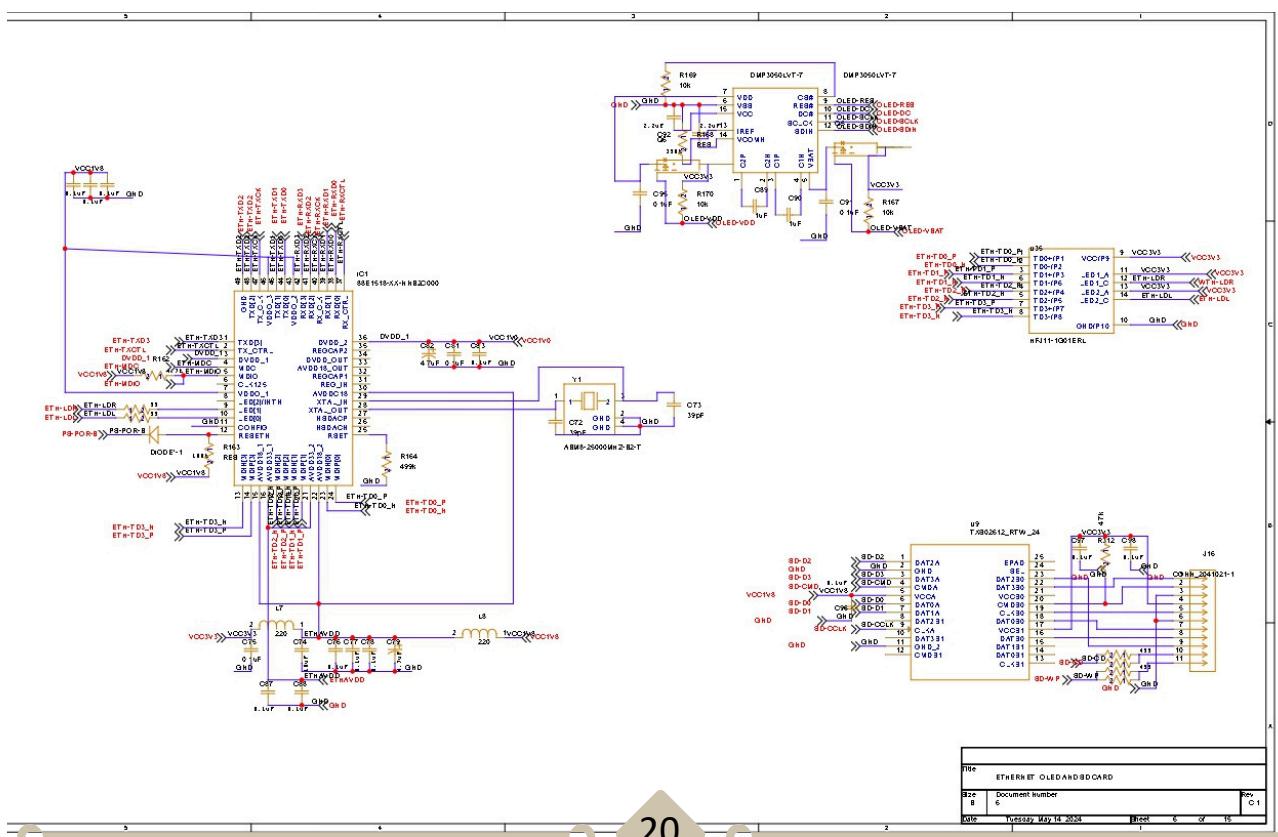
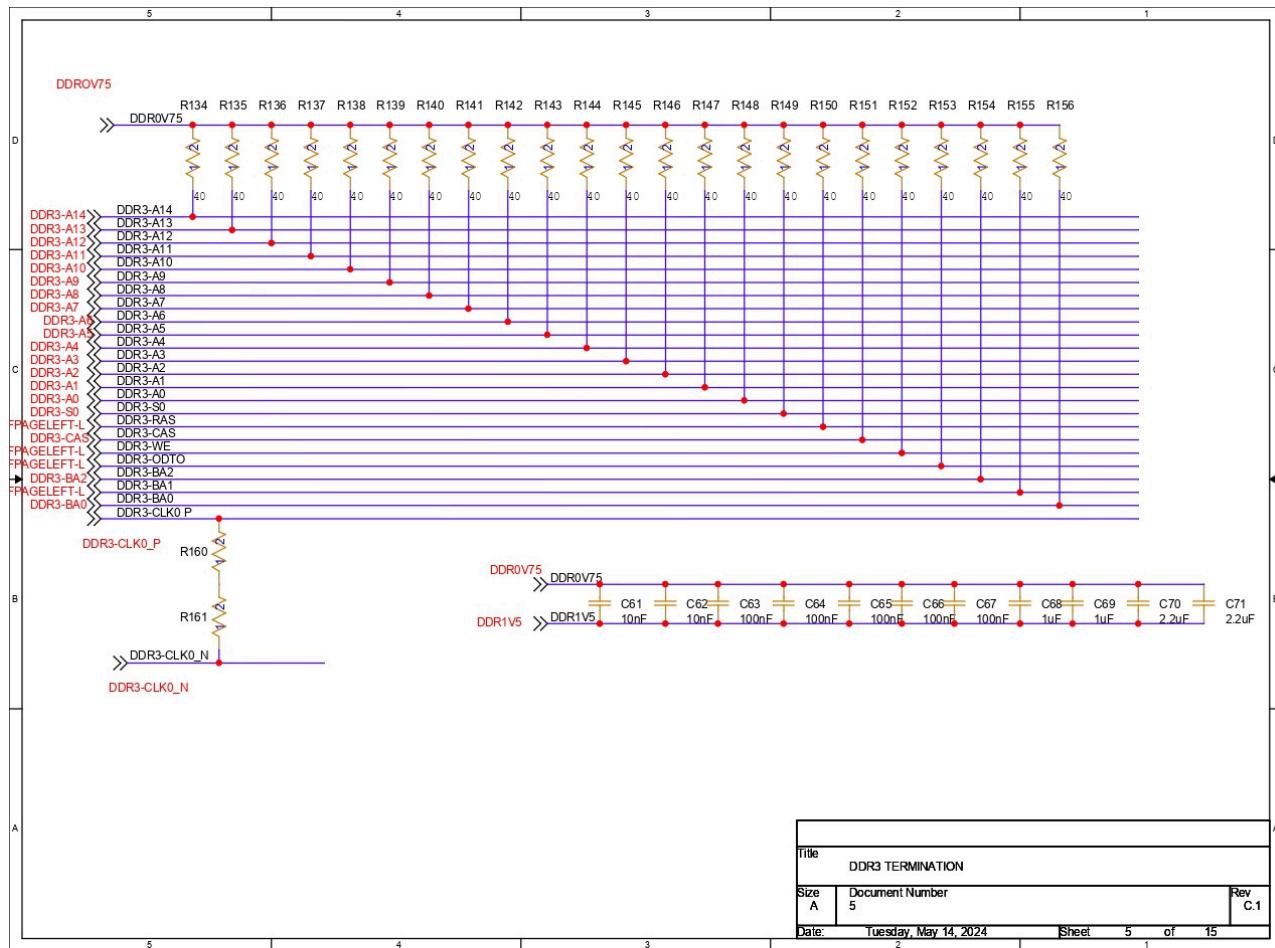


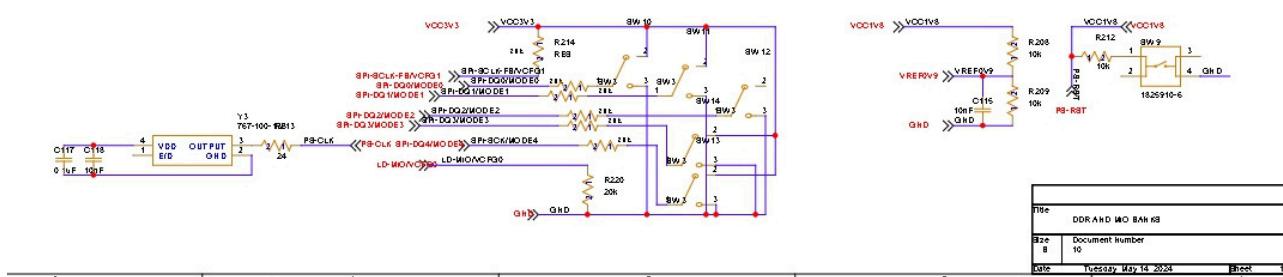
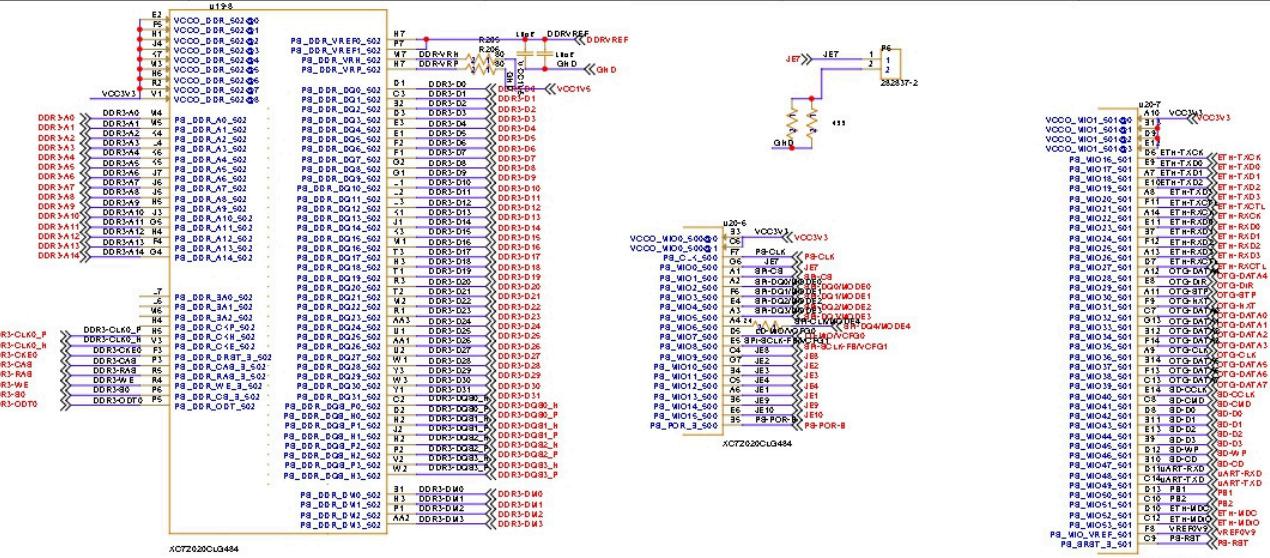
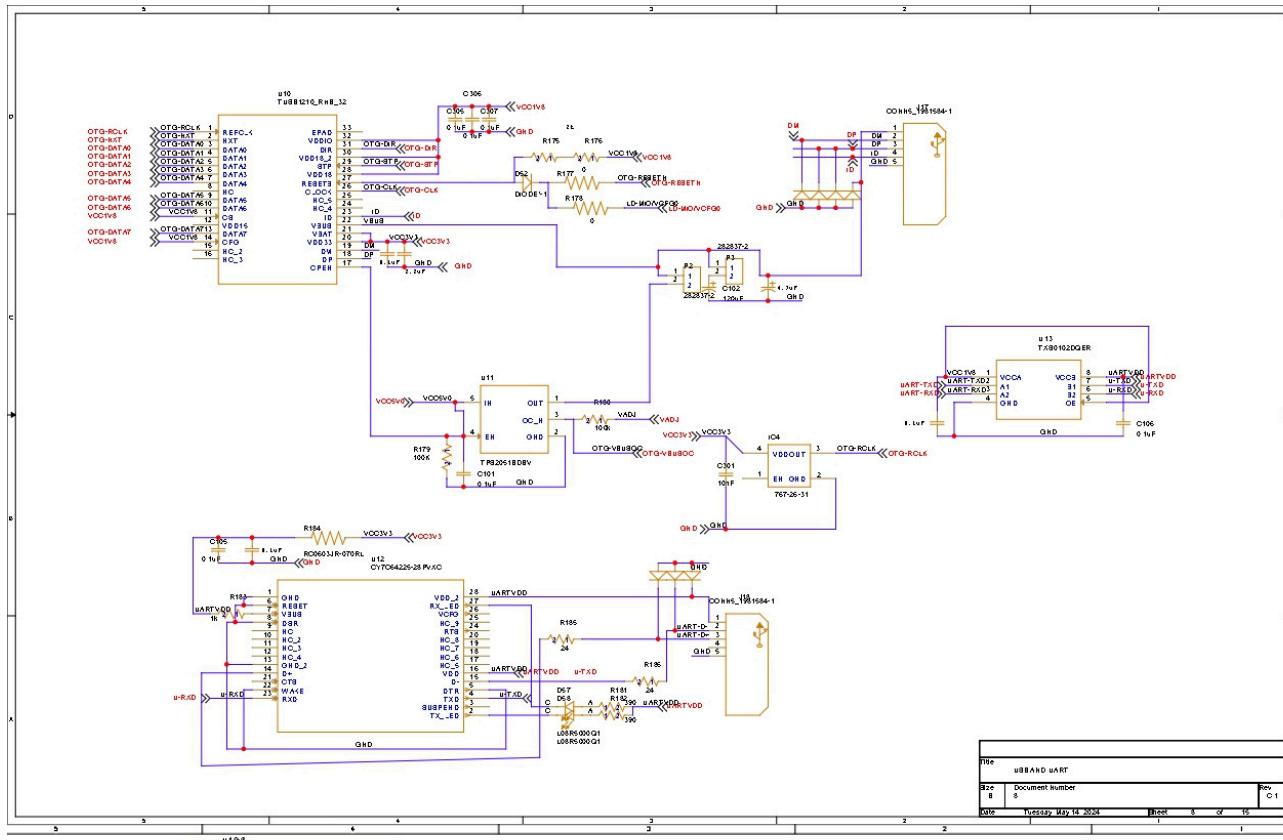
Fig 3.6.1 PMODS with general IO



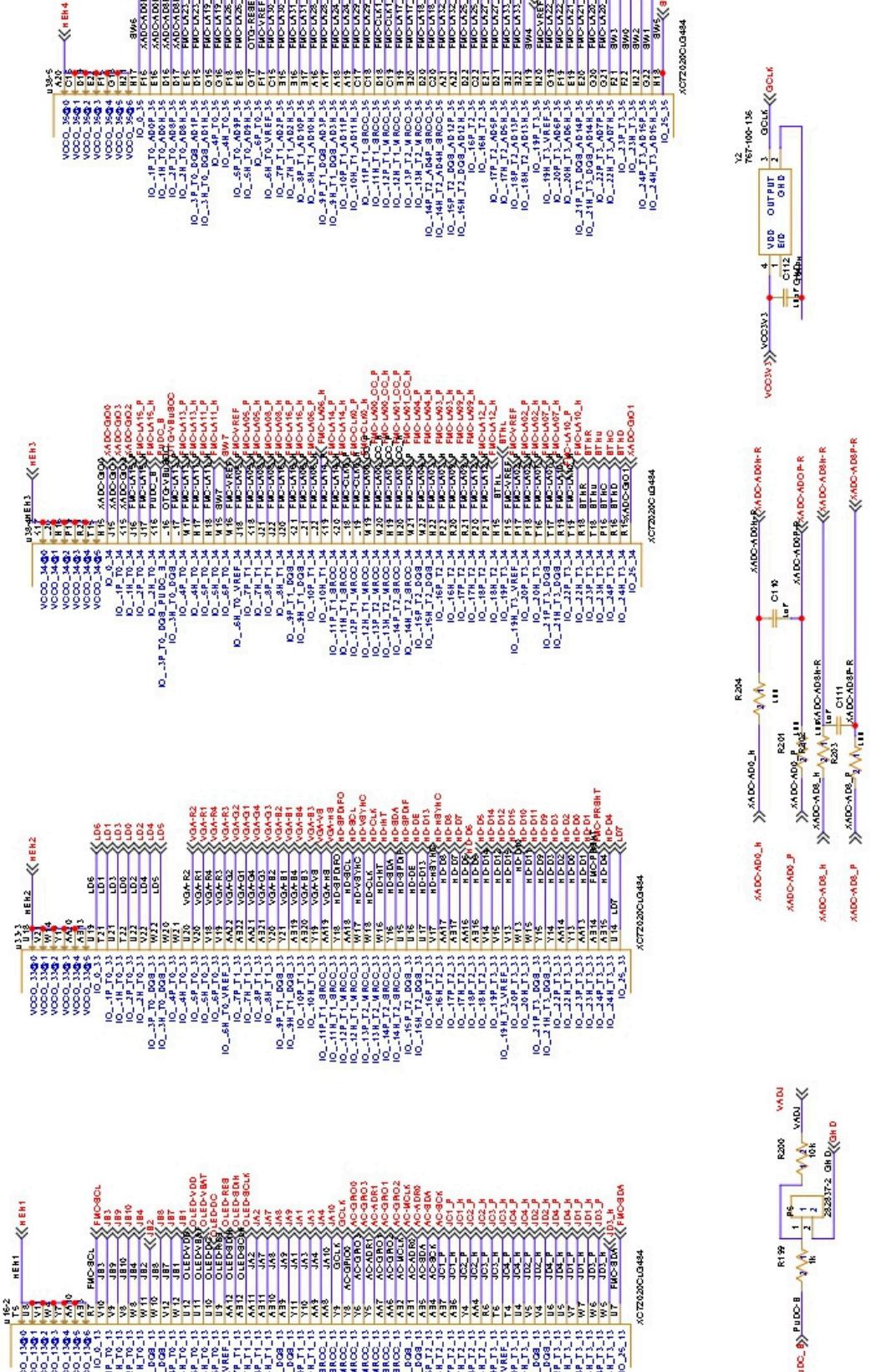
**Fig 3.6.2 Audio codac and HDMI and VGI**



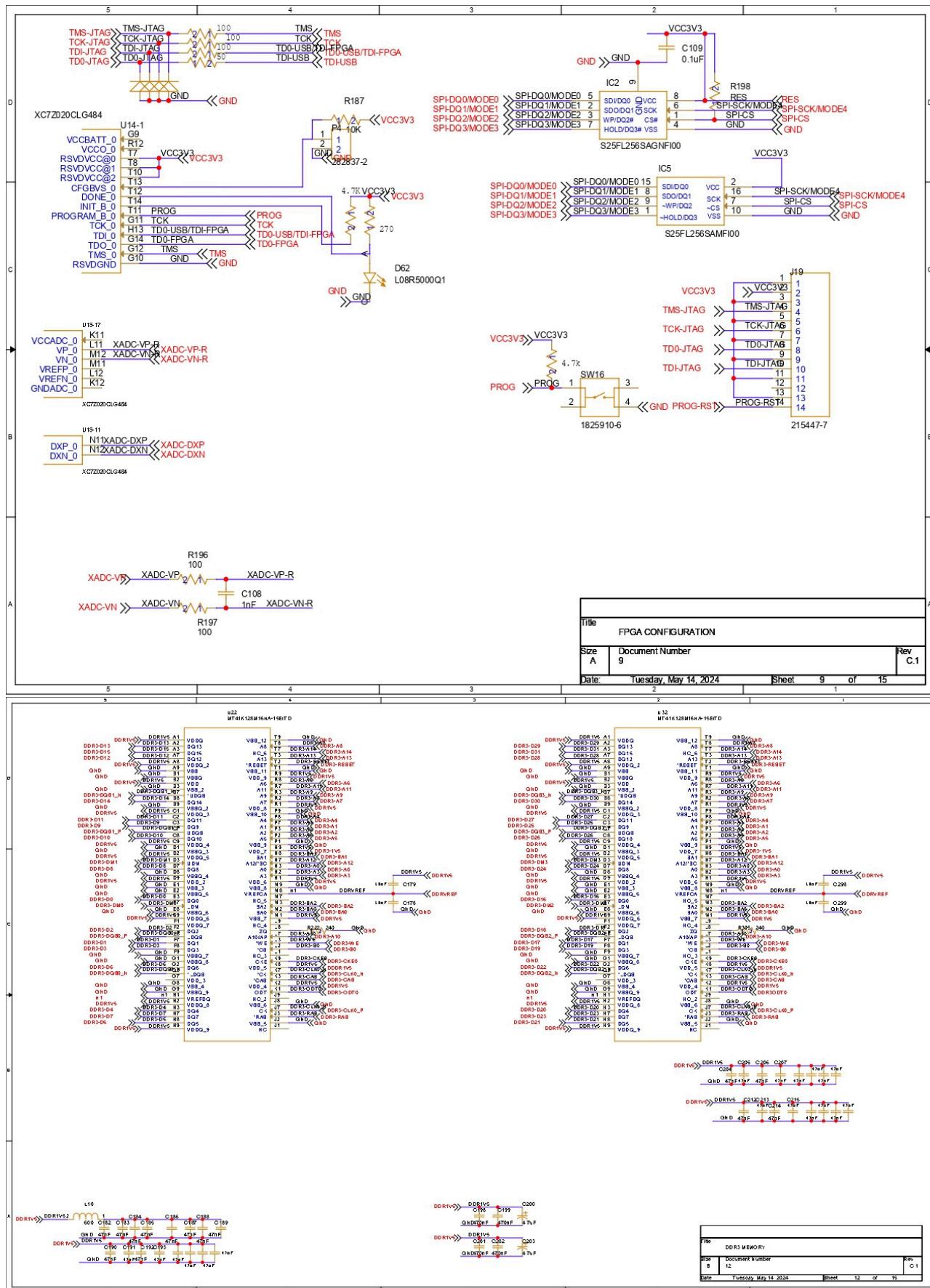
**Fig 3.6.3 DDR 3,Ethernet,OLED,SD card**



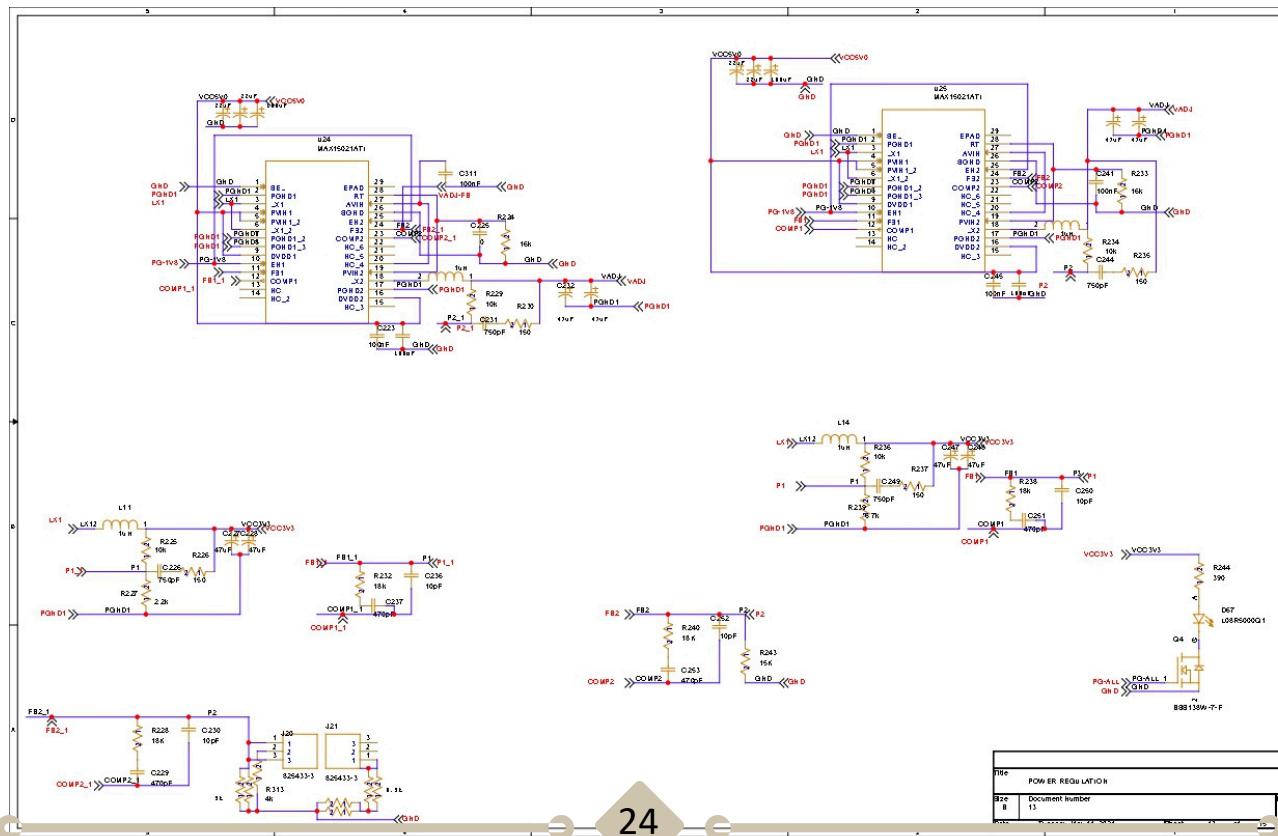
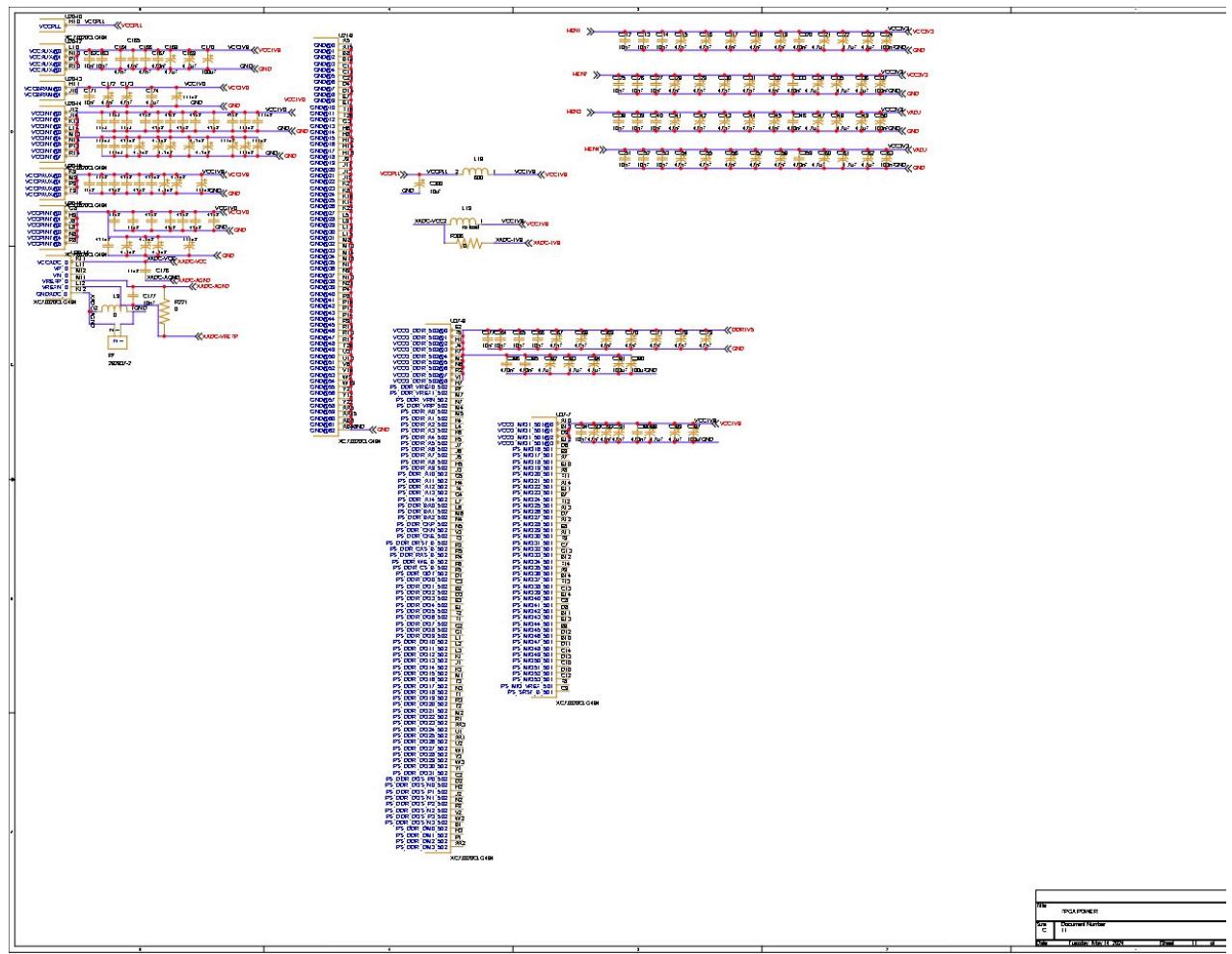
**Fig 3.6.4 USB and UART, DDR and IO bands**



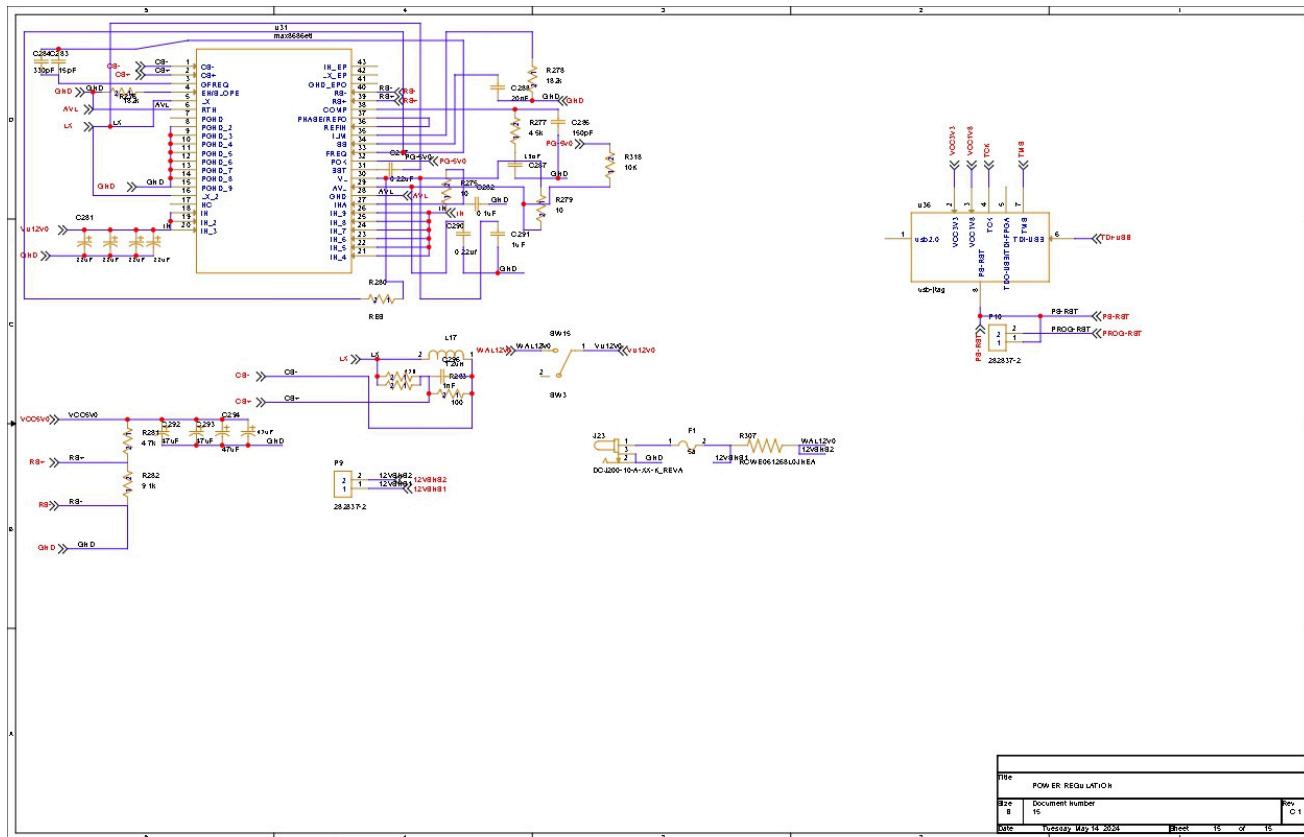
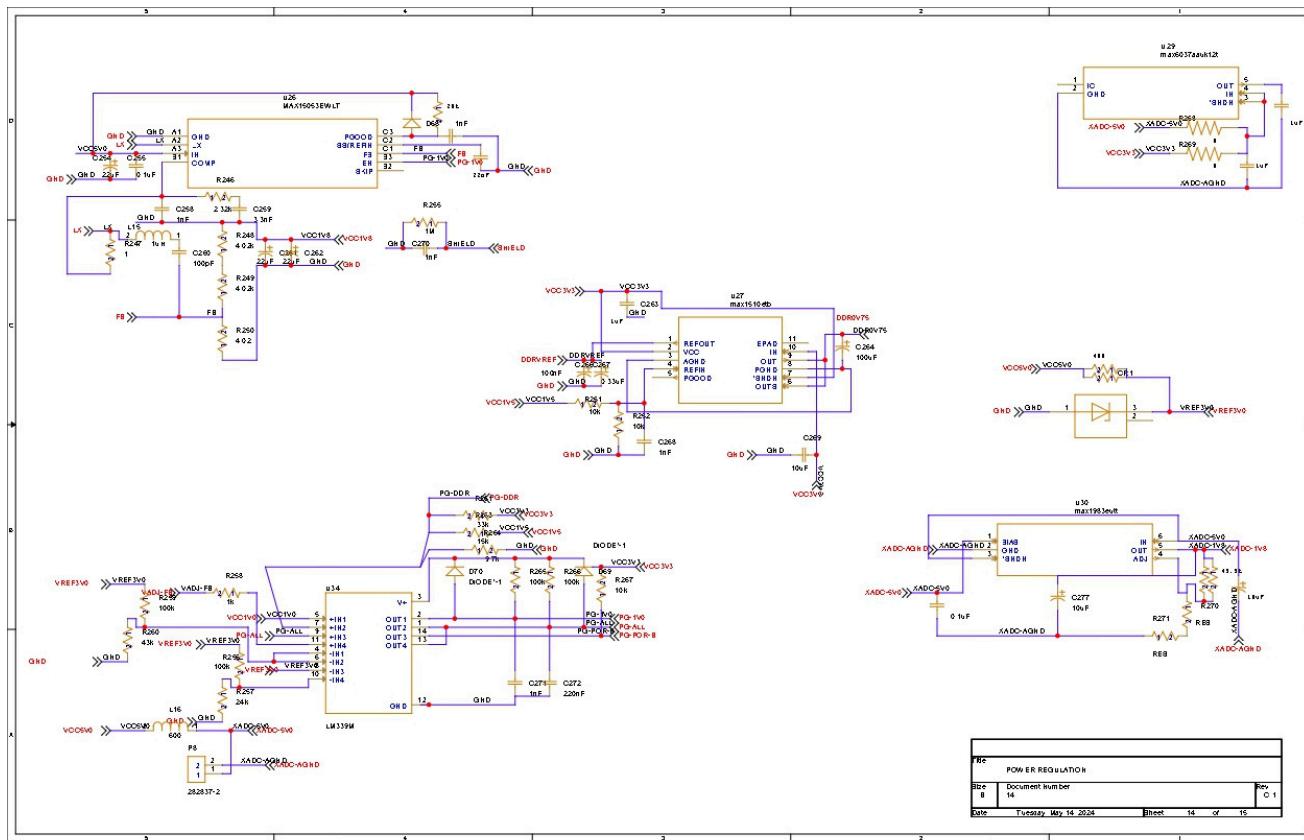
### Fig 3.6.5 FPGA Bands



**Fig 3.6.6 FPGA,DDR3 memory**



### Fig 3.6.7 FPGA power and power regulation



### Fig 3.6.8 Power Regulation

Top layer

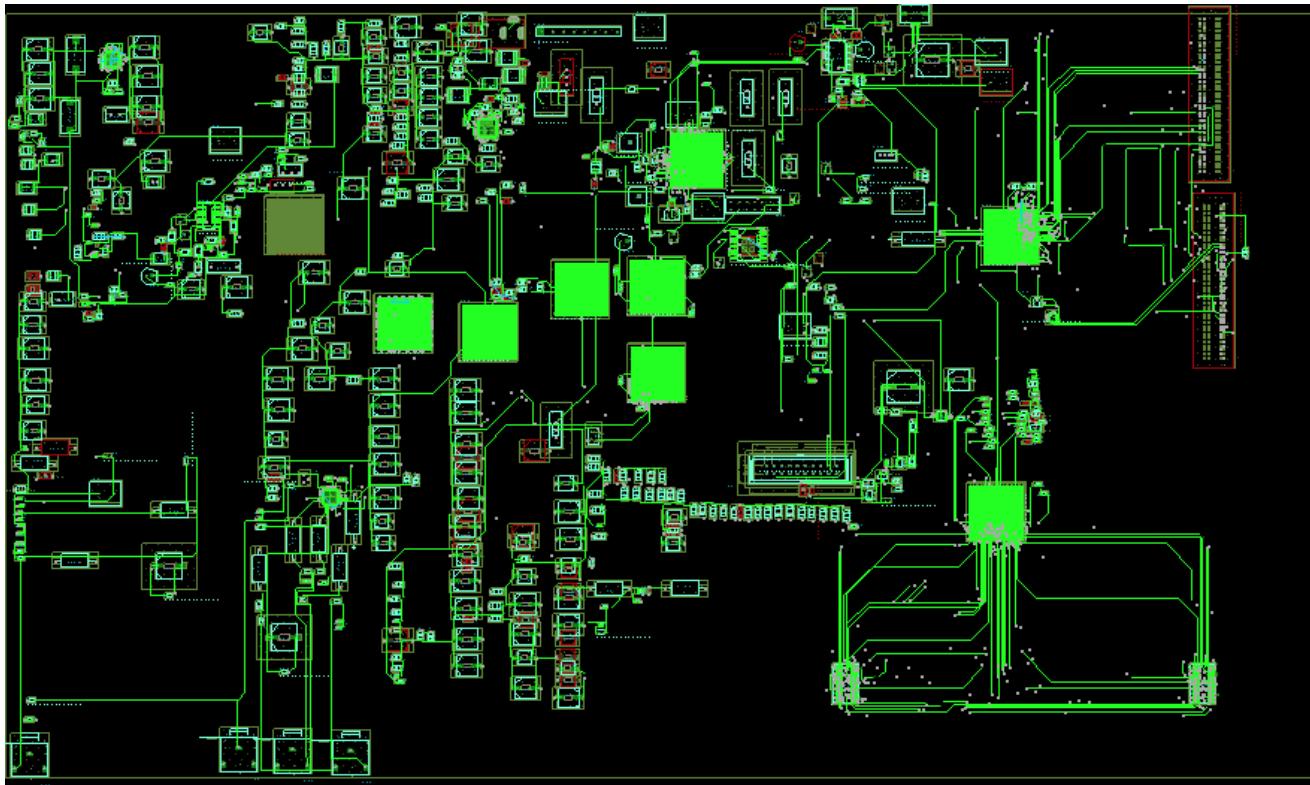


Fig 4.1 Top Layer

1st Layer

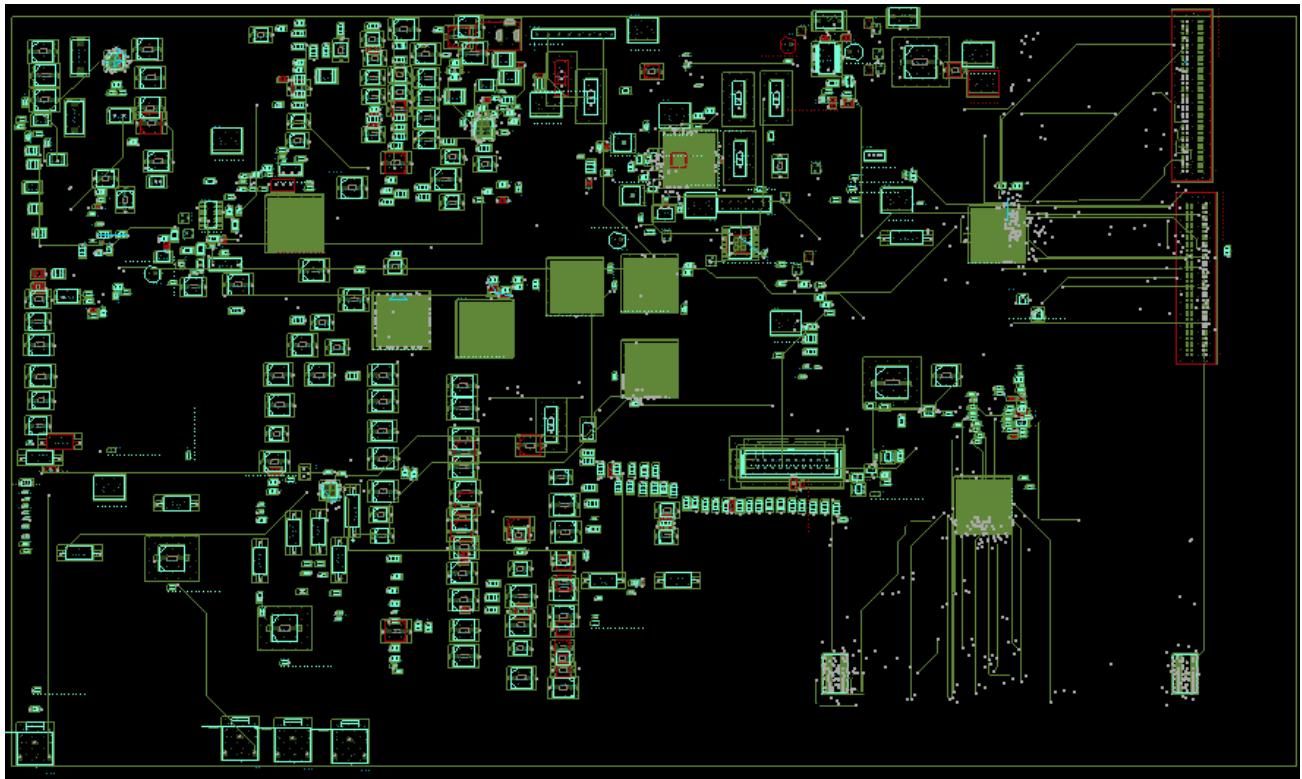


Fig 4.2 1st Layer

## 2nd Layer

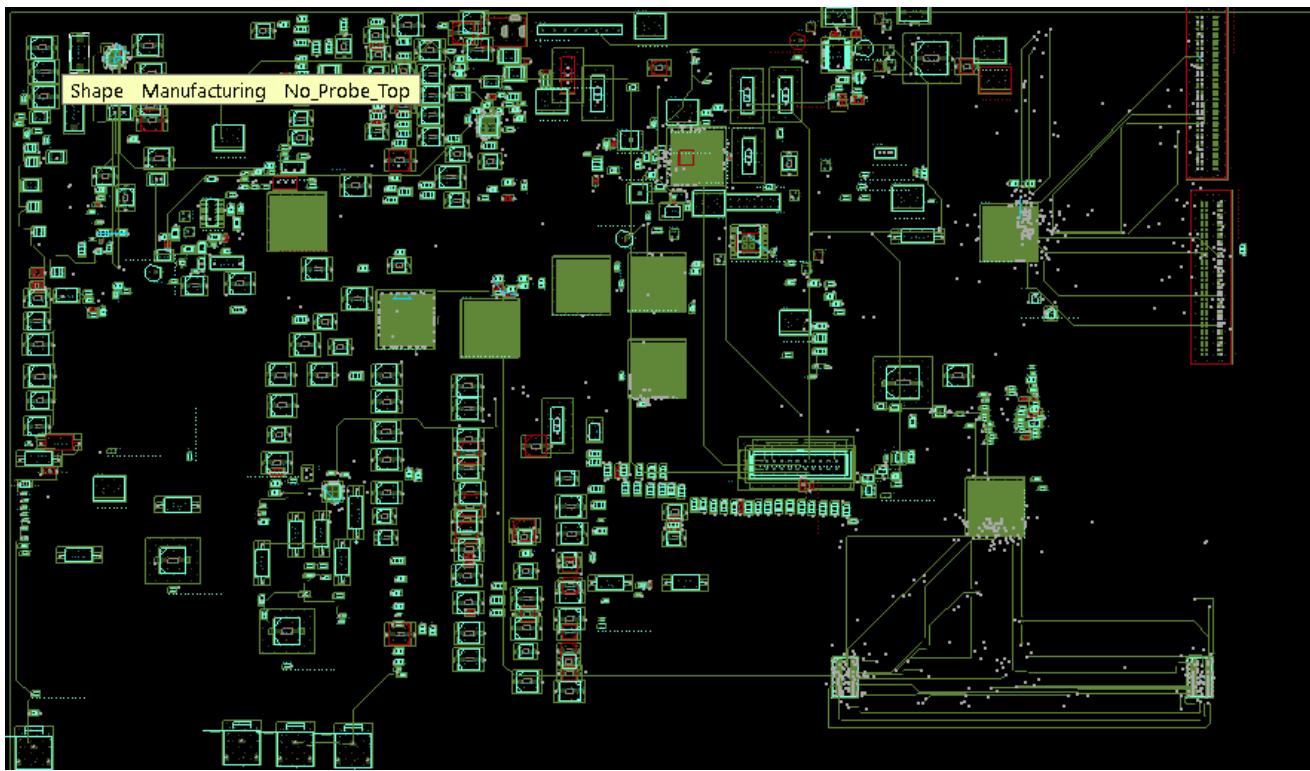


Fig 4.3 2nd Layer

## 3rd Layer

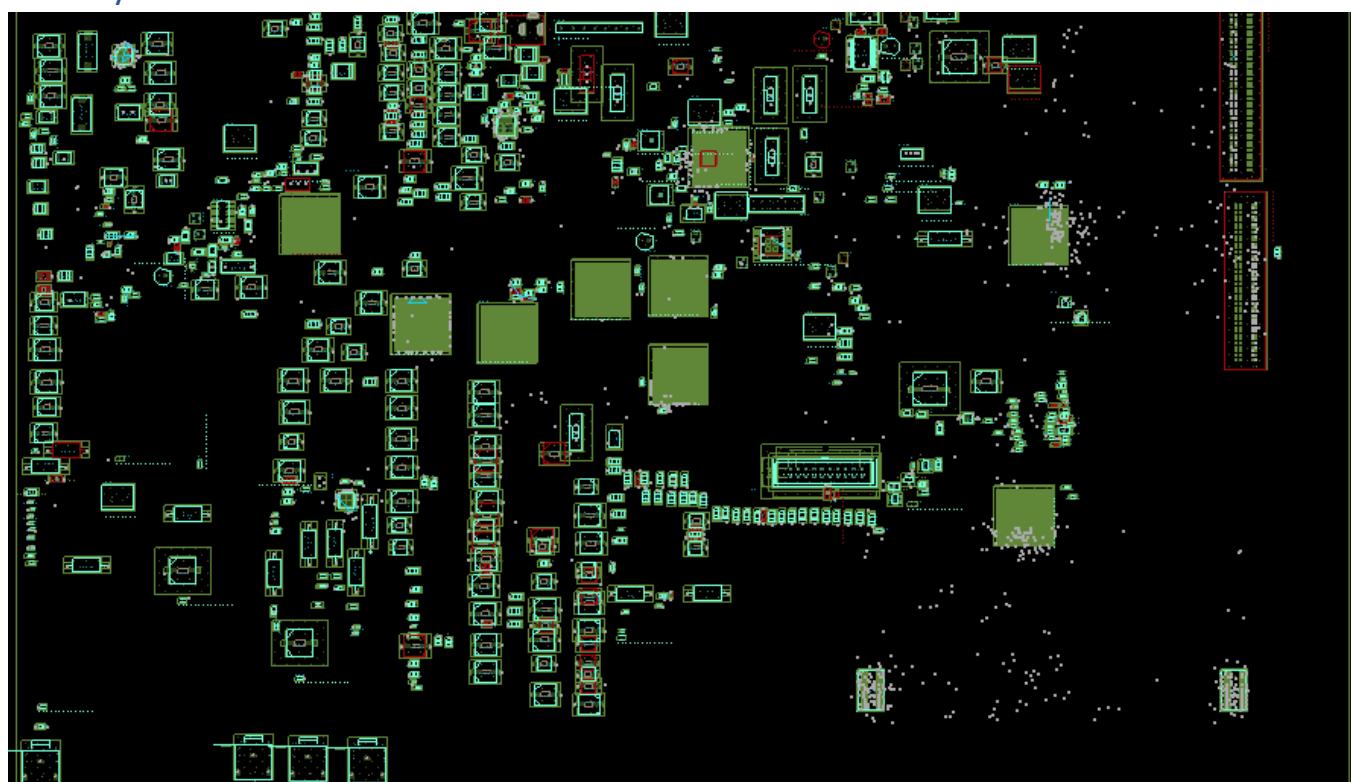


Fig 4.4 3rd Layer

4th Layer

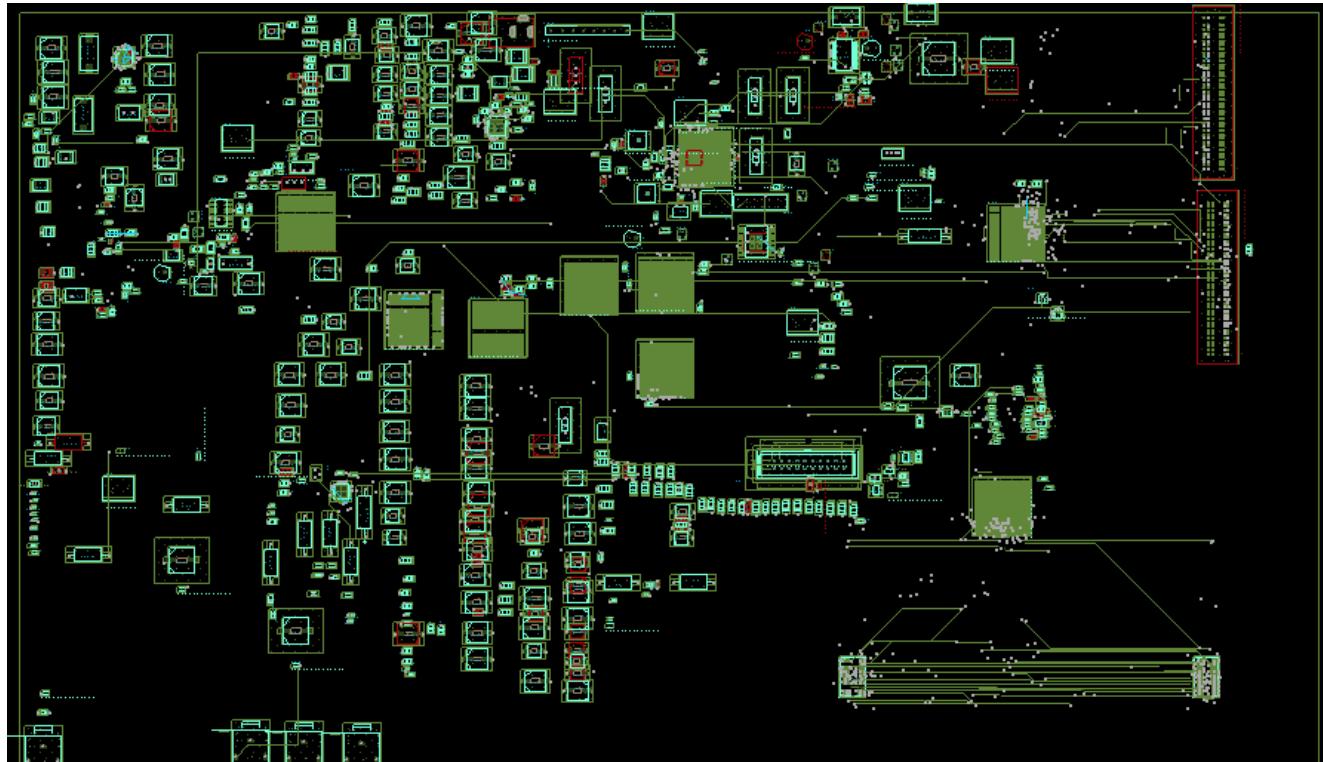


Fig 4.5 4th Layer

5th Layer

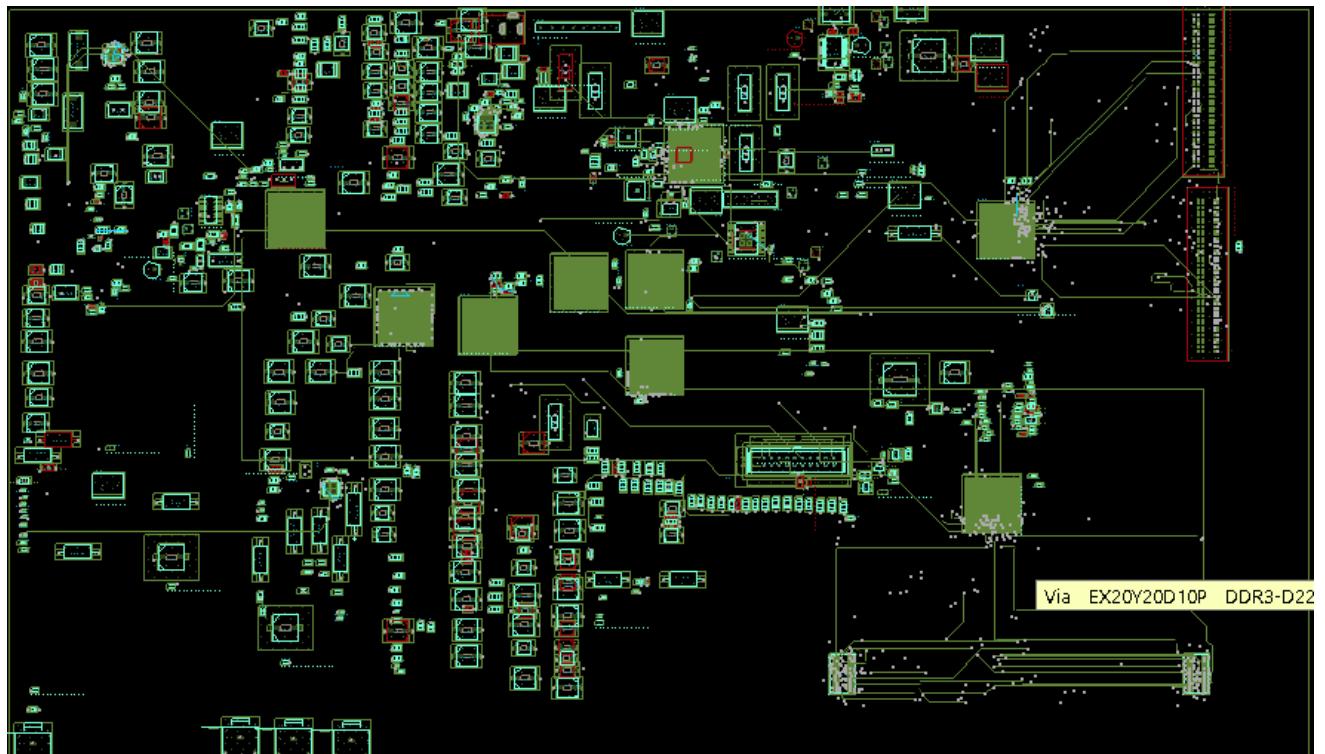


Fig 4.6 5th Layer

6th Layer

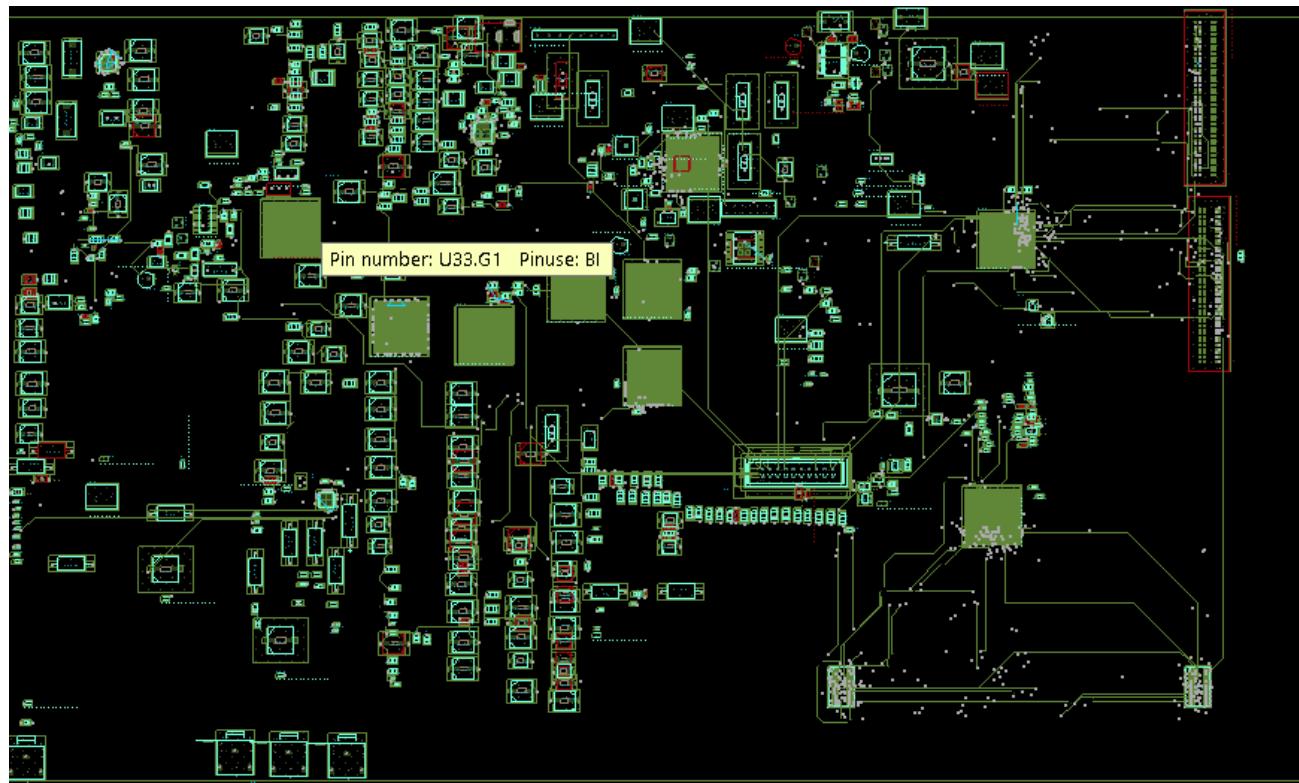


Fig 4.7 6th Layer

Bottom Layer

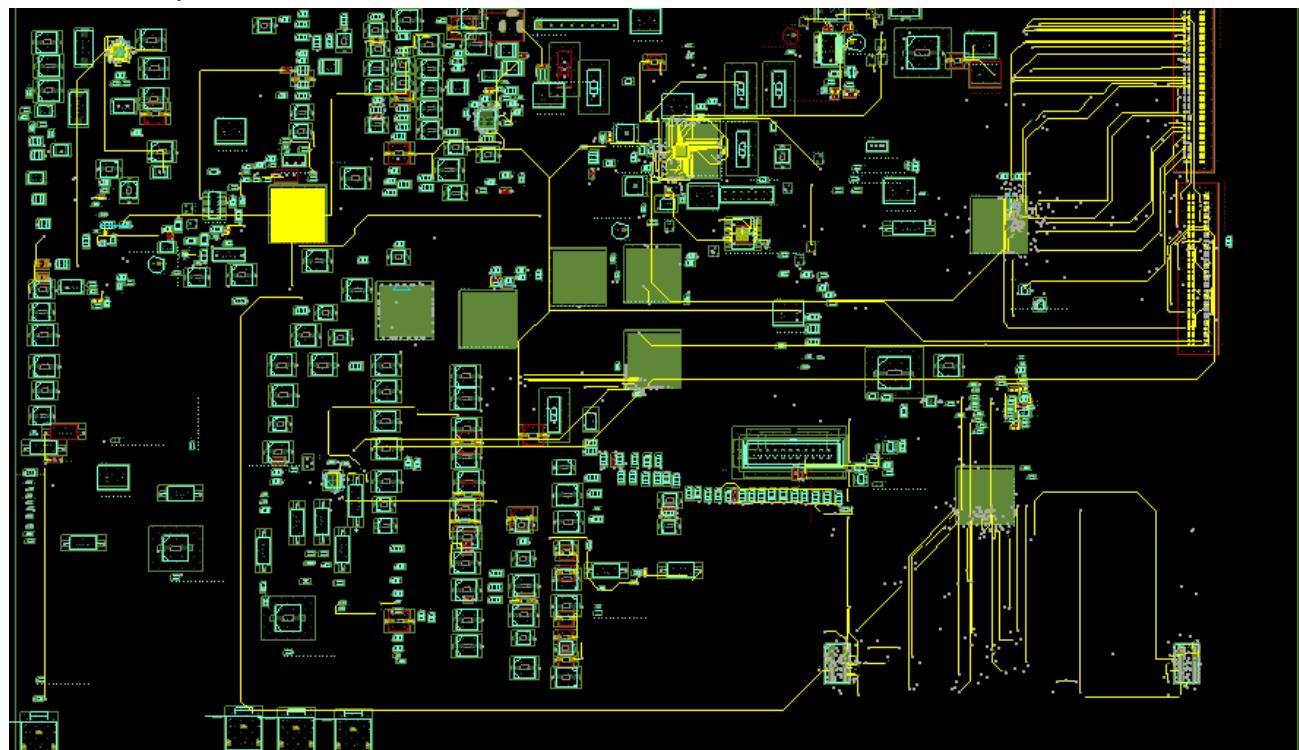
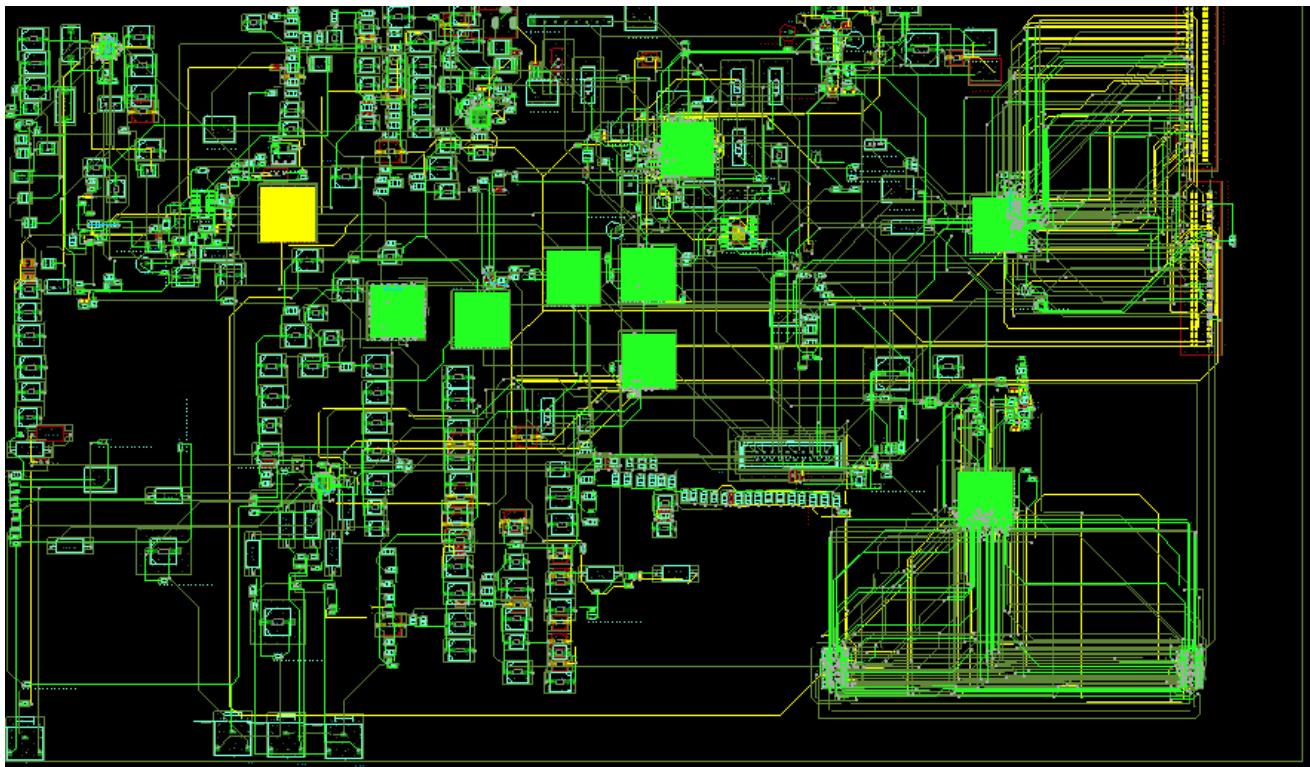


Fig 4.8 Bottom Layer

## PCB Routing



**Fig 4.9 Complete PCB Layer Routing**

## Before pcb Routing Consider following

### Clearance Constraints:

- Clearance between Components: Define the minimum clearance between components to prevent electrical interference and ensure manufacturability.
- Clearance to Board Outline: Specify the clearance between traces and the board outline to avoid issues during manufacturing.

### Routing Width and Spacing:

- Trace Width: Set the minimum and preferred widths for signal traces based on your design requirements.
- Trace Spacing: Define the minimum and preferred spacing between adjacent traces.

### Via Constraints:

- Minimum Via Size: Specify the minimum size for vias.
- Minimum Annular Ring: Set the minimum annular ring size to ensure reliable solder joints.

Allegro Constraint Manager (connected to Allegro PCB Venture 22.1) [zedboard] - [Spacing / Net / All Layers]

Type	S	Name	Referenced Spacing CSet	Line To		Thru Pin To		SMD Pin To		Test Pin To		Thru Via To		BB Via To	
				All	mm	All	mm	All	mm	All	mm	All	mm	All	mm
Dsn		zedboard	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AC-ADR1	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AC-GPO0	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AC-GPO1	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AC-GPO2	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AC-GPO3	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AC-MCLK	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AC-SCK	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AC-SDA	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AC-JV3	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		AGND_2	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		BTNC	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		BTND	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		BTNL	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		BTNR	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		BTNU	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		CEC	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		CEC_CLK	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		CLK+	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		CLK-	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		COMP1	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		COMP1_1	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		COMP2	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		CS-	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		CS-	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDCSCL	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDCSDA	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDR1RVS	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDR-VRN	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDR-VRP	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDRVREF	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDR0V75	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDR3-A0	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDR3-A1	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDR3-A2	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	
Net		DDR3-A3	DEFAULT	***	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	

Fig 5.1 Constraint Manager

3D View

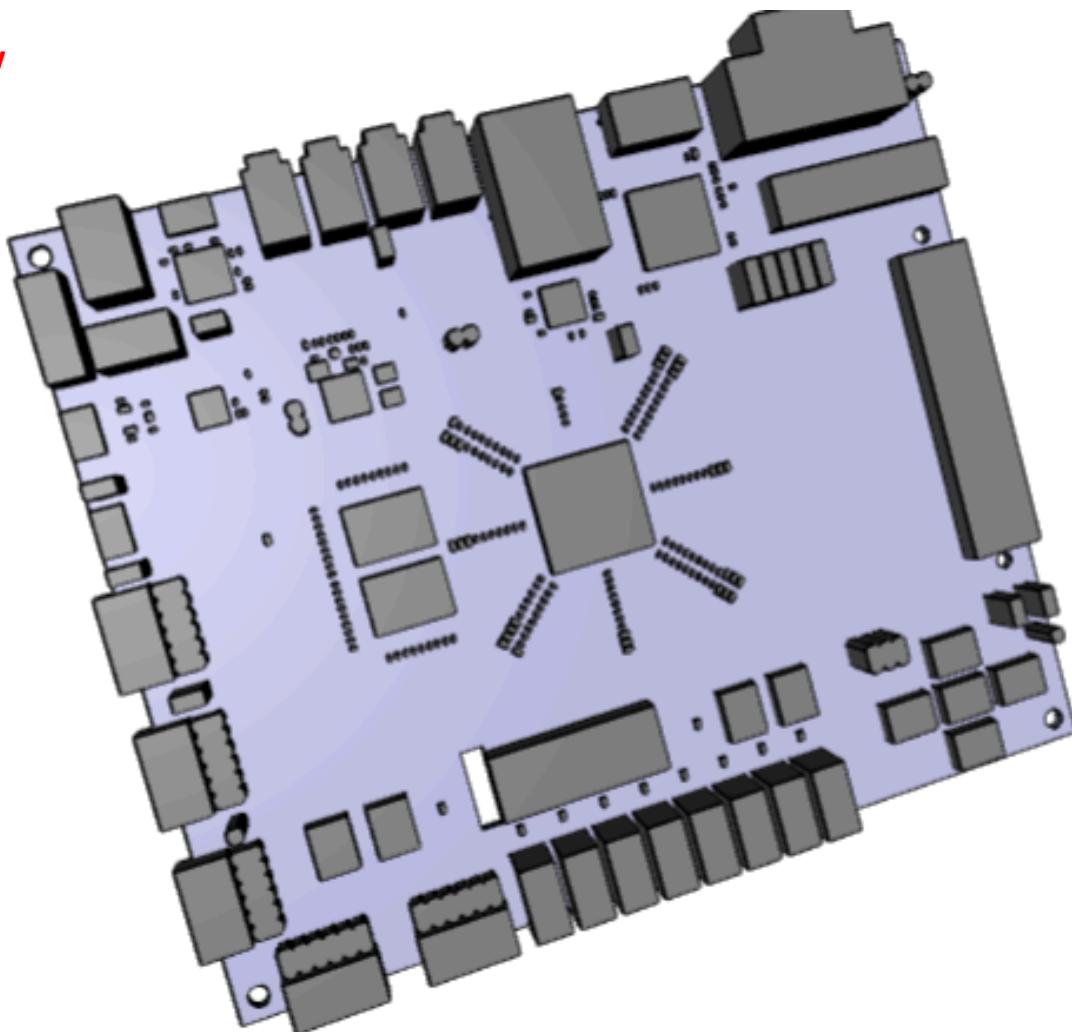


Fig 5.2 3D view

## XC7Z020CLG484

The XC7Z020CLG484 is a member of the Xilinx Zynq-7000 family of All Programmable System-on-Chip (SoC) devices. Here's a brief overview

1. Architecture: The Zynq-7000 family combines a dual-core ARM Cortex-A9 processor subsystem with programmable logic (FPGA fabric) in a single chip. This integration enables the development of highly flexible and high-performance embedded systems.
2. Processing System: The XC7Z020CLG484 features two ARM Cortex-A9 processor cores running at speeds of up to 667 MHz. These processors provide the main processing power for executing software applications and running the operating system.
3. Programmable Logic: In addition to the ARM processors, the XC7Z020CLG484 includes programmable logic that can be configured and programmed to implement custom hardware functionality. This allows developers to accelerate specific tasks and customize the behavior of the chip to meet their application requirements.
4. Memory Interfaces: The Zynq-7000 SoC supports various memory interfaces, including DDR3 SDRAM, NAND flash, NOR flash, and SD/MMC cards. These interfaces enable data storage, program execution, and memory access for software applications.
5. High-Speed Interfaces: The XC7Z020CLG484 includes a variety of high-speed interfaces such as Gigabit Ethernet, USB, PCIe, HDMI, and serial transceivers. These interfaces facilitate connectivity with external devices, networks, and peripherals, enhancing the versatility of the SoC.
6. Package: The "CLG484" designation in the part number refers to the package type and pinout of the chip. In this case, "CLG484" indicates a 484-pin plastic quad flat package (PQFP) with a specific pinout configuration.

Overall, the XC7Z020CLG484 is a powerful and versatile SoC device suitable for a wide range of embedded systems applications, including industrial automation, automotive, aerospace, telecommunications, and more. Its combination of ARM processors and programmable logic offers developers the flexibility and performance needed to create innovative and customized solutions.

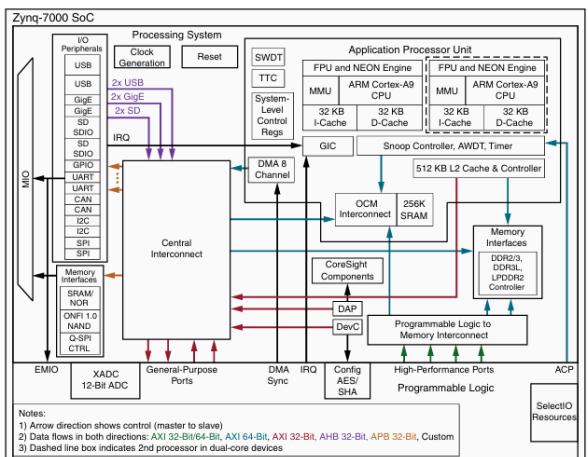
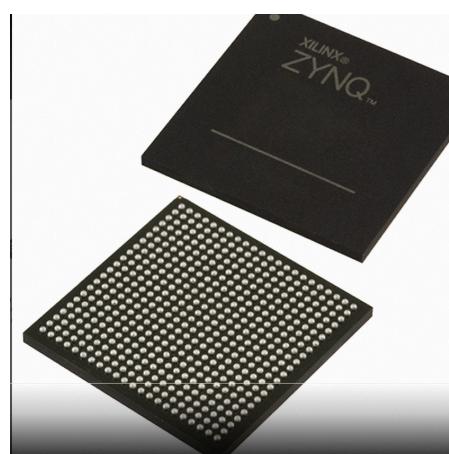


Fig 6.1 Architecture overview



## SEARAY™ High Density Open Pin Field Arrays

These high speed, high density open pin field arrays allow maximum grounding and routing flexibility.

0.050 pitch ASP-134603-01

-> ADG719BRTZ spdt switch

-> TST-110-01-G-D straight thru hole pcb header

-> 74LCX125BQX The LCX125 contains four independent non-inverting buffers with 3-STATE outputs. The inputs tolerate Voltages up to 7 V Allowing the interface of 5 V Systems to 3 V Systems

## Pmods

JA-JE are connected to the FPGA fabric, but Pmod JF is connected to the MIO bus of the Processing system. This means that the pins are not accessible from the FPGA for general purpose, but instead connected to the processor peripherals, such as the GPIO controller. This means there are only 40 externally routed I/Os connected to the FPGA, and 8 additional I/Os that can be controlled from the Zynq processor.

The Zynq Z7 has six Pmod ports, some of which behave differently than others. Each Pmod port falls into one of four categories: standard, MIO connected, XADC, or high-speed

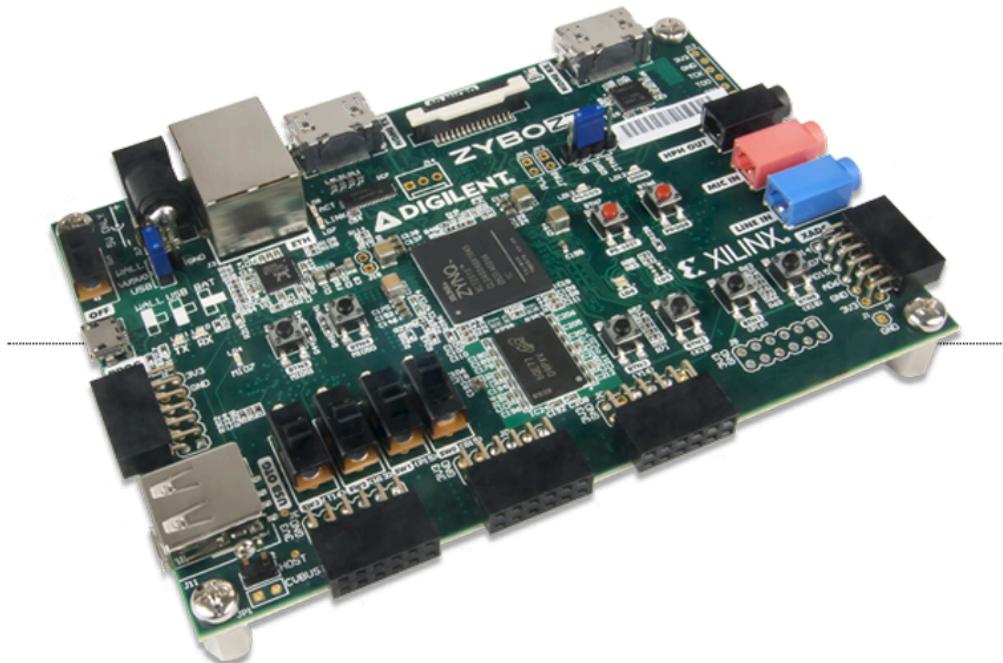


Fig 6.2 Zed Board

**audio codec**  
**cmos 3.3v regulator for audio codec ADP150ACBZ-3**

Ultralow Noise, 150 mA, CMOS Linear Regulator

**TYPICAL APPLICATION CIRCUITS**

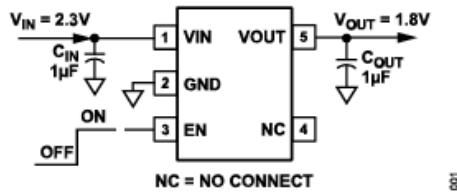


Figure 1. 5-Lead TSOT with Fixed Output Voltage, 1.8 V

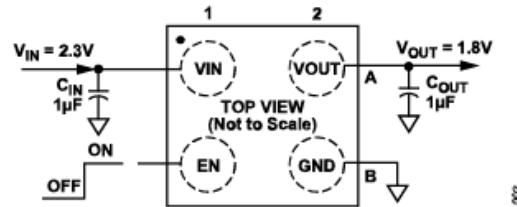


Figure 2. 4-Ball WLCSP with Fixed Output Voltage, 1.8 V

**FUNCTIONAL BLOCK DIAGRAM**

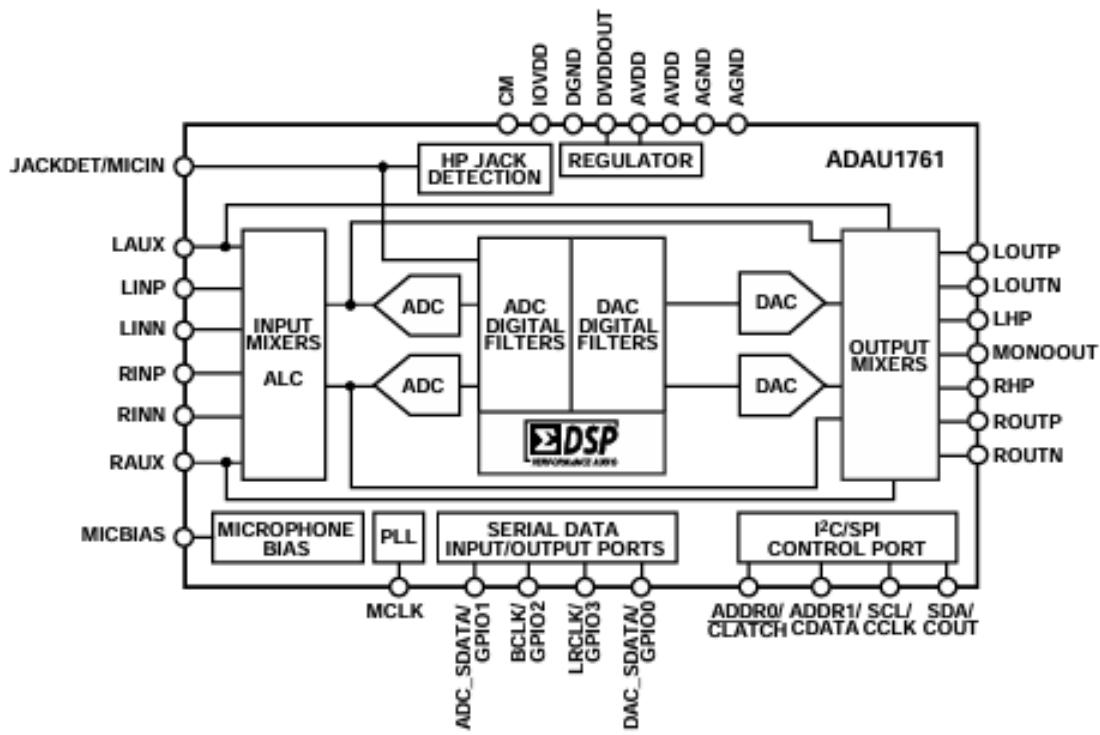
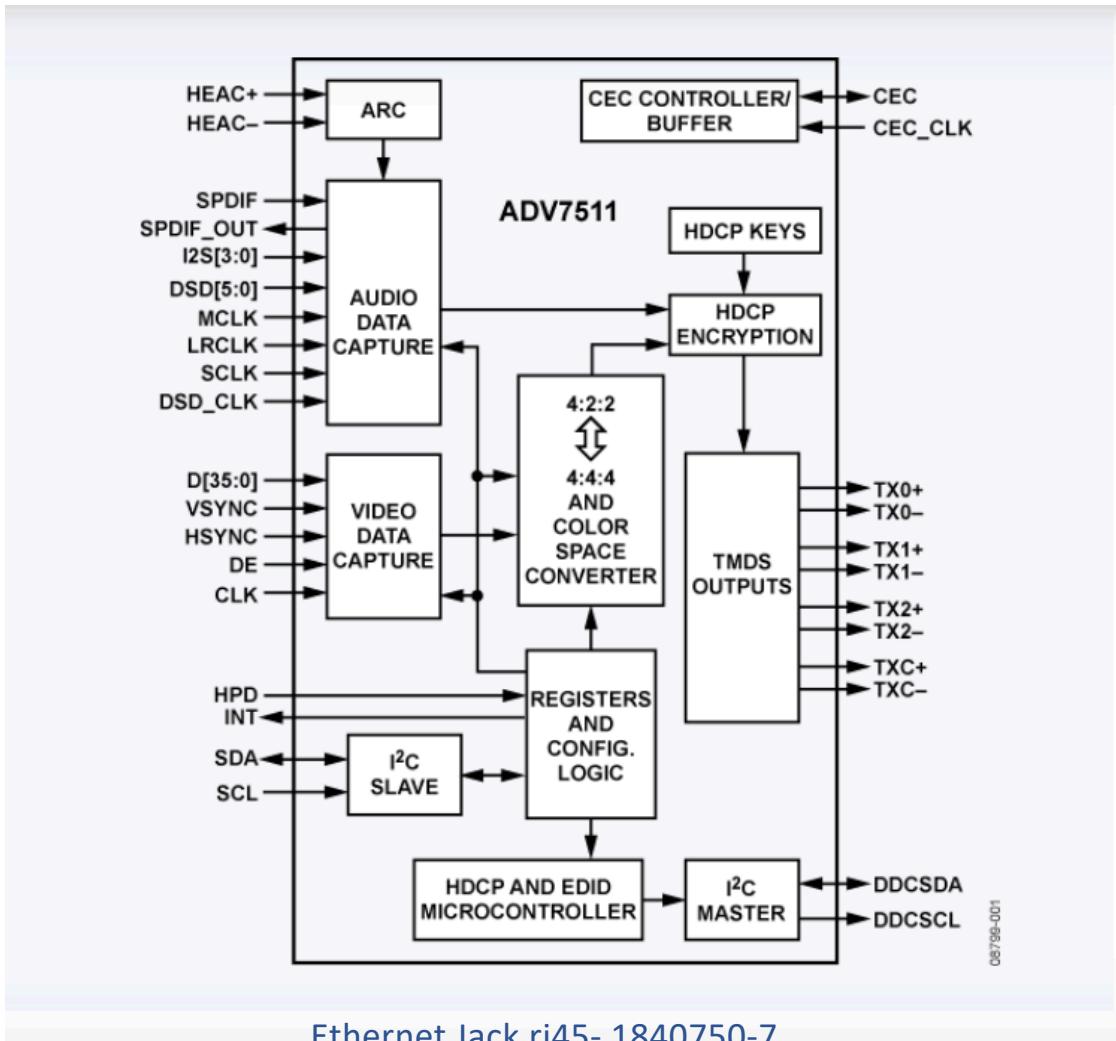


Fig 6.3 Functional Block diagram of Audio codac

## HDMI and VGA

### ADV7511KSTZ



08799-001

Ethernet Jack rj45- 1840750-7

Figure 5: 88E1510/88E1518 Device 48-Pin QFN Package (Top View)

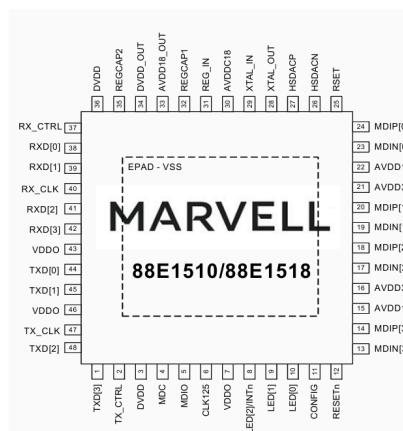
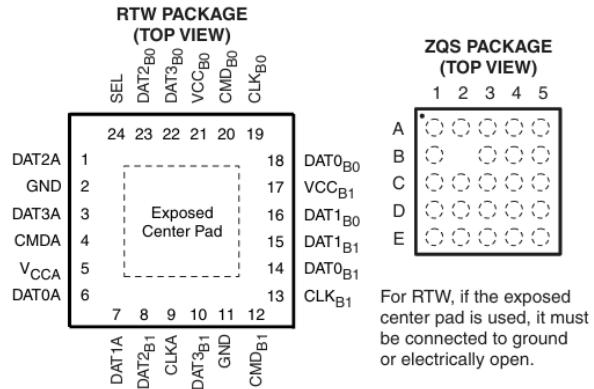


Fig 6.4 Ethernet jack rj45

MDI stands for media dependent interface sd card



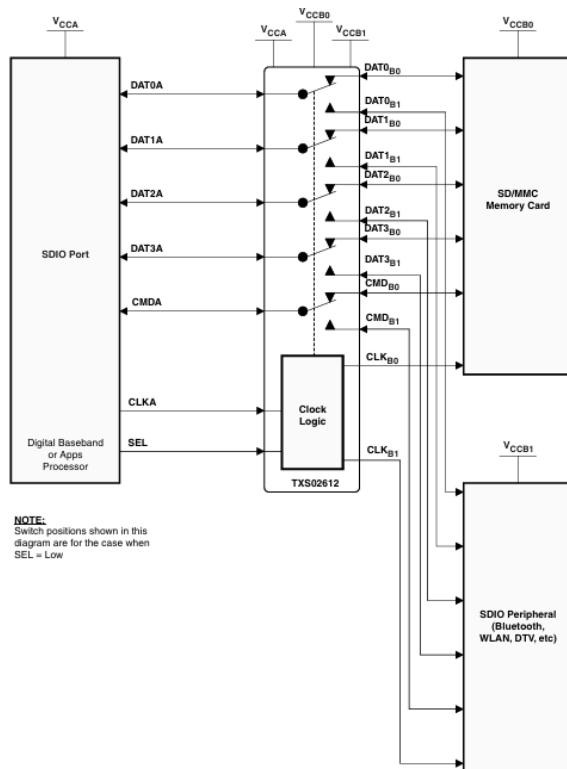
**Table 1. ZQS PACKAGE TERMINAL ASSIGNMENTS**

	1	2	3	4	5
<b>A</b>	DAT2A	SEL	DAT3B0	CMDB0	CLKB0
<b>B</b>	DAT3A		DAT2B0	VCCB0	DATOB0
<b>C</b>	CMDA	VCCA	GND	VCC B1	DAT1B0
<b>D</b>	DAT0A	CLKA	GND	DAT1B1	DATOB1
<b>E</b>	DAT1A	DAT2B1	DAT3B1	CMDB1	CLKB1

**Fig 6.5 SD Card Connector**

sd connector - 2041021-1

OLED connector UG-2832HSWEG04



**Fig 6.6 OLED connector**

## S25FL256SAGNF100

The S25FL256SAGNF100 is a 256-Mbit (32-MB) SPI Flash memory device from Cypress Semiconductor. It features:

Density: 256 Megabits (32 Megabytes)

Architecture: CMOS Flash technology

Interface: Serial Peripheral Interface (SPI) with multi I/O options (single, dual, and quad I/O)

Performance:

Maximum clock frequency of 133 MHz

Fast read speeds, supporting dual and quad I/O operations

## S25FL256SAGMF100

The S25FL256SAGMF100 is a 256-Mbit (32-MB) Serial NOR Flash memory device from Cypress Semiconductor, part of the FL-S family. Here are the key features and specifications:

1. Density: 256 Megabits (32 Megabytes)
2. Architecture: CMOS 3.0V core and I/O voltage
3. Interface: Serial Peripheral Interface (SPI) with multi I/O options (single, dual, and quad I/O)
4. Performance:
  - Maximum clock frequency of 133 MHz for SPI
  - Fast read speeds, supporting dual and quad I/O operations
  - Program and erase operations optimized for performance and endurance

## TUSB1210BRHB

The TUSB1210BRHB is a high-speed USB transceiver from Texas Instruments. It is typically used in USB 2.0 applications to provide the physical layer for USB communication. Here are the key features and specifications:

1. Compliance: Compliant with USB 2.0 specification
2. Data Rates: Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) data rates
3. Interface:
  - UTMI+ Low Pin Interface (ULPI)
  - 8-bit data bus with control and status signals
4. Power Supply:
  - Core supply voltage: 1.1V
  - I/O supply voltage: 1.8V or 3.3V

## CY7C64225-28PVXC

The CY7C64225-28PVXC is a USB-Serial Bridge Controller from Cypress Semiconductor, designed to facilitate the connection of serial interfaces to USB. Here are the key features and specifications:

### 1. USB Interface:

- USB 2.0 compliant
- Full-speed USB operation (12 Mbps)
- Integrated USB transceiver
- Supports USB Suspend, Resume, and Remote Wakeup operations

### 2. Serial Interface:

- Asynchronous serial interface with configurable data rates up to 1 Mbps
- Supports common UART serial protocols
- Integrated 256-byte buffer for both transmit and receive

### 3. Microcontroller:

- Integrated 8-bit microcontroller
- 48 MHz internal clock frequency
- 8 KB flash memory for user code and data
- 512 bytes SRAM

### 4. GPIO:

- Multiple configurable General-Purpose Input/Output (GPIO) pins

### 5. Power Supply:

- Operates at 3.3V or 5V power supply
- Internal power-on reset circuit

## TPS2051BDBV

The TPS2051BDBV is a power-distribution switch from Texas Instruments designed to distribute power to peripherals while protecting the host system. Here are the key features and specifications:

### 1. Operating Voltage:

- Input voltage range: 4.5V to 5.5V

### 2. Current Limit:

- Adjustable current limit: Typically set around 500 mA

### 3. Protection Features:

- Overcurrent Protection: Limits the output current to prevent damage due to short circuits or overload conditions
- Thermal Shutdown: Shuts down the switch if the junction temperature exceeds a specified threshold to prevent overheating
- Short-Circuit Protection: Automatically limits the current when a short circuit is detected
- Reverse Voltage Protection: Prevents current from flowing back into the power supply

## USB Micro AB

The USB Micro AB connector is a part of the USB On-The-Go (OTG) standard, which allows devices to act as either a host or a peripheral. Here are the key features and details about the USB Micro AB connector:

**Connector Type:**

Micro AB connector, which combines the capabilities of Micro A and Micro B connectors

### Compatibility:

Can accept both Micro A and Micro B plugs

Used in devices that need to switch between host and peripheral roles (OTG devices)

**Physical Characteristics:**

Smaller and more compact than standard USB and Mini USB connectors

Designed for portable devices, offering durability and space-saving advantages

### Pin Configuration:

The USB Micro AB connector has five pins: VBUS, D-, D+, ID, and GND

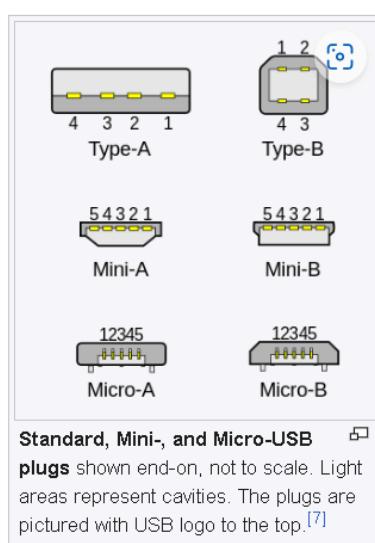
VBUS: Power supply (typically 5V)

D-: Data minus

D+: Data plus

ID: Used to determine the role of the device (host or peripheral)

GND: Ground



Type-A and -B pinout			
Pin	Name	Wire color <sup>[a]</sup>	Description
1	V <sub>BUS</sub>	Red or Orange	+5 V
2	D-	White or Gold	Data-
3	D+	Green	Data+
4	GND	Black or Blue	Ground

Mini/Micro-A and -B pinout			
Pin	Name	Wire color <sup>[a]</sup>	Description
1	V <sub>BUS</sub>	Red	+5 V
2	D-	White	Data-
3	D+	Green	Data+
4	ID	No wire	On-The-Go ID distinguishes cable ends: <ul style="list-style-type: none"><li>"A" plug (host): connected to GND</li><li>"B" plug (device): not connected</li></ul>
5	GND	Black	Signal ground

**Fig 6.7 USB Connector**

## voltage regulator

- Linear Technology LTC3619: This is a high-efficiency, 4MHz synchronous buck regulator that provides a regulated output voltage from a 2.25V to 5.5V input. It is used to provide power to the DDR3 memory on the ZedBoard.
- Texas Instruments TPS650250: This is a power management IC that integrates three highly efficient, step-down converters targeted at providing the core voltage, memory voltage, and I/O voltage in a processor-based system. It also includes a linear regulator for the RTC and a load switch for power sequencing.
- Linear Technology LTC3589: This is a highly integrated power management and battery charger IC that includes a synchronous buck-boost DC/DC converter, a synchronous buck regulator, a low dropout (LDO) regulator, and a battery charger.
- Linear Technology LTC3588: This is another power management and battery charger IC that integrates a synchronous buck-boost DC/DC converter, a low dropout (LDO) regulator, and a battery charger. It is used to provide power to the FPGA on the ZedBoard.
- Analog Devices ADP5052: This is a quad-output power supply that integrates two high-performance, low-noise, 2.5A synchronous step-down dc-to-dc converters and two 300mA LDO regulators.

## JP5 (2\*6 header)

JP5 on the ZedBoard is a 2x6 pin header used for various purposes, typically related to configuration or customization of the board. The specific function of JP5 can vary depending on the version or revision of the ZedBoard, but here are some common uses for headers like JP5 on development boards:

**JTAG Header:** JP5 may be used as a JTAG (Joint Test Action Group) header for programming and debugging the FPGA (Field-Programmable Gate Array) on the ZedBoard. JTAG headers allow for communication with the FPGA for tasks such as programming bitstreams or debugging designs.

**Configuration Jumper:** JP5 might also be used as a configuration jumper to select different boot modes or configuration options for the ZedBoard. By changing the position of jumpers on JP5, users can configure the board for different startup sequences or operating modes.

**Expansion Header:** In some cases, JP5 may serve as an expansion header for connecting additional peripherals or expansion boards to the ZedBoard. This allows users to extend the functionality of the board by adding custom hardware or interfaces.

**Customization and Debugging:** JP5 headers may also be provided for custom configuration or debugging purposes, allowing users to access specific signals or interfaces for testing or experimentation.

## FB8

FB8 on the ZedBoard typically refers to a ferrite bead component labeled "FB8" on the board. Ferrite beads are passive electronic components used in circuits for filtering high-frequency noise and interference. They are commonly employed in power supply circuits, signal lines, and other sensitive circuits to suppress electromagnetic interference (EMI) and improve circuit performance.

The specific function of FB8 can vary depending on its placement and the circuitry around it on the ZedBoard. Generally, ferrite beads like FB8 are used to attenuate high-frequency noise on power supply lines, preventing it from affecting sensitive components or signals on the board.

## ZedBoard USB-JTAG programming circuit

The ZedBoard utilizes USB-JTAG programming for configuring the FPGA and debugging embedded systems designs. The USB-JTAG circuitry typically consists of several components, including a USB connector, JTAG interface, and associated circuitry for communication between the host computer and the FPGA on the ZedBoard. Here's an overview of the USB-JTAG programming circuit for the ZedBoard:

1. USB Connector: The USB connector on the ZedBoard serves as the physical interface for connecting the board to a host computer. It allows for data transfer and power supply between the host and the board.
2. JTAG Interface: The JTAG interface on the ZedBoard provides a standardized protocol for programming and debugging the FPGA. It typically includes a JTAG connector or header, which connects to the JTAG programming cable or debugger on the host computer.
3. FPGA Configuration Pins: The programming circuitry connects to specific pins on the FPGA, such as the configuration pins (e.g., PROG\_B, DONE, INIT\_B) used for programming and configuration of the FPGA fabric.

## MT41L128M16HA-17E

The MT41L128M16HA-17E:D is indeed a DDR3 SDRAM chip commonly used on the ZedBoard, which is an evaluation and development board featuring the Xilinx Zynq-7000 All Programmable System-on-Chip (SoC). Here's how the MT41L128M16HA-17E:D fits into the ZedBoard:

1. **Memory Configuration:** The ZedBoard typically includes DDR3 SDRAM chips like the MT41L128M16HA-17E:D to provide system memory for the embedded processing system (PS) within the Zynq-7000 SoC. The PS utilizes DDR3 memory for storing program instructions, data, and other runtime information.
2. **System Performance:** The MT41L128M16HA-17E:D offers a high-speed, low-latency memory solution that complements the processing capabilities of the ARM Cortex-A9 cores within the Zynq-7000 SoC. This memory chip helps to ensure optimal system performance and responsiveness for applications running on the ZedBoard.
3. **Configuration and Control:** The ZedBoard's hardware design includes circuitry and interfaces for connecting the DDR3 SDRAM chips to the Zynq-7000 SoC. This includes memory controllers, data buses, address lines, and control signals that enable the SoC to access and communicate with the DDR3 memory devices

## DDR(Double Data rate) Memory

The ZedBoard, like many other development boards, utilizes DDR (Double Data Rate) memory for system memory. In the case of the ZedBoard, it specifically uses DDR3 SDRAM (Synchronous Dynamic Random-Access Memory). Here's how DDR memory fits into the ZedBoard:

1. **System Memory :** DDR memory serves as the main system memory for the ZedBoard's embedded processing system, which is based on the Xilinx Zynq-7000 All Programmable System-on-Chip (SoC). This memory is used to store program instructions, data, and other runtime information needed by the embedded software running on the board.
2. **High-Speed Data Transfer:** DDR memory offers high-speed data transfer rates compared to previous generations of memory technologies. This enables the ZedBoard to handle large volumes of data quickly and efficiently, supporting applications that require high bandwidth and low latency.
3. **Memory Capacity:** The ZedBoard typically includes one or more DDR3 SDRAM chips to provide sufficient memory capacity for the embedded processing system. The exact amount of memory can vary depending on the specific configuration and version of the ZedBoard.

## MAX15021ATI+, MAX15053EWL+

The MAX15021ATI+ is a DC-DC step-down (buck) converter IC (integrated circuit) manufactured by Maxim Integrated. It's commonly used for power management applications, providing efficient voltage regulation for various components on electronic devices, including development boards like the ZedBoard. Here's how the MAX15021ATI+ might be used on the ZedBoard:

- 1. Power Regulation:** The MAX15021ATI+ is likely used on the ZedBoard to regulate the voltage supplied to specific components or subsystems, ensuring stable and reliable operation. Development boards often require multiple voltage rails to power different sections, such as the FPGA, DDR memory, peripherals, and auxiliary components. The MAX15021ATI+ may be employed to generate one of these voltage rails.
- 2. Efficiency and Performance:** The MAX15021ATI+ offers high efficiency and fast transient response, making it suitable for applications where power consumption and performance are critical. By efficiently converting higher input voltages to lower, regulated output voltages, the MAX15021ATI+ helps minimize power dissipation and optimize the overall energy efficiency of the ZedBoard.
- 3. Compact and Integrated Design:** The MAX15021ATI+ is designed to be compact and integrate various features, including overcurrent protection, thermal shutdown, and adjustable output voltage. This integration simplifies the design and layout of the power supply circuitry on the ZedBoard, reducing board space and bill of materials (BOM) cost.

## MAX1510ETB:

The MAX1510ETB is a high-efficiency, step-up DC-DC converter (boost converter) IC (Integrated Circuit) manufactured by Maxim Integrated. Here's some information about this IC:

- 1. Functionality:** The MAX1510ETB is designed to step up a lower input voltage to a higher output voltage. It operates as a boost converter, which is useful in applications where the input voltage is lower than the required output voltage, such as battery-powered systems.
- 2. Applications:** This IC is commonly used in portable devices, battery-powered equipment, and other applications where efficient voltage conversion from a low-voltage source to a higher voltage is necessary. It can be used to power various components, subsystems, or peripherals that require a higher voltage than the available input.
- 3. Efficiency:** The MAX1510ETB is designed for high efficiency, minimizing power losses during the voltage conversion process. This helps to maximize battery life in portable or battery-powered applications and reduces heat dissipation in the system.

## LM339M:

The LM339 is a widely used quad voltage comparator IC (integrated circuit) manufactured by Texas Instruments. It consists of four independent voltage comparators designed to operate from a single power supply over a wide range of voltages.

The LM339M variant of the LM339 is the surface-mount (SOIC) package version of the IC.

1. **Voltage Monitoring:** Comparing multiple voltages and generating digital outputs based on the comparison results. For example, it can be used in overvoltage or undervoltage protection circuits.
2. **Signal Conditioning:** Comparing analog signals and providing logic-level outputs based on the comparison results. It can be used in signal conditioning circuits, such as in audio applications or sensor interfaces.
3. **Threshold Detection:** Detecting when a voltage exceeds a certain threshold and triggering actions accordingly. This can be useful in various control systems and automation applications.

## MAX1983EUT+

The MAX1983EUT+ is a step-up DC-DC converter (boost converter) IC (Integrated Circuit) manufactured by Maxim Integrated. Here's some information about this IC:

1. **Functionality:** The MAX1983EUT+ is designed to step up a lower input voltage to a higher output voltage. It operates as a boost converter, which is useful in applications where the input voltage is lower than the required output voltage, such as battery-powered systems.
2. **Applications:** This IC is commonly used in portable devices, battery-powered equipment, and other applications where efficient voltage conversion from a low-voltage source to a higher voltage is necessary. It can be used to power various components, subsystems, or peripherals that require a higher voltage than the available input.
3. **Efficiency:** The MAX1983EUT+ is designed for high efficiency, minimizing power losses during the voltage conversion process. This helps to maximize battery life in portable or battery-powered applications and reduces heat dissipation in the system.

## MAX6037AAUK12+T

The MAX6037AAUK12+T is a precision voltage reference IC (Integrated Circuit) manufactured by Maxim Integrated. Here's some information about this specific IC:

1. Functionality: The MAX6037AAUK12+T is a low-dropout (LDO), micropower voltage reference with a fixed output voltage of 1.2V. It is designed to provide a stable and accurate voltage reference for various analog and mixed-signal circuits.
2. Applications: This IC is commonly used in analog-to-digital converters (ADCs), digital-to-analog converters (DACs), voltage regulators, and other applications where a precise and stable voltage reference is required. It ensures accurate and reliable performance of these circuits by providing a consistent reference voltage.
3. Features: The MAX6037AAUK12+T offers features such as low dropout voltage, low quiescent current, low temperature coefficient, and high accuracy over temperature. These features make it suitable for use in battery-powered, portable, and other low-power applications where energy efficiency and precision are essential.
4. Package: The "AAUK12" suffix in the part number indicates the package type. In this case, it refers to a 5-pin SOT-23 package, which is compact and suitable for space-constrained applications. The "T" suffix denotes the tape-and-reel packaging option.
5. Input and Output Capacitors: The MAX6037AAUK12+T typically requires input and output capacitors to stabilize the voltage reference output and filter out noise.

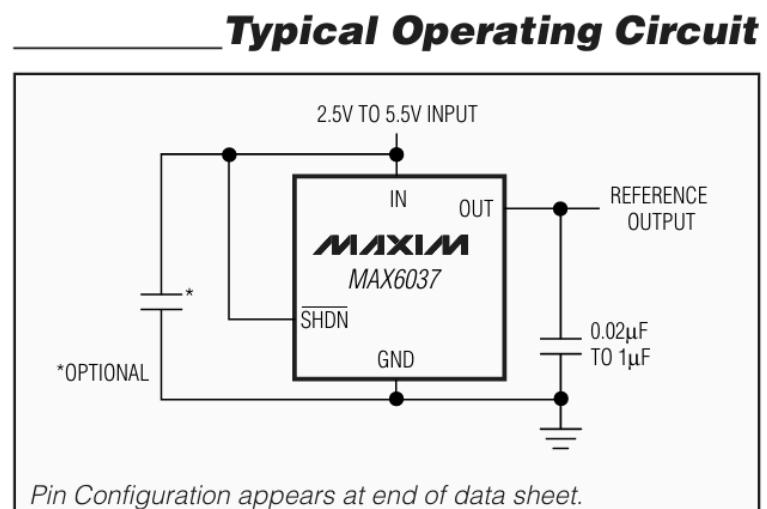
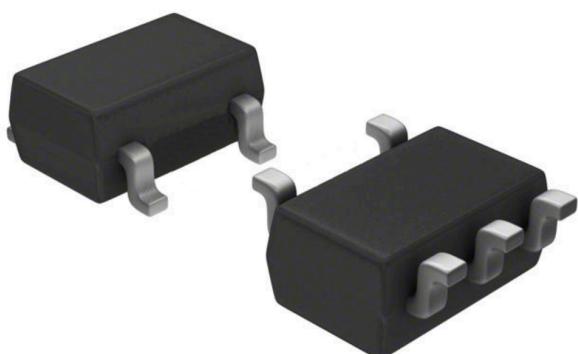


Fig 6.8 Voltage Reference IC

## DIFFICULTIES

In our current project using Allegro PCB, we are encountering significant difficulties with both component placement and routing. The highest challenge lies in optimizing the placement of components to ensure a logical flow and efficient use of space, which is critical for maintaining signal integrity and manufacturability. Additionally, routing has become complex due to the need to minimize vias, manage differential pair routing, and maintain appropriate trace widths and clearances. These issues are compounded by the necessity to balance power and ground plane allocations, adhere to design constraints, and ensure that thermal and signal integrity analyses are satisfactory. These challenges are affecting our project timeline and overall design efficiency, necessitating a thorough review and strategic approach to overcome these hurdles.

## FUTURE SCOPE OF OUR WORK

The future scope of our project involves the comprehensive manufacturing of the complete PCB, with meticulous consideration of all EMC (Electromagnetic Compatibility) and EMI (Electromagnetic Interference) effects. Our objective is to ensure that the final product not only meets all functional and performance requirements but also complies with industry standards for electromagnetic emissions and susceptibility. This will involve advanced simulation and testing to mitigate potential interference issues, optimizing component placement and routing to minimize EMI, and implementing effective shielding and filtering techniques. By addressing these factors, we aim to deliver a robust, reliable, and compliant PCB that performs optimally in its intended application environment.

- Continuous Improvement and Optimization: Implement a process for continuous improvement and optimization of the PCB design and manufacturing process. This may involve collecting feedback from field testing and post-production analysis to identify areas for enhancement in future iterations of the PCB design.

## Conclusion

In conclusion, undertaking the development of a ZedBoard as a mini-project presents an exciting and challenging opportunity. It involves meticulous design, fabrication, and testing processes, integrating STM32 microcontroller functionality with robust simulation features. This project not only enhances technical skills in PCB design and microcontroller programming but also provides a platform to explore advanced concepts such as EMC/EMI considerations and compliance testing. Additionally, completing this project successfully can showcase practical expertise in hardware design and firmware development, making it a valuable addition to one's portfolio and demonstrating readiness for more complex projects in the field of embedded systems.

## REFERENCES

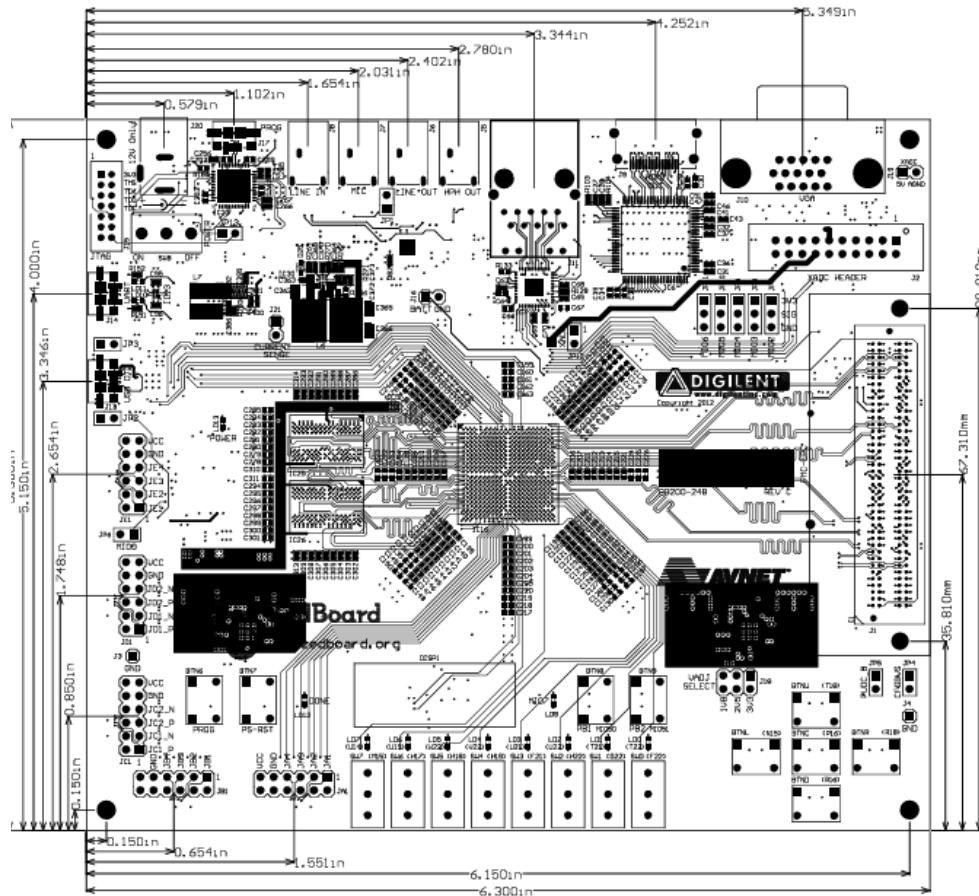
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## Mechanic Drawing

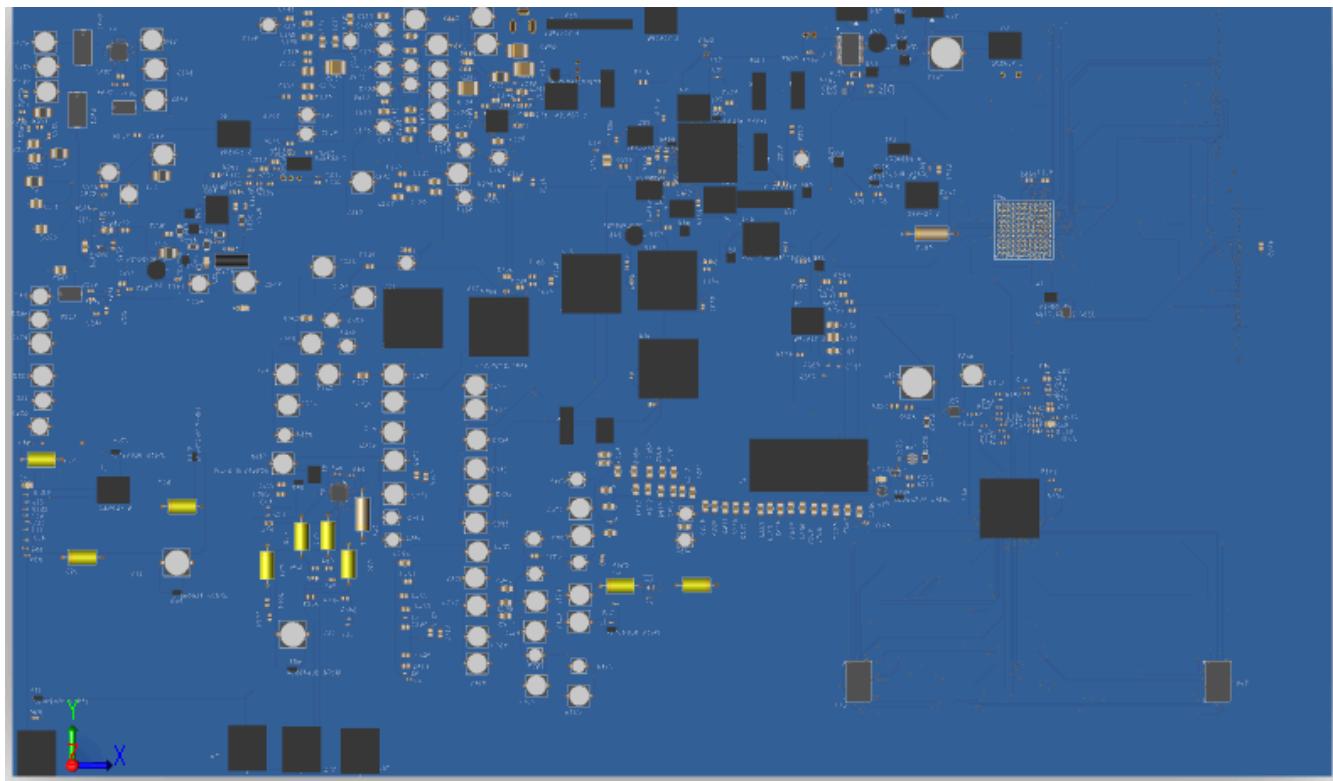


Layer Stack Up Detail for: ZED.PcbDoc

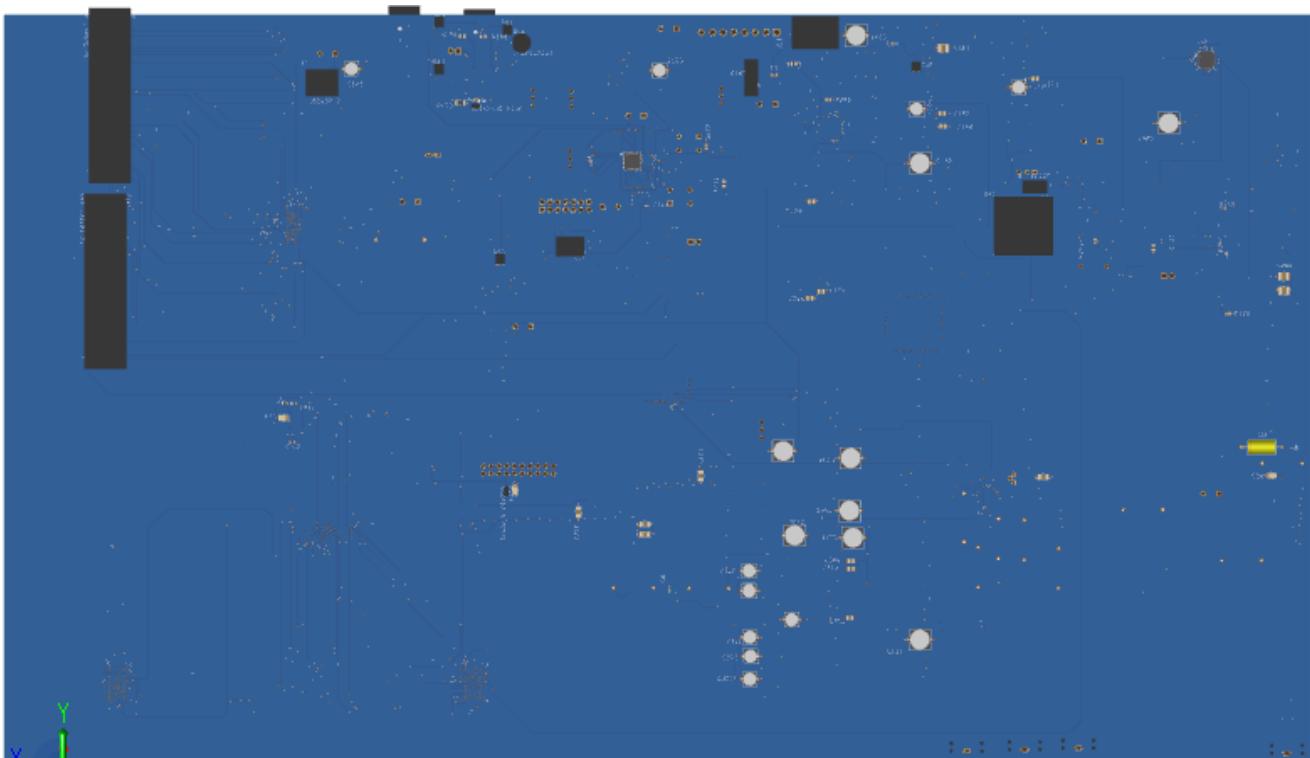
Layer Name	Outer Dimension	Copper Thickness	Dielectric Height	Dielectric Material	Dielectric Constant	Dielectric Type
Top Solder Mask	C_GTS1	0.0002mm		Solder Resist	3.80	
Top Layer	C_BTL1	0.0356mm	0.1mm	FR-4	4.80	Core
GND1	C_GD1	0.0356mm	0.125mm	FR-4	4.80	PrePreg
Mid-Layer 1	C_GD1	0.007mm	0.125mm	FR-4	4.80	Core
Mid-Layer 2	C_GD2	0.007mm	0.125mm	FR-4	4.80	Core
POWER1	C_BP2	0.0356mm	0.36mm	FR-4	4.80	Core
POWER2	C_BP3	0.0356mm	0.125mm	FR-4	4.80	PrePreg
MidLayer3	C_GD3	0.007mm	0.125mm	FR-4	4.80	Core
Mid-Layer 4	C_GD4	0.007mm	0.125mm	FR-4	4.80	PrePreg
GND4	C_BP4	0.0356mm	0.1mm	FR-4	4.80	Core
Bottom Layer	C_BBL1	0.0356mm		Solder Resist	3.80	
Bottom Solder Mask	C_GBS1	0.0002mm		Solder Resist	3.80	

Fig 6.9 Mechanical drawing of Zed Board

## Top view



## Bottom view



**Complete 3D view**

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