CVX601 Special Topics in Computer Science Technology

Lab Assignment #3

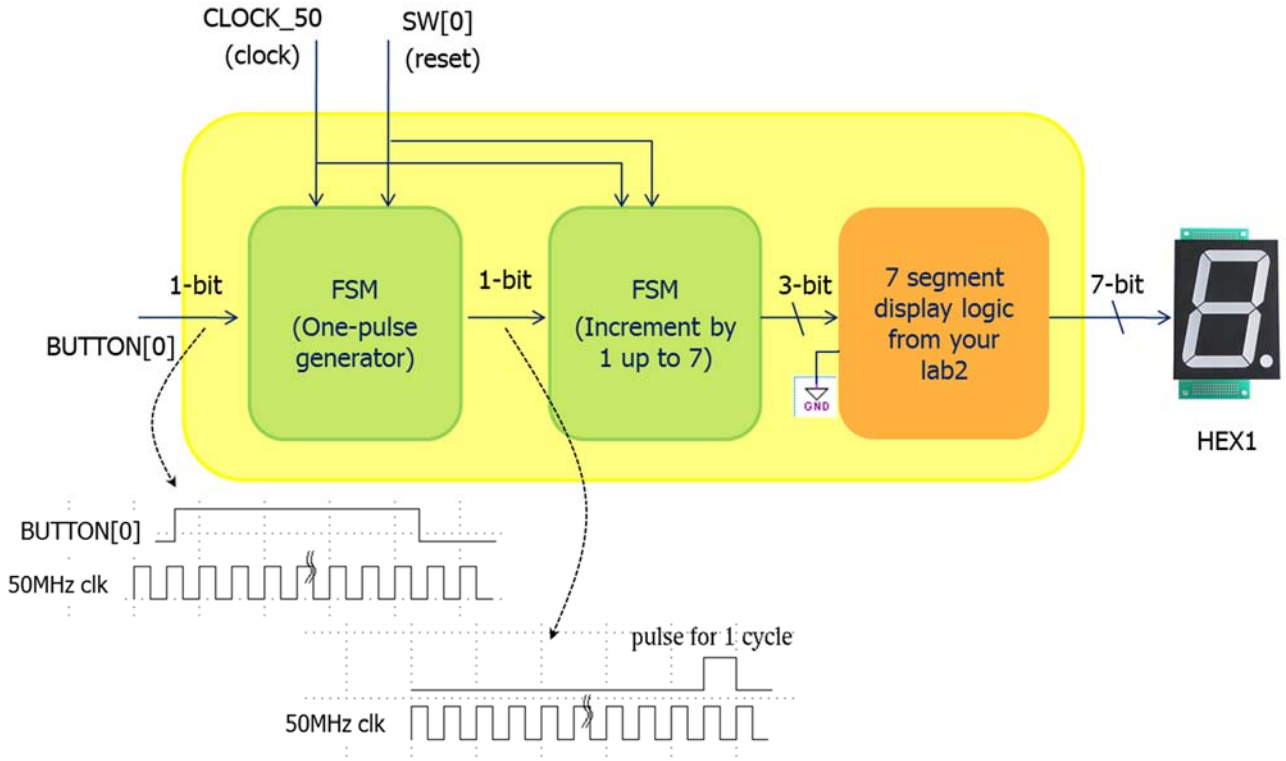
No late turn-in accepted

Design the following synchronous sequential logic with FSMs.

The DE0 board has a 50MHz clock source. Use the clock source in your design (Check out the excel file for the clock source naming). For the reset input, let's use SW[0]. We have only one normal input (BUTTON[0]), and output is sent to HEX1. The logic should satisfy the following requirements.

- Initially (when you reset the logic with SW[0]), HEX1 should display the number '0'
- When you push the button (BUTTON[0]), the number on HEX1 should be incremented by 1
- The number will be incremented up to 7, and then it wraps around to 0

Note that you should design 2 FSMs: one FSM generating a pulse for 1 clock cycle (1 cycle pulse) when you push and release the button, and the other incrementing the number based on the 1 cycle pulse. To display a number, you can re-use the 7-segment design you have done for the assignment #2. You may also want to use three 1-bit adders from the combinational logic #1 slide for the 2nd FSM.



What and How to submit:

1. Upload video clip (3-min?) to Blackboard. Your video clip should have **at least** the following contents:
    - Your smiling face
    - Understandable explanation of what you did for the assignment
    - Demo on DE0 board

Note: This is an individual assignment. You are welcome to discuss, but DO NOT COPY solutions. If you are found to copy solutions from others or slightly modify the solutions from others, both of you will be given 0 credits.

Information about D Flip-Flop (DFF) in Quartus-II

Refer to the following link:

http://quartushelp.altera.com/13.0/mergedProjects/hdl/prim/prim_file_dff.htm