CVX601 Special Topics in Computer Science Technology

Lab Assignment #4

No late turn-in accepted

Design the **Priority Circuit** with Verilog-HDL. Use the following pins as the inputs and outputs of your design. SW[9] has the highest priority and SW[0] has the lowest one. Refer to Examples below for the detailed operation.

- Input: SW[9] ~ SW[0]
- Output: HEX0

Examples:

- If SW[9] is pushed up, HEX0 should display a number “9”, no matter the positions of the other switches.
- If SW[9] is in a down position and SW[8] is pushed up, HEX0 should display a number “8”, no matter the positions of the other switches.
- If SW[9] ~ SW[1] are in down positions and SW[0] is pushed up, HEX0 should display a number 0.

What and How to submit:

1. Upload video clip (3-min?) and source code (Verilog code and Testbench) to Blackboard. Your video clip should have **at least** the following contents:
    - Your smiling face
    - Source code explanation (Verilog source code and Testbench)
    - ModelSim simulation explanation
    - Demo on DE0 board

Note: This is an individual assignment. You are welcome to discuss, but DO NOT COPY solutions. If you are found to copy solutions from others or slightly modify the solutions from others, both of you will be given 0 credits.