CVX601 Special Topics in Computer Science Technology

Lab Assignment #1

No late turn-in accepted

This assignment will help you start using Quartus-II and the DE0 board. There are 2 ways to design hardware: Schematic-based design and HDL (Hardware Description Language)-based design. We haven't studied HDL yet, but it is very straightforward to design a simple logic gate with HDL.

Follow and finish the instructions from a page #2. You are going to use a 2-input XOR gate and port it to an Altera FPGA device. FPGA stands for **F**ield **P**rogrammable **G**ate **A**rray. In other words, FPGA is a programmable hardware. It is mainly used for testing hardware design before fabrication in industry. It provides a perfect environment for testing your design.

What and How to submit:

1. Upload video clip (3-min?) to Blackboard. Your video clip should have **at least** the following contents:
    - Your smiling face
    - Demo on DE0 board

.

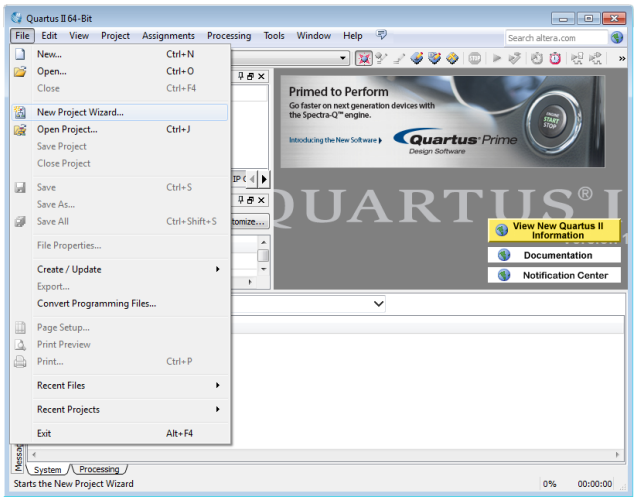
Note: This is an individual assignment. You are welcome to discuss, but DO NOT COPY solutions. If you are found to copy solutions from others or slightly modify the solutions from others, both of you will be given 0 credits.

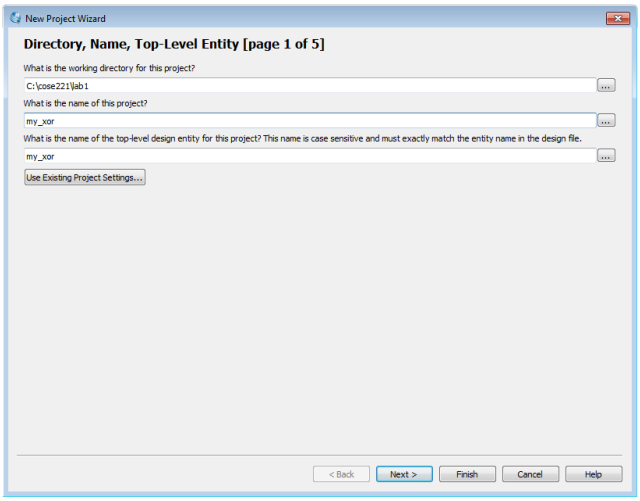
Getting Started with Quartus-II

In this lab, we are going to design a simple XOR gate with Quartus-II and download it to the DE0 board. There are 2 ways to design the XOR gate: Schematic-based design and HDL-based design. The XOR gate will take inputs from BUTTON0 and BUTTON1 on the DE0 board and display its output to LEDG0 (green LED 0)

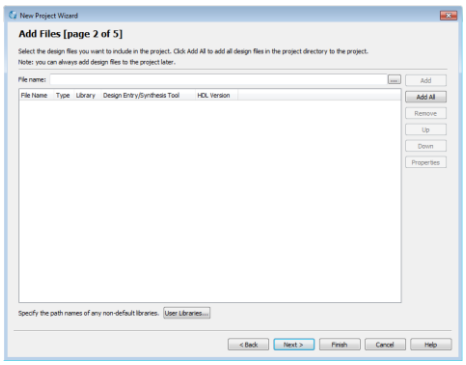
1. Schematic-based design

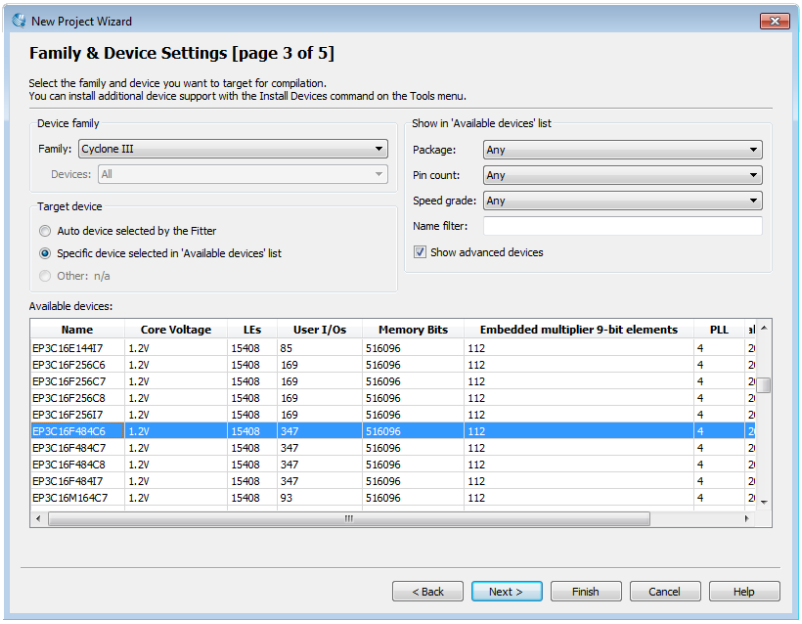
1. Select **File > New Project Wizard** to create a new project.
2. Change to the directory of your choice where you want to put your project, and enter your project name.



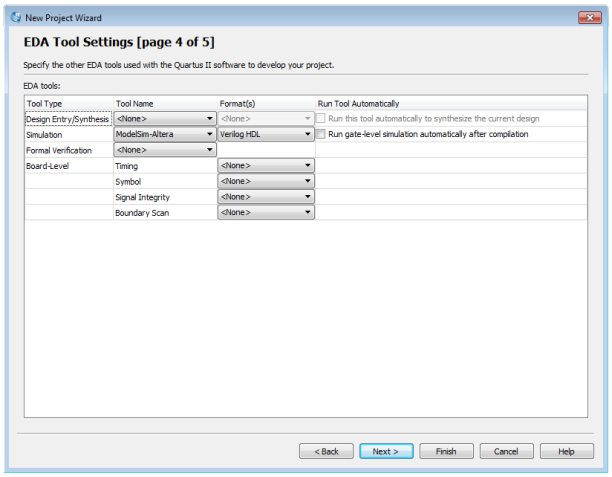


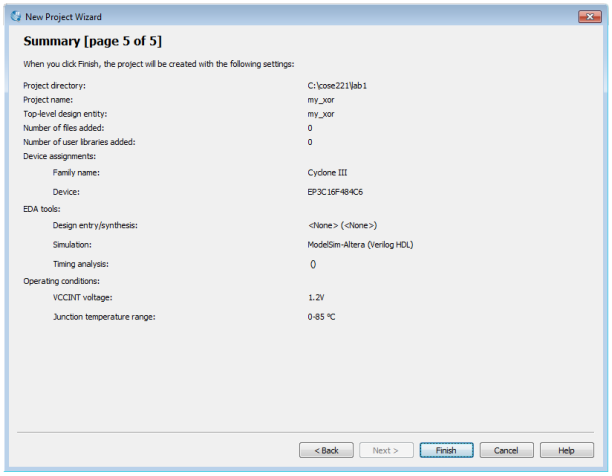
3. Click on **Next** in "Add Files" and choose the FPGA device (**Cyclone III EP3C16F484C6**) as follows.



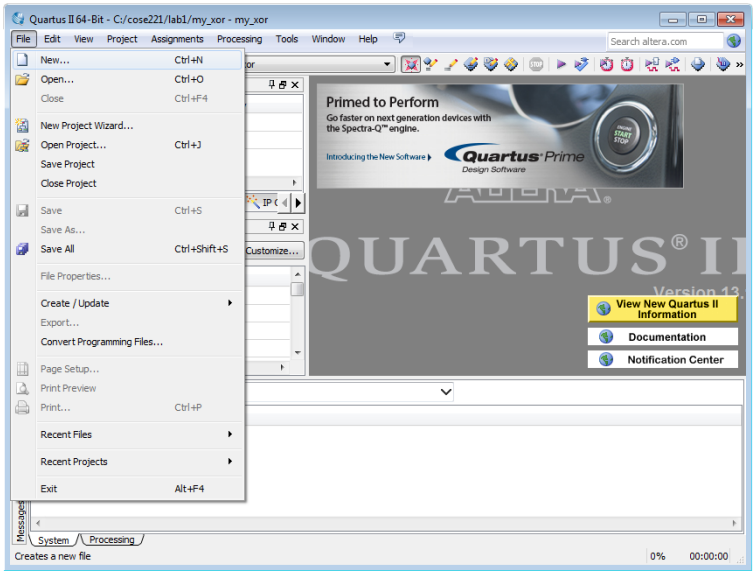


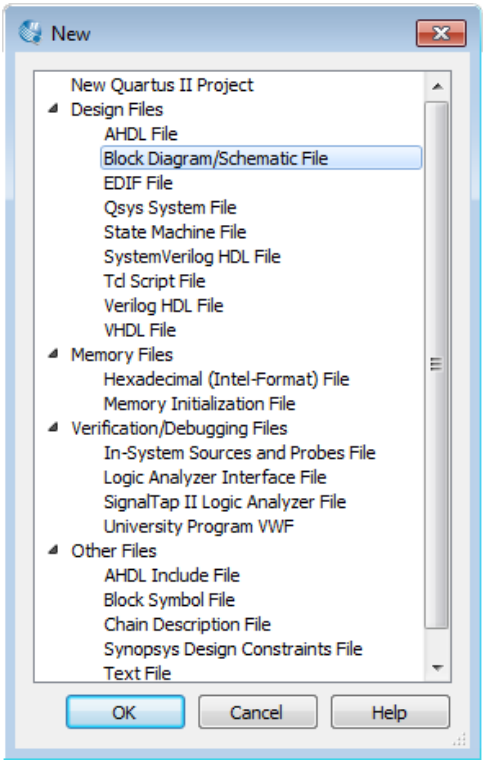
4. Click on **Next** in "EDA Tool Settings" and then click on **Finish**.



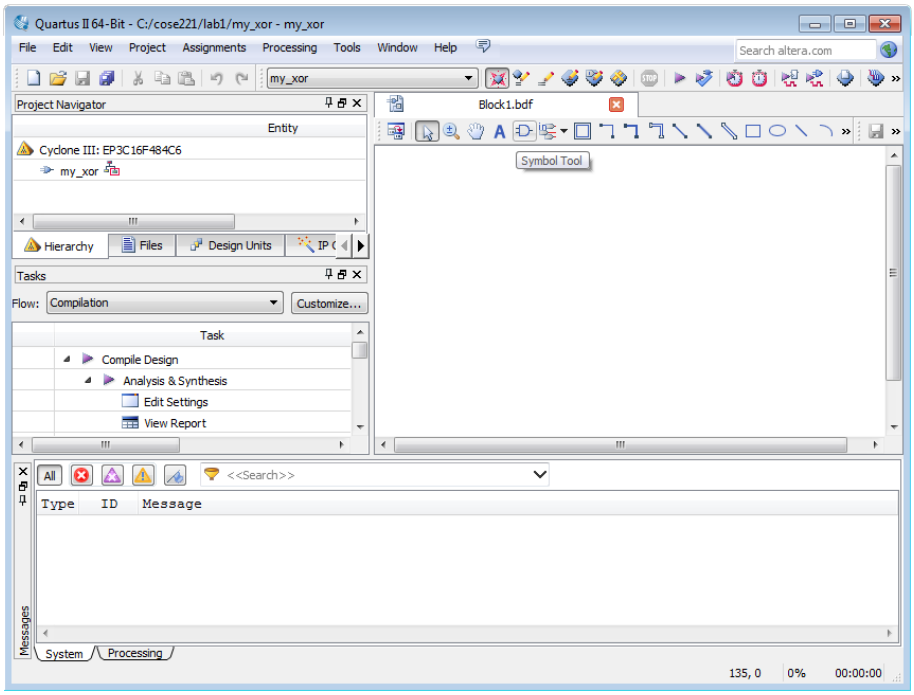


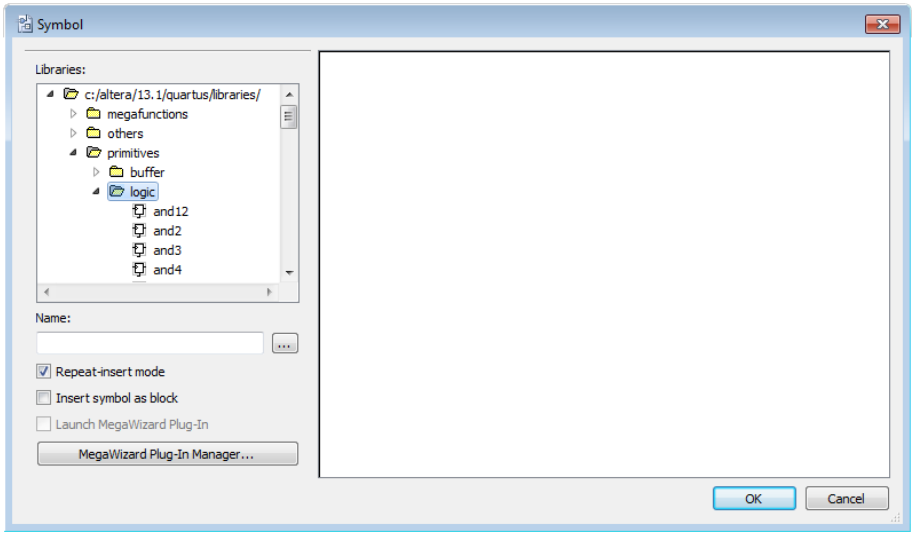
5. Select **File > New** and choose **Block Diagram/Schematic File** under Design Files category.

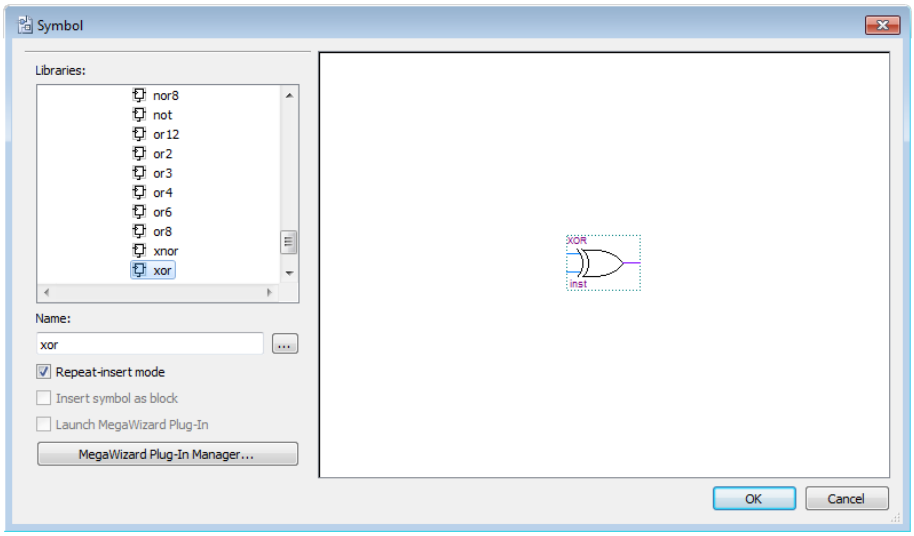




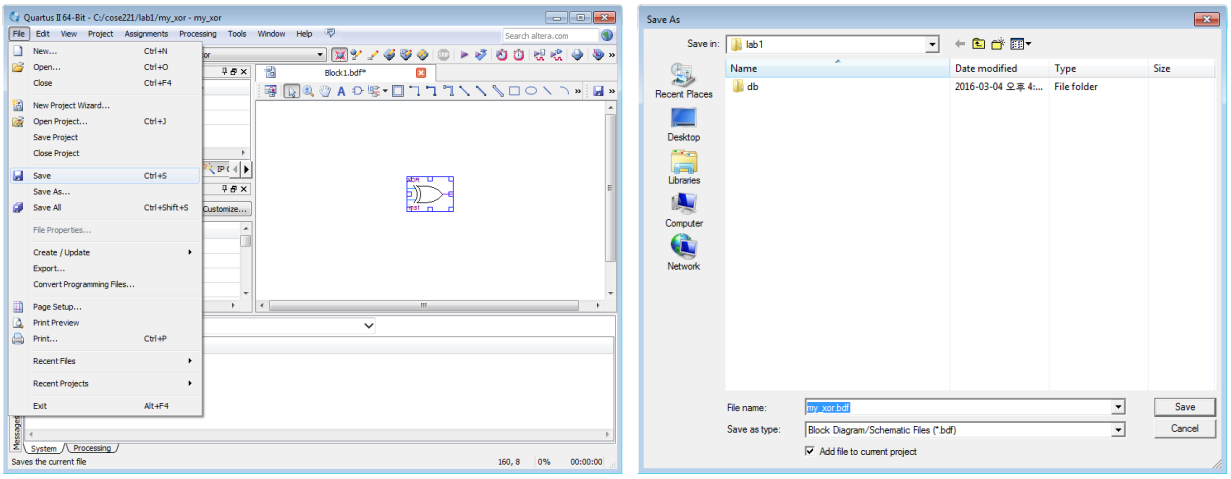
6. Click on **Symbol Tool** ( ), expand by clicking "▷", and select **xor** logic.



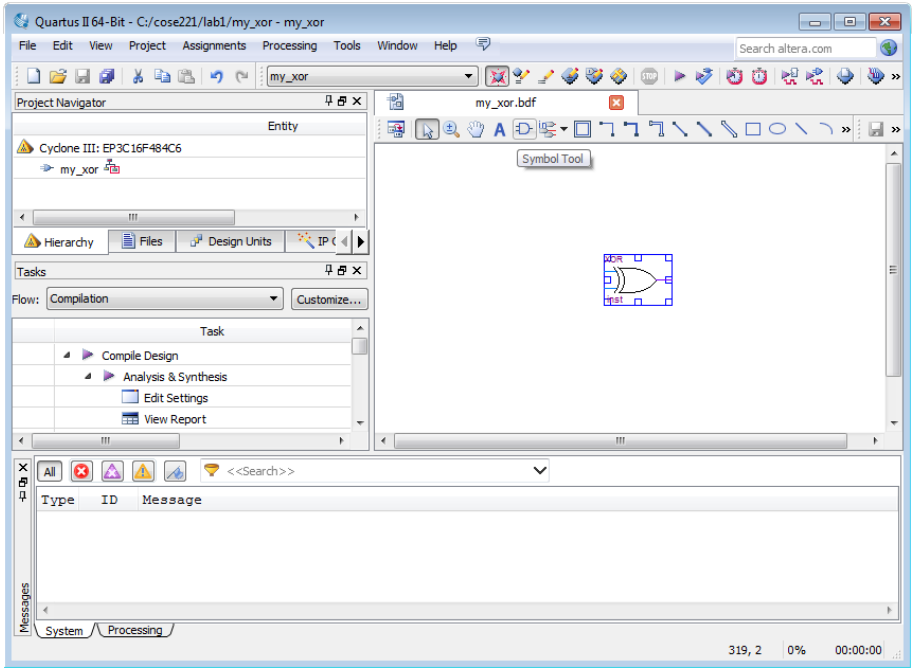


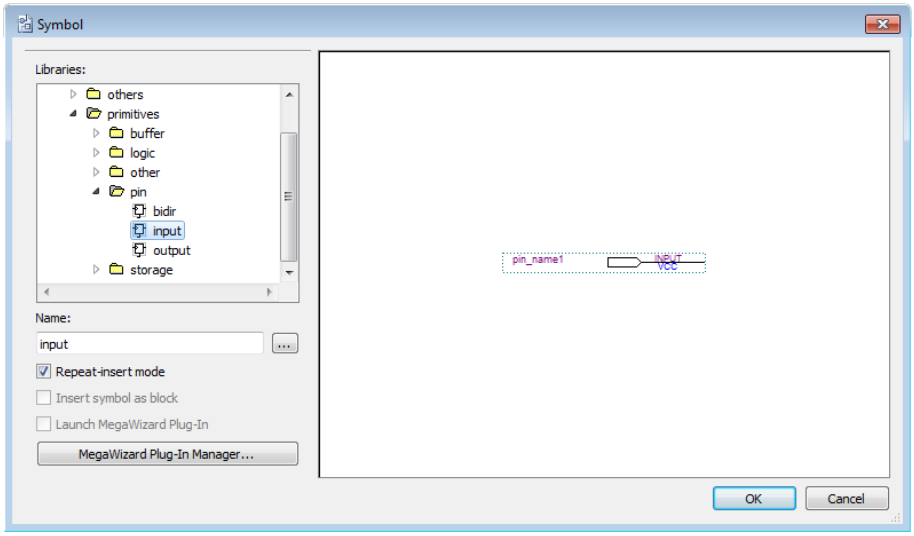


7. Select **File > Save** and type “my_xor” in the File name field, and click on **Save**.

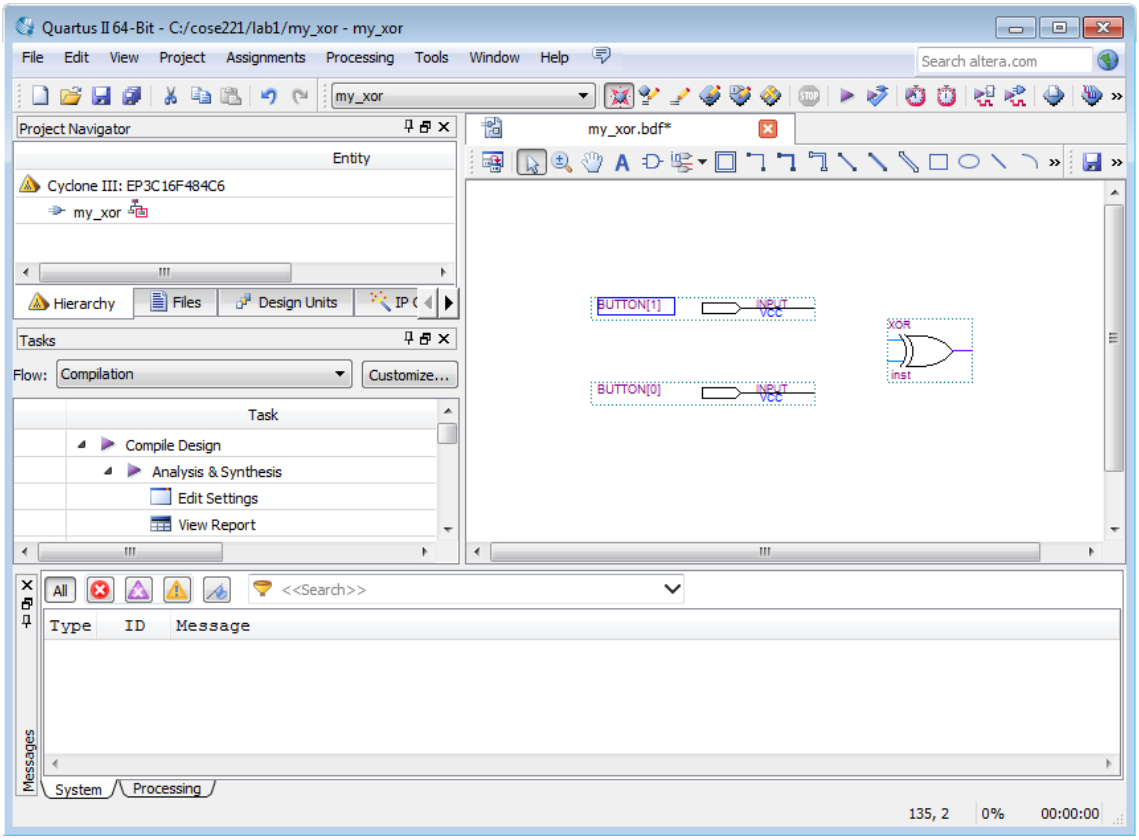


8. Click on **Symbol Tool** ( ) and select **input** pin.

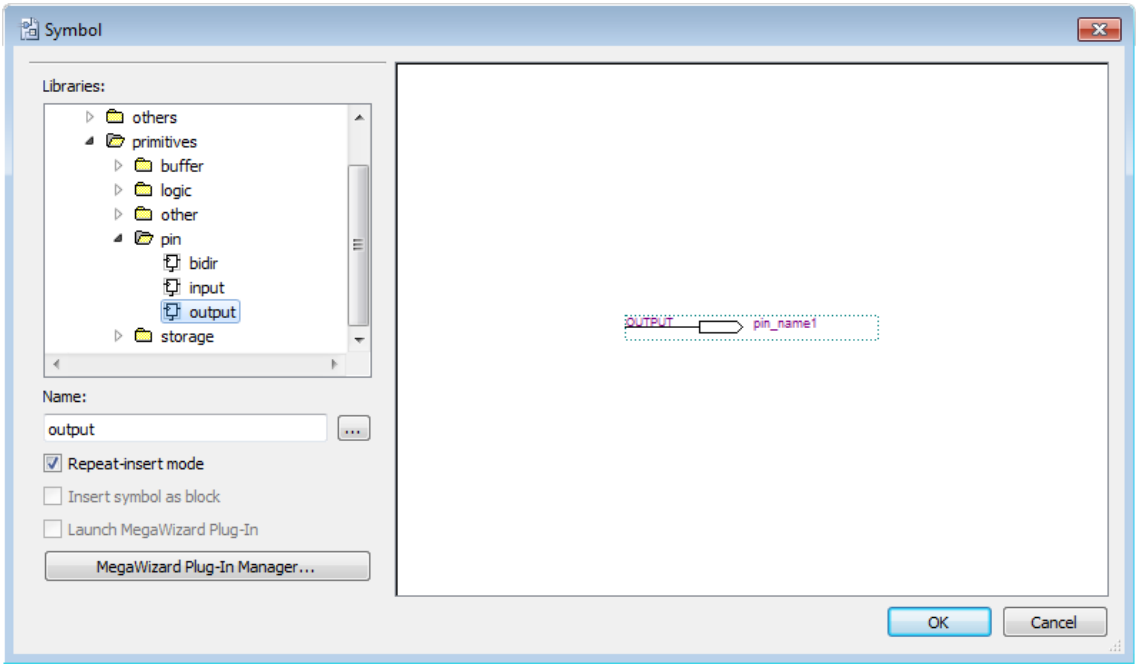


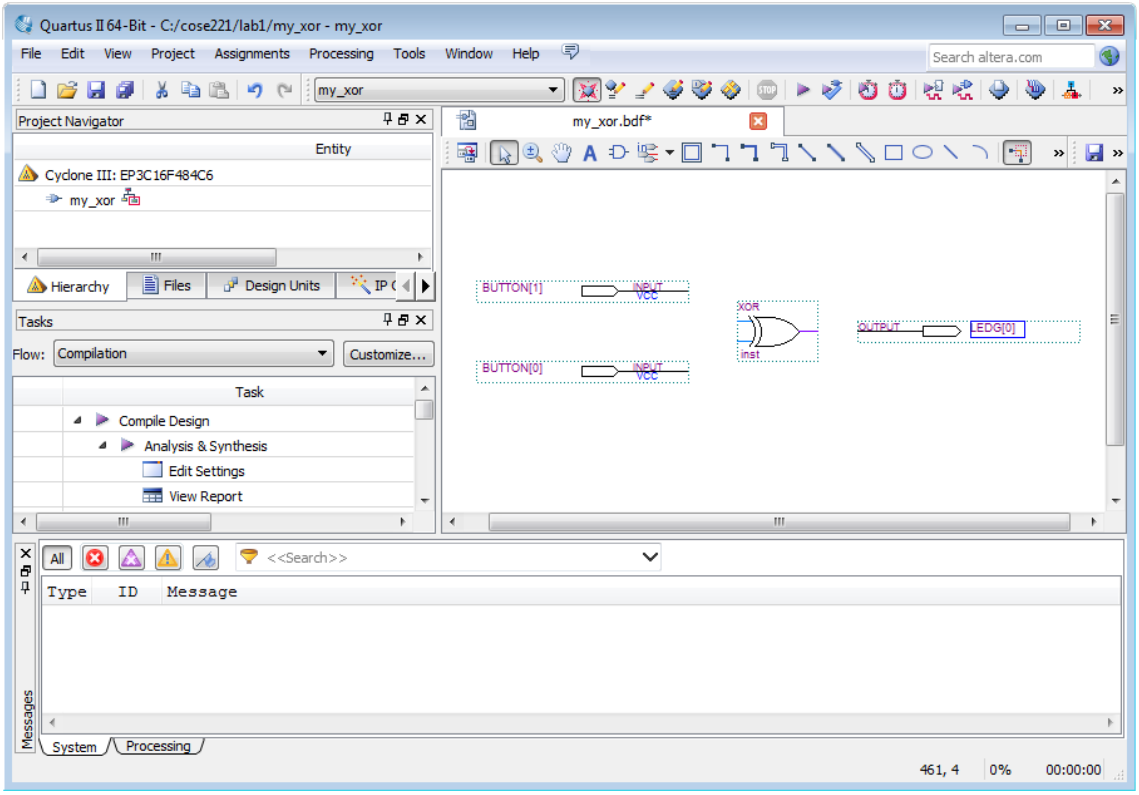


9. Instantiate the input pin two times and name it to “BUTTON[1]” and “BUTTON[0]”
    - Alera FPGA devices use pin names such as PIN_G3 and PIN_H2. It is not intuitive at all. So, Quartus-II provides a way to rename the pin names, which are specified in the excel file (DE0_pin_assignments.csv). The excel file is linked on the course page. If you open up the file, you will find that PIN_G3 is renamed to BUTTON[1], and PIN_H2 is renamed to BUTTON[0]. It is much more intuitive to use BUTTON than PIN_.. in your design, right?

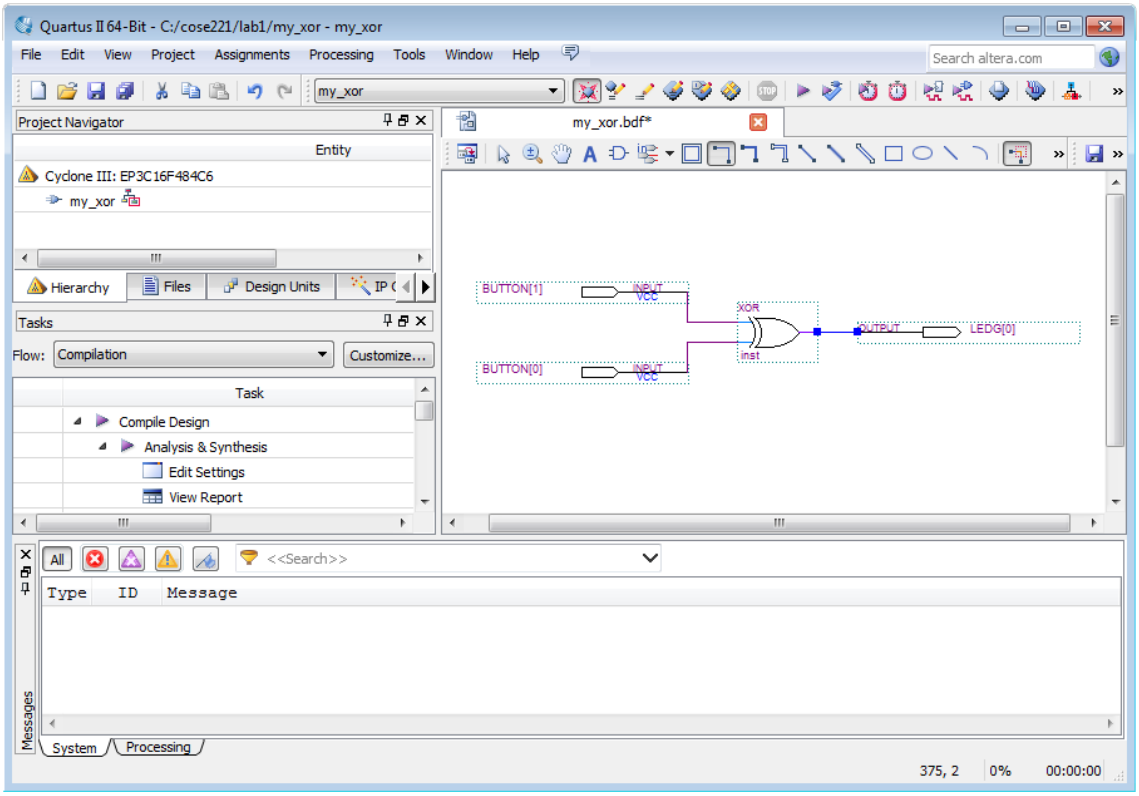


10. Instantiate the output pin and name it to “LEDG[0]”

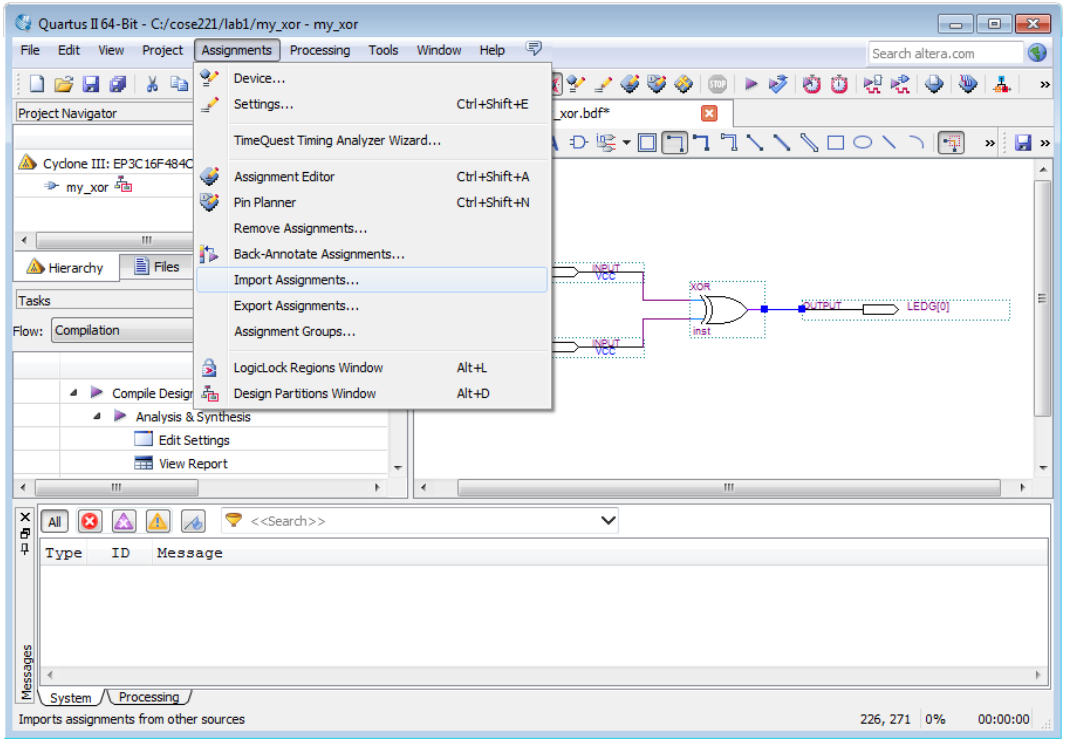


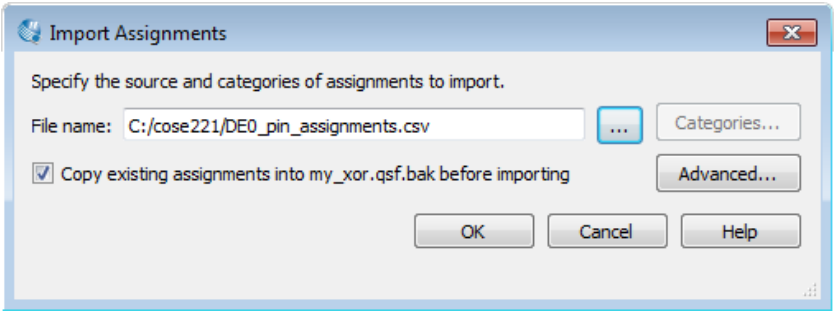


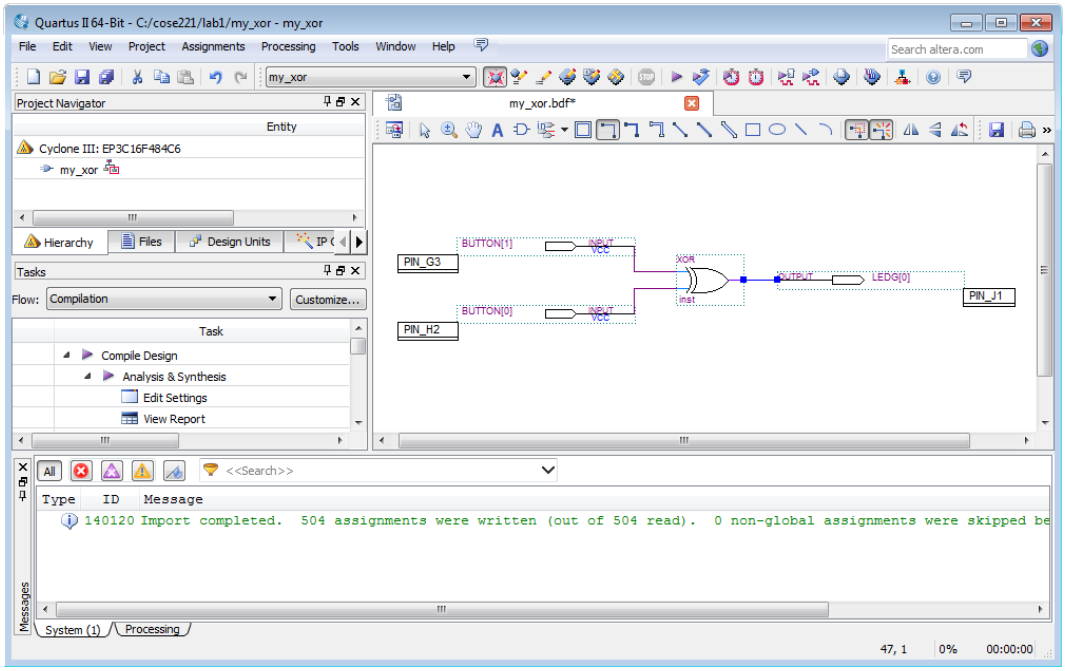
11. Connect the input pins to the xor gate inputs and the xor output to the output pin.



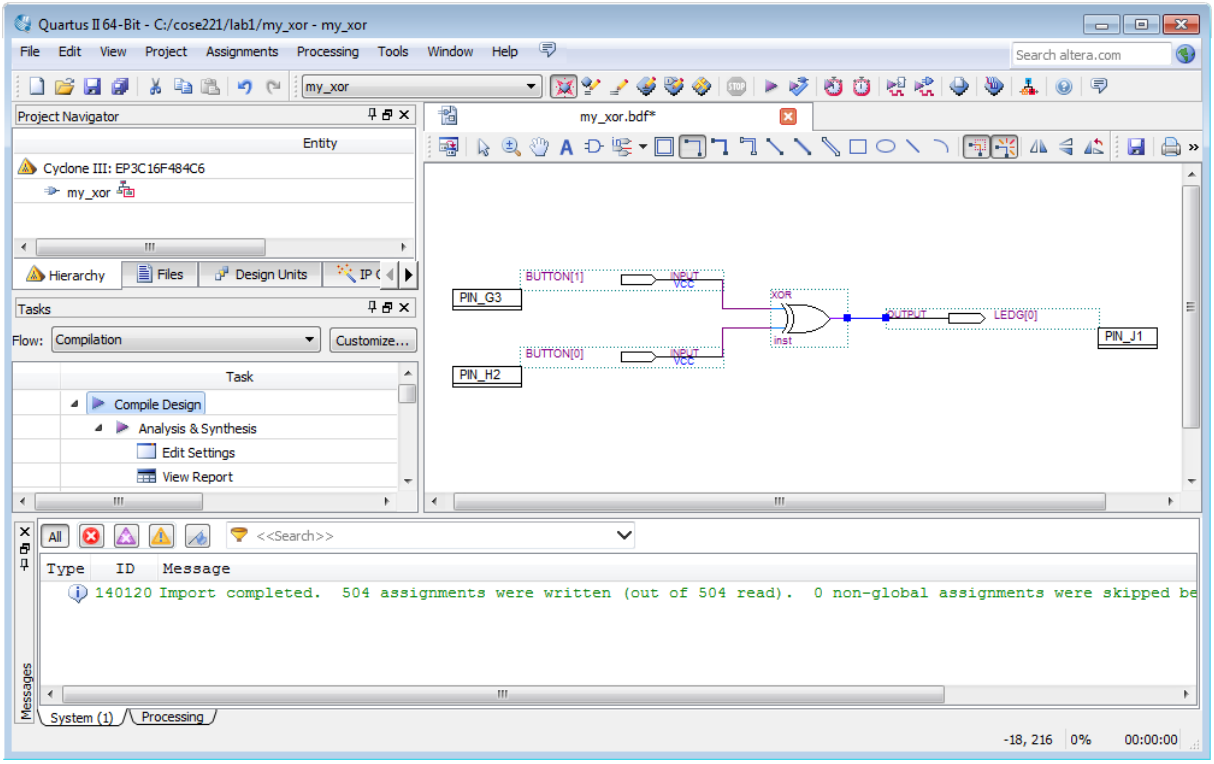
12. Select **Assignments > Import Assignments** and import the excel file linked on the class web.
    - The excel file (DE0_pin_assignments.csv) contains pin assignment mapping.



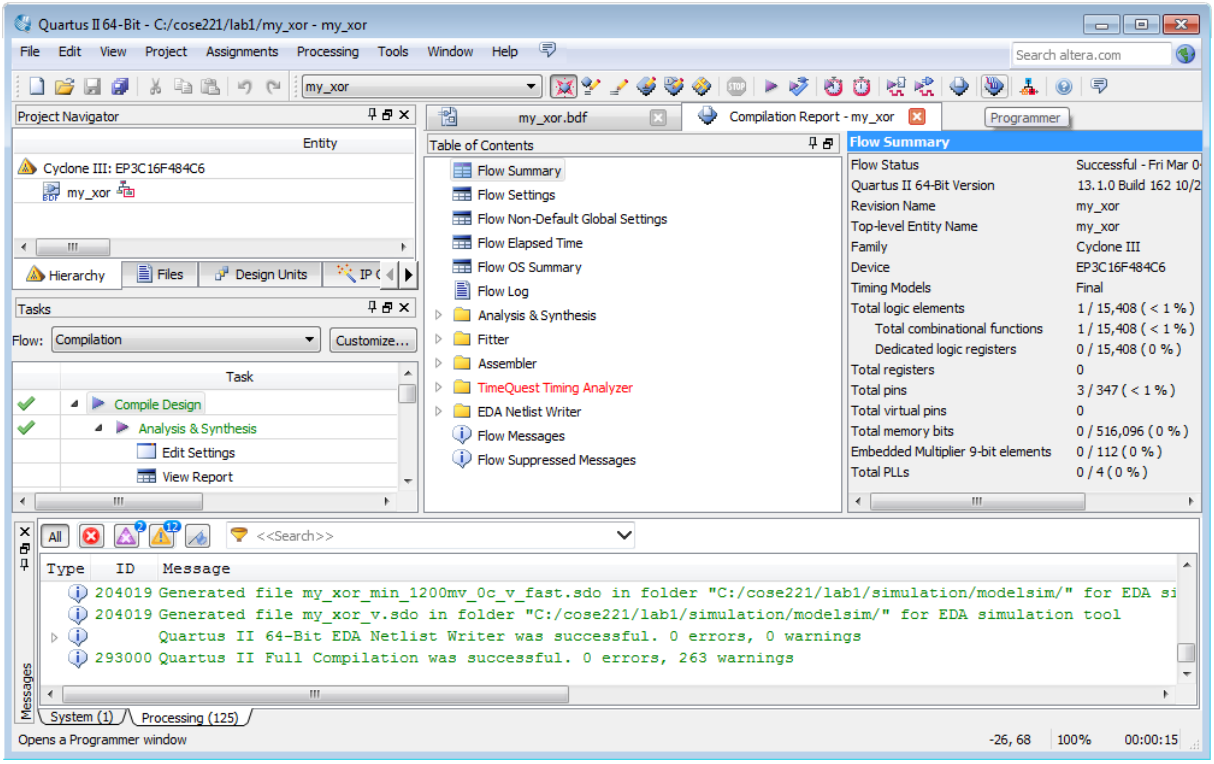




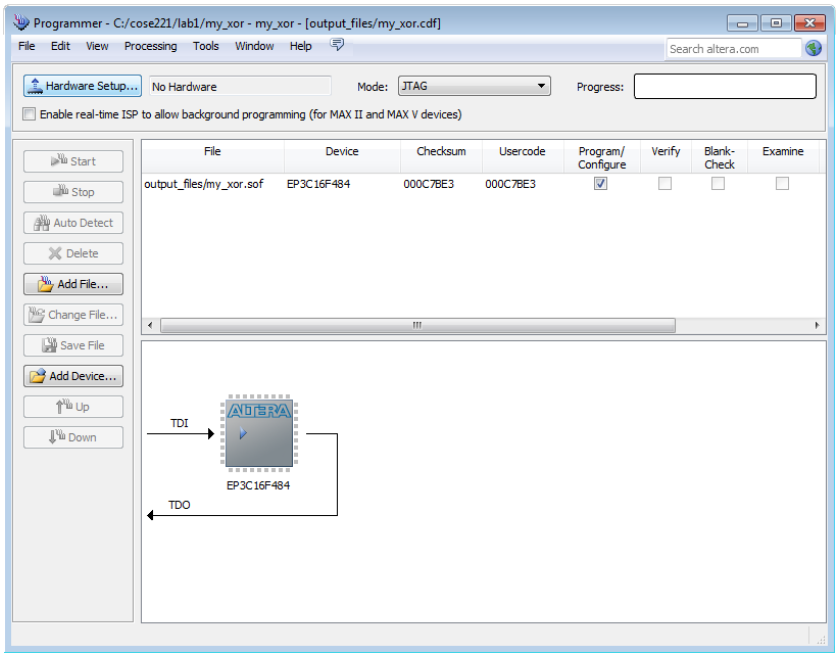
13. Ok. We are done with the design. Now double-click on **Compile Design** in the Tasks pane.

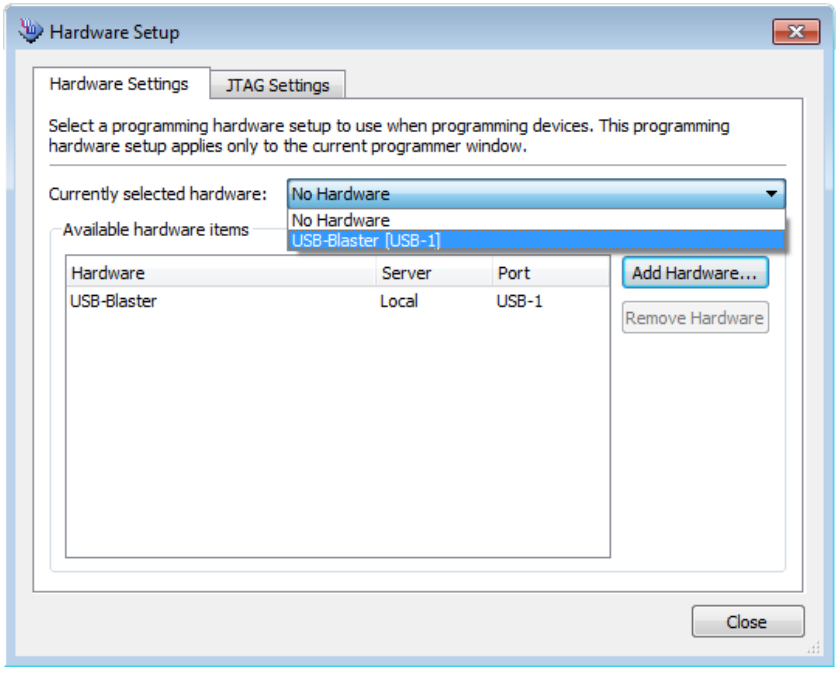


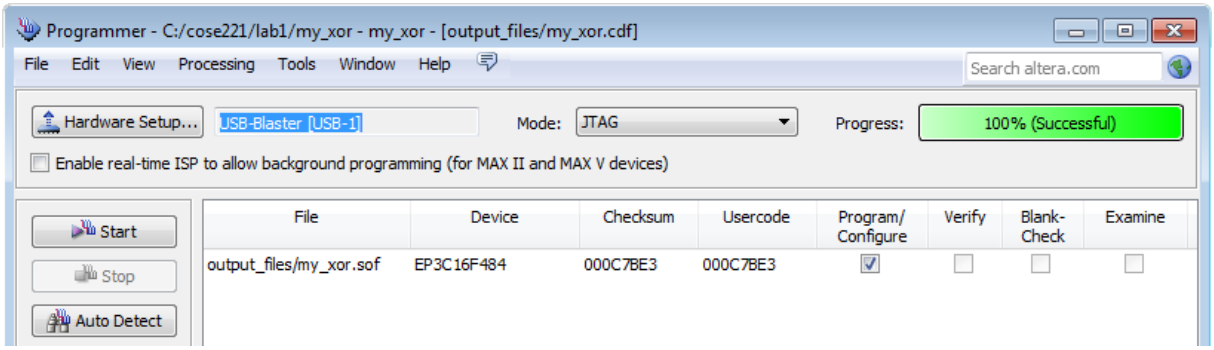
14. Download the design (my_xor) to the Cyclone-III FPGA on DE0 board by clicking on **Programmer** ( ).



15. Click on **Start**. Now test your XOR by pushing the buttons on the DE0 board.

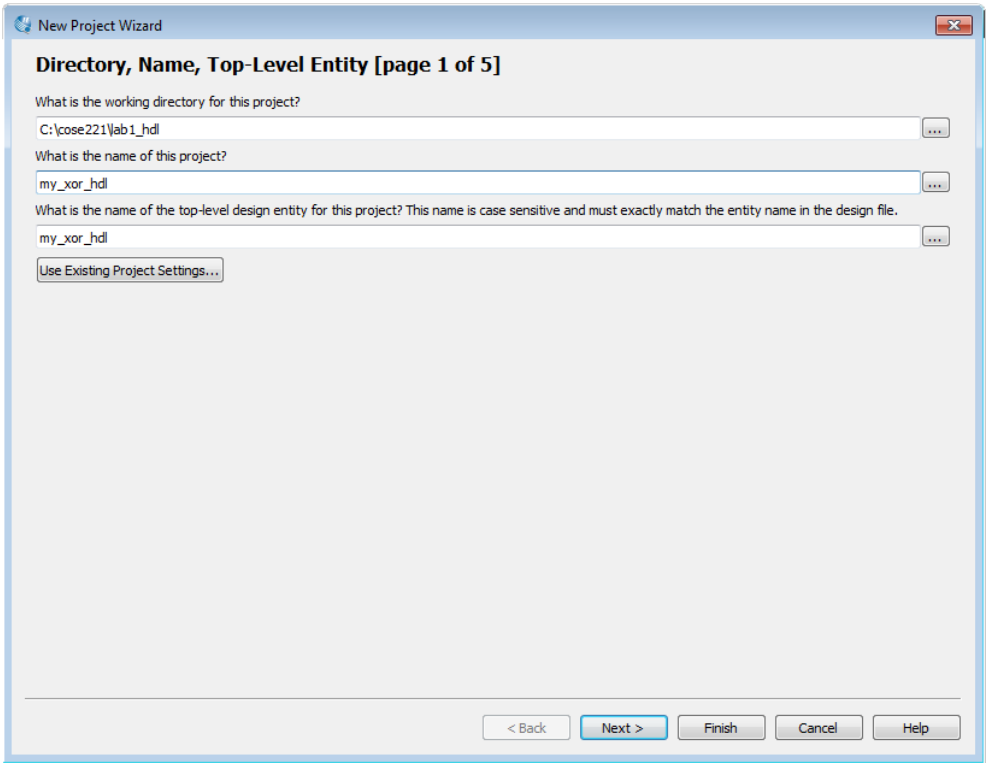




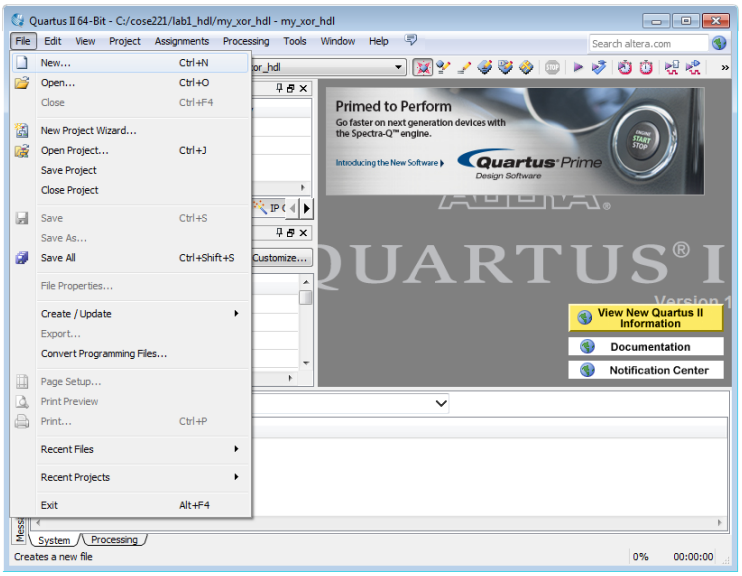


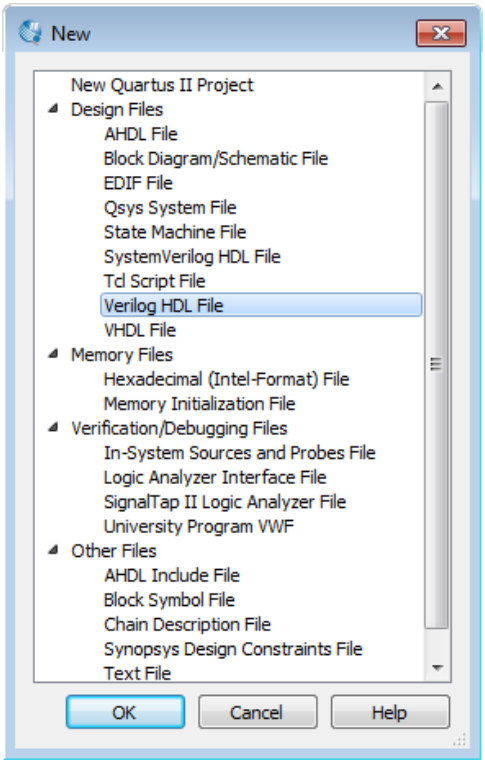
2. HDL-Based Design

1. Follow the same steps from step 1 to step 4 as in Schematic-based design.
    - But in this case, we create another directory called “lab1_hdl” and enter the project name to “my_xor_hdl” as shown below.



2. Select **File > New** and choose **Verilog HDL File** under Design Files category.





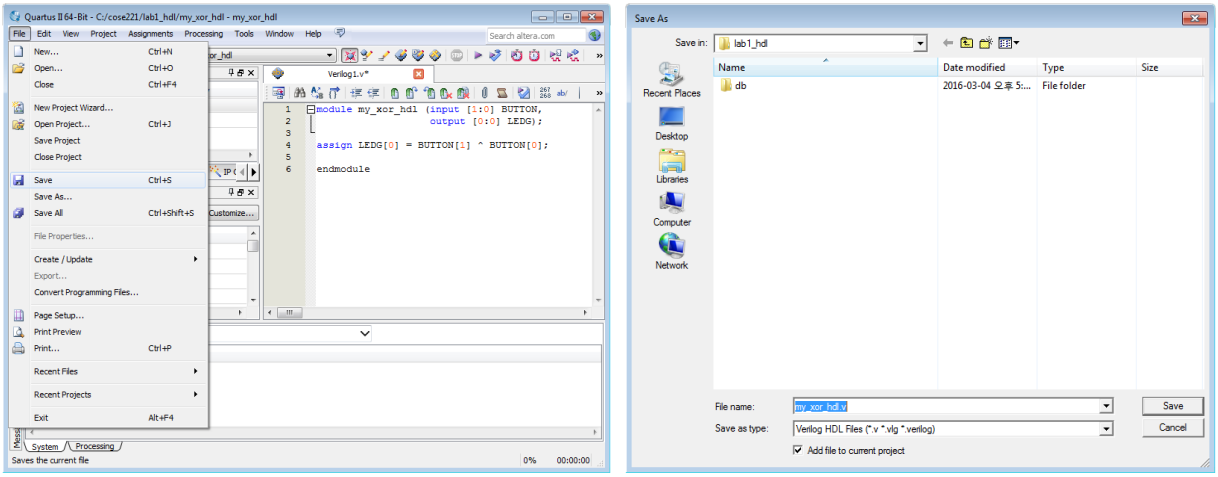
3. Copy the code shown below.

```
module my_xor_hdl (input  [1:0] BUTTON,
                   output [0:0] LEDG);

assign LEDG[0] = BUTTON[1] ^ BUTTON[0];

endmodule
```

4. Select **File > Save** and type "my_xor_hdl" in the File name field, and click on **Save**.



5. Follow the same steps from the step 12 to the end in Schematic-based design.