CVX601 Special Topics in Computer Science Technology

Lab Assignment #5

No late turn-in accepted

Design the digital logic inside coffee vending machine using Verilog-HDL. A cup of coffee costs 600 won. The vending machine only accepts 100 won, 500 won, and 1000 won. Use the following pins as the inputs and outputs.

- Reset: SW[9]
- Clock: 50MHz
- Inputs:
  - 100 won: SW[0]
  - 500 won: SW[1]
  - 1000 won: SW[2]
- 1 coffee out: SW[3]
- Change out: SW[4]
- Display the accumulated inserted money on 7 segments
  - Use HEX1, and HEX0 to display the inserted money (upper 2 digit numbers). For example, display 1 on HEX1 and 5 on HEX0 for 1500 won.
- Display the number of coffee that can be dispensed with the money on HEX3

Requirements:

- The machine accepts up to 2000 won.
- The other rules are the same as a real vending machine you use on campus.

What and How to submit:

1. Upload video clip (3-min?) and source code (Verilog code and Testbench) to Blackboard. Your video clip should have **at least** the following contents:
   - Your smiling face
   - Source code explanation (Verilog source code and Testbench)
   - ModelSim simulation explanation
   - Demo on DE0 board

Note: This is an individual assignment. You are welcome to discuss, but DO NOT COPY solutions. If you are found to copy solutions from others or slightly modify the solutions from others, both of you will be given 0 credits.