Exercise 3

AN4: Analog-to-digital inputs

C1IN-: Comparator negative input

CN6: Change notification which voltage changes on these pins can generate interrupts

RB4: Digital I/O pins

From table 2.2, pin 12 in PIC32MX795F512H does not have a 5.5 V tolerant.

Exercise 4

TRISx register bit = 1, configures the corresponding I/O pin as an input, and setting a TRISx register bit = 0, configures the corresponding I/O pin as an output.

PORTCINV is commonly used to toggle a bit which the operation is performed in hardware atomically and using fewer instructions. We can abbreviate the read-modify-write to the INV function.

Exercise 5

In 0-15 bit range, the reset value in hexadecimal is 0x00c3.

In 16-31 bit range, the reset value in hexadecimal is 0x0000.

Exercise 6

SYSCLK: SYSCLK clocks the CPU at a maximum frequency of 80 MHz, adjustable down to 0 Hz.

PBCLK: PBCLK is used by many peripherals, and its frequency is set to SYSCLK's frequency divided by 1, 2, 4, or 8.

PORTA to PORTG: Digital I/O ports allow you to read or output a digital voltage, and the buffer type of PORTA to PORTG is Schmitt Trigger input with CMOS levels not analog input.

Timer1 to Timer5: The PIC32 has five 16-bit counters/timers which the counter counts the number of the pulses of a signal and the timers are just counters with input at a fixed frequency.

10-bit ADC: The ADC can be programmed to continuously read data from a sequence of input pins, or to read a single value which has 10 bits of resolution allowing it to 1024 different voltage levels.

PWM OC1-5: Output compare is commonly used to generate pulse-width modulated signals that can control motors or be low-pass filtered to create a specified analog voltage output.

Data RAM: RAM where your temporary data stored is generally less plentiful on PIC32's which has 128 KB, volatile that its contents are not preserved when powered off, and faster to read and write.

Program Flash Memory: Flash where your program stored is generally more plentiful on PIC32's which has 512 KB, nonvolatile that its contents are preserved when powered off, but slower to read and write.

Prefetch Cache Module: It stores recently executed program instructions which are likely to be executed soon and run ahead of the current instruction and predictively prefetch future instruction into cache in linear code with no branches.

Exercise 7

PORTA to PORTG, Priority interrupt controller, USB, CAN1, CAN2, Ethernet, DMAC, ICD, Prefetch module, bus matrix and data RAM.

Exercise 8

For a 10-bit ADC with a reference voltage of 3.3 V, the integer output value of 2^{10}-1 corresponds to a voltage of approximately 3.297 V which means any voltage above this value will also give a digital output of 1023.

Exercise 9

For loops up to 256 bytes long can be completely stored in the cache which the sixteen fully associative lockable 16-byte cache lines supply an instruction every clock.

Exercise 10

The data path to the CPU is 32 bits wide, the data path to the program flash memory is 128 bits wide. This wide data path provides the same bandwidth to the CPU as a 32-bit path running at four times the frequency. The data path between the prefetch module and flash memory is 128 bits wide to allow it to run ahead of CPU execution despite the slower flash load times.

Exercise 11

An output pin can be configured as open drain. In this configuration, the pin is connected by an external pull-up resistor to a voltage of up to 5.5 V which allows digital output swing between 0 to 4 V powered by 3.3 V.

Exercise 12

(a)Flash memory: 512KB, 7 D000

(b)RAM: 128KB, 1 F400

Exercise 13

(a) PBDIV<1:2> bits, most of the peripherals on the device are clocked using the PBCLK. The peripheral bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals.

(b)

a. FWDTEN: Watchdog Timer Enable bit

1 = The WDT is enabled and cannot be disabled by software.

0 = The WDT is not enabled; it can be enabled in software.

b. The WDT has a 5-bit postscaler to create a wide variety of time-out periods. This postscaler provides 1:1 through 1:1048576 divider ratio.

WDTO: Watchdog Time-out bit

1 = A Watchdog Timer time-out has occurred since either the device was powered up or the WDTO bit was last cleared by software.

0 = A Watchdog Timer time-out has not occurred since either the WDTO bit was cleared by software or the device was reset.

c. The postscaler settings are selected using the WDTPS<4:0> Configuration bits in the DEVCFG1 register. WDTPS<4:0>=10100.

(c) bit 5

SLOCK: PLL Lock Status bit

1 = PLL module is in lock or PLL module start-up timer is satisfied

0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

Exercise 14

5 V regulator provides up to 1 A, $R = \frac{V}{I}$ and we can know the smallest resistance is 5 Ω.

Exercise 15

The PIC32 requires a supply voltage VDD between 2.3 and 3.6 V, and the NU32 provides a 3.3 V voltage regulator providing a stable voltage source for the PIC32 and other electronics on board. Since it is often convenient to have a 5 V supply available, the NU32 also has a 5 V regulator.

Exercise 16

The two LEDs, LED1 and LED2, are connected at one end by a resistor to 3.3 V and the other end to digital outputs RF0 and RF1 which is located at pin 58 and pin59 on the PIC32MX795F512H.