Midterm Project of Machine Vision

Lead Frame Inspection

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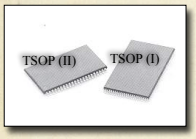
IC Packaging

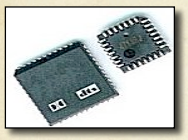
- IC packaging is the final stage of semiconductor device fabrication.
- The tiny block of semiconducting material is encased in a supporting case in order to be connected with other electronic components or devices.

Purposes of IC Packaging

- Power distribution
- Signal distribution
- Heat dissipation
- Support and protection

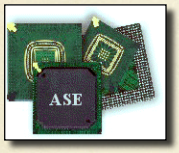
Categories of IC Packaging

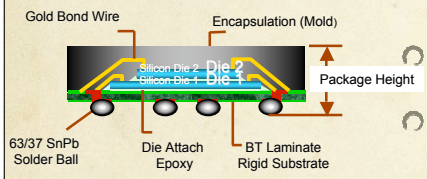


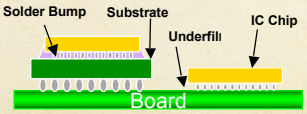


- **DIP (Dual Inline Package)**: low I/O (2-68 I/Os) , low cost
- **TSOP（Thin Small Outline Package）**: low I/O (2-68 I/Os)
- **PLCC（Plastic Leaded Chip Carrier）**: Medium I/O (18-100 I/Os)
- **QFP (Quad Flat Package)** : Medium I/O (36-308+ I/Os), **LQFP（Low QFP）, TQFP（Thin QFP）, VQFP（Very thin QFP）**

Categories of IC Packaging (cont'd)



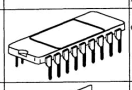
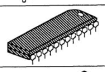
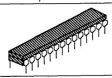
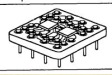




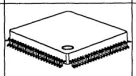
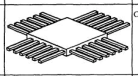
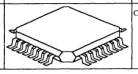
Flip Chip in Package (FCIP) Flip Chip on Board (FCOB)

- BGA (Ball Grid Array)
- CSP (Chip Size Package): High density packaging technique
- Flip Chip
- MCM (Multi-Chip Module)

Two Common Types

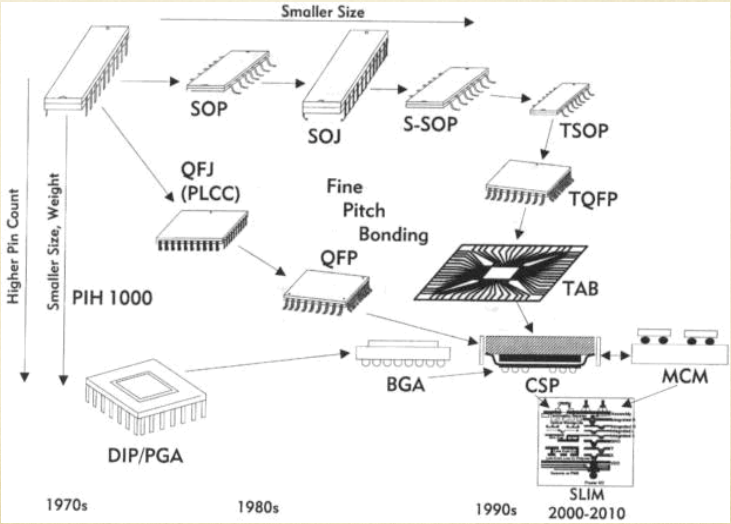
Through hole mount	Shape	Typical features		
		Material	Lead pitch	# of I/O pins
DIP Dual in-line package		Ceramic Plastic	• 2.54 mm (100mil)	8 - 64
SIP Single in-line package		Plastic	• 2.54 mm (100mil) • 1 direction lead	3 - 25
ZIP Zigzag in-line package		Plastic	• 2.54 mm (100mil) • 1 direction lead	16 - 24
S-DIP Shrink dual in-line package		Plastic	• 1.778 mm (70mil)	20 - 64
SK-DIP Skinny dual in-line package		Ceramic Plastic	• 2.54 mm • half- size pitch in the width direction	24 - 32
PGA Pin grid array		Ceramic Plastic	• 2.54 mm (100mil)	

Through-hole packages

Surface mount	Shape	Typical features		
		Material	Lead pitch	# of I/O pins
SOP Small outline package		Plastic	• 1.27mm (50mil) • 2 direction lead	8 - 40
QFT Quad flat-pack		Plastic	• 1.0 mm • 0.8 mm • 0.65 mm • 4 direction lead	88 - 200
FPG Flat package of glass		Ceramic	• 1.27 mm (50mil) • 0.762mm (30mil) • 2 direction lead • 4 direction lead	20 - 80
LCC Leadless chip carrier		Ceramic	• 1.27mm (50mil) • 1.016mm (40mil) • 0.762mm (30mil)	20 - 40
PLCC Plastic leaded chip carrier		Ceramic	• 1.27mm (50mil) • j-shaped bend • 4 direction lead	18 - 124
VSQF Very small quad flatpack		Ceramic	• 0.5mm	32 - 200

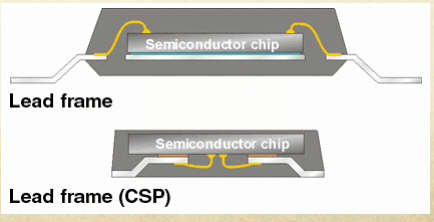
Surface Mount Technology (SMT)

Trend of IC Packaging



Lead Frames

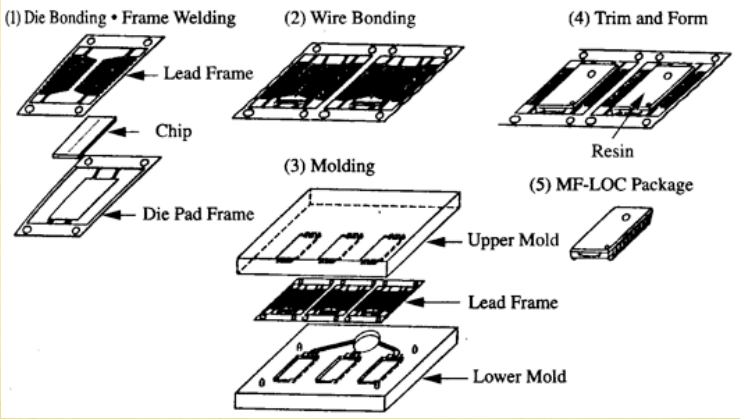
- The metal structures inside a chip package that carries signal from the die to the outside
- A die is a small block of semiconductor material, on which a given functional circuit is fabricated.
- In the last stage of the manufacturing process, the lead frame is molded in plastic case, and outside of the lead frame is cut-off, separating all leads



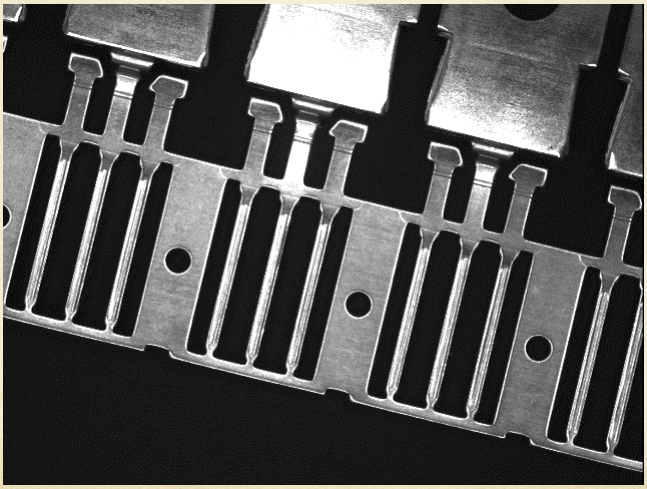
Manufacturing Process

- Lead frames are manufactured by removing material from a flat plate of copper or copper-alloy.
- Etching (for high density of leads)
- Stamping (for low density of leads)

LOC Package Manufacturing Process



A Sample Lead frame



Midterm Project: Lead frame Inspection

1. Your program should be able to "read" an image of lead frame as shown in previous slide.
2. The input is an image of lead frame and the output should include
   * The number and diameter of circular holes
   * The width of all leads
   * The inclination angle of the lead frame
3. Try to make your inspection algorithm as automatic as possible. In other words, make human intervention as little as you can.
4. **Good luck!**