Youngjin (YJ) Eum

(650) 804-0321 ◇ Pittsburgh, PA (open to relocation) ◇ F-1 student on OPT
yjeum@cmu.edu ◇ linkedin.com/in/yjeum11

Education

Carnegie Mellon University — Pittsburgh, PA
Master of Science in Electrical & Computer Engineering — May 2026
Bachelor of Science in Electrical & Computer Engineering, Minor in Mathematical Sciences — May 2025
GPA: 3.97/4.00
Relevant Coursework: Modern Computer Architecture, Logic Design and Verification, Digital IC Design

Experiences

SPIRAL Lab — Pittsburgh, PA
Research Assistant — Mar 2024 – Present
- Built ISA extension for RISC-V multi-word modular arithmetic, achieving 5x speedup for FFT benchmarks
- Designed RTL modifications to open-source hardware to implement ISA extension and verified correctness
- Utilized C and assembly benchmarks to analyze performance and presented findings at IEEE HPEC conference

Structure and Design of Digital Systems TA — Pittsburgh, PA
Teaching Assistant — Aug 2023 – Present
- Lead small group sections of 10 students to review digital design concepts and mentor students
- Manage lab sessions where students implement FPGA projects, teaching valuable debugging skills
- Grade homework assignments and lab reports, providing comprehensive feedback to a class of over 100 students

Bayer — Indianola, PA
Electrical Engineering Intern — May 2023 – Aug 2023
- Developed a buck converter using LTSpice, achieving >95% efficiency by optimizing for thermal performance
- Utilized oscilloscope and logic analyzer to probe and debug high-speed signals, improving rise time and ringing
- Created analysis reports of test results/observations and presented to management and adjacent teams

Projects

Build18 Project — Pittsburgh, PA
Hardware Hackathon — January 2024
- Built a real-time bus tracker using ESP32 using the Pittsburgh Regional Transit API to accurately track 8 bus lines
- Managed a tight timeline of a week with 4 teammates to complete a functional prototype of the physical model
- Won the Officer's choice award, chosen by student officers out of 30 teams

RISC-V CPU Project — Pittsburgh, PA
Course Project — January 2024 – May 2024
- Built an RTL-level implementation of an in-order RISC-V core supporting the full RV32I instruction set with a team of 3 using SystemVerilog
- Optimized the core, achieving a 2x increase in MIPS/watt by analyzing tradeoffs in terms of performance and power using a cache and out-of-order writeback

SRAM Project — Pittsburgh, PA
Course Project — October 2023 – November 2023
- Designed and implemented a 256 x 16-bit SRAM in Cadence Virtuoso using the Cadence generic PDK
- Analyzed engineering trade-offs regarding device sizing and circuit topologies to meet PPA requirements
- Verified read and write functionality and timing by running simulations, checked noise margins to ensure stability of cell

Skills

Technical FPGA, gem5, Cadence Virtuoso, Unix, Static Timing Analysis, Oscilloscope
Programming Python, SystemVerilog, SystemVerilog Assertions, Chisel HDL, C/C++, Tcl