Youngjin (YJ) Eum

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Education

Carnegie Mellon University — Pittsburgh, PA
Master of Science in Electrical & Computer Engineering — May 2026
Bachelor of Science in Electrical & Computer Engineering, Minor in Mathematical Sciences — May 2025
GPA: 3.97/4.00
Relevant Coursework: Modern Computer Architecture, Logic Design and Verification, Digital IC Design

Experiences

Apple — Beaverton, OR
CPU Design Verification Intern — May 2025 – Aug 2025

- Built Python framework to categorize hard-to-debug simulation timeouts using simulation trace
- Collaborated across teams to integrate system into internal triage database, providing debugging information at a glance
- Leveraged performance monitoring data to provide insights into performance behavior of random tests
- Debugged assertion failures in CPU using waveforms and contributed to analysis and root-causing of hardware bugs

SPIRAL Lab — Pittsburgh, PA
Research Assistant — Mar 2024 – Aug 2024

- Built ISA extension for RISC-V multi-word modular arithmetic, achieving 5x speedup for FFT benchmarks
- Designed RTL modifications to open-source hardware to implement ISA extension and verified correctness
- Utilized C and assembly benchmarks to analyze performance and presented findings at IEEE HPEC conference

Structure and Design of Digital Systems TA — Pittsburgh, PA
Teaching Assistant — Aug 2023 – May 2025

- Led small group sections of 10 students to review digital design concepts and mentor students
- Managed lab sessions where students implement FPGA projects, teaching valuable debugging skills
- Graded homework assignments and lab reports, providing comprehensive feedback to a class of over 100 students

Projects

Tapeout — Pittsburgh, PA
Course Project — January 2025 – May 2025

- Designed and verified custom radiation-hardened system-on-chip for use in aerospace environement
- Modified open-source bus protocol and memory module to use error correction for robustness against radiation
- Collaborated with a team of 5 to successfully manufacture custom chip with TSMC within strict deadlines

RISC-V CPU Project — Pittsburgh, PA
Course Project — January 2024 – May 2024

- Built an RTL-level implementation of an in-order RISC-V core supporting the full RV32I instruction set with a team of 3 using SystemVerilog
- Optimized the core, achieving a 2x increase in MIPS/watt by analyzing tradeoffs in terms of performance and power using a cache and out-of-order writeback

SRAM Project — Pittsburgh, PA
Course Project — October 2023 – November 2023

- Designed and implemented a 256 x 16-bit SRAM in Cadence Virtuoso using the Cadence generic PDK
- Analyzed engineering trade-offs regarding device sizing and circuit topologies to meet PPA requirements
- Verified read and write functionality and timing by running simulations, checked noise margins to ensure stability of cell

Skills

Programming Python, SystemVerilog, SystemVerilog Assertions, Perl, C/C++, Tcl, Unix