
Qspice KSKelvin Symbol Explanation

KSKelvin Kelvin Leung

Created on 9-3-2023

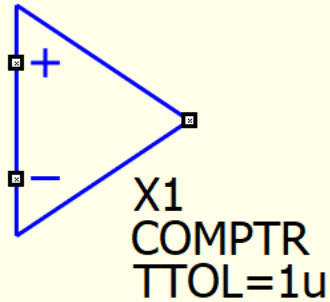
Last Updated on 7-11-2024

analog

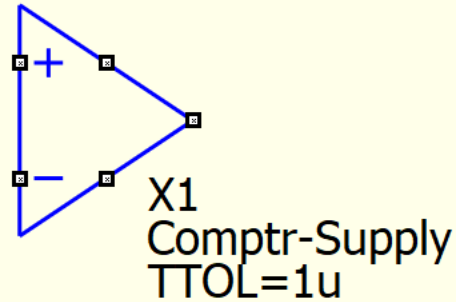
Comptr : 3 type of Ideal Comparators Overview

Qspice : Comptr.qsym | Comptr-OD.qsym | Comptr-Supply.qsym

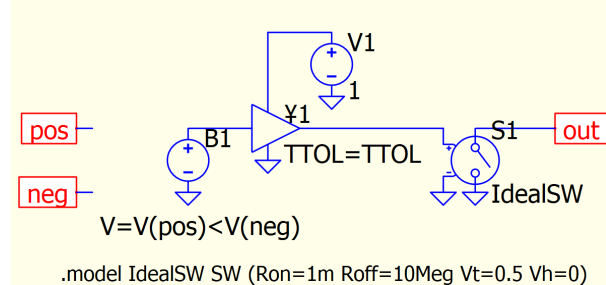
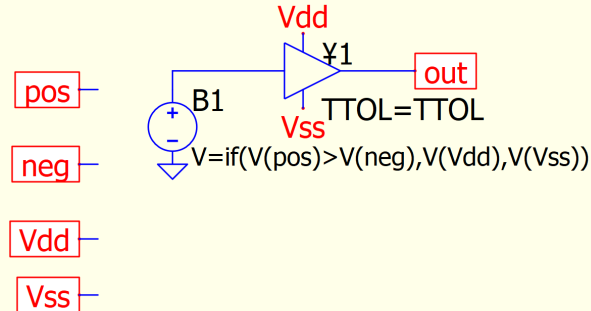
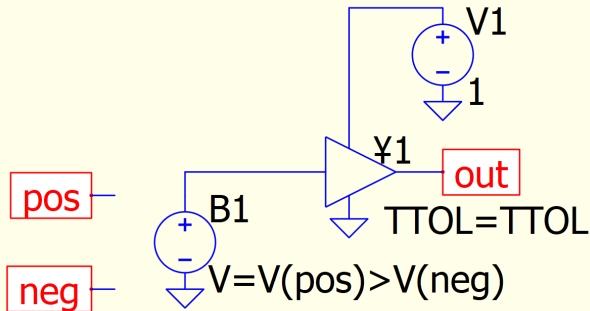
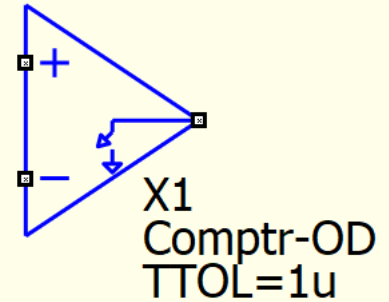
Ideal Comparator (Output 0/1)
Comptr.qsym



Ideal Comparator (Vdd/Vss)
Comptr-Supply.qsym

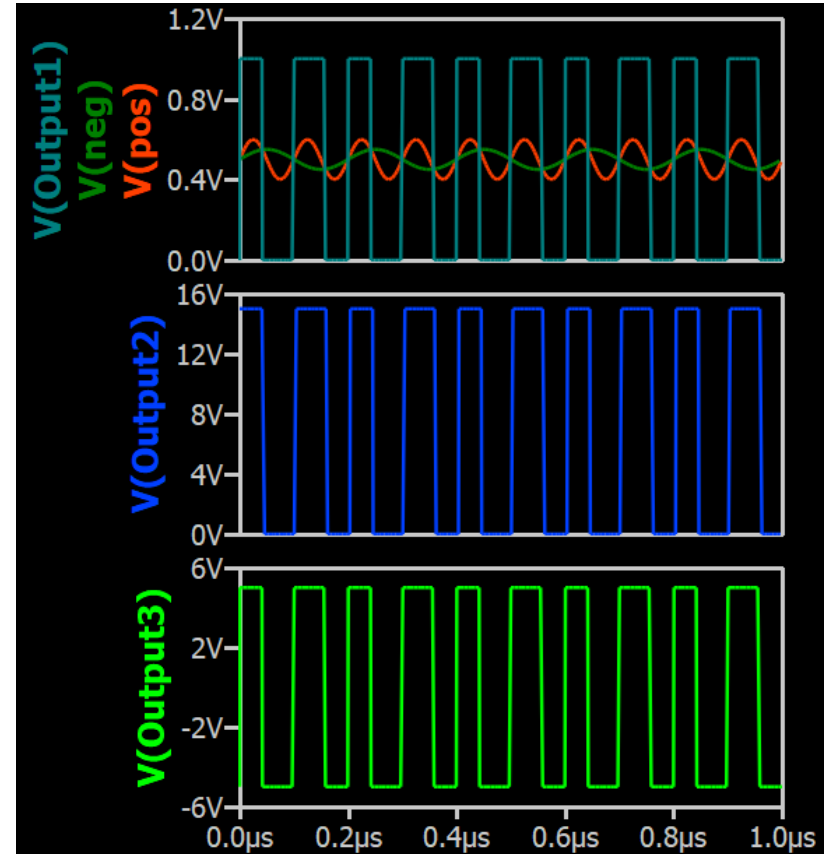
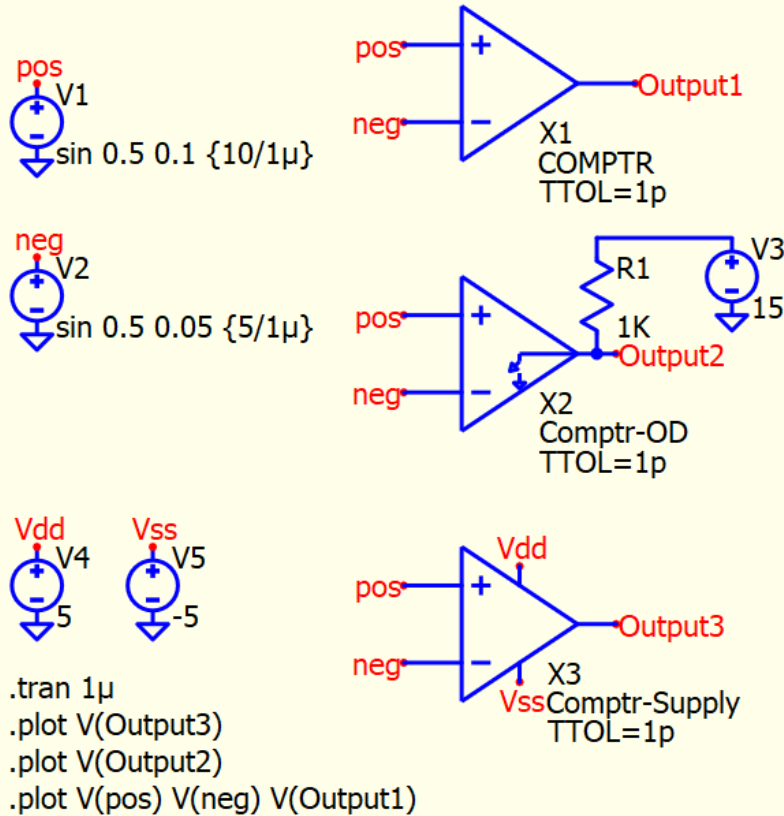


Ideal Comparator (Open Drain)
Comptr-OD.qsym



Comptr : 3 type of Ideal Comparators – Simulation Results

Qspice : Parent - Comparator.qsch



Delay

Qspice : Delay.qsym

- Delay

- Reason for Implementation

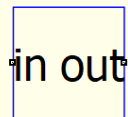
- Qspice B-source not offers delay function before 09/22/2023, but after that, Mike Engelhardt implemented delay(input,time) for arbitrary behavioral sources.

- Concept of Design

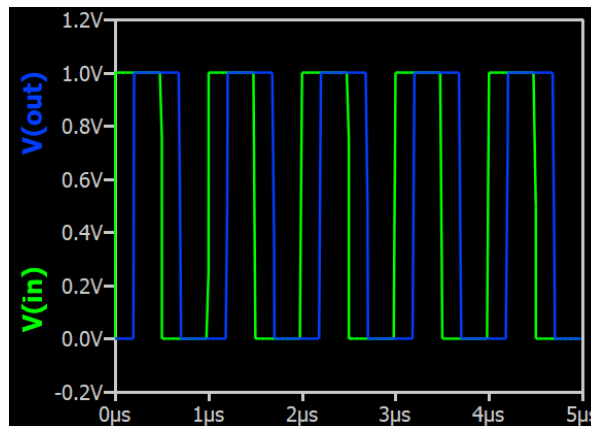
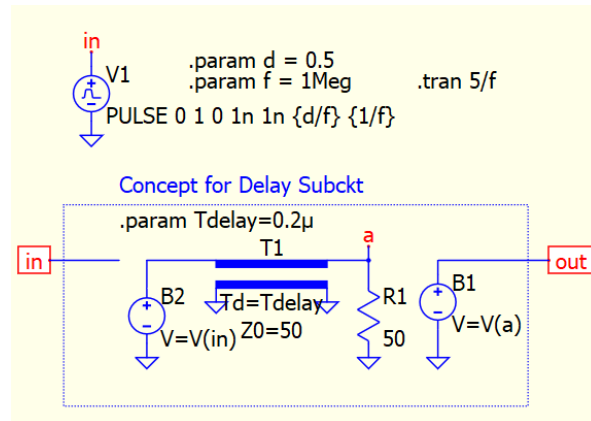
- T1 : T_d (delay) in ideal transmission line determines signal delay time
- R1 : To prevent signal reflection, transmission line must terminate with Z_0
- B1 : To prevent loading effect when using delay block

- Symbol of delay.qsym

X1



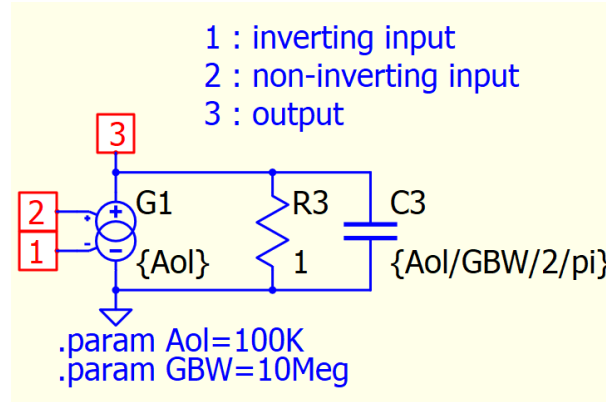
Tdelay=1m



Opamp-SinglePole : Operation Amplifier Single Pole

Qspice : Opamp-SinglePole.qsch

- Single Pole Opamp
 - This is single pole opamp subckt which used by LTspice and in its opamp.sub library
- Equivalent Formula
 - $V_{output} = Z(R_3, C_3) \times Aol \times I_{G1}$
 - $V_{output} = (R_3 // \frac{1}{j\omega C_3}) \times Aol \times (V_p - V_n)$



opamp.sub in LTspice library

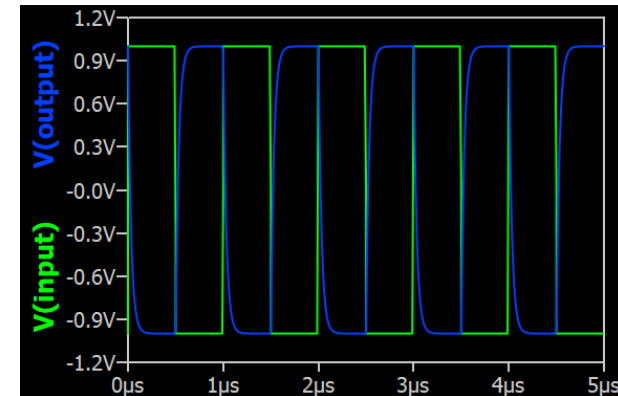
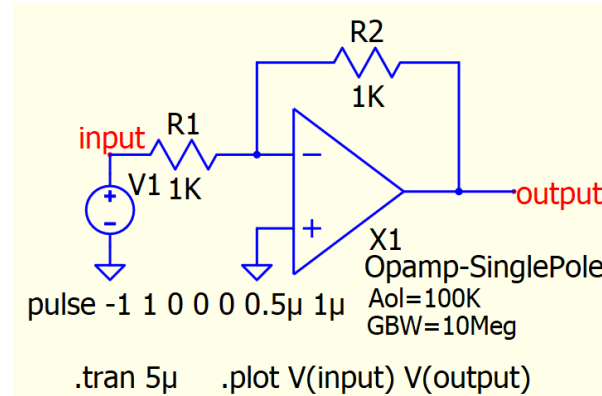
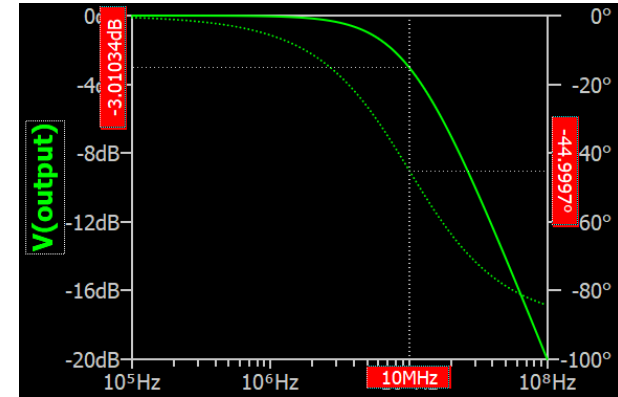
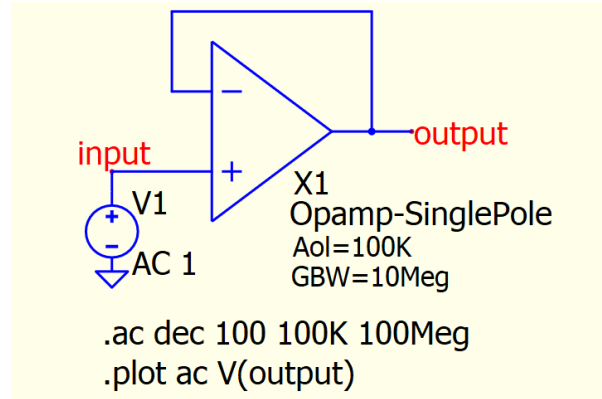
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```
.subckt opamp 1 2 3
G1 0 3 2 1 {Aol}
R3 3 0 1.
C3 3 0 {Aol/GBW/6.28318530717959}
.ends opamp
```

Opamp-SinglePole : Operation Amplifier Single Pole

Qspice : Parent.Opamp-SinglePole (.ac).qsch | Parent.Opamp-SinglePole (.tran).qsch

- Test Example
 - Single Pole Opamp in .ac and .tran analysis



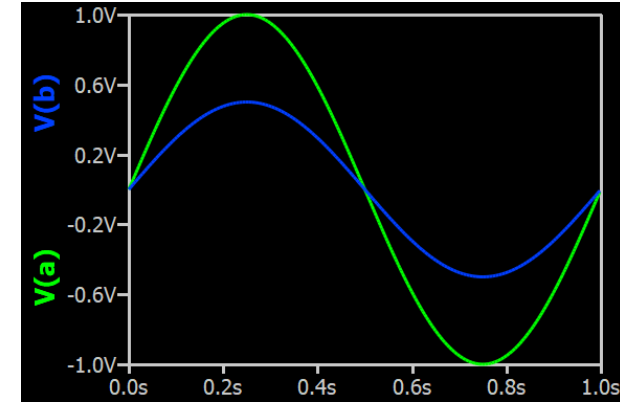
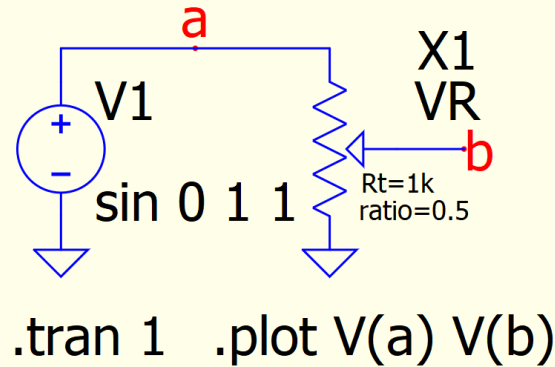
Potentiometer

Qspice : Potentiometer.qsym

- Potentiometer

- Symbol : Potentiometer.qsym
- Ratio is limited to [1m,0.999]
- Sub-circuit script

```
.subckt VR + - m params: Rt=1k ratio=0.5  
.param w = limit(1m,ratio,0.999)  
R1 + m (1-w)*Rt  
R2 m - (w)*Rt  
.ends VR
```



VCCS-Ilimit : Voltage Control Current Source with Current Limit

Qspice : VCCS-Ilimit1.qsym | VCCS-Ilimit2.qsym

- VCCS-Ilimit

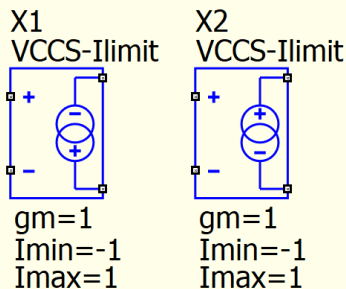
- Use Behavioral source with $\text{limit}(x,y,z)$ function

- Intermediate value of x , y , and z

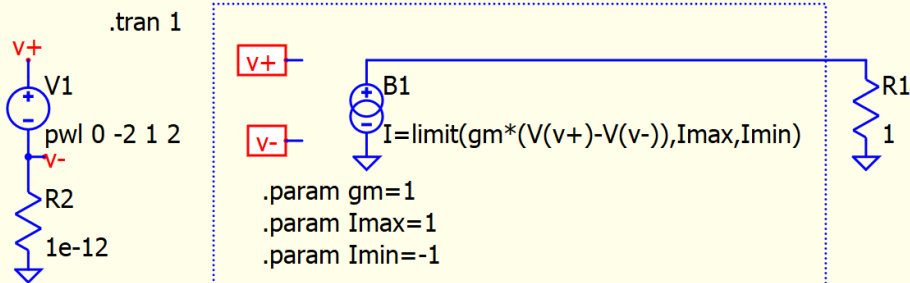
- Sub-circuit

```
.subckt VCCS-Ilimit v+ v- out+ out-  
B1 out- out+ I=limit(gm*(V(v+)-V(v-)),Imax,Imin)  
.ends VCCS-Ilimit
```

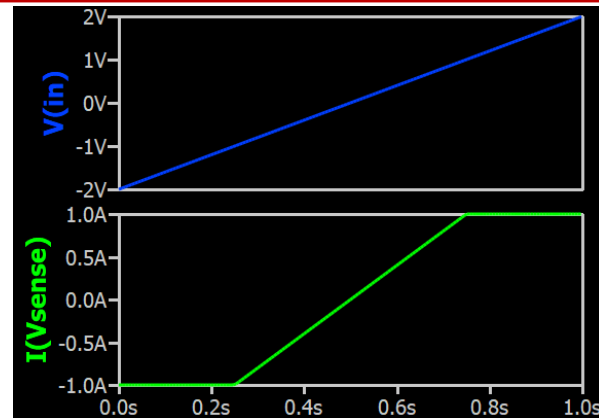
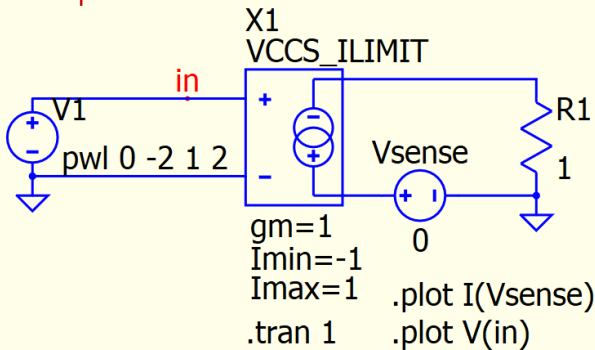
- Symbols



Idea of VVCS with Current Limit



Example



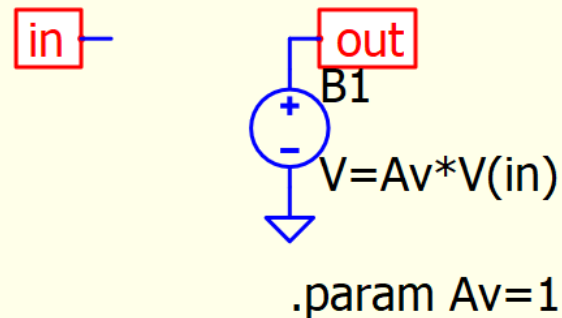
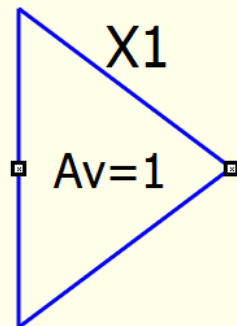
control

Gain and Signal-Limiter

Qspice : Gain.qsym | Signal-Limiter.qsym

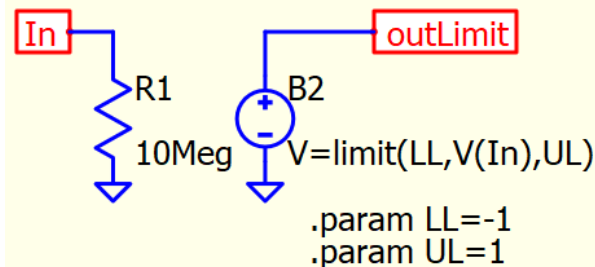
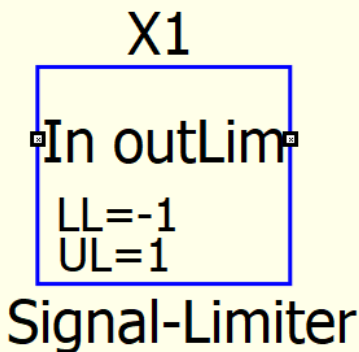
- Gain

- Gain.qsym
- $V_{out} = A_v \times V_{input}$



- Signal Limiter

- Signal-Limiter.qsym
- limit(x,y,z) | intermediate value of x, y, and z, equivalent to $\min(\max(x,y),z)$

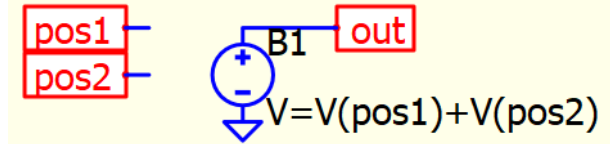
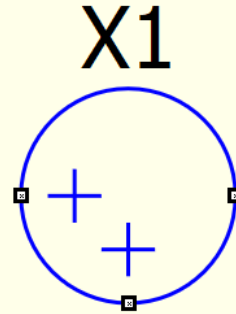


Sum and Difference

Qspice : Sum.qsym | Difference.qsym

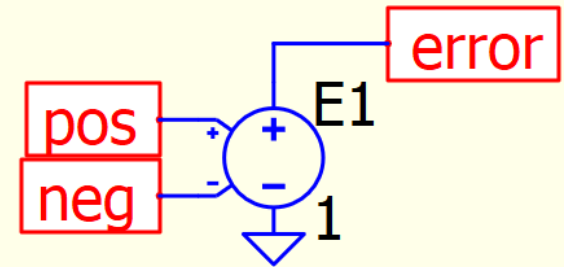
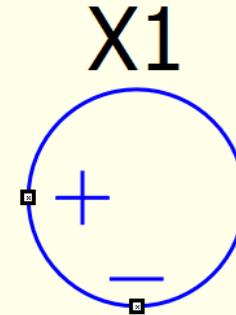
- Sum

- Sum.qsym
- $V_{out} = V_{+1} + V_{+2}$



- Difference

- Difference.qsym
- $V_{out} = V_{+} - V_{-}$



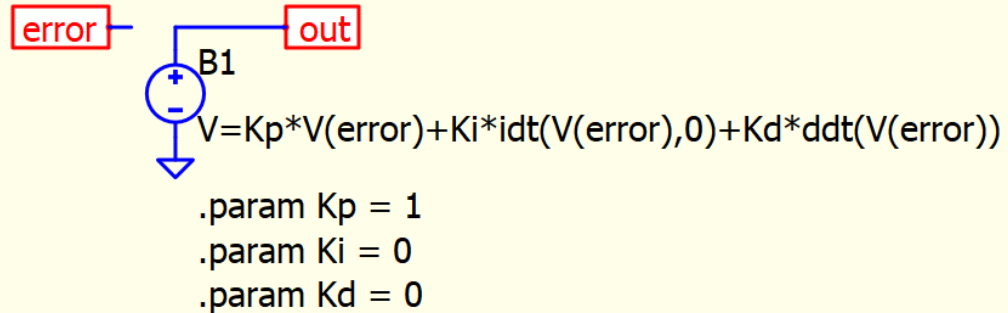
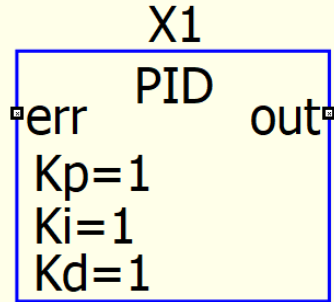
PID (Proportional-Integral-Derivative) Controller

Qspice : PID.qsym

- PID (Proportional-Integral-Derivative) Controller

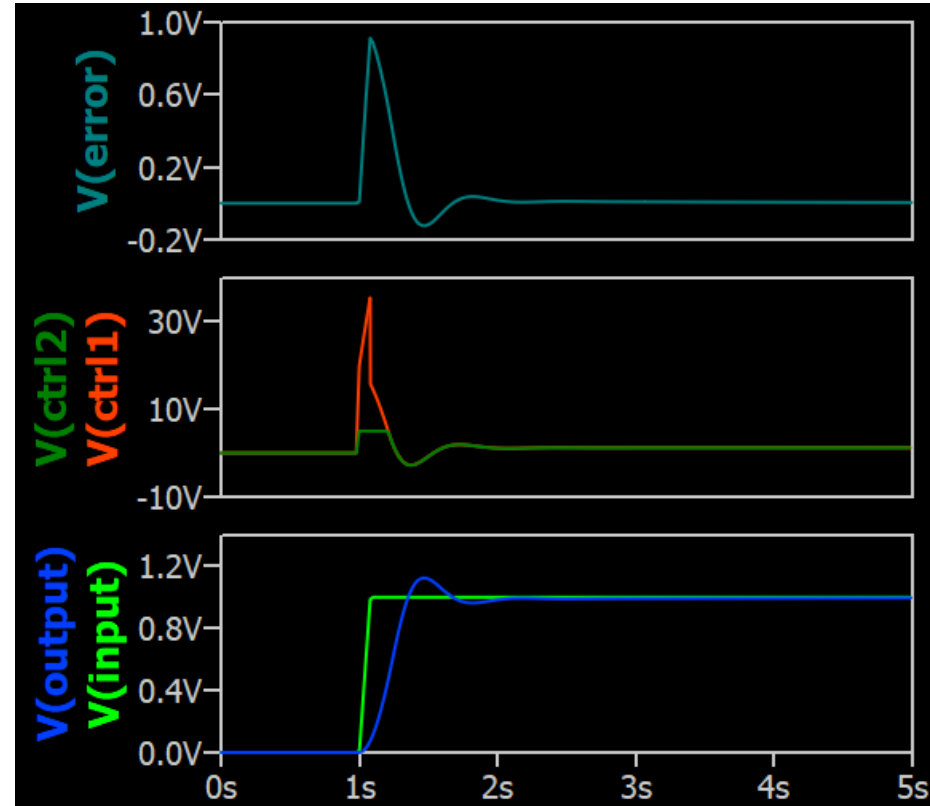
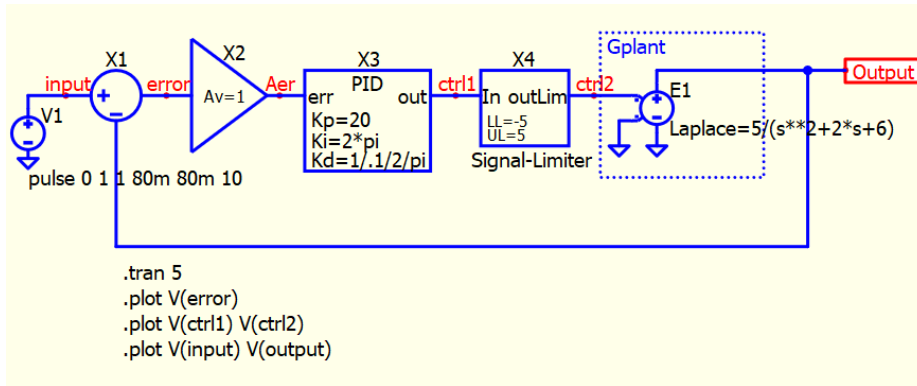
- PID.qsym

- $$V_{out} = K_p V_{error} + K_i \int V_{error} dt + K_d \frac{dV_{error}}{dt}$$



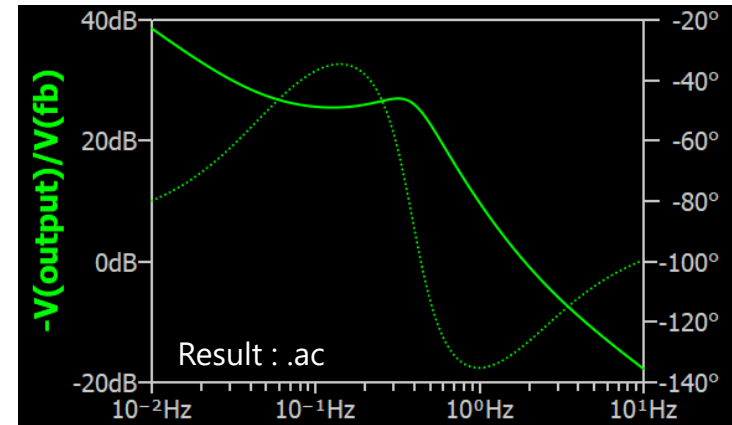
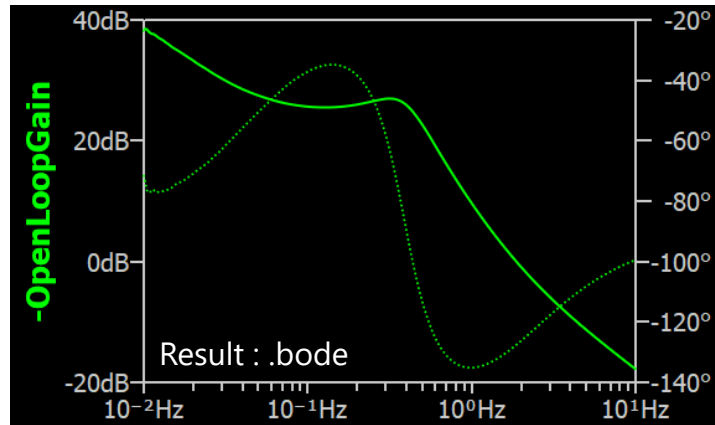
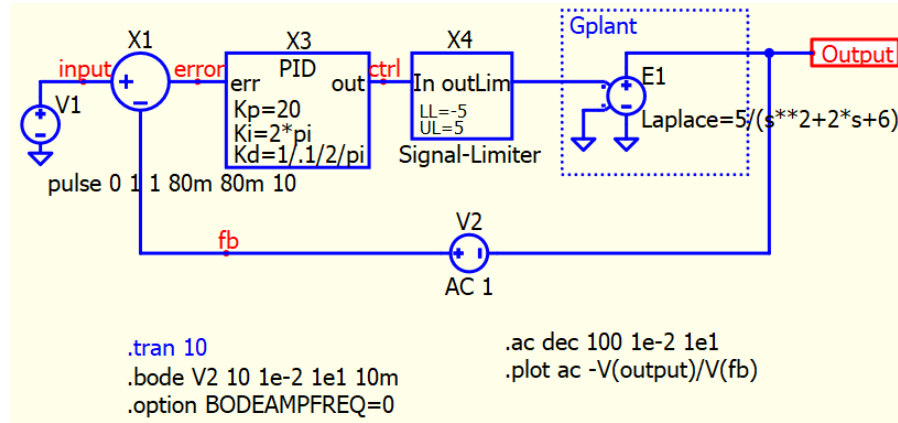
Control System Symbol : Transient Simulation Example

Qspice : CloseLoop Example with control symbol (.tran).qsch



Control System Symbol : AC and Bode Simulation Example

Qspice : CloseLoop Example with control symbol (.ac).qsch

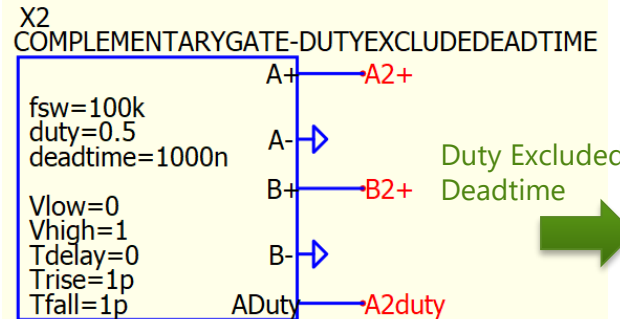
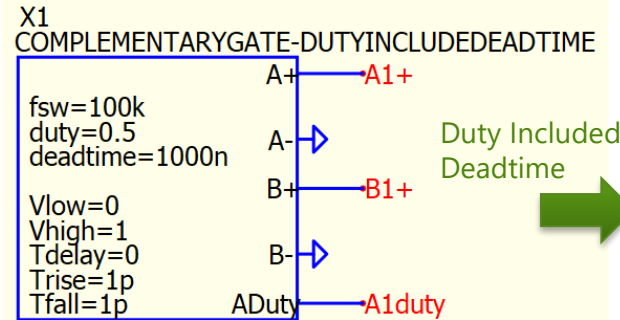


power electronics

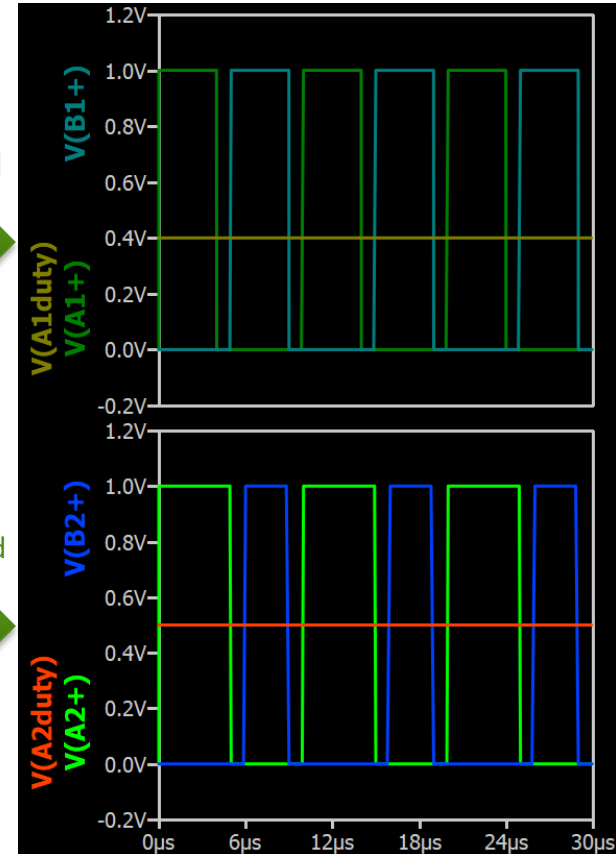
Complementary Gate Signal with Deadtime

Qspice : ComplementaryGate-DutyExcludeDeadtime.qsym | ComplementaryGate-DutyIncludeDeadtime.qsym

- Complementary Gate
 - To generate complementary gate signal (differential output) with deadtime
 - Symbol with duty to include or exclude deadtime
 - Include Deadtime, A+ ON time is $\frac{\text{duty}}{\text{period}} + \text{deadtime}$
 - Exclude Deadtime, A+ ON time is $\frac{\text{duty}}{\text{period}}$



```
.tran 3/100K  
.plot V(A2+) V(B2+) V(A2duty)  
.plot V(A1+) V(B1+) V(A1duty)
```



Complementary Gate Driver with Deadtime

Qspice : Gate-DeadTime.qsym

- Complementary Driver

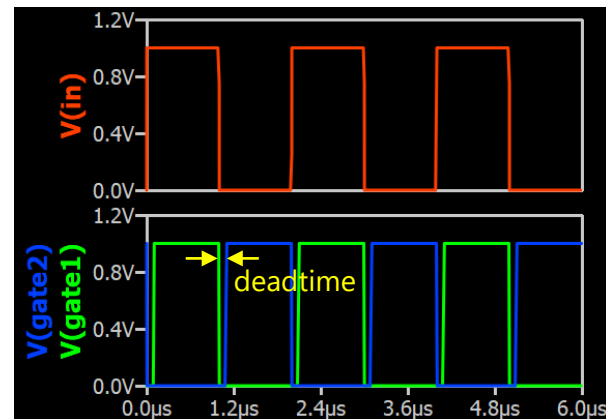
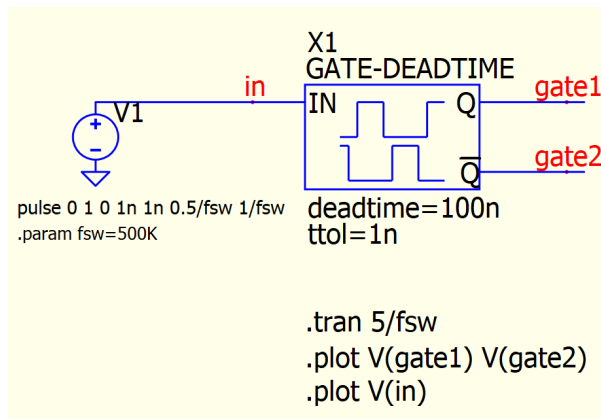
- Symbol

- Gate-DeadTime.qsym
 - Gate driver with complementary output signal separated by deadtime

- Input Parameters

- Deadtime : deadtime in second
 - TTOL : Temporal tolerance
 - (Invisible) Hi : Output High Level
 - (Invisible) Lo : Output Low Level

- ** beware that as deadtime is required, the ON duration of IN and Q will be different by the deadtime

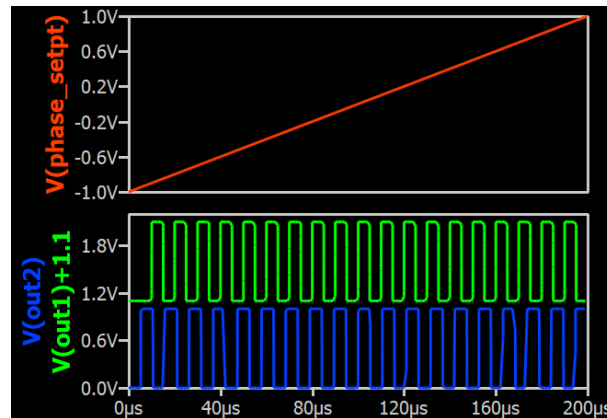
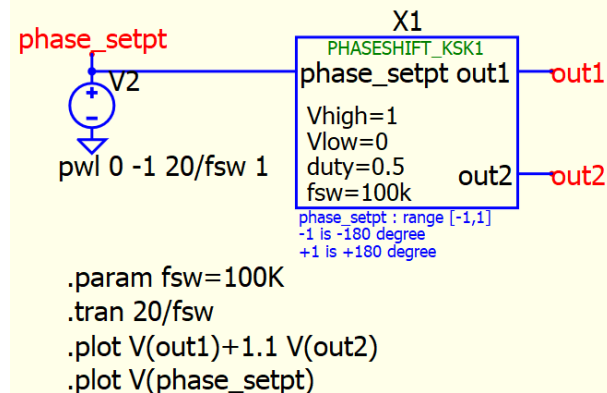
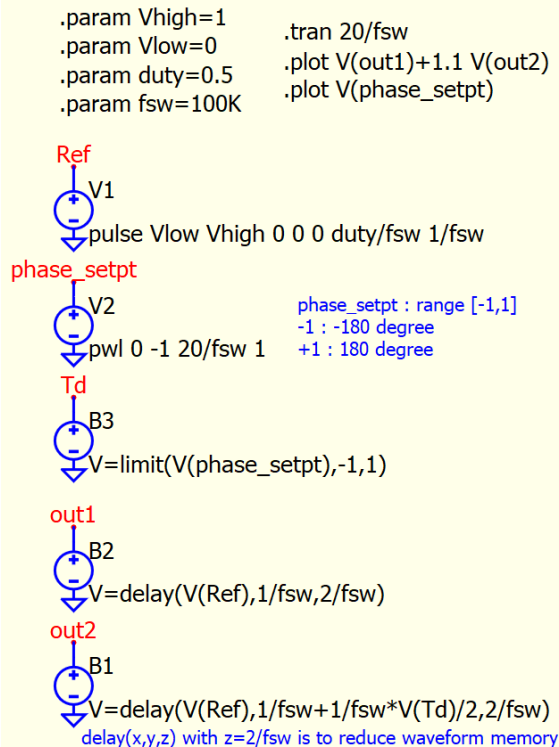


Phase Shift Pulse with Delay Control

Qspice : PhaseShift_KSK1.qsym

- PhaseShift_KSK1.qsym
 - Use behavioral source with delay function to generate phase controlled pulse source
 - User to define switching frequency and duty as input parameters (these cannot be change during simulation)
 - Phase_setpt is input port which control delay time in delay(), the delay is controlled with formula $\frac{v_{phase_setpt}}{2f_{sw}}$
 - A $\frac{1}{f_{sw}}$ is used to prevent negative y value into delay(x,y,z)
 - z set to $2f_{sw}$ to reduce waveform memory in simulation
- PhaseShift_KSK2.qsym
 - Same as above but with an extra pulsing source sync with delay to resolve missing pulse

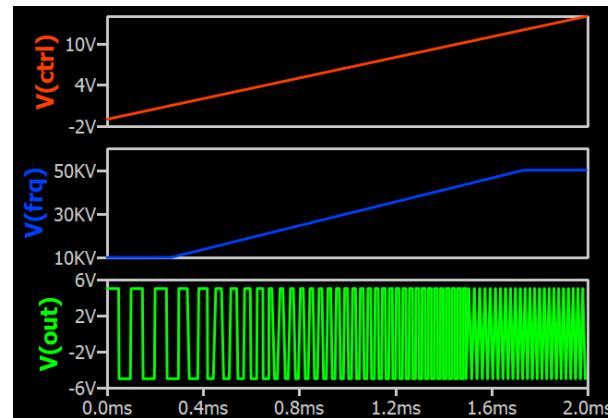
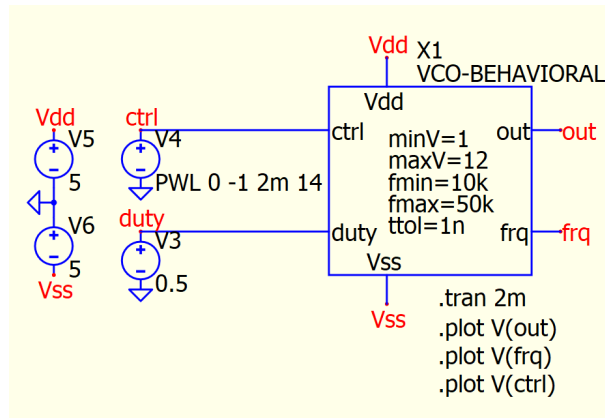
Ideal of PhaseShift_KSK1 subckt



Voltage Controlled Oscillator (VCO) Behavioral Model

Qspice : VCO-Behavioral.qsym

- Voltage Controlled Oscillator (VCO)
 - This is a behavioral model that generates a pulse-frequency controlled output signal linearly proportional to the input
- Pin Description
 - Ctrl : control voltage to output fmin at minV and fmax at maxV
 - Duty : duty ratio ranging from 0 to 1
 - Out : oscillator output with high/low levels determined by the external voltage relative to Vdd/Vss
 - Frq : frequency value represented in voltage



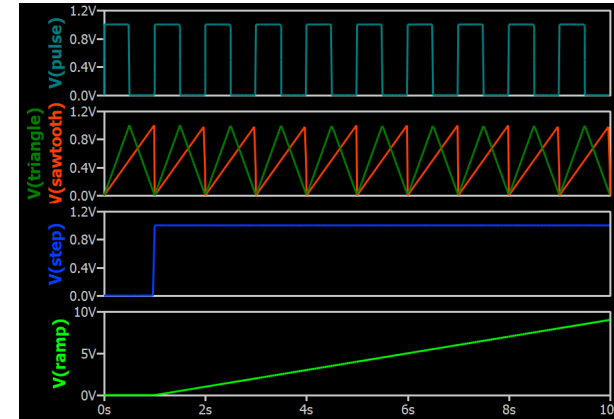
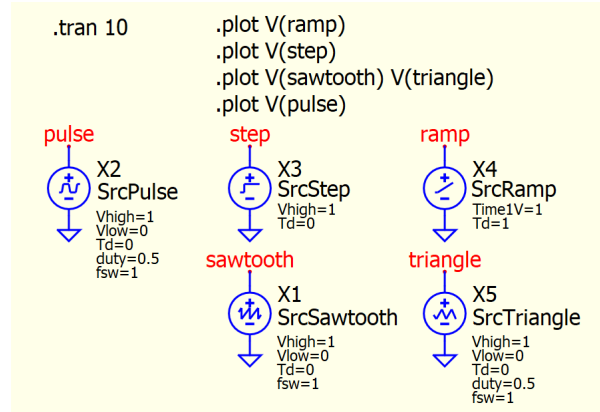
source

SrcXXX Special Voltage Source and Potentiometer

Qspice : Scrxxxx.qsym

- SrcXXX

- SrcPulse.qsym
- SrcSawtooth.qsym
- SrcTriangle.qsym
- SrcStep.qsym
- SrcRamp-Slew.qsym
- SrcRamp-Time1V.qsym



special