HW 2 Writeup

Computer Architecture

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1 Introduction

In this homework, I was asked to build the 2-bit decoder with enable, four input multiplexer and 1-bit full adder in structural Verilog. The code for realizing all three circuits are in the Github. This document will show the truth tables from test bench results and the waveforms that show the propagation delays.

2 2-bit decoder with enable

```
Structural Decoder Truth Table
En A0 A1| O0 O1 O2 O3 | Expected Output
0  0  0 |  0  0  0  0 | All false
0  1  0 |  0  0  0  0 | All false
0  0  1 |  0  0  0  0 | All false
0  1  1 |  0  0  0  0 | All false
1  0  0 |  1  0  0  0 | O0 Only
1  1  0 |  0  1  0  0 | O1 Only
1  0  1 |  0  0  1  0 | O2 Only
1  1  1 |  0  0  0  1 | O3 Only
```

Figure 1: Truth table for 2-bit decoder.

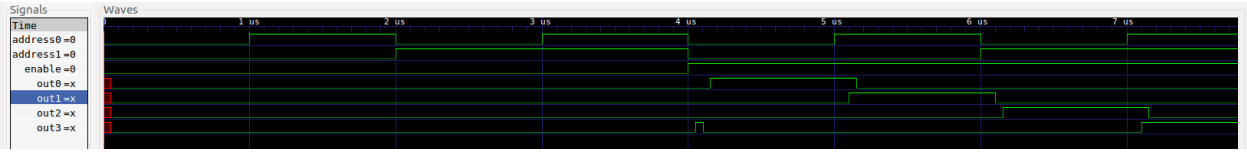

Figure 2: Wave form for 2-bit decoder.

3 Four input multiplexer

Structural Multiplexer Truth Table

I0	I1	I2	I3	Addr0	Addr1	Out	Expected Output
0	0	0	0	0	0	0	0 (Follows I0)
1	0	0	0	0	0	1	1 (Follows I0)
0	0	0	0	1	0	0	0 (Follows I1)
0	1	0	0	1	0	1	1 (Follows I1)
0	0	0	0	0	1	0	0 (Follows I2)
0	0	1	0	0	1	1	1 (Follows I2)
0	0	0	0	1	1	0	0 (Follows I3)
0	0	0	1	1	1	1	1 (Follows I3)

Figure 3: Truth table for 4 input multiplexer.

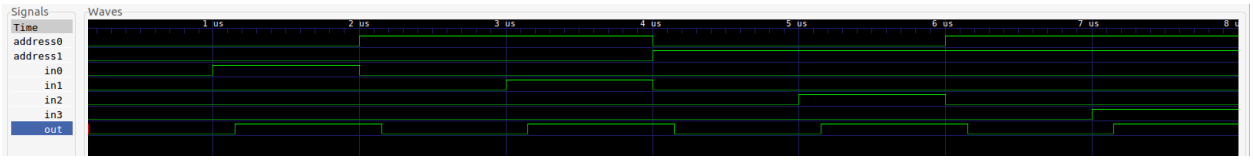

Figure 4: Wave form for 4 input multiplexer.

4 1-bit full adder

Structural Full Adder Truth Table

a	b	Cin	sum	Cout	Expected Output	
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	1	1	1

Figure 5: Truth table for 1-bit full adder.

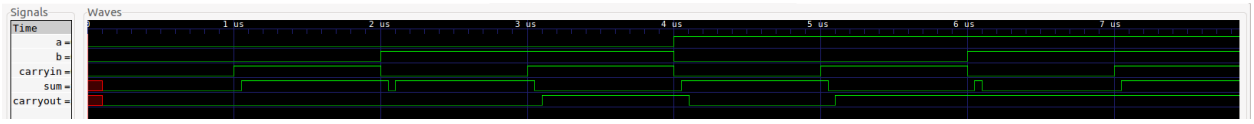

Figure 6: Wave form for 1-bit full adder.