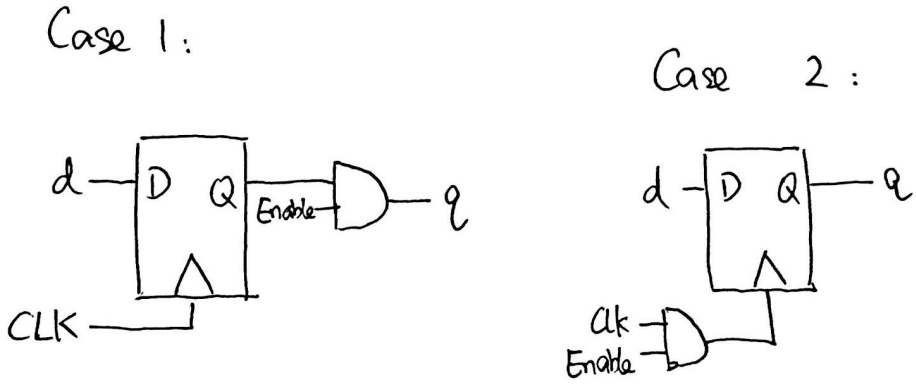
Computer Architecture HW6
Yichen Jiang

Deliverable 1:



This is the circuit diagram for the two presented register implementation.

Deliverable 6:

The << operator means bit shift to the left in verilog. First, one bit of the output will be 1 only when enable is 1. And that 1 will be bit shifted to the left by the number in the address to select the output channel. This will select the correct register file to write to and function as a decoder.