An Energy Efficient Fully Integrated OOK Transceiver SoC for Wireless Body Area Networks

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***Abstract*—This work presents a low-power high-speed system-on-chip (SoC) for wireless body area networks (WBANs). The SoC is fully integrated with a 10 Mb/s on-off keying (OOK) RF transceiver, digital processing units, an 8051 micro-controlled unit (MCU), a successive approximation (SAR) ADC, and etc. The receiver adopts envelop detector (ED) based structure to improve the energy efficiency. Conventional ED based structure has a poor sensitivity when reaching a bit rate of Mb/s level. To resolve the problem, we design a receiving (Rx) front-end with 77 dB gain at 10 Mb/s data rate, and propose a novel supply isolation scheme to avoid the instability induced by such a high gain. The transmitter is based on a 2 GHz digitally controlled oscillator (DCO), which uses bond wires as inductors to further reduce the power at transmitting (Tx) mode. The digital baseband is designed by a near-threshold design (NTD) method for low power consumption. The chip is implemented with 0.13 μm CMOS technology, measured results show that the receiver consumes 0.214 nJ/bit at -65 dBm sensitivity, and the Tx energy efficiency is 0.285 nJ/bit at an output power of -5.4 dBm. In addition, the digital baseband consumes 34.8 pJ/bit with its supply voltage lowered to 0.55 V, indicating its energy per bit is reduced to nearly 1/4 of the super-threshold operation.**

I. Introduction

Wireless body area network (WBAN) will play an important role in future healthcare. Several types of applications require high data rate such as retina implants, capsule endoscopy, and neural recording systems. For such applications, wireless transceiver consumes significant power. Thus, it is crucial to improve power efficiency of wireless transceiver in WBAN applications. Considering the short communication distance used in WBAN, simple modulation schemes such as binary frequency shift keying (BFSK), binary phase shift keying (BPSK), and on-off keying (OOK) are widely adopted [1]–[4].

Among different modulation schemes, OOK transceiver has shown a high data rate at Mb/s level by using simple modulation-demodulation circuits. For example, OOK transceiver with down-conversion receiving (Rx) front-end was reported in [1] which attained a data rate of 2 Mb/s. However, down conversion usually needs power-hungry modules, such as high-performance mixers and a frequency synthesizer. This was evidenced by the energy efficiency of 1.7 nJ/bit at Rx and 1.55 nJ/bit at transmitting (Tx) in [1]. Envelope detector (ED) based OOK receiver has shown a better Rx energy efficiency, e.g. 0.5 nJ/bit in [2] and 0.295 nJ/bit in [3], respectively. However, ED based approach usually leads to poor Rx sensitivities, e.g. -37 dBm in [2] and -45 dBm in [3], which result in a limited communication distance. In addition, data rates in those designs [1]–[3] are limited to less than 2 Mb/s, which is not adequate for some WBAN applications such as endoscope capsule and neural recording system. A 5 Mb/s super-regenerative OOK transceiver was reported in [4], which boosted energy efficiency to 0.363 nJ/bit. The high efficiency, however, was at the cost of several off-chip components. This increases the device size, which is not favored in implants.

In this work, we implemented a fully integrated OOK transceiver system-on-chip (SoC) in 0.13 μm CMOS technology. To improve the sensitivity of conventional ED based receivers as well as power efficiency, we boost the gain of Rx front-end by a single-end inverter-based design while keeping power in check. The high-gain induced instability is addressed by a low-power supply isolation scheme. For the transmitter, a bond-wire digitally controlled oscillator (DCO) is implemented for low-power carrier generation. For the digital baseband, we lowered its power consumption by near-threshold design (NTD) technique. Therefore, the energy efficiency of the SoC is significantly improved.

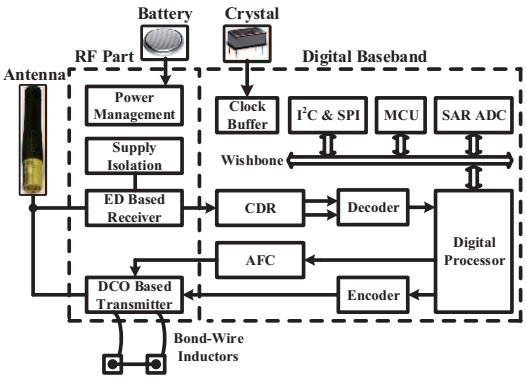

Fig. 1. System architecture.

II. System Architecture

The SoC architecture is shown in Fig. 1, assisted by an antenna, a 1.5 V button battery, a crystal, and bond-wire inductors. There are two main blocks in the SoC, i.e. RF part and digital baseband. The RF transceiver contains an ED based receiver and a DCO based transmitter, whereas a novel low-power supply isolation scheme is proposed for

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the receiver. The blocks of digital baseband include clock-data recovery (CDR), automatic frequency calibration (AFC), MCU, encoder, decoder, and etc. The AFC module is used to calibrate the frequency deviations induced by the bond-wire inductors of transmitter. The digital submodules exchange data by a wishbone bus, and I^2C and SPI bus are also supported. A 10 bit successive approximation (SAR) ADC with 50 KS/s sampling rate is also adopted here as an interface for sensor.

III. Transceiver Design

The block diagram of proposed OOK transceiver is presented in Fig. 2. The receiver consists of a low-noise amplifier (LNA), a cascaded amplifier (CA) for gain enhancement, and several other blocks for demodulation, i.e. ED, baseband amplifier (BA), and comparator. The use of CA is mainly for the sensitivity improvement. To achieve a sensitivity of -60 dBm to -70 dBm while taking into consideration of at least 100 mV input for the ED, the front-end must provide gains in the range of 60 dB to 70 dB. LNA itself is not sufficient for such a large gain, so an inverter-based structure is adopted for CA to achieve a high gain. .

The transmitter contains a DCO and a power amplifier (PA), where baseband data are used to directly control the power switch of the two modules for lowering the average power at Tx mode. The DCO frequency deviations induced by bond-wire inductors are calibrated by digital baseband.

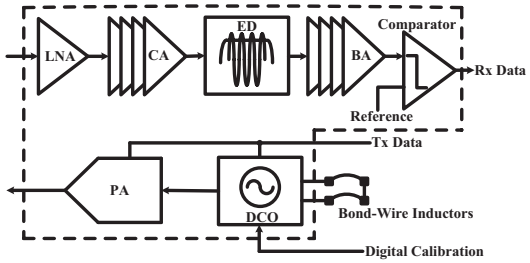

Fig. 2. Transceiver architecture.

A. Power Isolation Scheme for Receiver

The overall gain for LNA and CA is set to 70 dB. To balance noise figure and power, the LNA is designed with current-reused common-gate typology [5] for 10 dB gain. The rest of gain is provided by the CA, which was set to 67 dB by taking into consideration of process variations. One of issues in design high gain inverter-based CA is stability, especially under low-power condition where all inverters are single-end without bias current. As a result, every two stages form a closed loop with a forward path for RF signal and a backward path for power line, as shown in Fig. 3. Instability may appear if the gain of each loop is higher than 0 dB. Fig. 4 shows the close-loop gains versus frequencies at different forward gains (FGs). It can be seen that the loop gain is raised to 0 dB level when the forward gain becomes higher than 66 dB. In our design, the Rx front-end gain is set to 77 dB which will lead to unstable state at the output of Rx front-end.

To maintain the stability while achieving 77 dB of gain, we proposed a new supply isolation scheme. Different from

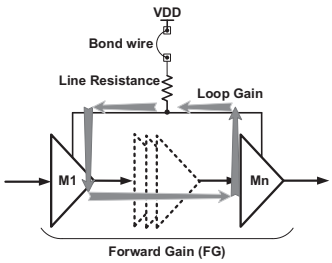

Fig. 3. Close loop between each two stages.

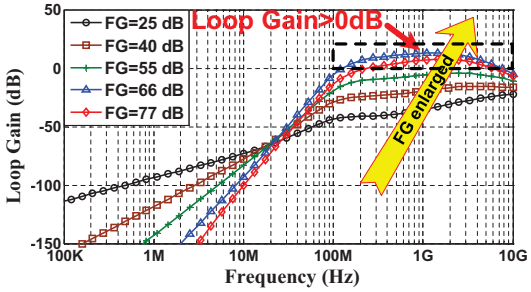

Fig. 4. Close-loop gains at different FGs.

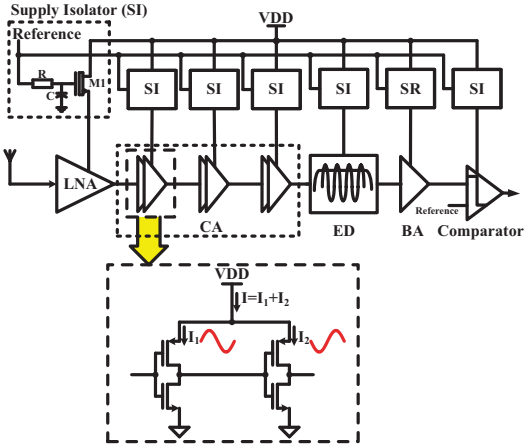

Fig. 5. Proposed low-power supply isolation scheme.

traditional stable power management schemes that utilize complex regulators to minimize the supply interactions among sub-modules [6], we propose a power management scheme based on simple supply isolators (SIs), as shown in Fig. 5, where every sub-module is protected by a SI, except the BA. The SI consists of R, C and M1 as shown in dotted box in Fig. 5. The corner frequency of RC is set to 2.5 MHz.

The supply current of LNA changes little since it processes small signals. For the inverter-based CA, two adjacent inverters are attached to one SI; so overall supply current of these two stages has small fluctuations because the currents of these two inverters are complementary to each other, as show in the dashed box of Fig. 5. The ED is a victim of supply noise due to its low current of 30 μA, so it is protected by the SI. BA is the most significant supply-noise aggressor for two reasons: First, its signal amplitude and power consumption are relatively large; second, the BA is used to amplify the low-frequency signals at analog baseband, generating low-frequency supply noise which is not easy to remove by the SI. Therefore, a dedicated shunt regulator [7] is introduced to

block its supply noise.

With newly introduced power isolation scheme, the close-loop gain is kept far below 0 dB while the forward gain attains 77 dB as illustrated in Fig. 6, so the receiver maintains its stability under such a high gain.

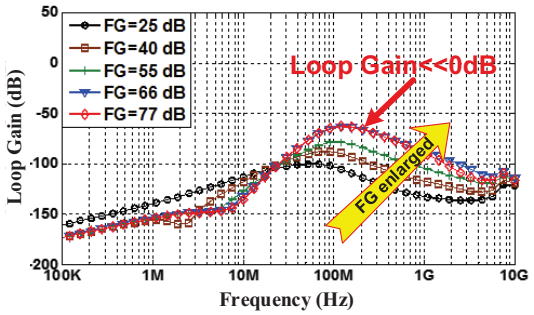

Fig. 6. Close-loop gains under the proposed supply isolation scheme.

The current consumption of LNA, CA, ED, and BA are 430 μA, 700 μA, 30 μA, and 140 μA, respectively. As a result, the overall power of receiver can be less than 1.43 mA.

B. Bond-Wire Transmitter

The OOK transmitter contains a bond-wire DCO and a PA, as shown in Fig. 7. The Tx data modulates the transmitter by switching the supply power of all blocks. The maximum RF power is -5.4 dBm.

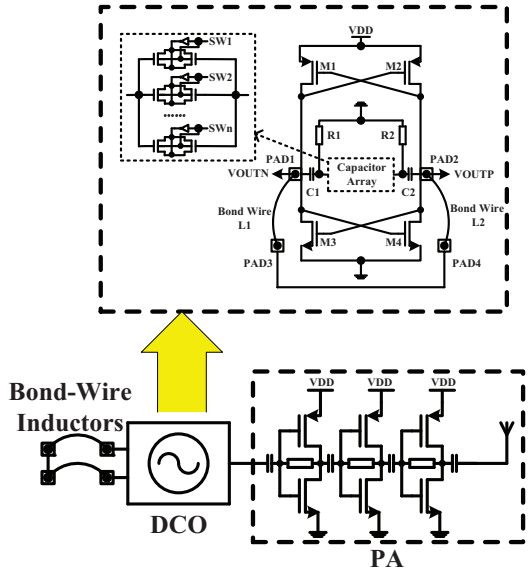

Fig. 7. Transmitter architecture.

The DCO uses bond wires as inductors. The DCO circuit is shown in Fig. 7, where two on-die pads are connected to the differential output port, whereas another two are the bond pads for packaging. A digitally controlled MOS capacitor array is used to calibrate the frequency deviations caused by the bond wires. The AFC is realized by the digital baseband.

Bond-wire DCO helps reduce the power due to high Q-factor of bond wires. As the Tx/Rx data rate is 10 Mb/s, the phase noise at 10 MHz offset decide the error vector magnitude (EVM) of transmitter. For the same DCO, and we compare its phase noise in case of on-chip inductors and bond-wire inductors in Fig. 8, indicating that our proposed bond-wire technique improves phase noise by 6 dB@10 MHz. Therefore, the power can be reduced by 50% since the oscillator phase noise is inversely proportional to the square of current consumption [8].

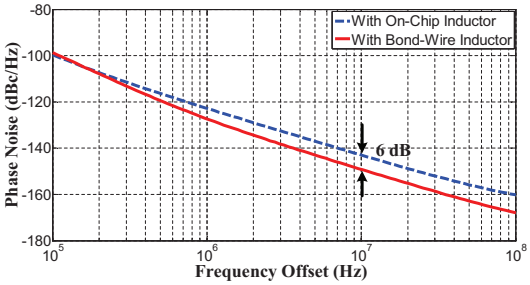

Fig. 8. Bond-wire induced noise improvement of DCO.

IV. Digital Baseband

The power reduction of digital baseband is realized by NTD. Compatible with the OOK RF specifications, and the digital baseband contains direct sequence spectrum spread (DSSS) and packet processing units. To address process, voltage and temperature (PVT) issues in NTD, we filtered out some standard cells with minimal size or multi-stack transistors that are vulnerable to PVT variations. Therefore, the digital part can work robustly under an ultra-low supply voltage such as 0.4 V, supporting a low-speed mode with 30 μW power consumption.

V. Measured Results

The SoC is fabricated with 0.13 μm CMOS technology. The chip core can operate from a 1.5 V button battery, and the die area is about 3.4 mm×2.5 mm, including the testing buffer and IO pads. The die photo is shown in Fig. 9, which contains the LNA, CA, BA, ED, DCO, PA, digital baseband, and etc.

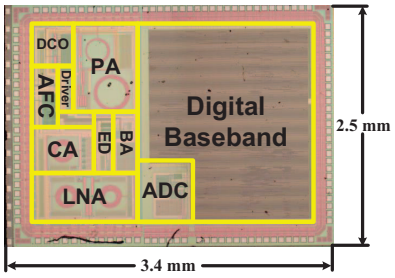

Fig. 9. Die photo.

For 0.1% BER, the receiver achieves a sensitivity of -65 dBm at a data rate of 10 Mb/s. The transient waveform is shown in Fig. 10, where the input RF signal is a -65 dBm carrier modulated by a 10 Mb/s random Tx signal. Note that the demodulated data is inverted with reference to Tx signal, so the Rx data are consistent with the Tx data in Fig. 10. The average power of receiver is 2.14 mW, which results in an energy efficiency of 0.214 nJ/bit.

The Tx output signal is shown in Fig. 11. The amplitude is about 170 mV and the settling time is less than 20 ns,

TABLE I
PERFORMANCE COMPARISON.

	Common				Rx			Tx		
	Type	Process	Carrier	Data Rate	Sensitivity	Power	nJ/bit	Output	Power	nJ/bit
JSSC'07 [2]	Only RF	180 nm	916.5 MHz	1 Mb/s	-37 dBm	0.5 mW	0.5	-2.2 dBm	3.8 mW	3.8
ESSCIRC'11 [1]	Only RF	180 nm	425 MHz	2 Mb/s	-80.2 dBm	3.4 mW	1.7	-2.17 dBm	3.1 mW	1.55
BioCAS'11 [3]	Only RF	180 nm	406 MHz	2 Mb/s	-45 dBm	0.59 mW	0.295	-17 dBm	0.84 mW	0.42
ISSCC'11 [4]	SoC	90 nm	2.4 GHz	5 Mb/s	-75 dBm	1.815 mW	0.363	0 dBm	3.68 mW	0.736
This Work	SoC	130 nm	2 GHz	10 Mb/s	-65 dBm	2.14 mW	0.214	-5.4 dBm	2.85 mW	0.285

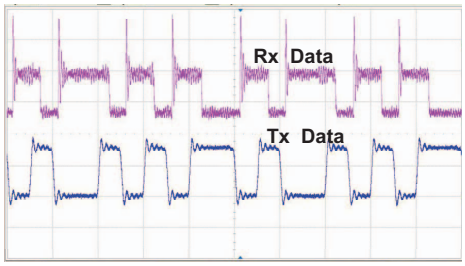

Fig. 10. Waveforms of Tx and Rx data.

indicating that the output power is -5.4 dBm and the maximum Tx data rate reaches 100 Mb/s. At 10 Mb/s data rate, the power consumption of transmitter is 2.85 mW, resulting the Tx energy efficiency of 0.285 nJ/bit@10 Mb/s.

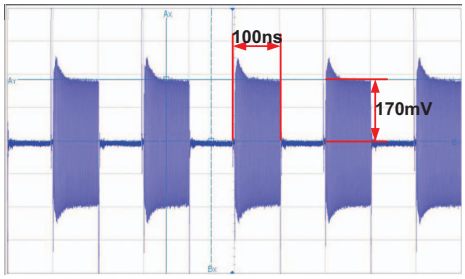

Fig. 11. Tx output signal.

The power performance of NTD digital part is also measured. The maximum working frequency and power consumption are plotted in Fig. 12. The energy efficiency is 130 pJ/bit under normal 1.2 V supply voltage, whereas the maximal energy efficiency reaches 34.8 pJ/bit at 0.55 V. In addition, the digital baseband supports a low-speed mode, when the power consumption can be reduced to 30 μW by lowering the operating voltage to 0.4 V.

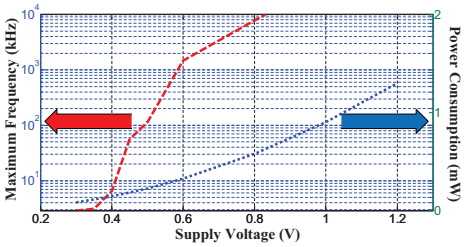

Fig. 12. Power consumption of digital baseband.

The key specifications of the SoC are summarized in Table I, and compared with some typical OOK chips in recent years. Our transceiver consumes the lowest energy per bit at both Rx and Tx states. In addition, our chip is implemented without additional off-chip components.

VI. Conclusion

In this work, we have presented the implementation of an energy efficient 10 Mb/s OOK transceiver SoC for WBAN applications. The problem of poor sensitivity of conventional ED based OOK receiver is resolved by a novel supply isolation scheme, whereas the low power advantage of ED based structure is maintained, i.e. 0.214 nJ/bit at Rx mode. By using bond wires as DCO inductors, the energy efficiency of transmitter is reduced to 0.285 nJ/bit at output power of -5.4 dBm. The energy per bit of digital baseband has been improved to nearly 1/4 when compared to the super-threshold operation.

VII. Acknowledgments

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