Using Nonvolatile Processors to Reduce Leakage in Power Management Approaches

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***Abstract*—Over the last few years, static energy(mainly induced by leakage current) has dominated a large portion of total energy consumption in chips. Although power management approaches have been used to reduce active power, they are ineffective in reducing static power when applied in normal volatile processors. In this paper, we explored the usage of nonvolatile processors(NVPs), which are able to maintain states during power failures, to reduce leakage power in power management approaches. We evaluated several existing power management strategies and experimental results show that using NVPs in the leakage-aware power management is able to save 15% extra energy and achieve 30% more static energy savings compared with volatile processors.**

I. Introduction

High leakage current is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced [1]. It leads to substantial growth of static power consumption in modern processors. According to the prediction from International Technology Roadmap for Semiconductors(ITRS) [2], static power consumption in the consumer or portable devices will increase by 4 times in the later 12 years. Therefore, reduction techniques for static power are drawing more and more attentions.

Plenty of power management(PM) approaches have been proposed to reduce energy consumptions. For instance, *Dynamic power management(DPM)* puts processors into low power modes during idle periods. However, conventional volatile processors can not be totally shut down to remain data, hence leakage current always exists. *Dynamic voltage scaling(DVS)* and *critical speed strategy(CSS)* varies the speed of processors to reduce dynamic power, but the prolonged operating time may even increase the leakage energy. In [3], a scheduling scheme named *FPTW(Fixed Priority Threshold Work-Demand)* leverages DVS and CCS for energy savings. However, they do not consider leakage power.

The increasing demand of low static power consumption leads to the invention of nonvolatile processors(NVPs). Compared with the volatile ones, NVPs are fabricated with nonvolatile registers. A typical architecture of NVPs is presented in reference [4]. It is fabricated with ferroelectric flip-flops which can backup data in parallel before power failures. NVPs have several advantages compared with normal volatile processors, such as zero-standby power, instant on and off and high resilience to power failures. Due to the above characteristics, NVPs have the potentials to mitigate the static power problem.

In this paper, we focus on using NVPs in power management approaches and optimize the PM strategies regarding to high static power. We evaluated several power management approaches and showed that NVPs consume less static power than volatile processors. Furthermore, we added leakage optimization in *CSS* models to achieve the highest energy savings for NVPs.

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II. Power management for NVPs

A. Problem model

The power consumption for a volatile processor can be represented as follows [5] :

$$P(f) = P_{\text{sta}} + \hbar(P_{\text{ind}} + P_{\text{d}}) = P_{\text{sta}} + \hbar(P_{\text{ind}} + C_{\text{ef}} f^{\gamma}) \quad (1)$$

where $P_{\text{sta}}, P_{\text{ind}}$ and P_{d} are static power, speed-independent active power and speed-dependent active power. C_{ef} and γ refer to the switch capacitance and the dynamic power related constant. $\hbar$ is set to 1 or 0 when the processor is in active or sleep modes. Note that the static power dissipation always exists in either mode because the power supply cannot be totally shut down to maintain data.

The power equation for NVPs is as follows:

$$P(f) = \hbar(P_{\text{sta}} + P_{\text{ind}} + P_{\text{d}}) = \hbar(P_{\text{sta}} + P_{\text{ind}} + C_{\text{ef}} f^{\gamma}) \quad (2)$$

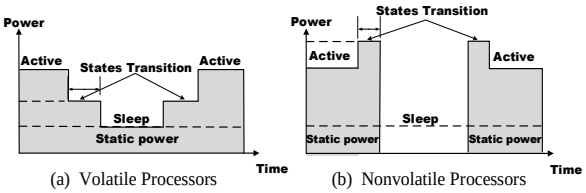
$\hbar$ is moved to the left side of the equation because NVPs can be totally shut down in the sleep mode.

The job set on processors is given as $\jmath = \{J_1, J_2, ...J_N\}$ and $J_i = (r_i, w_i, d_i)$, where r_i, w_i and d_i are arrival time, the worst case execution time under the highest frequency and job deadline.

B. Leakage-Aware FPTW(LA-FPTW)

Given a job $J = \{r, w, d\}$ by a *critical frequency strategy(CFS)* scheduler, a processor runs at the critical frequency and transfers into a sleep mode after job completed. However, this approach is sometimes less efficient than *DVS* method. The *FPTW* strategy [3] switches between *DVS* and *CFS* in real time and saves more energy than either *CFS* or *DVS* approach. However, *FPTW* ignored static power in its critical frequency's calculation, which is inaccurate when static

power is high. We proposed a method to compute the critical frequency where the static power is considered. f_{crit} is the optimal operating frequency at which a processor can be more energy efficient. It can be calculated by the following equation: $f_{cirt} = \sqrt[\gamma]{\frac{P_{ind}+P_{sta}}{C_{ef}(\gamma-1)}}$. The processor will run at f_{crit} and move into the sleep state when job completed. Under this scheduling method, Figure 1 demonstrates the difference between NVPs and volatile processors by comparing their detailed power profiles. NVPs need higher transition power for data backup/restoration due to the parallel operations, however they can achieve much shorter backup/restore time and zero standby power.



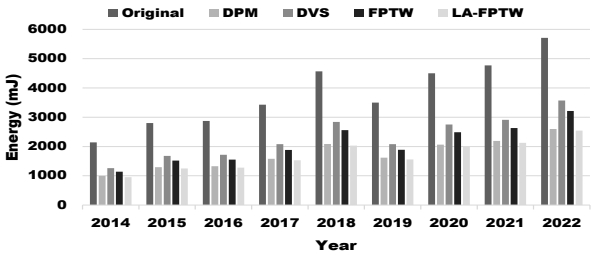
(a) Volatile Processors (b) Nonvolatile Processors

Fig. 1. Power profile after using LA-FPTW

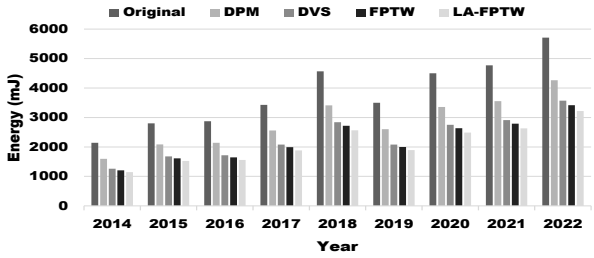
III. Evaluation

To compare the power management effects with NVPs or volatile processors, we use the measured parameters from THU1010N(a nonvolatile processor [4]) and MSP430(an industrial volatile processor [6]). To evaluate the power management effects under future technology nodes, we adopt ITRS data which predicts both of active power and static power are increasing and the ratio of static power varies from 0.33 to 0.51. The arrival time of jobs follows a Poisson distribution. The average arrival time r is 10ms and the average worst case execution time is 3ms. We set the arrival time of the next job to be the deadline of the previous job, which means $d_i = r_{i+1}$. Under above configurations, we compare the power metrics of NVPs and volatile processors under *DPM*, *DVS*, *FPTW* and proposed *LA-FPTW*.

In Figure 2(a) and Figure 2(b), we can find that the total energy consumption of NVPs is always less than that of volatile processors under *DPM*, *FPTW* and *LA-FPTW*. It is because NVPs consume less energy in the sleep mode. *FPTW* can not achieve the optimal energy savings because of the inaccurate f_{crit}. The proposed *LA-FPTW* achieves the maximum energy reductions. Furthermore, *DPM* only induces 4% more power consumption compared with the ideal *LA-FPTW* approach in the evaluations. Therefore, it implies that *DPM* can be promising in NVPs because it does not need multi-voltage & frequency inputs. Figure 3 demonstrates that NVPs can reduce static power consumption in *DPM*, *FPTW* and *LA-FPTW* significantly. Although dynamic energy consumption may increase(in *FPTW* and *LA-FPTW*), total energy consumption is reduced. Considering the most energy-efficient approach *LA-FPTW*, using NVPs can save 15% extra energy and achieve 30% more static energy savings compared with volatile processors.



(a) Power trend of THU-1010N(NVPs)



(b) Power trend of MSP430(VPs)

Fig. 2. Energy consumption of NVPs and VPs under different power management approaches

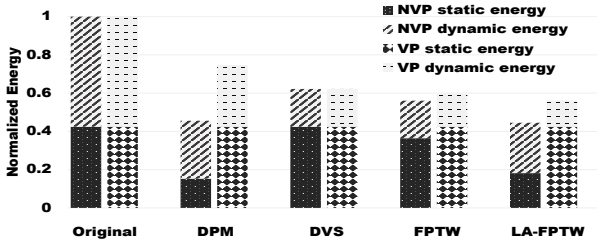


Fig. 3. Power comparison between NVPs and VPs under different power management approaches(Assume static power is half of dynamic power)

IV. Conclusion

This paper explores the superiority of using NVPs in power management approaches. In order to reduce the energy consumption, we proposed a *Leakage-aware FPTW* approach considering the static power in future technology nodes. Experimental results illustrate that the *LA-FPTW* approach can achieve the best static energy savings using NVPs. It implies that NVPs will be more widely used with the increasing of static power consumption in future CMOS technology.

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