A Compare-and-write Ferroelectric Nonvolatile Flip-Flop for Energy-Harvesting Applications

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***Abstract*—In this paper, a novel compare-and-write ferroelectric nonvolatile flip-flop is developed, which can be used in the checkpoint processor for energy-harvesting applications. It can make the processor nonvolatile, secure and instant recoverable from power failures. The behavior model of ferroelectric capacitor is set up to characterize its electrical property. An improved architecture of ferroelectric capacitor based flip-flop is proposed in which a compare-and-write block is used to decide if the state of ferroelectric capacitor should be changed. Thus, the presented architecture can prolong the lifetime of the ferroelectric capacitor by removing the unnecessary programming cycles. The design is implemented in HJTM 0.18um CMOS process and simulation results show that the proposed ferroelectric nonvolatile flip-flop operates properly and reduces 40-80% programming cycles, which increases the lifetime of the ferroelectric capacitors effectively and expands its application in checkpoint processors for energy-harvesting area.**

I. INTRODUCTION

Recent advances in SoC demand much faster and larger nonvolatile memories, not only for stand-alone storage, but also for alternatives of on-chip SRAM [1]. Ferroelectric random access memory (FeRAM) is a low-cost nonvolatile memory technology fabricated with two additional masks to a standard CMOS technology [2], which has been widely used in low-cost and low-power applications, such as smart cards, power meters, printers and RF tags [3]. However, the fatigue of the ferroelectric materials restricts the program cycles (polarization change) of each cell.

Energy-harvesting is a technology which is important for green circuits and systems. There are many works in this area recently [4, 5]. Because the power is unstable in the energy-harvesting system, the frequent power failure is a problem. Therefore, the technique of checkpoint processors can be used for avoiding the effect of power failure [6]. Furthermore, using nonvolatile memory and logic, such as ferroelectric material, is helpful for these systems to instantly recover from power failure.

However, the application of ferroelectric material is restricted because of its limit lifetime. There are plenty of works focus on extending the lifetime of ferroelectric materials under repeated programming. All the works fall into the following two categories. The first category is to develop novel materials to sustain more polarization changes [7, 8], while the other is to exploit the characteristic of application to reduce the programming cycles. This paper belongs to the latter aspect.

Although previously presented FeRAM based NV-SRAM enables unlimited read cycles [9, 10], its program cycles are still restricted by the worn-out. Masui et al. proposed a circuit mechanism to program the ferroelectric capacitance only when the power down happens. However, as the fine-grained power management or frequent state backups are adopted, plenty of power downs or state backups in ferroelectric capacitance will be observed, which poses great challenges for the lifetime of ferroelectric materials. Accordingly, this paper proposed a novel circuit mechanism to reduce the unnecessary programming cycles of FeRAM by exploiting the fact that the memory cell should only be programmed when its present state is different from the next state.

Our contribution of this paper is listed as followings: in Section II, a behavior model for ferroelectric capacitance is developed to characterize its electrical property in both power on and off modes. After that, a ferroelectric capacitance based flip-flop is presented. This flip-flop can be adopted in checkpoint processors for energy-harvesting applications. And in order to remove the unnecessary programming cycles in frequent power down and state backup operations, we have inserted a state comparing module and presented an improved architecture of ferroelectric capacitance based flip-flop in Section III. Experimental results which shown in Section IV validate the functionality of the proposed design and show most unnecessary programming cycles are avoided by the compare-and-write module.

II. FERROELECTRIC FLIP-FLOP

A. *Ferroelectric Capacitance Model*

Ferroelectric capacitor based flip-flop (FC-FF) can be built based on ferroelectric materials, which are distinguished from other dielectric materials by the polarization-voltage (P-V) hysteresis loop [11]. Therefore, it is very essential for a

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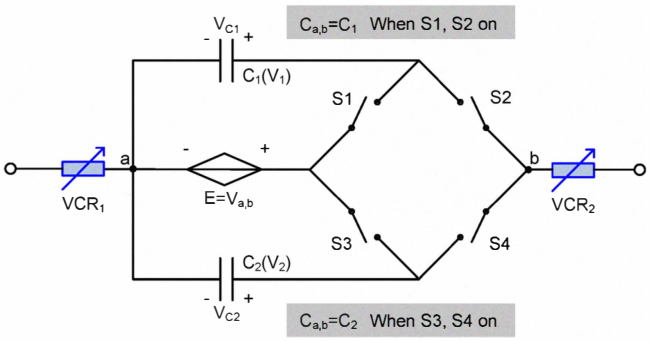


Figure 1. Ferroelectric capacitance SPICE model

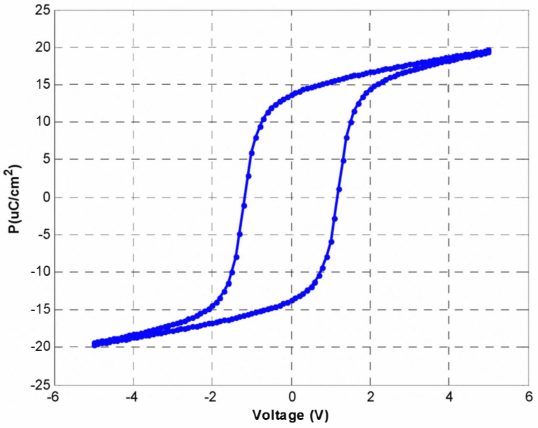


Figure 2. Simulation result of P-V hysteresis loop

ferroelectric capacitor model to describe the P-V hysteresis loops accurately for the simulation of FC-FF circuit. There are some different models for ferroelectric capacitors, such as zero-switching-time macromodeling [12, 13]. Howerver, this approach is computationlly expensive. Furthermore, previous models generally omitted the ferroelectric capacity model in the power off state, which is inconvenient for the unified simulation framework.

For the FC-FF simulation, we need a bahavior model which can compute quickly with SPICE, and characterize the nonvolatile property when power failure occurs. Therefore, we used the ferroelectric capacitance model which is shown in Figure 1. Two non-linear voltage control capacitors, a voltage control voltage source and some voltage control switches are needed. The control signal for swithches S1-S4 are produced by a Schmitt trigger. Two voltage control resistants are used in the model to simulate the nonvolatile characteristic. Their value is zero when the power is on, and tends to infinite when the power is down. So the charge can be stored in the capacitors.

This model can be easily implemented in SPICE and the simulation result of P-V hysteresis loop is shown in Figure 2. By tuning the circuit parameters of the above model, the curve coincides with the measured data. This behavior model of ferroelectric capacitance can be used in the SPICE simulation for the nonvolatile flip-flop design.

B. Architecture of Ferroelectirc Flip-Flop

SRAM based master-slave flip-flops are widely used. The master and slave parts are both clock-controlled latches. As shown in Figure 3, we propose an architecture of FC-FF in which a backup module is connected to the slave part.

When the signal RW is low, the FC-FF works as a conventional flip-flop. In the cycle of programming to the backup module, the signal *RW* is set to high and *Pch* remains low. The signal *PL* produces a positive pulse during the positive *Clk* period and data can be stored into the pair of ferroelectric capacitors FeC_1 and FeC_2.

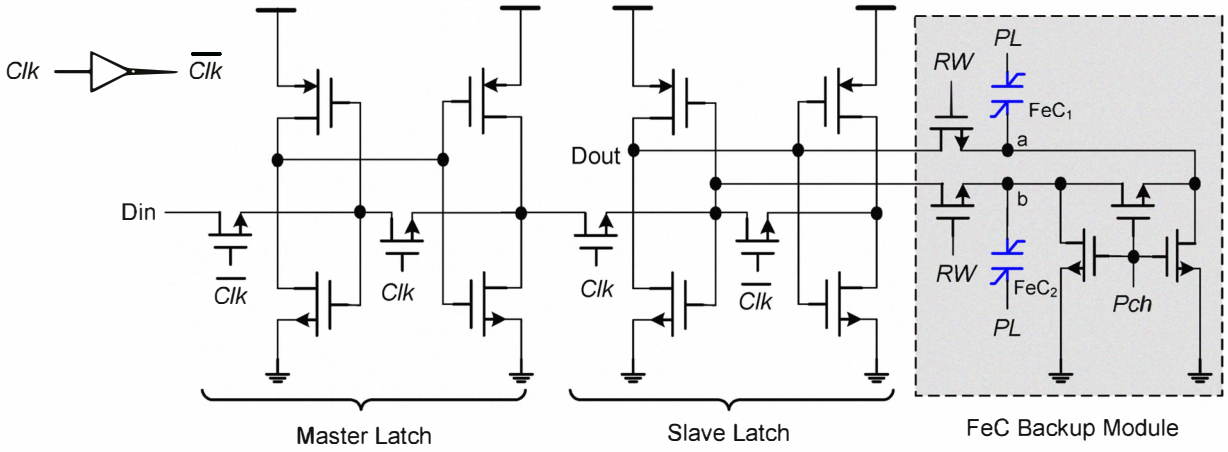


Figure 3. Architecture of FC-FF

After the power failure, lost data can be restored to flip-flop from the backup module. In the reading phase, *Din* and *Clk* remain low. At first, *Pch* produces a positive pulse to pre-discharge. Then *PL* produces a positive pulse to drive the pair of ferroelectric capacitors. Because the polarization states of two ferroelectric capacitances are different, the voltages of node *a* and *b* are different. This voltage difference is amplified by the latch feedback loop, so the data can be restored to the slave part of flip-flop.

FC-FF allows high speed data processing since it works as a conventional flip-flop in normal cases. The use of FC-FF brings nonvolatile characteristic.

III. IMPROVED FERROELECTRIC FLIP-FLOP

A. *Checkpoint Processor for Energy-Harvesting Applications*

Energy-harvesting is the process by which energy is derived, captured and stored from external sources, such as solar power, wind energy, thermal energy and kinetic energy. Currently energy harvesters don't produce sufficient energy to perform mechanical work, but instead provide small amount of power for powering low-energy electronics [4, 5]. Usually, it is applied in small, wireless autonomous devices, like those used in wearable electronics and wireless sensor networks. The energy of these systems is naturally present and is considered free. Therefore this technology is important in the area of green circuits and systems.

Because the power of these systems is derived from external sources which are always unstable, the power failure may occur at anytime and it is frequent under some condition. Therefore, the technique technology of checkpoint is necessary in energy-harvesting system for avoiding the effect of power failure. Checkpointing is a technique for inserting some fault tolerance into computing systems [14]. It basically consists of storing a snapshot of the current states, and later on, uses the stored states for restarting the execution in case of failure, such as the data loss due to power failure.

There is already some work using the technique of checkpoint for the energy-harvesting applications. Such as [6], in which a computational RFIDs was presented by using energy-aware computational checkpoints and voltage-aware program reordering that maintains program semantics. The author used checkpointing strategies in the RFID system to ensure no loss of state when there is no ambient power harvesting. And it is proved that checkpointing strategy is useful and effective in energy-harvesting applications.

B. *FC-FF in Checkpoint Processor*

In traditional checkpoint processors, the data and states are stored in nonvolatile memory, such as Flash, which is separate with the logic circuit. But it spends much time and energy for transferring and mapping all the data and states. If nonvolatile flip-flop can be used in checkpoint processors, the states can be stored in logic cell itself. After the power failure, the logic cells can restore data and state in last checkpoint without transferring and mapping it from the other memory. Therefore it will save some time and energy.

In checkpoints, the FC-FF stores its state in nonvolatile cell. After power failures, the processor can immediately recover the state by reading from the nonvolatile backup module in flip-flops. The recovery state is the same with the one stored in the last checkpoint before the power failure. It reduces the execute time and energy consumption of recovery by exploiting the nonvolatile flip-flops in checkpoint processor. Scientific and other long-running computations will benefit from the checkpoint protection against data loss on power failures [15].

As the fine-grained power management or frequent state backups are adopted, the frequency of checkpoints should be increased. Plenty of state backups in ferroelectric capacitance will be observed which poses great challenges for the lifetime of ferroelectric materials. The polarization can be reversed about 10^{12} to 10^{14} times [16]. The limited lifetime of ferroelectric capacitance restricts the application of FC-FF in checkpoint processors. Therefore, we developed an improved architecture of FC-FF which can remove the unnecessary programming cycles effectively in frequent state backup checkpoint processors.

C. *Architecture of Improved Ferroelectirc Flip-Flop*

The improved architecture of FC-FF (IFC-FF) is shown in Figure 4. The state comparing module can check whether it is necessary to re-write the ferroelectric capacitance in the checkpoint phase. It is only programmed when its present states in the nonvolatile backup module is different from the next state, so the programming cycles of ferroelectric capacitance are reduced effectively.

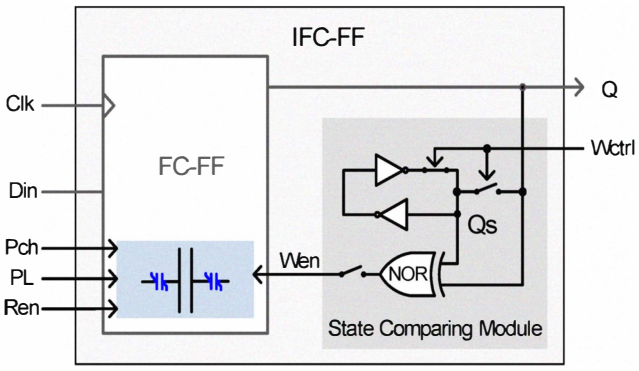


Figure 4. Architecture of IFC-FF

In the first checkpoint, data is stored in ferroelectric capacitance and latched by the inverter chain in state comparing module under the control of signal *Wctrl*. So the data stored in ferroelectric capacitance is the same with the one latched in state comparing module. The operation schedule of next checkpoints is shown in Figure 5. The operation process of IFC-FF is described as following:

- Positive clock in checkpoint phase: state comparing module compares Q with the state stored in node Q_S and outputs the signal *Wen*. It is low if the states are the same and high if they are different. So it can

estimate whether it is necessary to program the ferroelectric capacitance and control the signal *PL* to produce a positive pulse to drive the pair of ferroelectric capacitors or not.

- Negative clock in checkpoint phase: signal *Wctrl* produces a positive pulse to control the switches of the inverter chain in state comparing module. The new value of Q can be stored in the node Q_S to prepare the state comparison in next checkpoint.
- Normal phase: signal *Wctrl* remains low in this phase. The ferroelectric capacitance backup module and the state comparing module are isolated with the master and slave flip-flop parts, so the IFC-FF works as a conventional flip-flop in this phase.

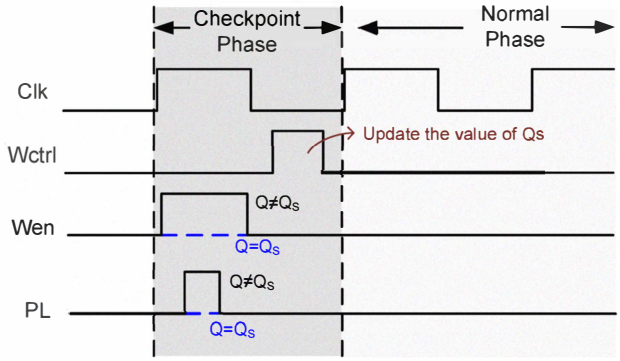


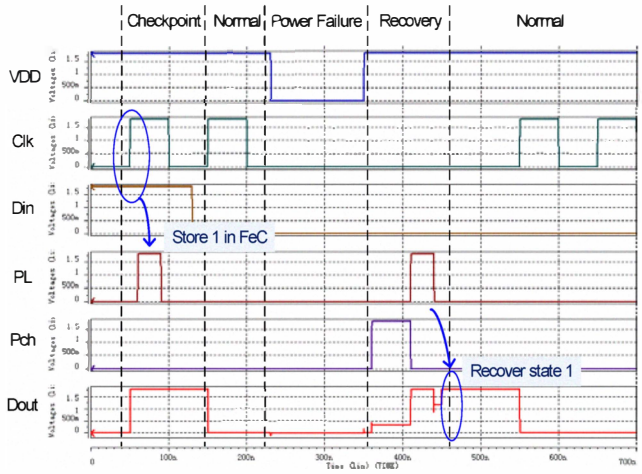
Figure 5. Schedule of IFC-FF based checkpoint processor

The checkpoint phase can be finished in one clock period and work in parallel with the main flip-flop circuit, so there is no overhead of execute time. Furthermore, the process of state comparison is not need to read from ferroelectric capacitances, so it adds no overhead of read operation.

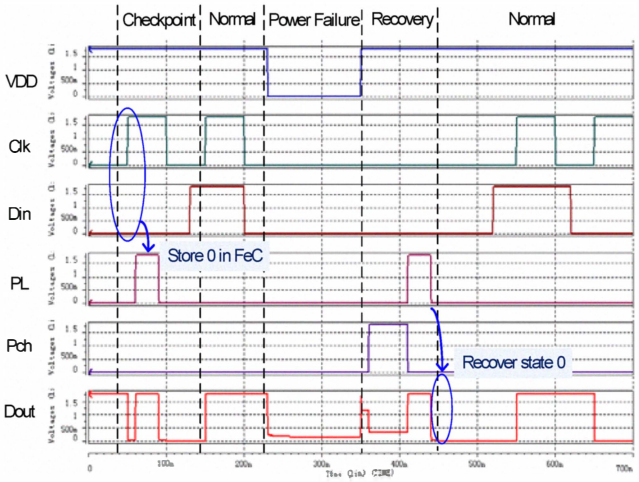
IV. Simulation Results

In the simulation of FC-FF and IFC-FF, the circuits are designed by using HJTM 0.18um CMOS technology library which increase the credibility of the results.

Figure 6 shows the functional simulation results. Before the power failure, data '1' and '0' are stored in the ferroelectric capacitance backup module in the last checkpoint, respectively. Then the power is off suddenly in the normal phase and the data in main part of flip-flop is lost. After the power is on again, the circuit enters to the recovery phase immediately. In this phase, the flip-flop reads from the ferroelectric capacitances and restores the state which is stored in the last checkpoint before the power failure. It can be observed from Figure 6 that data '1' and '0' are restored in the flip-flop respectively after recovering. Then the flip-flop works in the normal phase again. The simulation results show that this flip-flop has the nonvolatile capability and instantly recover from power failure.



(a)



(b)

Figure 6. IFC-FF SPICE simulation results: (a) Store '1' in the last checkpoint; (b) Store '0' in the last checkpoint

The effect and advantage of IFC-FF in checkpoint processor also has been simulated. Our group has developed a platform of wireless sensor network node chip which is implemented by 1-poly 6-metal 0.18um CMOS technology [17]. It provides the actual test data for our simulation of flip-flops. The clock frequency of the platform's processor is 10MHz, and checkpoint frequency is set as 1MHz for frequent state backups. The executing time is assumed as 1ms and 50 flip-flops in the processor are observed. The programming cycles of FC-FF and IFC-FF are compared under the same experimental conditions, and the result is shown in Figure 7.

It can be seen that the programming cycles of FC-FF is unchanged and equals to the number of checkpoints. On the other hand, the programming cycles of IFC-FF is reduced effectively. The number is smaller when the toggle rate decreases. In general cases, IFC-FF programs the ferroelectric capacitor of about 20%-60% compared to FC-FF. The power

dissipation of IFC-FF also could be well reduced compared to FC-FF since the most unnecessary programming cycles are avoided effectively.

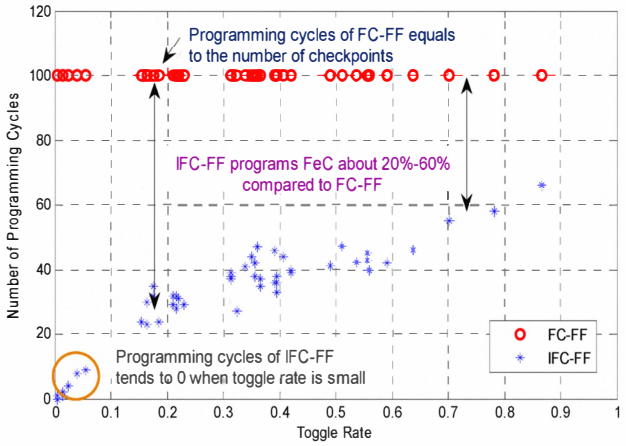


Figure 7. Comparison the programming cycles of FC-FF and IFC-FF

V. CONCLUSION

In this paper, a novel compare-and-write ferroelectric nonvolatile flip-flop is developed, which can be used in the checkpoint processor for energy-harvesting applications. The behavior model of ferroelectric capacitor is set up, and the normal and improved architecutres of ferroelectric capacitor based flip-flop are proposed, which features simultaneously non-volatility, low power dissipation. This flip-flop can be used to replace all the registers in checkpoint processor to make it nonvolatile, secure and can be recovered quickly after the power failures.

By using the complete simulation model of 0.18um CMOS, the circuit has been simulated in SPICE to evaluate the functions and performances. The results show that the flip-flop can recover the state which is stored in the ferroelectric capacitor backup module in the last checkpoint before the power failure. And the improved ferroelectric capacitor based flip-flop can reduce about 40-80% cycles of programming nonvolatily module, which can increase the lifetime of the ferroelectric capacitors effectively.

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