EE 165: Digital Design Verification
Spring 2021

Meeting time: TuTh 4:30-5:45
Format: Virtual/hybrid
Instructor: Joel Grodstein
TA: TBD

Prerequisites: Either EE 126, EE 25, graduate status or consent of the instructor.

Course Overview:

We will learn about verification of digital hardware designs at the Register-Transfer Level (RTL) using System Verilog. Industrial ASIC-design groups, who live or die based on their ability to produce working designs, have evolved numerous best-in-class practices that we will learn.

In fact, entire teams of people typically work to find bugs in a design and, eventually, declare the design bug-free. We will learn the techniques and infrastructures that these teams use.

Why would I care about this course?

In most university Computer-Engineering departments, verification is a poor stepchild of design. We learn, in great detail, how circuits work and how to design them. But while we are responsible for debugging the circuits we build, we never really learn the methods to do that task well. As a result, many (most?) of the projects we build in school never fully work.

When we then transition to our first job after graduation, a bit of a rude surprise awaits us – people expect our projects to work 😊. We quickly find that by and large, we are not being paid because of our shining intellect, nor even because of our great ideas. Instead, we are paid because we are good at taking a big, complex project and getting it to work. And – doing that on a tight schedule!

Verification is the process of testing whether a chip's implementation (as given by its description in, e.g., Verilog or VHDL) matches the chip's specification (often given in English), and debugging any mismatches. This course will help you learn the techniques and tools that are used for debugging (a.k.a. verifying) large industrial designs at the register-transfer level.

Mentor (one of the large EDA companies) surveys the ASIC and gate-array industries every two years. Their 2020 survey showed that:

- The average project employs roughly 10% more people with the title "verification engineer" than "design engineer."
- People with the title "design engineer" nonetheless spend roughly 50% of their time doing verification
- The job-growth rate from 2012-2020 was 5.5%/year for verification engineers vs. 1.5%/year for design engineers

Course Objectives:

Upon completion of the course, students will:

1. Understand what it means to verify designs at the register-transfer level.
2. Learn the various standard parts in an industrial design-verification testbench and infrastructure.
3. Learn about test writing, test coverage, and deciding when you are done testing.

4. Be competent in writing tests in SystemVerilog (which is essentially the standard language for that task).

Course format

The course format is hybrid. However, the exact format will evolve during the course.

Most of the course work will be done in small groups of 2-3 students. You will work on your assignments as a group and hand in just one assignment per group.

Each group will have a weekly time slot (likely 30 minutes) to meet with the instructor(s). For the most part, you can use your time slot for whatever you like; help with concepts, help debugging or anything else. We will probably also use the slots for oral quizzes; a short quiz where, again, your group works as a whole and you all get the same grade. We do not plan to have any written quizzes.

We will decide during the course whether to have the lectures "flipped" (i.e., prerecorded short videos that you can watch whenever you like), synchronous, or a mix of the two.

In February, the weekly meetings will be indoors or virtual. When the weather warms up, we may hold them outdoors if the logistics work.

Rough course sequence:

- What is verification? Why is it important?
- Introduction to SystemVerilog and the FIFO
- Understanding a design
- Verification overvioew
- Writing a test plan
- Writing a testbench
- Building and verifying a basic FIFO; basics of SystemVerilog
- Building a mesh router
- Generating stimulus
- Correctness checking
- Measuring and improving test coverage

Grade Formula

The exact grading breakdown is TBD. One reasonable version could be

- Programming assignments – 65%
- Quizzes – 35%

Quizzes and exams:

There will be several quizzes assigned during class. Dates will be posted on the course calendar and communicated in class. Quizzes are typically graded and returned promptly; thus, they can only be taken late by prior arrangement (e.g., for sickness or a hard scheduling conflict). We do not plan to have any exams.

Programming Assignments:

There will be programming assignments throughout the term. You will be writing the RTL for your hardware (a mesh router) and writing the verification testbench for it. We will likely do multiple rounds of testing each other's designs to learn from each other's strategies.

Final project or exam:

We do not plan to have a final exam. We may do a final project; we will decide partway through the course based on interest. If we do the project, then you may work in teams.

Late Assignments:

Late assignments will be penalized by 10% per day. Any extensions due to extenuating circumstances (illness or family emergencies) must be arranged ahead of time with the instructor before the original due date.

Textbook and references

The textbook for the course is "*SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*" by Chris Spear. It is available online at Tisch Library for free.

"*Verilog and SystemVerilog gotchas: 101 common coding errors and how to avoid them*" by Stuart Sutherland is another tried-and-true textbook.

There are numerous textbooks on SystemVerilog available for purchase as well.

Collaboration policy

Learning is a creative process. Individuals must understand problems and discover paths to their solutions. During this time, discussions with friends and colleagues are encouraged—you will do much better in the course, and at Tufts, if you find people with whom you regularly discuss problems. But those discussions should take place in English, not in code. If you start communicating in code, you're breaking the rules. When you reach the coding stage, therefore, group discussions are no longer appropriate. Each program, unless explicitly assigned as a pair problem, must be entirely your own work. Do not, under any circumstances, permit any other student to see any part of your program, and do not permit yourself to see any part of another student's program. In particular, you may not test or debug another student's code, nor may you have another student test or debug your code. (If you can't get code to work, consult a teaching assistant or the instructor.) Using another's code in any form or writing code for use by another violates the University's academic regulations. Do not, under any circumstances, post a public question to Piazza that contains any part of your code. Private questions directed to the instructors are OK. Suspected violations will be reported to the University's Judicial Officer for investigation and adjudication. Be careful! As described in the handbook on academic integrity, the penalties for violation can be severe. A single bad decision made in a moment of weakness could lead to a permanent blot on your academic record. The same standards apply to all homework assignments; work you submit under your name must be entirely your own work. Always acknowledge those with whom you discuss problems! Suspected violations will be reported to the University's Judicial Officer for investigation and adjudication. Again, be careful

Academic Support at the StAAR Center:

The StAAR Center (formerly the Academic Resource Center and Student Accessibility Services) offers a variety of resources to all students (both undergraduate and graduate) in the Schools of Arts and Science, Engineering, the SMFA and Fletcher; services are free to all enrolled students. Students may make an appointment to work on any writing-related project or assignment, attend subject tutoring in a variety of disciplines, or meet with an academic coach to hone fundamental academic skills like time management or overcoming procrastination. Students can make an appointment for

any of these services by visiting go.tufts.edu/TutorFinder, or by visiting our website (https://students.tufts.edu/staar-center).

Accommodations for Students with Disabilities:

Tufts University values the diversity of our students, staff, and faculty; recognizing the important contribution each student makes to our unique community. Tufts is committed to providing equal access and support to all qualified students through the provision of reasonable accommodations so that each student may fully participate in the Tufts experience. If you have a disability that requires reasonable accommodations, please contact the StAAR Center (formerly Student Accessibility Services) at StaarCenter@tufts.edu or 617-627-4539 to make an appointment with an accessibility representative to determine appropriate accommodations. Please be aware that accommodations cannot be enacted retroactively, making timeliness a critical aspect for their provision.