CS 301 High-Performance Computing

$\underline{\text{Lab } 4}$

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February 28, 2024

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1 Hardware Details

1.1 HPC Cluster

```
[202101418@gics0 ~]$ lscpu
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 24
On-line CPU(s) list: 0-23
Thread(s) per core: 2
Core(s) per socket: 6
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 63
Model name: Intel(R) Xeon(R) CPU E5-2620 v3 @ 2.40GHz
Stepping: 2
CPU MHz: 2600.062
BogoMIPS: Virtualization: VT-x
Lld cache: 32K
Lli cache: 32K
Ll cache: 32K
Ll cache: 15360K
NUMA node0 CPU(s): 0-5,12-17
NUMA node0 CPU(s): 6-11,18-23
[202101418@gics0 ~]$
```

Figure 1: lscpu in cmd

As we can see from the above image

- CPU 16
- \bullet Socket 2
- Cores per Socket 8
- \bullet Size of L1 cache 32K
- \bullet Size of L2 cache 256K
- Size of L3 cache 15360K

1.2 Lab 207 PC

Figure 2: lscpu in cmd

- CPU 4
- Socket 1
- Cores per Socket 4
- Size of L1 cache 32K
- Size of L2 cache 256K
- $\bullet\,$ Size of L3 cache 6144K

2 Description of Problem

Sorting arrays with merge sort algorithm optimized with multiple threads

3 Complexity of algorithm (serial)

O(N*LogN)

4 Optimization strategy

- 1. used iterative approach instead of recursive
- 2. Parallelized merging of sorted arrays

5 Graphs

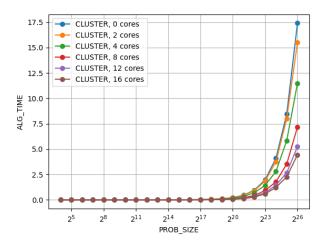


Figure 3: Cluster results

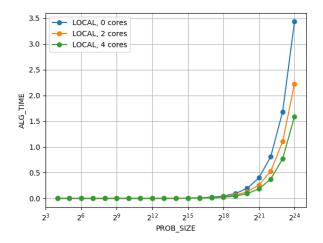


Figure 4: Lab results

6 Explanation of results

As the number of threads increases, time decreases as more operations are done simultaneously.