9 附录 B 指令码一览

指令	操作数	编码 (bit 31 → 0)
RDCNTID.W	rj	`0000000000000000011000` | rj | `00000`
RDCNTVL.W	rd	`0000000000000000011000` | `00000` | rd
RDCNTVH.W	rd	`0000000000000000011001` | `00000` | rd
ADD.W	rd, rj, rk	`00000000000100000` | rk | rj | rd
SUB.W	rd, rj, rk	`00000000000100010` | rk | rj | rd
SLT	rd, rj, rk	`00000000000100100` | rk | rj | rd
SLTU	rd, rj, rk	`00000000000100101` | rk | rj | rd
NOR	rd, rj, rk	`00000000000101000` | rk | rj | rd
AND	rd, rj, rk	`00000000000101001` | rk | rj | rd
OR	rd, rj, rk	`00000000000101010` | rk | rj | rd
XOR	rd, rj, rk	`00000000000101011` | rk | rj | rd
SLL.W	rd, rj, rk	`00000000000101110` | rk | rj | rd
SRL.W	rd, rj, rk	`00000000000101111` | rk | rj | rd
SRA.W	rd, rj, rk	`00000000000110000` | rk | rj | rd
MUL.W	rd, rj, rk	`00000000000111000` | rk | rj | rd
MULH.W	rd, rj, rk	`00000000000111001` | rk | rj | rd
MULH.WU	rd, rj, rk	`00000000000111010` | rk | rj | rd
DIV.W	rd, rj, rk	`00000000001000000` | rk | rj | rd
MOD.W	rd, rj, rk	`00000000001000001` | rk | rj | rd
DIV.WU	rd, rj, rk	`00000000001000010` | rk | rj | rd
MOD.WU	rd, rj, rk	`00000000001000011` | rk | rj | rd
BREAK	code	`00000000001010100` | code
SYSCALL	code	`00000000001010110` | code
SLLI.W	rd, rj, ui5	`00000000010000` | `001` | ui5 | rj | rd
SRLI.W	rd, rj, ui5	`00000000010001` | `001` | ui5 | rj | rd
SRAI.W	rd, rj, ui5	`00000000010010` | `001` | ui5 | rj | rd
FADD.S	fd, fj, fk	`00000001000000001` | fk | fj | fd
FADD.D	fd, fj, fk	`00000001000000010` | fk | fj | fd
FSUB.S	fd, fj, fk	`00000001000000101` | fk | fj | fd
FSUB.D	fd, fj, fk	`00000001000000110` | fk | fj | fd
FMUL.S	fd, fj, fk	`00000001000001001` | fk | fj | fd
FMUL.D	fd, fj, fk	`00000001000001010` | fk | fj | fd
FDIV.S	fd, fj, fk	`00000001000001101` | fk | fj | fd
FDIV.D	fd, fj, fk	`00000001000001110` | fk | fj | fd
FMAX.S	fd, fj, fk	`00000001000010001` | fk | fj | fd
FMAX.D	fd, fj, fk	`00000001000010010` | fk | fj | fd
FMIN.S	fd, fj, fk	`00000001000010101` | fk | fj | fd

Bit positions (31 → 0):

`3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0`
`1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0`

Instruction	Operands	Encoding (bits 31–0)
FMIN.D	fd, fj, fk	0 0 0 0 0 0 1 0 0 0 0 1 0 1 1 0 · fk · fj · fd
FMAXA.S	fd, fj, fk	0 0 0 0 0 0 1 0 0 0 0 1 1 0 0 1 · fk · fj · fd
FMAXA.D	fd, fj, fk	0 0 0 0 0 0 1 0 0 0 0 1 1 0 1 0 · fk · fj · fd
FMINA.S	fd, fj, fk	0 0 0 0 0 0 1 0 0 0 0 1 1 1 0 1 · fk · fj · fd
FMINA.D	fd, fj, fk	0 0 0 0 0 0 1 0 0 0 0 1 1 1 1 0 · fk · fj · fd
FCOPYSIGN.S	fd, fj, fk	0 0 0 0 0 0 1 0 0 0 1 0 0 1 0 1 · fk · fj · fd
FCOPYSIGN.D	fd, fj, fk	0 0 0 0 0 0 1 0 0 0 1 0 0 1 1 0 · fk · fj · fd
FABS.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 0 0 0 0 1 · fj · fd
FABS.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 0 0 0 1 0 · fj · fd
FNEG.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 0 0 1 0 1 · fj · fd
FNEG.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 0 0 1 1 0 · fj · fd
FCLASS.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 0 1 1 0 1 · fj · fd
FCLASS.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 0 1 1 1 0 · fj · fd
FSQRT.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 1 0 0 0 1 · fj · fd
FSQRT.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 1 0 0 1 0 · fj · fd
FRECIP.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 1 0 1 0 1 · fj · fd
FRECIP.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 1 0 1 1 0 · fj · fd
FRSQRT.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 1 1 0 0 1 · fj · fd
FRSQRT.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 0 1 1 0 1 0 · fj · fd
FMOV.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0 0 1 0 1 · fj · fd
FMOV.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0 0 1 1 0 · fj · fd
MOVGR2FR.W	fd, rj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0 1 0 0 1 · rj · fd
MOVGR2FRH.W	fd, rj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0 1 0 1 1 · rj · fd
MOVFR2GR.S	rd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0 1 1 0 1 · fj · rd
MOVFRH2GR.S	rd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 0 1 1 1 1 · fj · rd
MOVGR2FCSR	fcsr, rj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 1 0 0 0 0 · rj · fcsr
MOVFCSR2GR	rd, fcsr	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 1 0 0 1 0 · fcsr · rd
MOVFR2CF	cd, fj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 1 0 1 0 0 · fj · 0 0 · cd
MOVCF2FR	fd, cj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 1 0 1 0 1 · 0 0 · cj · fd
MOVGR2CF	cd, rj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 1 0 1 1 0 · rj · 0 0 · cd
MOVCF2GR	rd, cj	0 0 0 0 0 0 1 0 0 0 1 0 1 0 0 1 1 0 1 1 1 · 0 0 · cj · rd
FCVT.S.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 0 1 0 0 0 1 1 0 · fj · fd
FCVT.D.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 0 1 0 0 1 0 0 1 · fj · fd
FTINTRM.W.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 1 0 0 0 0 0 0 1 · fj · fd
FTINTRM.W.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 1 0 0 0 0 0 1 0 · fj · fd
FTINTRP.W.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 1 0 0 1 0 0 0 1 · fj · fd
FTINTRP.W.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 1 0 0 1 0 0 1 0 · fj · fd
FTINTRZ.W.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 1 0 1 0 0 0 0 1 · fj · fd
FTINTRZ.W.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 1 0 1 0 0 0 1 0 · fj · fd
FTINTRNE.W.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 1 0 1 1 0 0 0 1 · fj · fd
FTINTRNE.W.D	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 1 0 1 1 0 0 1 0 · fj · fd
FTINT.W.S	fd, fj	0 0 0 0 0 0 1 0 0 0 1 1 0 1 1 0 0 0 0 0 1 · fj · fd

Instruction	Operands	31...22 / encoding
FTINT.W.D	fd, fj	0 0 0 0 0 0 0 1 0 0 0 1 1 0 1 1 0 0 0 0 1 0 | fj | fd
FFINT.S.W	fd, fj	0 0 0 0 0 0 0 1 0 0 0 1 1 1 0 1 0 0 0 1 0 0 | fj | fd
FFINT.D.W	fd, fj	0 0 0 0 0 0 0 1 0 0 0 1 1 1 0 1 0 0 1 0 0 0 | fj | fd
SLTI	rd, rj, si12	0 0 0 0 0 0 1 0 0 0 | si12 | rj | rd
SLTUI	rd, rj, si12	0 0 0 0 0 0 1 0 0 1 | si12 | rj | rd
ADDI.W	rd, rj, si12	0 0 0 0 0 0 1 0 1 0 | si12 | rj | rd
ANDI	rd, rj, ui12	0 0 0 0 0 0 1 1 0 1 | ui12 | rj | rd
ORI	rd, rj, ui12	0 0 0 0 0 0 1 1 1 0 | ui12 | rj | rd
XORI	rd, rj, ui12	0 0 0 0 0 0 1 1 1 1 | ui12 | rj | rd
CSRRD	rd, csr	0 0 0 0 0 1 0 0 | csr | 0 0 0 0 0 | rd
CSRWR	rd, csr	0 0 0 0 0 1 0 0 | csr | 0 0 0 0 1 | rd
CSRXCHG	rd, rj, csr	0 0 0 0 0 1 0 0 | csr | rj!=0,1 | rd
CACOP	code, rj, si12	0 0 0 0 0 1 1 0 0 0 | si12 | rj | code
TLBSRCH		0 0 0 0 0 1 1 0 0 1 0 0 1 0 0 0 0 0 1 0 1 0 | 0 0 0 0 0 | 0 0 0 0 0
TLBRD		0 0 0 0 0 1 1 0 0 1 0 0 1 0 0 0 0 0 1 0 1 1 | 0 0 0 0 0 | 0 0 0 0 0
TLBWR		0 0 0 0 0 1 1 0 0 1 0 0 1 0 0 0 0 0 1 1 0 0 | 0 0 0 0 0 | 0 0 0 0 0
TLBFILL		0 0 0 0 0 1 1 0 0 1 0 0 1 0 0 0 0 0 1 1 0 1 | 0 0 0 0 0 | 0 0 0 0 0
ERTN		0 0 0 0 0 1 1 0 0 1 0 0 1 0 0 0 0 0 1 1 1 0 | 0 0 0 0 0 | 0 0 0 0 0
IDLE	level	0 0 0 0 0 1 1 0 0 1 0 0 1 0 0 0 1 | level
INVTLB	op, rj, rk	0 0 0 0 0 1 1 0 0 1 0 0 1 0 0 1 1 | rk | rj | op
FMADD.S	fd, fj, fk, fa	0 0 0 0 1 0 0 0 0 0 0 1 | fa | fk | fj | fd
FMADD.D	fd, fj, fk, fa	0 0 0 0 1 0 0 0 0 0 1 0 | fa | fk | fj | fd
FMSUB.S	fd, fj, fk, fa	0 0 0 0 1 0 0 0 0 1 0 1 | fa | fk | fj | fd
FMSUB.D	fd, fj, fk, fa	0 0 0 0 1 0 0 0 0 1 1 0 | fa | fk | fj | fd
FNMADD.S	fd, fj, fk, fa	0 0 0 0 1 0 0 0 1 0 0 1 | fa | fk | fj | fd
FNMADD.D	fd, fj, fk, fa	0 0 0 0 1 0 0 0 1 0 1 0 | fa | fk | fj | fd
FNMSUB.S	fd, fj, fk, fa	0 0 0 0 1 0 0 0 1 1 0 1 | fa | fk | fj | fd
FNMSUB.D	fd, fj, fk, fa	0 0 0 0 1 0 0 0 1 1 1 0 | fa | fk | fj | fd
FCMP.cond.S	cd, fj, fk	0 0 0 0 1 1 0 0 0 0 0 1 | cond | fk | fj | 0 0 | cd
FCMP.cond.D	cd, fj, fk	0 0 0 0 1 1 0 0 0 0 1 0 | cond | fk | fj | 0 0 | cd
FSEL	fd, fj, fk, ca	0 0 0 0 1 1 0 1 0 0 0 0 0 0 | ca | fk | fj | fd
LU12I.W	rd, si20	0 0 0 1 0 1 0 | si20 | rd
PCADDU12I	rd, si20	0 0 0 1 1 1 0 | si20 | rd
LL.W	rd, rj, si14	0 0 1 0 0 0 0 0 | si14 | rj | rd
SC.W	rd, rj, si14	0 0 1 0 0 0 0 1 | si14 | rj | rd
LD.B	rd, rj, si12	0 0 1 0 1 0 0 0 0 0 | si12 | rj | rd
LD.H	rd, rj, si12	0 0 1 0 1 0 0 0 0 1 | si12 | rj | rd
LD.W	rd, rj, si12	0 0 1 0 1 0 0 0 1 0 | si12 | rj | rd
ST.B	rd, rj, si12	0 0 1 0 1 0 0 1 0 0 | si12 | rj | rd
ST.H	rd, rj, si12	0 0 1 0 1 0 0 1 0 1 | si12 | rj | rd
ST.W	rd, rj, si12	0 0 1 0 1 0 0 1 1 0 | si12 | rj | rd
LD.BU	rd, rj, si12	0 0 1 0 1 0 1 0 0 0 | si12 | rj | rd

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD.HU	**rd, rj, si12**	0	0	1	0	1	0	1	0	0	1	si12												rj					rd				
PRELD	**hint, rj, si12**	0	0	1	0	1	0	1	0	1	1	si12												rj					hint				
FLD.S	**fd, rj, si12**	0	0	1	0	1	0	1	1	0	0	si12												rj					fd				
FST.S	**fd, rj, si12**	0	0	1	0	1	0	1	1	0	1	si12												rj					fd				
FLD.D	**fd, rj, si12**	0	0	1	0	1	0	1	1	1	0	si12												rj					fd				
FST.D	**fd, rj, si12**	0	0	1	0	1	0	1	1	1	1	si12												rj					fd				
DBAR	**hint**	0	0	1	1	1	0	0	0	0	1	1	1	0	0	1	0	0	hint														
IBAR	**hint**	0	0	1	1	1	0	0	0	0	1	1	1	0	0	1	0	1	hint														
BCEQZ	**cj, offs**	0	1	0	0	1	0	offs[15:0]																0	0	cj			offs[20:16]				
BCNEZ	**cj, offs**	0	1	0	0	1	0	offs[15:0]																0	1	cj			offs[20:16]				
JIRL	**rd, rj, offs**	0	1	0	0	1	1	offs[15:0]																rj					rd				
B	**offs**	0	1	0	1	0	0	offs[15:0]																offs[25:16]								
BL	**offs**	0	1	0	1	0	1	offs[15:0]																offs[25:16]								
BEQ	**rj, rd, offs**	0	1	0	1	1	0	offs[15:0]																rj					rd				
BNE	**rj, rd, offs**	0	1	0	1	1	1	offs[15:0]																rj					rd				
BLT	**rj, rd, offs**	0	1	1	0	0	0	offs[15:0]																rj					rd				
BGE	**rj, rd, offs**	0	1	1	0	0	1	offs[15:0]																rj					rd				
BLTU	**rj, rd, offs**	0	1	1	0	1	0	offs[15:0]																rj					rd				
BGEU	**rj, rd, offs**	0	1	1	0	1	1	offs[15:0]																rj					rd				