A Reconfigurable Passive Voltage Multiplier for Wireless Mobile IoT Applications

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***Abstract*—Battery-less wireless systems generate their supply voltage from the incoming RF signal, and need to deal with the problem of generating sufficient voltage level required by their various blocks from weak input signals, while maintaining high efficiency. The presented voltage multiplier (VM) seeks to maximize the power conversion efficiency (PCE) by changing the RF-to-DC converter topology in the VM based on the incoming signal. Besides topology, the number of stages in the VM can change for the desired output dc voltage from the varying RF input signal. A prototype is fabricated in 0.35-μm standard CMOS process, operating at 13.56 MHz with a 2 kΩ load. The core element in the VM yields a peak PCE of 76% with the cross-coupled topology at low input power, while the hybrid topology provides 70% PCE at higher input power. This reconfigurable VM can be used in RFID or Internet-of-Things (IoT) mobile applications to regulate power against changes in the distance between the power source and the target.**

***Index Terms*—RF-to-DC converter, voltage multiplier, wireless power transfer, energy harvesting, Internet-of-Things (IoT).**

I. Introduction

THE GROWING demand for Internet-of-Things (IoT) applications increases the need for next-generation sensors and actuators with wireless power and data transmission capability, which is one of the imperious features for these devices [1]. Major achievements in wireless communication in the past decades also motivate employing wireless powering of the next generation devices towards fully wireless systems. Even though the complexity of these devices increases with new functionalities, which in turn increases the power requirement, the inductive wireless power transfer (WPT) can play a critical role to wirelessly power up or recharge these higher power devices [2].

Most efforts to increase the power conversion efficiency (PCE) of wireless devices focus on the RF-to-DC conversion block [3]. However, when the amplitude of the incoming signal is insufficient, even a rectifier with very high PCE cannot generate enough DC voltage to energize the circuits in a wireless system. In such a case, voltage doublers or multipliers are required to supply the necessary DC voltage at the cost of lower PCE [4], [5]. Another important challenge is the maintenance of sustainable high PCE due to the large variability in the strength of the incoming RF signal. Conventional RF-to-DC converters that can only perform with high PCE at a specific power range are not well-suited in this kind of applications, which need an input dynamic range [6]. Moreover, large variability in available power at the input causes large variability in the rectified DC voltage at the output, particularly at the low input power range. Even though researchers recently attempt to address this issue with new reconfigurable rectifiers and doublers [8]–[12], the number of reconfigurable voltage multipliers (RVM) studies are still limited in the literature [8].

In this brief, we present a reconfigurable passive voltage multiplier (VM), which adapts according to the strength of the incoming RF signal to maintain the required DC voltage with high PCE from available input power. Section II gives a brief summary of the state-of-the-art VMs for low input power. Section III presents implementation details and operating principles behind the proposed VM. Section IV includes the measurement results and performance metrics, followed by concluding remarks.

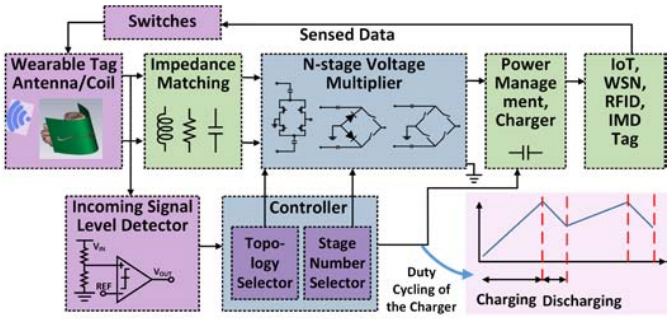

Fig. 1. Block diagram of a generic wireless IoT system with emphasis on the energy harvesting unit.

II. State-of-the-Art in Voltage Multipliers

A comparison of some of the most popular VMs, including Dickson VM (DVM) with Schottky diodes, regular, native, and low-threshold transistors, ultra-low-power diodes (ULPD), and cross-coupled VM (CCVM), presented in Fig. 2, has been conducted in [6]. In this comparison, to be fair, all topologies are migrated to the same fabrication process, and adjusted for the same target specifications, and analyzed with the same set of input constraints. According to the outcome of this analysis in Fig. 3, changes at the input power strongly affect the PCE of most VMs, which are suitable only for a particular power level. We propose a reconfigurable topology that is standard

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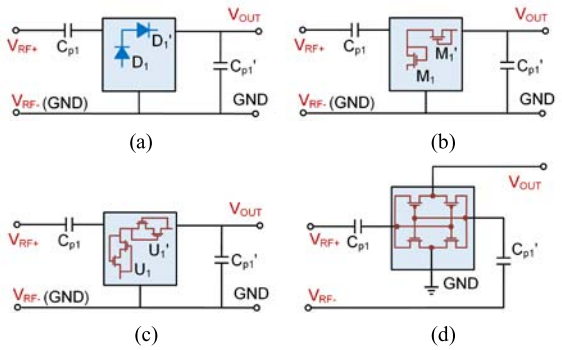

Fig. 2. A set of existing VM solutions. Dickson VM with (a) Schottky diodes, (b) with regular, low-threshold, native transistors, (c) with regular and low-threshold transistors form ULPD, (d) cross-coupled VM with regular and low-threshold transistors [6].

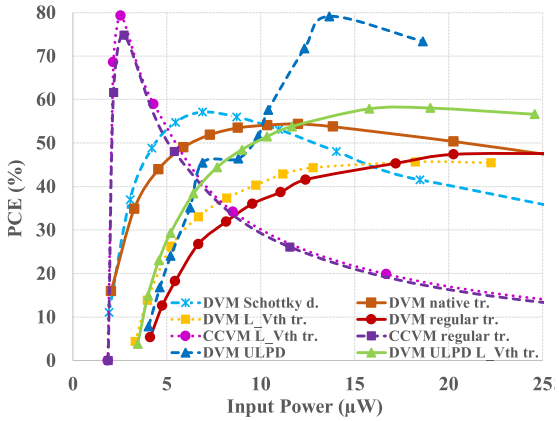

Fig. 3. Simulated PCE of the voltage multipliers by varying input power [6].

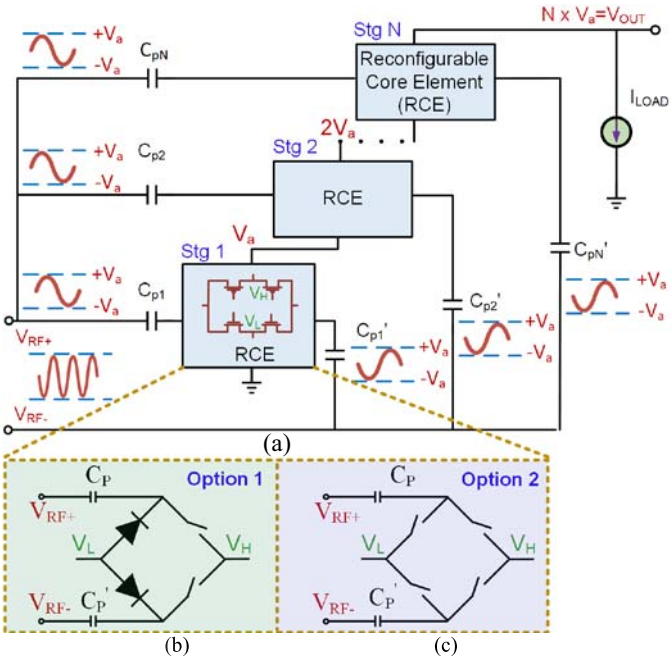

Fig. 4. (a) Block diagram of an RVM with RCEs, (b) ND-PS topology, and (c) ALL-S topology.

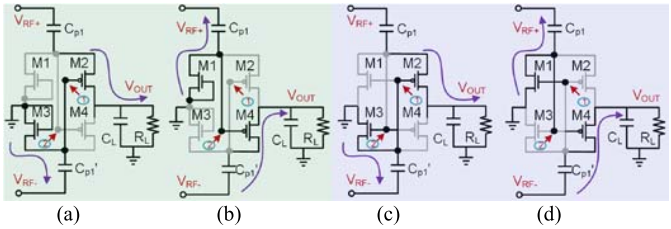

Fig. 5. Operation of a single-stage ND-PS hybrid rectifier in (a) positive half-cycle, and (b) negative half-cycle. Operation of a single-stage ALL-S rectifier in (c) positive half-cycle, and (d) negative half-cycle.

CMOS-compatible, easily adjustable to a variety of power levels and remains efficient in a wider input power range.

III. Proposed Voltage Multiplier Topology and Its Operating Principles

Our recent study presents a reconfiguration scheme among four well-known types of rectifiers, which are bridge, cross-coupled, and hybrid rectifiers [12]. As rectifiers are composed of diodes and/or switches, they can be implemented with transistors. The reconfiguration is performed by altering the transistors from switch to diode and vice versa by configuring their gate connections. In this brief, we employ this scheme as a reconfigurable core element (RCE) in an RVM to attain high PCE at varying input power levels.

Fig. 4a shows the block diagram of the RVM. According to [12], hybrid topologies have similar behaviors and numeric results for PCE in the measured range. The four-switch (ALL-S) topology has the highest PCE at the low power range, while the four-diode (ALL-D) topology has the lowest PCE in the whole measured power range. To reduce the switching complexity of the system, particularly when several stages are deployed in a fully automatic RVM, we decided to eliminate some of these topologies. We opted to realize the reconfiguration scheme only with NMOS diodes and PMOS switches (ND-PS) hybrid and ALL-S topologies, as shown in Figs. 4b and 4c.

Reasons behind this choice are: i) ALL-D topology does not have a competitive performance in the range of interest, up to several mW. ii) Since ALL-S topology has the highest PCE at the low input power range, it is the natural choice for this range. iii) Although hybrid topologies have similar performance, ND-PS topology achieves slightly higher PCE than that of NS-PD topology at the higher input power range. However, NS-PD topology performs slightly better at the low input level. This is mainly due to the lower dropout voltage of diode-connected NMOS (V_{thn}) than diode-connected PMOS (V_{thp}) transistors. Because of the same reason at low power level, PMOS switches slightly degrade PCE of ND-PS. As ALL-S will take care of the low power region, we can ignore the PCE degradation of ND-PS because of PMOS switches in this range and choose the ND-PS topology for the high power range.

In the steady-state with the assumption of lossless charge transfer, the output DC voltage of the multiplier is directly proportional to the stage number and calculated by $V_{OUT} = V_a \times \mathrm{N}$, where N is the stage number and V_a is the amplitude of the input signal, derived from the given expression $V_{RF} = V_{RF+} - V_{RF-} = V_a \cos \omega t$, where $\omega = 2\pi f$ is the angular frequency. However, in the real case, semiconductor devices, e.g., switches and diodes, have dropout voltages, V_{DR}, which reduce the output DC voltage, V_{OUT}. Another reason for losses is the energy accumulated in the parasitic capacitors.

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The operation of the RCE in the positive and negative half cycles is illustrated in Fig. 5. When V_{RF+} is positive, in ND-PS and ALL-S configurations, M2 and M3 transistors are on and M1 and M4 transistors are cut-off. While M2 transistors form a switch in both topologies, M3 transistor is a switch in the ALL-S topology and a diode in the ND-PS topology, shown in Figs. 5a and 5c, respectively. In positive half cycle, charge flows from C_{p1} to C_L through M2. Similarly, when V_{RF-} is positive in the negative half cycle, M1 and M4 transistors are on and M2 and M3 transistors are cut-off. While M4 transistors form a switch in both topologies, M1 transistor forms a switch in ALL-S topology and a diode in ND-PS topology, shown in Figs. 5b and 5d, respectively. In the negative half cycle, charge flows from C'_{P1} to C_L through M4. According to this explanation, with ND-PS topology, the output DC voltage of a single-stage core element is,

$$V_{OUT} = 2V_a - \left(V_{DR\_ND} + V_{DR\_PS}\right), \tag{1}$$

where V_{DR_ND} is the dropout voltage of the diode-connected NMOS transistor and V_{DR_PS} is the dropout voltage of the PMOS switch. With ALL-S topology, the output DC voltage of a single-stage core element is,

$$V_{OUT} = 2V_a - \left(V_{DR\_NS} + V_{DR\_PS}\right), \tag{2}$$

where V_{DR_NS} is the dropout voltage of the NMOS switch. The transient values of V_{DR_ND}, V_{DR_NS}, and V_{DR_PS} depend on the input voltage and in turn operating region of the transistors, which determines PCE of the VM.

The internal voltages, nodes 1 and 2 in Fig. 5, are generated at the gate of each switch. Since switches are bidirectional, unlike diodes, reverse and forward current of transistors generate a common mode-voltage in the labeled nodes. The common-mode voltage is the DC combination of the voltages of nodes 1 and 2 and it is close to the half of the rectified output voltage. Common-mode voltage at the gate of the switch-connected transistors reduces the effective threshold voltage of these transistors. Therefore, V_{DR_PS} and V_{DR_NS} become lower than V_{th}. On the other hand, effective threshold voltage for a diode-connected transistor remains at V_{th}. Because of the abovementioned reasons, a switch-connected transistor operates with higher efficiency than a diode-connected transistor when the amplitude of the incoming signal, V_a, is below the threshold voltage level. Once the amplitude of the input signal, V_a, exceeds threshold voltage and when $V_{OUT} > V_a$ in the periodic cycle, the switch-connected transistor conducts in the reverse direction. In this case, the greater V_a causes the greater leakage and the lower PCE. The aspect ratio of all transistors in the core element is the same, $\frac{W}{L} = \frac{1.5\ mm}{0.35\ \mu m}$. Pump capacitors are 1 nF, and the load capacitance is 100 nF in the VM.

When we cascaded the RCEs, an N-stage RVM generates a rectified-output voltage as [12],

$$V_{OUT} = 2NV_a - N\left(V_{DR\_ND} + V_{DR\_PS}\right) \tag{3}$$

when it is reconfigured as ND-PS VM and,

$$V_{OUT} = 2NV_a - N\left(V_{DR\_NS} + V_{DR\_PS}\right) \tag{4}$$

when it is reconfigured with ALL-S VM.

In cascaded structures, V_{th} of transistors increases due to body effect, an increase in the source-body voltage, V_{sb}, which directly affects the dropout voltage of switches and diode-connected transistors. The increased dropout voltage reduces the conductivity of transistors, which leads to an increase in the output resistance and in turn decreases V_{OUT}. The higher N leads to higher power loss due to higher V_{sb}. On the other hand, a VM with fewer stages may not generate the required V_{OUT}. Therefore, there is a trade-off, which should be resolved by an optimization process. Particularly in mobile wireless applications, a configuration mechanism is helpful to adjust V_{OUT} according to varying input signal strength. By default, the VM can startup with all stages and the stage number can be adjusted according to the power of the incoming signal by a simple controller.

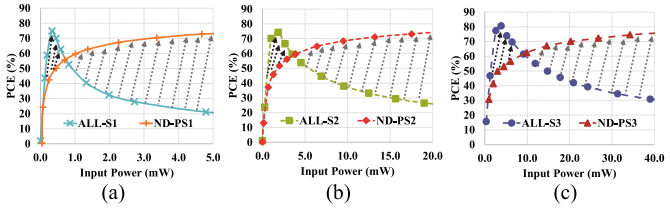

Fig. 6. Simulated PCE of VM with (a) one stage (b) two stages, and (c) three stages vs. input power at 13.56 MHz with 2 kΩ load and demonstrated enhancement in PCEs with the employment of RCEs.

As seen from Fig. 5a, the symmetric placement of capacitors and RCEs helps to excite the diodes/switches with the same input signal. This arrangement reduces the reflected harmonics, which might cause current imbalance in the VM. Another important point is variation of the input impedance of the VM with N, the selected topology, and the input power. Even though this effect does not severely degrade the PCE at the low frequency range, the designer should pay special attention at higher frequency range, in the GHz range by having a reconfigurable impedance matching circuitry between the VM and the antenna/coil.

We have analyzed the PCE for RVMs with one, two, and three stages at 13.56 MHz under a 2 kΩ loading. PCE performances of VMs with up to three stages are presented in Fig. 6. The PCE enhancements with the RCEs in the RVMs are demonstrated with the arrows added to the figures compared to a fixed topology of ALL-S and ND-PS rectifiers. Particularly, enhancement in the low-power level significantly improves the read range of mobile devices. The VM should start-up with an ALL-S type RCE as a precaution for insufficient power for the ND-PS type to operate efficiently. The controller can alter the topology to ND-PS, when the received power is high enough.

We have also analyzed the output DC voltage of VMs vs. input voltage and power. Fig. 7a depicts the output voltage with the varying input power, while Fig. 7b magnifies the low voltage range. Fig. 7c shows the output voltages vs. input voltage, while Fig. 7d magnifies the low input voltage range. This result indicates the significance of reconfiguration for mobile devices, which might have different input voltage/power depending on their distance from the power source. The output voltage behavior for varying power demonstrates different characteristics than the behavior for varying input voltage, shown in Fig. 7. This is due to the complex nature of the input impedance, which is affected by N, the incoming power especially in the low power range, and the type of the topology of the RCE. Note that even with the same input power, the input voltage can be different because of these factors. Voltage multipliers, by definition, multiply the input voltage at the output. However, the input power also affects the performance of the VM, and should be considered along with the input voltage. The nonlinear nature of the input impedance

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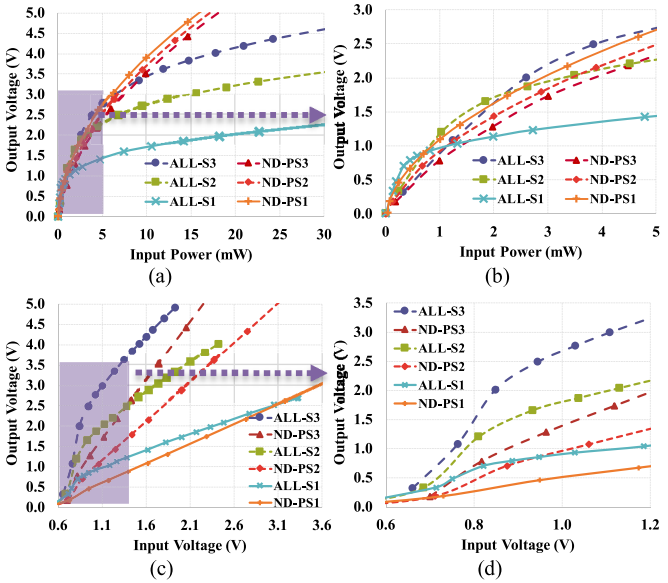

Fig. 7. Simulated output DC voltage of VMs vs. (a) input power and (c) input voltage. (b) A magnified view of (a) for the low input power range. (d) A magnified view of (c) for the low input voltage range.

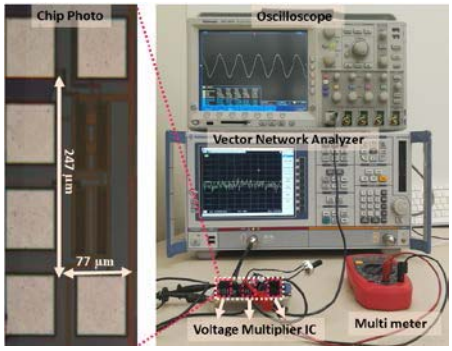

Fig. 8. The measurement setup of the RVM with the chip photo of the RCEs.

prevents to extract a straight forward relation between the input power and the output voltage. In the simulation in Fig. 7c, to increase the input voltage further we need to increase the input power significantly; therefore, we preferred to keep the input power at a range of less than 40 mW, which caused input voltages stayed at 1.8 V for ALL-S3 and 2.5 V for ALL-S2.

IV. Measurement Results and Discussion

The RVM shown in Fig. 4 was fabricated in the TSMC 0.35-µm standard-CMOS process. Fig. 8 shows the measurement setup and chip micrograph of the core element. Reconfiguration of the VM has been performed at the board level, as shown in Fig. 9. Measurements were conducted using a VNA (Rohde & Schwartz, ZVB 4). The power at the input of the VM has been estimated by calculating the power losses from the measured S_{11} parameter and subtracting the power losses from the power supplied from the VNA 50 Ω port. Since calculated power at the input of the VM would be enough to conduct our analysis, we opted to leave the design of an impedance matching network outside of the scope of this brief. However, an on-board varactor would be a proper choice in an inductive link setting at 13.56 MHz. AC input voltage generated by the VNA at a single tone by setting the span to

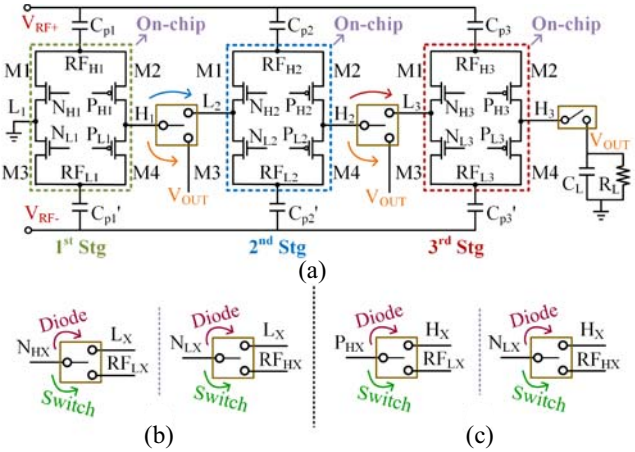

Fig. 9. (a) Reconfiguration mechanism of N of the VM. Switch/Diode selector for (b) NMOS and (c) PMOS transistors in the RCEs deployed in the VM.

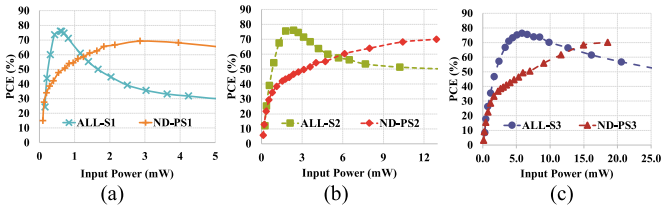

Fig. 10. Measured PCE of voltage multiplier with (a) one stage (b) two stages, and (c) three stages vs. input power at 13.56 MHz with 2 kΩ load.

minimum (in VNA ZVB4 the minimum span is 2 Hz), and the center frequency to 13.56 MHz is applied and a 2 kΩ load in parallel with 100 nF capacitor is connected to the multiplier output. Another method of applying a single-tone AC signal is increasing the step size of the frequency sweep. VNA sweeps through various frequencies step by step. The step duration can be selected long enough to get the measurement result at the frequency set. Measurements of all VMs were conducted under the same condition. The reconfiguration mechanism of the RCE, switching between ALL-S and ND-PS topologies, took place by controlling the gate biasing of transistors in the RCEs. We have externally changed the biasing of the gates on the PCB, as shown in Fig. 8b. The gates of the transistors are connected to the middle pin of the header and by changing the position of the jumper, the transistor is configured as a diode or a switch. The other reconfiguration mechanism, changing the output voltage level, took place by increasing the number of stages of the RF-to-DC converter by cascading the RCEs as demonstrated in Fig. 9a. We measured the output voltage and the PCE of the VMs with input power up to 14 dBm (25.11 mW), which is the maximum power level that VNA ZVB4 can supply.

Fig. 10 presents the measured PCE performance of VMs with one stage, two stages, and three stages, respectively, by varying input power. At low-power range, the RVMs operate with ALL-S topology, which exhibits a PCE ∼76%. Since the circuit needs higher power when N increases, the peak PCE point with the varying input power changes. As we have discussed in Section III, this high PCE is achieved because of higher overdrive voltage ($V_{GS} - V_{th}$), lower R_{on}, which in turn reduces the dissipated power in the switches. Moreover, the increased V_{sb} with the increased N does not severely affect the PCE of ALL-S topology because the common mode signal, shown in Fig. 5 as node 1 and node 2 at the gate of switches,

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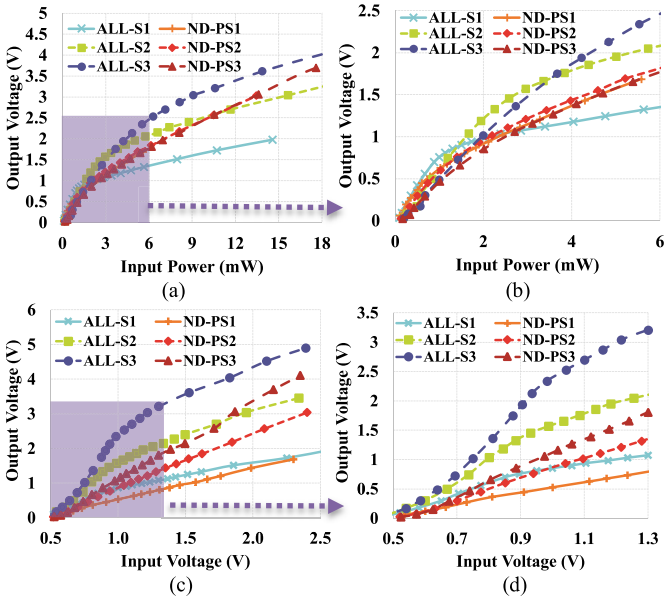

Fig. 11. Measured output DC voltage of VMs vs. (a) input power and (c) input voltage. (b) A magnified view of (a) for the low input power range. (d) A magnified view of (c) for the low input voltage range.

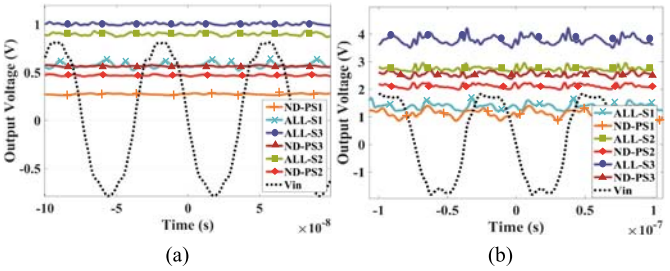

Fig. 12. The transient view of the measured output voltage of VMs with (a) 0.75 V_{peak} at 2 kΩ load and (b) 1.75 V_{peak} at 2 kΩ load.

TABLE I
COMPARISON OF PERFORMANCE PARAMETERS

	[4] 2014	[7] 2018	[8] 2017	[13] 2017	This work 2019
Peak Efficiency (%)	96.5	92.2	89-75	80.2	76
Frequency (MHz)	0.2	6.78	1.4	50	13.56
Load (Ω)	195**	500	12k**	5k	2k
Power (mW)	19.58*	14.5*	0.12**	0.9*	9-15
Structure	Cross-coupled	Active Doubler	Reconfi-gurable	Cross-couple	Reconfi-gurable
Area (mm^2)	0.49	NA	1.25	1.07	0.057
Stage Number	2	2	2-4	6	2-3
Boosting Ratio	1.982	1.72	1.84-2.35	3.99	1.47-2.05
Sim/Meas	Meas	Sim	Sim	Meas	Meas
Technology (nm)	350	350	180	130	350

Calculated from (*) resistive load and (**) loading current information.

increases with incoming power and the effective overdrive voltage still remains relatively high to support the high PCE ∼76%. As the applied input power is limited with power that VNA can provide, particularly for the three-stage VM, the measurement could not be conducted for higher power levels as in the simulation. Except for this limitation, simulations and measurements are in good agreement.

The measured output DC voltages with varying input AC power are depicted in Fig. 11. In the low power range, the ALL-S topology with single stage achieves the highest V_{OUT} until the input power is 1 mW. From this point to 3 mW the same topology with two stages has the highest V_{OUT}. The ALL-S topology with 3 stages generates the highest V_{OUT}; however, we have observed in the simulation, the output of 3-stage ND-PS exceeds the output of 3-stage ALL-S in the higher power range. Measured transient output DC voltages of voltage multiplies are presented in Fig. 12. 0.75 V_{peak} and 1.75 V_{peak} input voltages at 13.56 MHz are applied and output load is set to 2 kΩ. Measured transient values reflect a similar behavior of output voltages exhibited in Figs. 11c and 11d. Table I compares the proposed VM with those in literature. This brief presents one of the limited RVM topologies in the literature and exhibits the best boosting ratio among VMs with stage numbers higher than two.

V. CONCLUSION

We propose to use a reconfigurable rectifier as a core element in variable VM stages. Because of the reconfiguration mechanism, a high PCE is attained even with increasing number of stages at varying input power condition. The number of stages can also be changed to generate the necessary V_{OUT}. By selecting the best VM topology, the highest possible output DC voltage with the highest possible PCE can be achieved.

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