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APPROVED BY: DATE		
	SPECIFICATION	

DEVICE SPECIFICATION for

CGS Color LCD Module

(1440× RGB × 2560 dots)

Model No.

LS063R1SX01

☐ CUSTOMER'S APPROVALDATE

DATE _____

BY _____

PRESENTED BY _____

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DATE	REF.PAGE PARAGRAPH DRAWING No.	REVISED NO.	SUMMARY
27.Nov.2014			First Issue
6.Mar.2015	Page 30	A	Change the OCA's material name.(ZY404→CBS-HC01)
	Page 34		Change the Outline dimensions(change the S/N area)

SHARP	SPEC No. LCY－W14Y04A	MODEL No. LS063R1SX01	PAGE 1

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○ Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

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○ Contact and consult with a SHARP sales representative for any questions about this device.

○If operate or store the LCD module under outside of specified environmental conditions and methods. The ITO pattern corrosion, we cannot be guaranteed.

[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators
Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers
Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ Floor
Floor is an important part to leak static electricity which is generated from human body or equipment.
There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure(electrostatic earth:$1\times10^{8}\Omega$) should be made.

④Humidity
Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage
Storage materials must be anti-static to prevent causing electrostatic discharge.

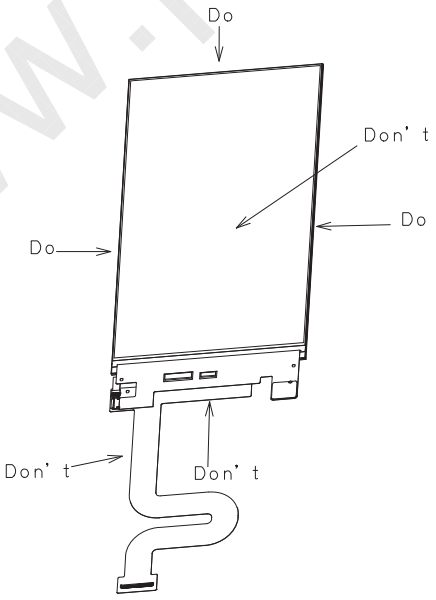
⑥Others
Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

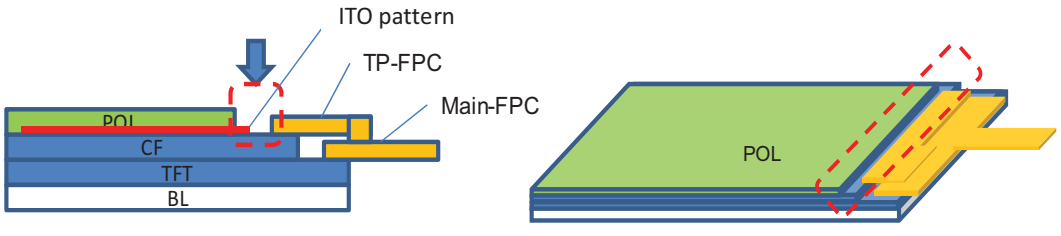
(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

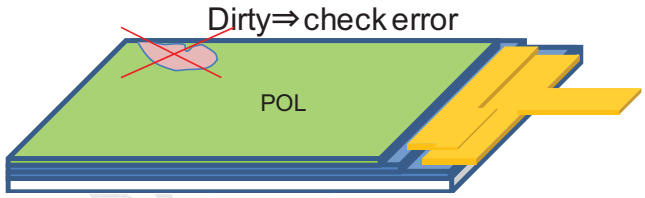
(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

(22) Do not touch or soiled the ITO pattern area. Otherwise the ITO pattern may be corrosion .



(23) After the module from the packing, please as soon as possible to assemble the CG .
Otherwise the ITO pattern may be corrosion.

(24) Do not soiled the surface of the polarizer film ,
Because the touch panel is sensitive ,the dirty on the polarizer film could occur the check error.



[For operating LCD module]

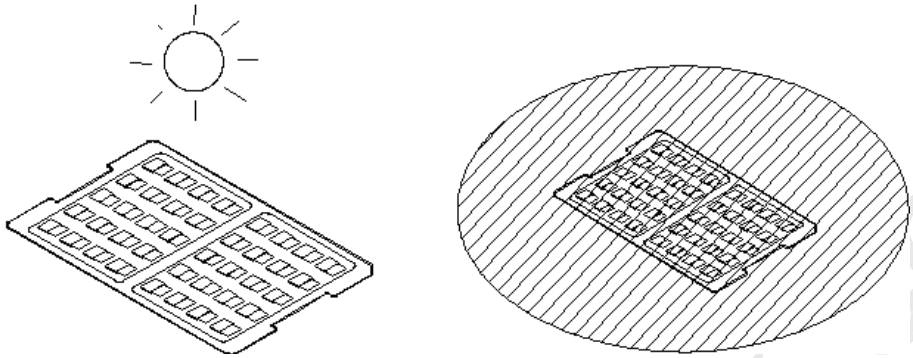
(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

[Precautions for Storage]

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C,60±10%RH) in order to avoid exposing the front

polarizer to chronic humidity.
(3) Keeping Method
a. Don't keeping under the direct sunlight. b. Keeping in the tray under the dark place.

DON'T DO



(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VDDIO-GND) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

(8) The connector used in this LCD module is the one Sharp have not ever used.
Therefore, please note that the quality of this connector concerned is out of Sharp's guarantee.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.
LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.
-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material is employed.
FPC: Dispose of as similar way to circuit board from electric device.

1. Application

This data sheet is to introduce the specification of LS063R1SX01 active matrix 16,777,216 color LCD module. Main color LCD module is controlled by Driver IC (R63419 with 1/3RAM). Capactive touch panel is controlled by Atmel controller (mXT640T).

If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.

As to basic specification of driver IC refer to the IC specification and handbook. As to basic specification of touch panel controller IC refer to the IC specification and handbook.

2. Construction and Outline

Construction: LCD panel(on-cell), Driver (COG), FPC with electric components,
16 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame and metal frame to fix them mechanically. touch panel controller FPC.

Outline: See page 34

Connection: B to B connector (HIROSE, BM14B(0.8)-60DP-0.4V,60pin, 0.4mm pitch)

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

Rejection criteria shall be noted in Inspection Standard

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.

So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

3. Mechanical Specification

Table 1

Parameter		Specifications	Unit
Outline dimensions (typ)		80.84(W)×148.92 (H)×1.475 (D)(mm)	mm
Main LCD Panel	Active area	78.84(W)×140.16(H)	mm
	Display format	1440(W)×RGB×2560(H)	-
	Dot pitch	0.01825 (W) ×0.05475 (H)	mm
	Base color *1	Normally Black	-
Mass		About 30.5	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

4. Absolute Maximum Ratings

(4-1) Electrical absolute maximum ratings

Table 2-1 LCD module Ta=25 ℃

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	IOVCC-GND	-0.3	+4.6	V	*1
	VSP-GND	-0.3	+6.5	V	*1
	VSN-GND	-6.5	+0.3	V	*1

*1: Voltage applied to GND pins.GND pin conditons are based on all the same voltage(0V).
Always connect all GND externally and use at the same voltage.

Table 2-2 Touch panel Ta=25 ℃

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	AVDD-GND	-0.3	3.6	V	*1
	VDDIN-GND	-0.3	3.6	V	*1
	VDDIO-GND	-0.3	3.6	V	*1

*1: Input terminal of logic system,SDA,SCL,INT.
Voltage value is based on GND=0V.

Environment Conditions

Table 3

Item	Top		Tstg		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-20 °C	+60°C	-30 °C	+70°C	Note 2)
Humidity	Note 1)		Note 1)		No condensation

Note1) Ta ≤ 40 °C.....90% RH Max
Note2) Ta > 40 °C.....Absolute humidity shall be less than Ta=40 °C /90 % RH.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

Be sure not to exceed the rated voltage, otherwise a malfunction may occur.

5. Electrical Specifications

(5-1) LCD Electrical characteristics

Table 4

Ta=25 ℃, GND=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable Pin
LCD Supply voltage1	IOVCC-GND	Ta=-20～60 °C	1.7	1.8	1.9	V	(note 1)
LCD Supply voltage2	VSP-GND	Ta=-20～60 °C	5.8	5.9	6.0	V	(note 1)
LCD Supply voltage3	VSN-GND	Ta=-20～60 °C	-6.0	-5.9	-5.8	V	(note 1)
"H" level input voltage	V_{IH}	Ta=-20～60 °C	0.7 IOVCC	-	IOVCC	V	(note 2)
"L" level input voltage	V_{IL}		0	-	0.3 IOVCC	V	
"H" level Input current	I_{IH}	Ta=-20～60 °C	-	-	10	μA	
"L" level Input current	I_{IL}		-10	-	-	μA	
"H" level Output voltage	V_{OH}	Ta=-20～60 °C	0.8 IOVCC	-	IOVCC	V	I_{OH}=-0.1mA
"L" level Output voltage	V_{OL}		-	-	0.2 IOVCC	V	I_{OL}=+0.1mA
MIPI high speed mode							
Common mode voltage High Speed receive mode	VCMRX(DC)	Ta=-20～60 °C	70		330	mV	(note 3)
Differential input high threshold voltage	VIDTH	Ta=-20～60 °C	-	-	70	mV	(Note 3)
Differential input low threshold voltage	VIDTL	Ta=-20～60 °C	-70	-	-	mV	(Note 3)
Single-ended input high voltage	VIHHS	Ta=-20～60 °C	-	-	460	mV	(Note 3)
Single-ended input low voltage	VILHS	Ta=-20～60 °C	-40	-	-	mV	(Note 3)
MIPI LP mode							
Logic High level input voltage	VIH	Ta=-20～60 °C	880		1350	mV	(Note 3)
Logic Low level input voltage	VIL	Ta=-20～60 °C	-50		550	mV	(Note 3)
Logic High level output voltage	VOH	Ta=-20～60 °C	1.1	1.2	1.3	V	(Note 3)
Logic Low level output voltage	VOL	Ta=-20～60 °C	-50		50	mV	(Note 3)
Logic 0 contention threshold	VILCD	Ta=-20～60 °C	-	-	200	mV	(Note 3)
Logic 1 contention threshold	VIHCD	Ta=-20～60 °C	450	-	-	mV	(Note 3)
LCD Current consumption	Iiovcc1	Ta=25 °C	-	24.33	30.34	mA	(note 4)
	Ivsp1	Ta=25 °C	-	22.22	29.47	mA	(note 4)
	Ivsn1	Ta=25 °C	-	17.29	22.94	mA	(note 4)
	Iiovcc1	Ta=25 °C	-	0.005	0.02	mA	(note 5)
	Ivsp1	Ta=25 °C	-	0.005	0.02	mA	(note 5)
	Ivsn1	Ta=25 °C	-	0.005	0.02	mA	(note 5)

(Note 1) Include Ripple Noise

(Note 2) Applied overshoot

(Note 3) VCMRX(DC)=(VP+VDN)/2;
Minimum 110mV/-110mV HS differential swing is required for display data transfer.

(Note 4) Measurement conditions: Ta=25℃Full screen white pattern, VSP=5.9V/VSN=-5.9V/IOVCC=1.8V, 60HZ Refresh MIPI-DSI Video bypass mode.

(Note5) Measurement conditions: Deep standby mode.

(5-2) TP Electrical characteristics

Table 5

Ta=25 ℃, GND=0V

TP Supply voltage1	VDDH_3.3V-GND	Ta=-20～60 °C	3.1	3.3	3.47	V	(note 1)
TP Supply voltage2	VDD_3.3V-GND	Ta=-20～60 °C	3.1	3.3	3.47	V	(note 1)

(Note 1) Include Ripple Noise

(5-3) LED back light

(1) The back light uses 8*2pcs edge light type white LED.

Table 6

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward current	Ta=25 °C	I_{LED}	-	20*1	-	mA	LED1+/LED1- LED2+/LED2-

LED lamp: SHARP

*1 per one piece of LED

*Please consider Allowable Forward Current on used temperature
(refer to Ambient Temperature vs. Allowable Forward Current curve)

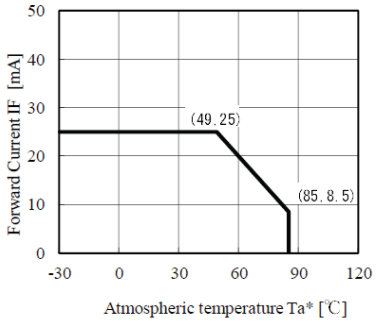


Fig.1 LED Characteristic(De-rating Curve)

(Ta*＝25℃)

Parameter	Symbol	Rating	Unit
Power dissipation	P	77.5	mW
Forward current	I_F	25	mA
Peak pulsed forward current(*1)	I_{FM}	50	mA
Forward current derating factor	DC	-0.46	mA/℃
	Pulse	-0.67	mA/℃
Reverse voltage	V_R	5	V
Operating temperature(*3)	Topr	-30 to +85	°C
Storage temperature	T_{stg}	-40 to +90	°C

(Ta*＝25℃)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Forward Voltage	V_F	I_F=20 mA	-	2.9	3.1	V
Luminous flux (*4)	Φv		6.10	6.7	-	lm
Chromaticity coordinates(*5)	x1		0. 26	0.273	0. 286	-
	y1		0. 24	0.253	0. 266	

(5-4) Interface signals

Table 7-1 LCD module Interface layout

Pin No	Symbol	Description	I/O	Remarks
1	DSIB_D3_N	MIPI DSI (-) of Port B	I	
2	DSIB_D3_P	MIPI DSI (+) of Port B	I	
3	GND	Ground	-	
4.	DSIB_D0_N	MIPI DSI (-) of Port B	I/O	
5	DSIB_D0_P	MIPI DSI (+) of Port B	I/O	
6	GND	Ground	-	
7	DSIB_CLK_N	MIPI DSI clock (-) of Port B	I	
8	DSIB_CLK_P	MIPI DSI clock (+) of Port B	I	
9	GND	Ground	-	
10	DSIB_D1_N	MIPI DSI (-) of Port B	I	
11	DSIB_D1_P	MIPI DSI (+) of Port B	I	
12	GND	Ground	-	
13	DSIB_D2_N	MIPI DSI (-) of Port B	I	
14	DSIB_D2_P	MIPI DSI (+) of Port B	I	
15	GND	Ground	-	
16	DSIA_D2_P	MIPI DSI (+) of Port A	I	
17	DSIA_D2_N	MIPI DSI (-) of Port A	I	
18	GND	Ground	-	
19	DSIA_D1_P	MIPI DSI (+) of Port A	I	
20	DSIA_D1_N	MIPI DSI (-) of Port A	I	
21	GND	Ground	-	
22	DSIA_CLK_P	MIPI DSI clock (+) of Port A	I	
23	DSIA_CLK_N	MIPI DSI clock(-) of Port A	I	
24	GND	Ground	-	
25	DSIA_D0_P	MIPI DSI (+) of Port A	I/O	
26	DSIA_D0_N	MIPI DSI (-) of Port A	I/O	
27	GND	Ground	-	
28	DSIA_D3_P	MIPI DSI (+) of Port A	I	
29	DSIA_D3_N	MIPI DSI (-) of Port A	I	
30	GND	Ground	-	
31	GND	Ground	-	
32	LED2-	LED back light power group2 negative	I	
33	LED1-	LED back light power group1 negative	I	
34	LED2+	LED back light power group2 positive	I	
35	LED1+	LED back light power group1 positive	I	
36	GND	Ground	-	
37	VDDH_3.3V	Power Input（3.3v）for TP	I	
38	GND	Ground	-	
39	/RST	Reset pin for TP	I	
40	INT	State change interrupt-TP	OD	
41	GND	Ground	-	
42	SDA	Serial interface data-TP	OD	
43	SCL	Serial interface dock-TP	OD	
44	GND	Ground	-	
45	VBUS	Power input-TP	I	
46	VDD_3.3V	Power input（3.3v）-TP	I	
47	GND	Ground	-	
48	XRES	Device reset signal	I	
49	PWM	Backlight LED driver PWM	O	
50	GND	Ground	-	
51	*HSYNC*	*Horizontal Synchronizing signal*	*O*	
52	TE	Tearing signal output from driver IC	O	

53	GND	Ground	-	
54	VDDIO	Power supply for I/O	-	
55	AVDD-	Power supply for source negative	-	
56	AVDD+	Power supply for source positive	-	
57	NC	NC	-	
58	CTSI/ID0	ID(connect to GND in FPC)		
59	CTSI/ID1	ID(connect to GND in FPC)		
60	GND	Ground	-	

Mounted connector : 60pins; 0.4mm pitch; B to B connector. (HIROSE- BM14B(0.8)-60DP-0.4V)

Corresponded connector : 60pins; 0.4mm pitch; B to B connector. (HIROSE- BM14B(0.8)-60DS-0.4V)

Signals connect to LCD module. Symbols correspond able to Circuit diagram in Page 12.

Table 7-2 Touch Panel Interface layout

Pin No	Symbol	Description	I/O	Remarks
1	GND	Ground	-	
2	VDDH_3.3V(AVDD)	Power Input（3.3v）for TP(AVDD)	I	
3	GND	Ground	-	
4	/RST	Reset pin for TP	I	
5	INT	State change interrupt-TP	OD	
6	GND	Ground	-	
7	SDA	Serial interface data-TP	I/O	
8	SCL	Serial interface dock-TP	OD	
9	GND	Ground	-	
10	VBUS(VDDIO)	Power input-TP(VDDIO)	I	
11	VDD_3.3V(VDDIN)	Power input（3.3v）-TP(VDDIN)	I	

Mounted connector : 11pins; 0.6mm pitch; ZIF connector. (HIROSE- FH42-11S-0.3SHW)

Signals connect to TP module. Symbols correspond able to Circuit diagram in Page 13.

(5-5) Schematic of LCD module system

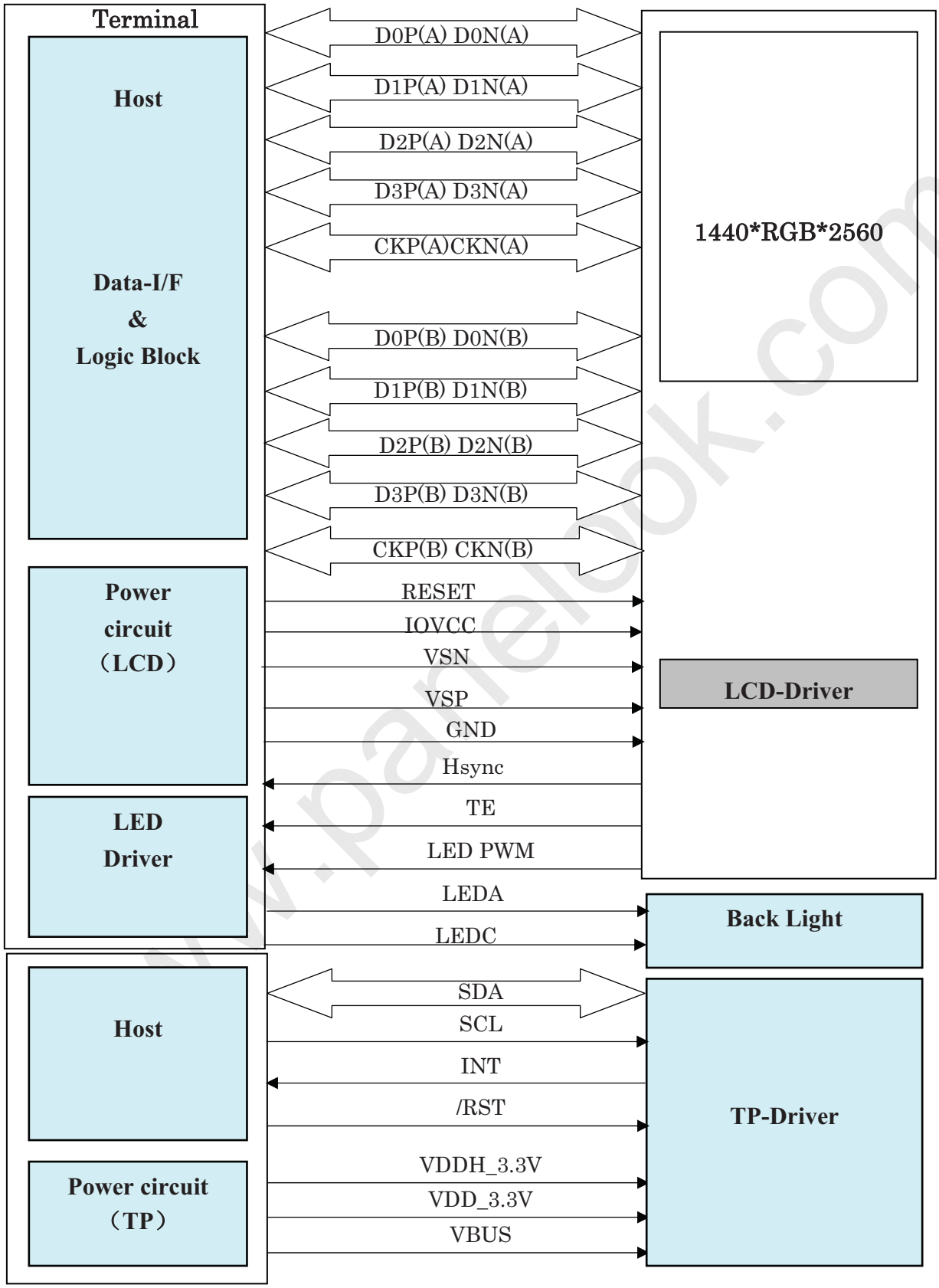


Fig.2 Schematic of LCD module system

(5-6-1) Circuit Diagrams

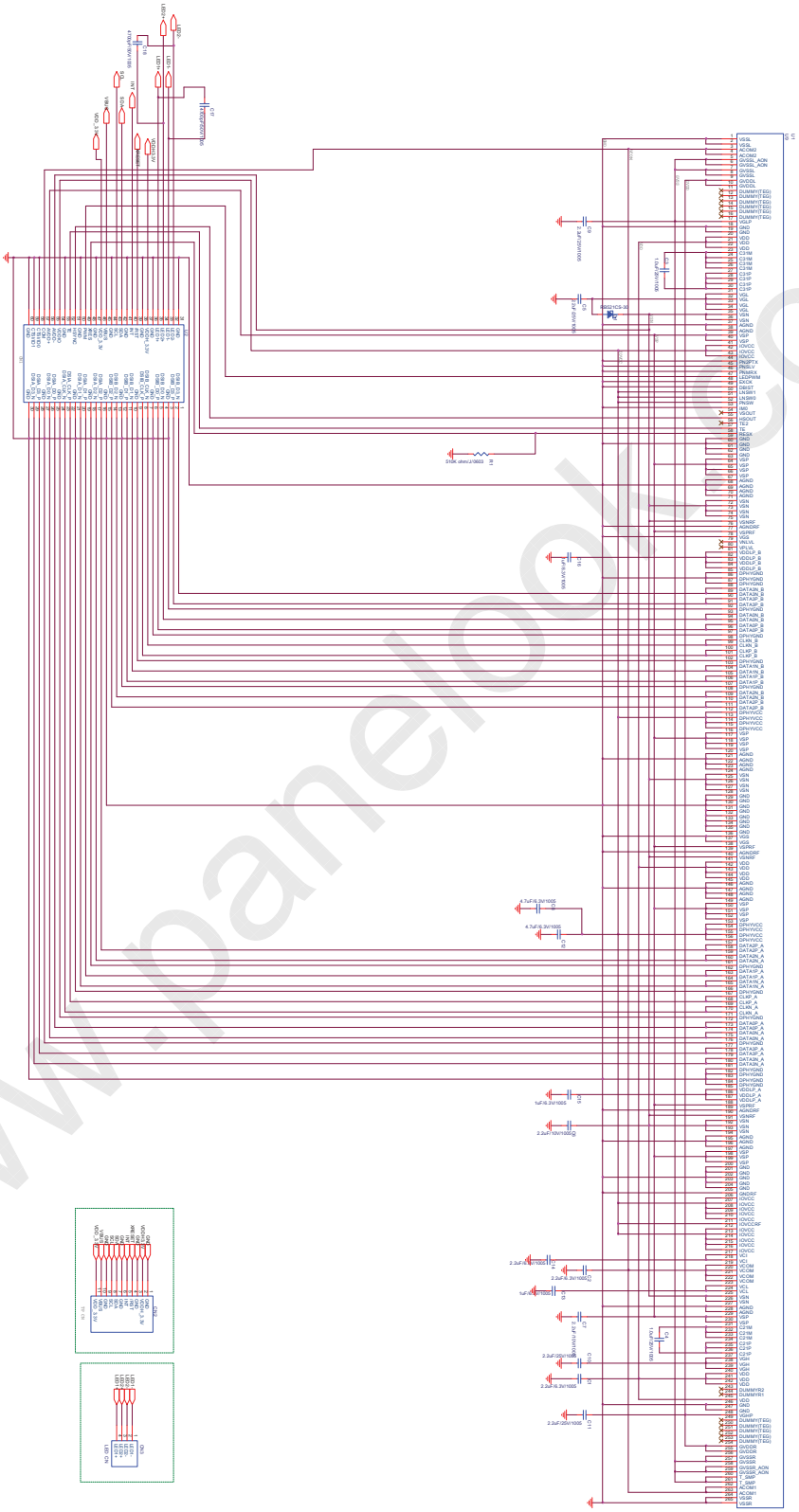


Fig.3 Main-FPC Circuit diagram

(5-6-2) Circuit Diagrams

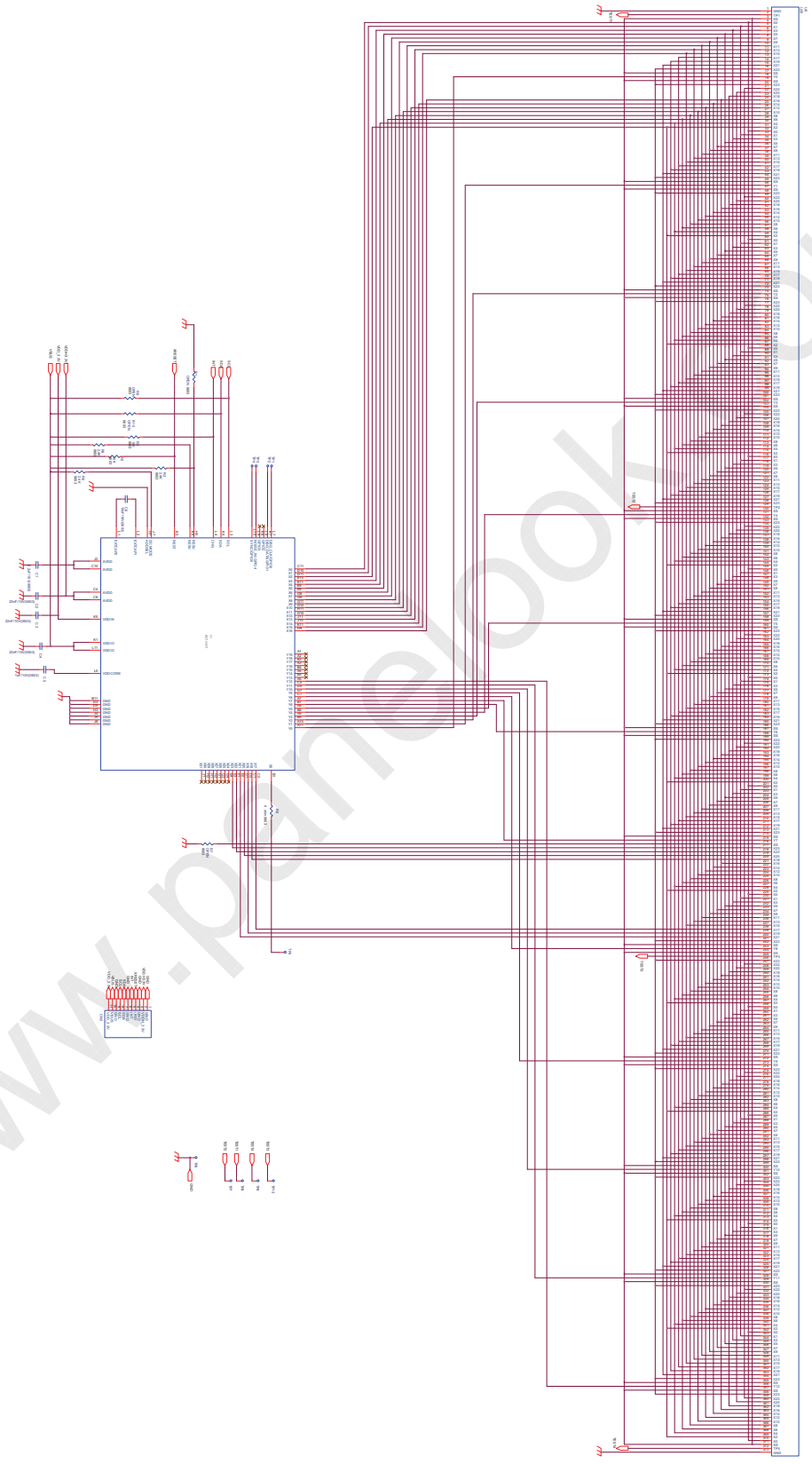


Fig.4 TP-FPC Circuit diagram

(5-7-1) Parts List

Table 8 Main-FPC

Category	Ref. No.	Spec			Vendor
Capacitor	C1	2.2uF	6.3V	1005	Multi Vendor
	C2	2.2uF	6.3V	1005	Multi Vendor
	C3	1.0uF	25V	1005	Multi Vendor
	C4	1.0uF	25V	1005	Multi Vendor
	C5	2.2uF	25V	1005	Multi Vendor
	C6	2.2uF	10V	1005	Multi Vendor
	C7	2.2uF	10V	1005	Multi Vendor
	C8	4.7uF	6.3V	1005	Multi Vendor
	C9	2.2uF	25V	1005	Multi Vendor
	C10	2.2uF	25V	1005	Multi Vendor
	C11	2.2uF	25V	1005	Multi Vendor
	C12	4.7uF	6.3V	1005	Multi Vendor
	C13	1uF	6.3V	1005	TAIYO YUDEN
	C14	2.2uF	6.3V	1005	TAIYO YUDEN
	C15	1uF	6.3V	1005	Multi Vendor
	C16	1uF	6.3V	1005	Multi Vendor
	C17	4700pF	50V	1005	Multi Vendor
	C18	4700pF	50V	1005	Multi Vendor
Resistor	R1	510kΩ/J		0603	ROHM
Diode	D1	VF<0.4V VR≧max.25V		1006	ROHM
Connector	CN1	1.0mm(max) BtoB 60pin			HIROSE
	CN2	0.8mm(max) ZIF 11pin			HIROSE
	CN3	0.75mm(max) ZIF 4pin			KYOSERA

(5-7-2) Parts List

Table 9 TP-FPC

Category	Ref. No.	Spec			Vendor
Capacitor	C1	2.2uF	10V	0603	Multi Vendor
	C2	22nF	10V	0603	Multi Vendor
	C3	22nF	10V	0603	Multi Vendor
	C4	22nF	10V	0603	Multi Vendor
	C5	1uF	10V	0603	Multi Vendor
	C6	10nF	16V	0603	Multi Vendor
Resistor	R2	2.4kΩ/J		0603	Multi Vendor
	R3	10kΩ/J		0603	Multi Vendor
	R4	2.4kΩ/J		0603	Multi Vendor
	R5	10kΩ/J		0603	Multi Vendor
	R6	2.4kΩ/J		0603	Multi Vendor
	R8	0Ω/J		0603	Multi Vendor
LSI	LSI	0.6mm(max) ATmXT640T-CCU			ATMEL

6. Timing characteristics of input signals

(6-1)LCD MIPI DC/AC Characteristics

<DC characteristics>

Table 10 Ta=+25°C, GND=0V

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVDD= 1.65V~3.30V	-	-	70	2
	Differential input low threshold	VIDTL	mV	IOVDD= 1.65V~3.30V	-70	-	-	2
	Single-ended input low voltage	VILHS	mV	IOVDD= 1.65V~3.30V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVDD= 1.65V~3.30V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVDD= 1.65V~3.30V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVDD= 1.65V~3.30V	-	100	-	
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVDD= 1.65V~3.30V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVDD= 1.65V~3.30V	880	-	1350	
	I/O leakage current	ILEAK	μA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVDD= 1.65V~3.30V	-50	-	50	
	Thevenin output high level	VOH	V	IOVDD= 1.65V~3.30V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVDD=1.80V	110	-	-	
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVDD= 1.65V~3.30V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVDD= 1.65V~3.30V	450	-	-	

Notes: 1. VCMRX (DC) = (VP+VDN)/2

2. Minimum 110mV/-110mV HS differential swing is required for display data transfer.

<AC Characteristics>

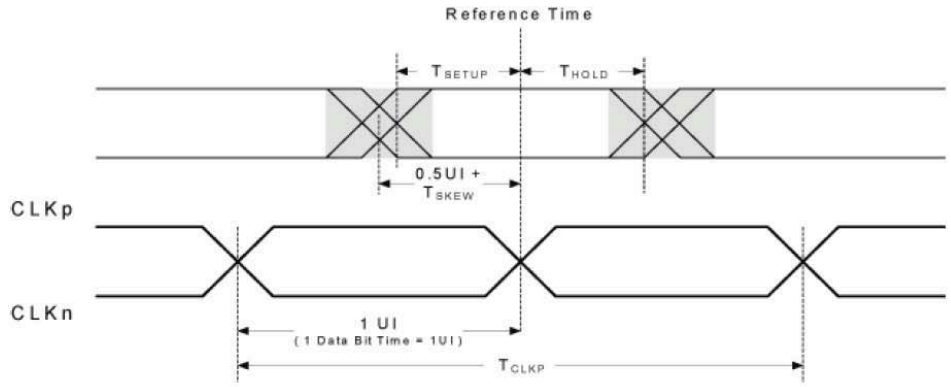
Table 11 Ta=+25°C, GND=0V

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	100	-	500	1
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	1	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V DSI 2 lanes, 3 lanes,4lane	200	-	1000	1
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	3
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	2 ,3
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	3
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	2,3

Notes: 1. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.

2. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.

3. tSETUP/tHOLD Time are measured without HS-TX Jitter.



(6-2) LCD Reset Timing Characteristics

Table 12 Ta=+25°C, GND=0V

Item	Symbol	Unit	Test condition	Min.	Max.
Reset low-level width1	tRW1	us	Power supply on	1000	–
Reset low-level width2	tRW2	us	Operation	1000	–
Reset time (Sleep IN)	tRT1	ms	–	–	3
Reset time (Sleep OUT)	tRT2	ms	–	–	3
Noise reject width	tRESNR	us	–	–	1

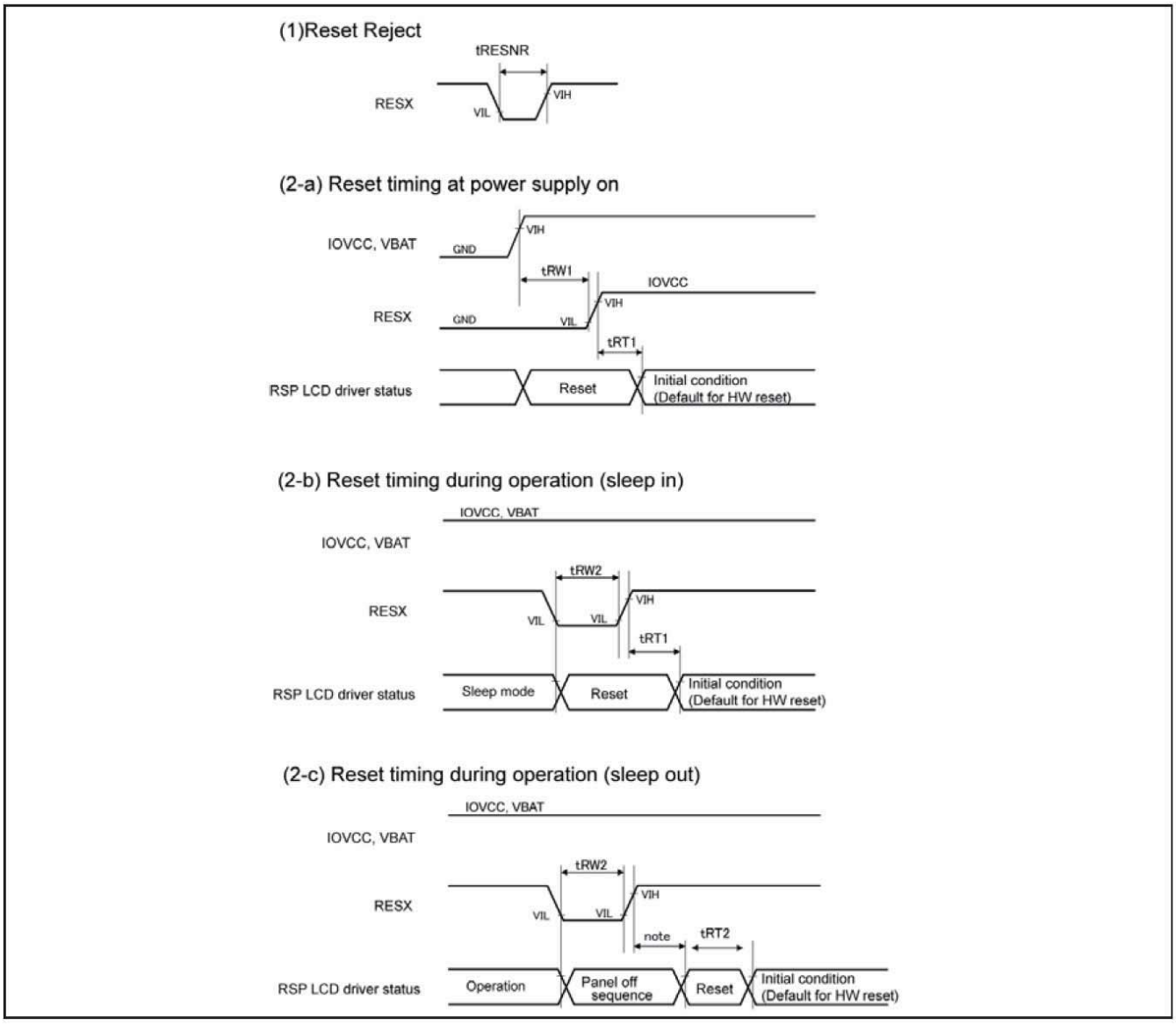


Fig .5 Reset timing characteristics

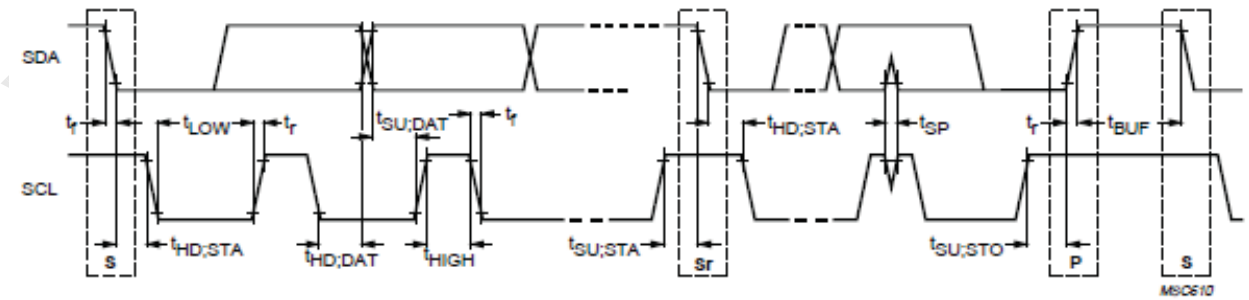
(6-3)Touch Panel Interface Timing Chart

Table 13

Ta=+25°C, GND=0V

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
LOW level input voltage: fixed input levels V_{DD}-related input levels	V_{IL}	 −0.5 −0.5	 1.5 $0.3V_{DD}$	 n/a −0.5	 n/a $0.3V_{DD}$ (1)	 V V
HIGH level input voltage: fixed input levels V_{DD}-related input levels	V_{IH}	 3.0 $0.7V_{DD}$	 (2) (2)	 n/a $0.7V_{DD}$(1)	 n/a (2)	 V V
Hysteresis of Schmitt trigger inputs: V_{DD} > 2 V V_{DD} < 2 V	V_{hys}	 n/a n/a	 n/a n/a	 $0.05V_{DD}$ $0.1V_{DD}$	 – –	 V V
LOW level output voltage (open drain or open collector) at 3 mA sink current: V_{DD} > 2 V V_{DD} < 2 V	 V_{OL1} V_{OL3}	 0 n/a	 0.4 n/a	 0 0	 0.4 $0.2V_{DD}$	 V V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	t_{of}	–	250(4)	$20 + 0.1C_b$(3)	250(4)	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	n/a	n/a	0	50	ns
Input current each I/O pin with an input voltage between $0.1V_{DD}$ and $0.9V_{DDmax}$	I_i	−10	10	−10(5)	10(5)	µA
Capacitance for each I/O pin	C_i	–	10	–	10	pF

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V



Required pull-up resistance for standard mode (100 kHz)	1 kΩ to 10 kΩ (1)
Required pull-up resistance for fast mode (400 kHz)	1 kΩ to 3 kΩ (1)

Notes: 1. The values of pull-up resistors should be chosen to ensure SCL and SDA rise and fall times meet the I²C specification. The value required will depend on the amount of stray capacitance on the line.

7. Mipi Video Mode Setting
(7-1) General Timing Diagram

1) Display Timing (Video Mode)

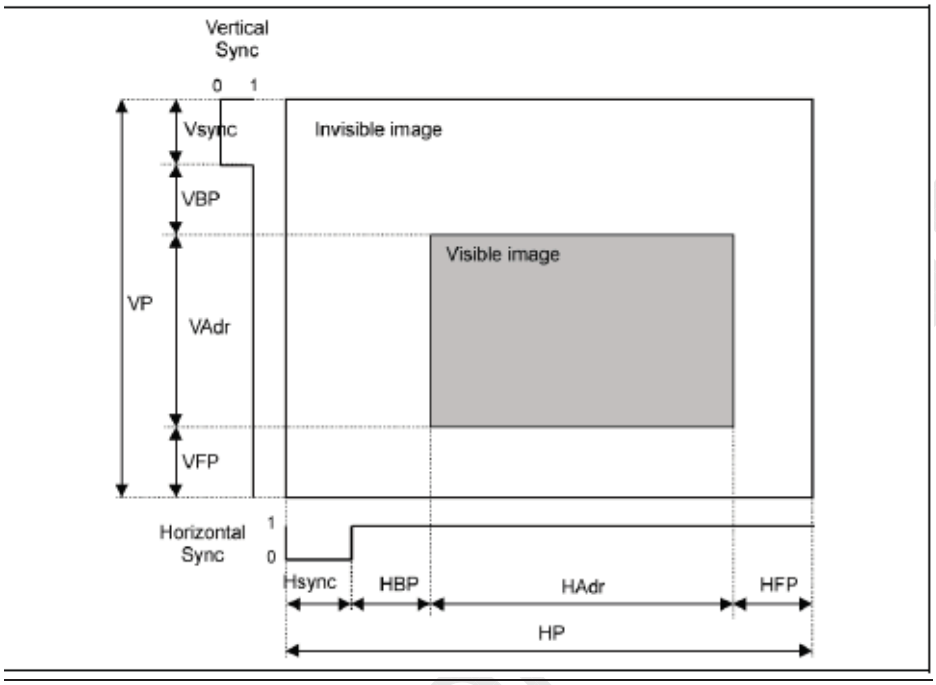


Fig .6

(7-2) Vertical Timing

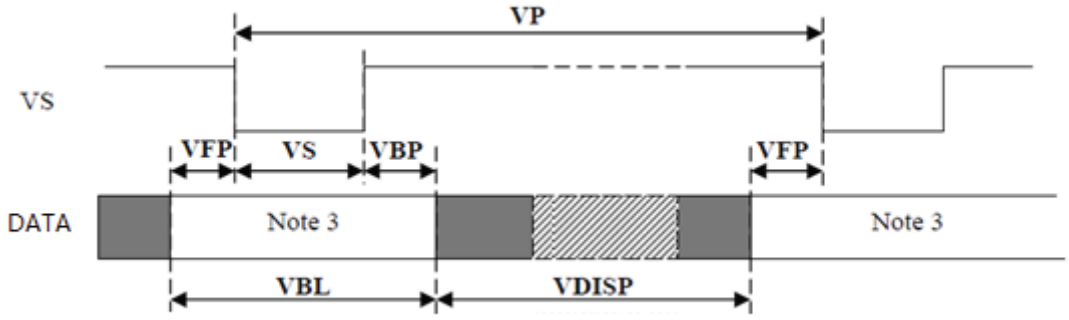


Fig .7

Table 14

Ta = -20 °C ~ +60°C, VDDIO= 1.8 V, VSP=5.9V, VSN=-5.9V, GND = 0 V

Item	Symbol	Conditions	Min	Recommend	Max	Unit
Vertical cycle	VP		-	2568	-	Line
Vertical low pulse width	VS		1	2	-	Line
Vertical front porch	VFP		2	4	-	Line
Vertical back porch	VBP		2	2	-	Line
Vertical data start point		VS+VBP	4	4	-	Line
Vertical blanking period	VBL	VFP+VS+VBP	6	8	-	Line
Vertical active area		VDISP	-	2560	-	Line
Vertical Refresh Rate	VRR		57	60	63	Hz

(7-3) Horizontal Timing

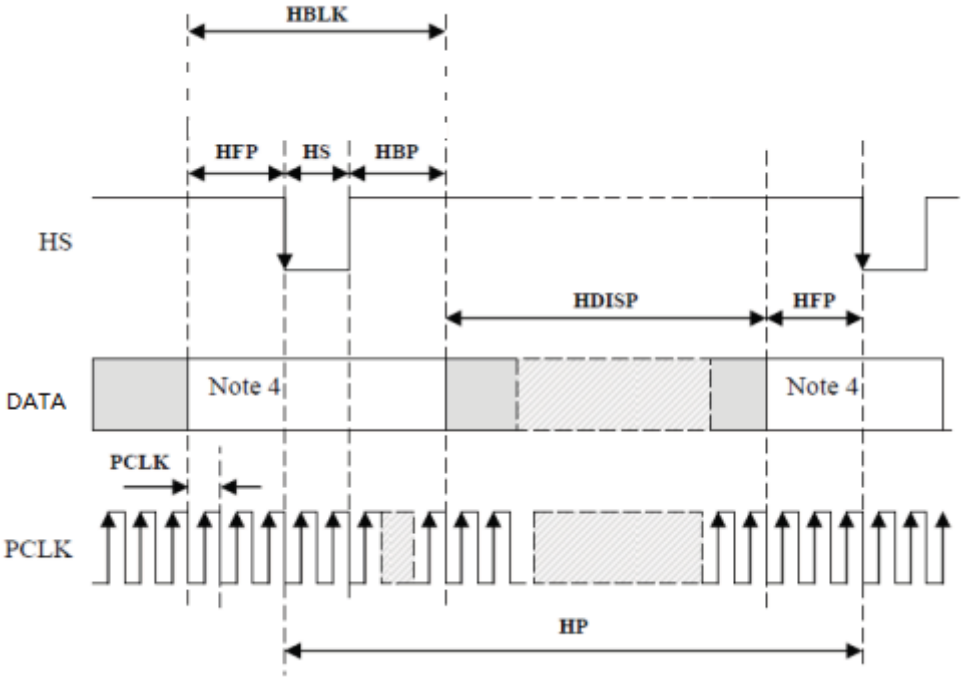


Fig .8

Table 15

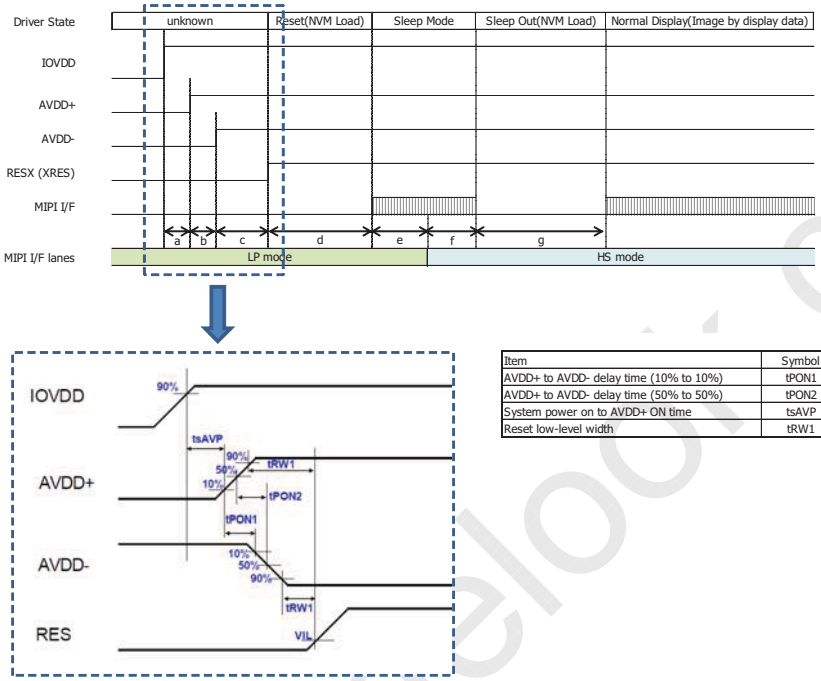
Ta = -20 °C ~ +60°C, VDDIO= 1.8 V, VSP=5.9V, VSN=-5.9V, GND = 0 V

Item	Symbol	Conditions	Min	Recommend	Max	Unit
HS cycle	HP		-	1688	-	PCLK
HS low Pulse width	HS		-	20	-	PCLK
Horizontal back porch	HBP		-	80	-	PCLK
Horizontal front porch	HFP		-	148	-	PCLK
Horizontal data start point		HS+HBP	-	100	-	PCLK
Horizontal blanking period	HBLK	HFP+HS+HBP	-	248	-	PCLK
orizontal active area	HDISP		-	1440	-	PCLK
1 Horizontal timing			6.472	6.472	-	us
Pixel clock frequency	PCLK		-	3.8	-	ns
			-	260.8	-	MHz
MIPI Speed(4 lane)*2ports	-	-	780	-	1000	Mbps/lane

8. Initial Sequence

(8-1) LCD Power On Sequence

I/F: MIPI 4lane*2ports
Panel Size : WQHD (1440xRGBx2560)
VSP=5.9,VSN-=-5.9V, VDDIO=1.8V
Color Mode:24bit
Frame frequency:60Hz



Item	Symbol	min
AVDD+ to AVDD- delay time (10% to 10%)	tPON1	0ms
AVDD+ to AVDD- delay time (50% to 50%)	tPON2	0ms
System power on to AVDD+ ON time	tsAVP	1ms
Reset low-level width	tRW1	1ms

Fig .9

Table 16

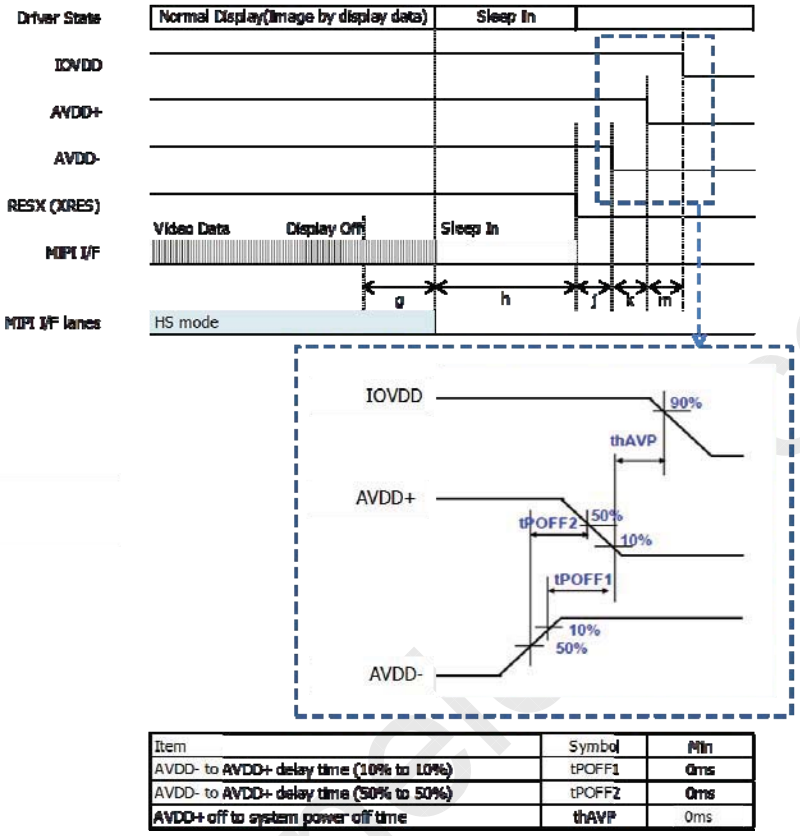
	State	Action/Command	DSI Data Type		Adress	Para.	Data	Note
1		RESX = L						
2		Power Supply IOVDD ON (Typ1.8V)						
3		- Wait Min. 200ms						Wait to IOVDD=90% (depends on Power Supply Circuit)
4		Power Supply AVDD+ ON (Typ5.9V)						
5		- Wait 20ms						Wait for VSP->VSN ordering (depends on Power Supply Circuit)
6		Power Supply AVDD- ON (Typ-5.9V)						
7		- Wait 20 ms						
8		RESX = L						
9		- Wait Min. 10ms						Wait to VSP/VSN=±90% and RESX=Low period (depends on Power Supply Circuit)
10		RESX = H						
11		- Wait MIN 10ms						
12	NVM Auto Load							
13	Sleep Mode On							
14		Manufacture Command Access Protect	Generic	29h	B0h	P1	04h	Unlock manufacturing command write (CE etc.)
15		NVM Load setting	Generic	29h	D6h	P1	01h	The command to remove NVM reload after sleep out
16		Set Mipi display mode	Generic	29h	B3h	P1	08h	Set Mipi display mode 0x08(command mode enable) 0x18(video RAM bypass mode enable)
17	(note1)	set column address	DCS	39h	2Ah	P1	00h	0x00/00h : Start Column Address = 0
						P2	00h	
						P3	05h	0x05/9Fh : End Column Address = 1439
						P4	9Fh	
18		If customer need, please add initial command in here						
19		Manufacture Command Access Protect	Generic	29h	B0h	P1	03h	Lock manufacturing command write
20	(note2)	**DSI signal transfer Start**						
21		Exit_sleep_mode	DCS	39h	11h	-	-	
22	Sleep Mode exit	- Wait 200ms						After Wait Min. 6 frame, automaticaly sleep mode off.
23		Write_Display_Brightness	DCS	39h	51h	P1	FFh	0xFFh : LED 100% Duty
24		Write_CTRL_Display	DCS	39h	53h	P1	0Ch	0x0Ch : LED ON(BL=1h), Dimming ON(DD=2h)
25	Display on	Set_display_on	DCS	39h	29h	-	-	
26		Send Picture image						Image write

NOTE1: STEP17 can be deleted if video mode is used.

NOTE2: The above Sequence applies on the premise of MIPI command mode.

If MIPI Video has been used, please set step20.

(8-2)LCD Power Off sequence



Item	Symbol	Min
AVDD- to AVDD+ delay time (10% to 10%)	tPOFF1	0ms
AVDD- to AVDD+ delay time (50% to 50%)	tPOFF2	0ms
AVDD+ off to system power off time	thAVP	0ms

Fig .10

Table 17

Step	State	Action/Command	DSI Data Type		Adress	Para.	Data	Note
1	Backlight OFF	Backlight OFF	DCS	39h	53h	P1	00h	LED OFF
2	Display OFF	set_display_off	DCS	39h	28h	-	-	
3		- Wait Min. 20ms						
4		enter_sleep_mode	DCS	39h	10h	-	-	
5	Sleep Mode On	- Wait Min. 120ms						
6	note 3	**DSI signal transfer stop**						
7		RESX=L						
8		- Wait 10ms						
9		Power Supply AVDD- OFF (GND=0V)						
10		- Wait 20ms						Wait for VSN->VSP ordering (depends on Power Supply Circuit)
11		Power Supply AVDD+ OFF (GND=0V)						
12		- Wait 20ms						Wait to VSP=10%, VSN=10% (depends on Power Supply Circuit)
13		Power Supply IOVDD OFF (GND=0V)						
14	Power OFF	- Wait 20ms						Wait to IOVDD OFF stable

NOTE3：STEP6　can be deleted if command mode is used.

(8-3)Deep standby IN Sequence

Table 18

Step	State	Action/Command	DSI Data Type		Adress	Para.	Data	Note
1	Backlight OFF	Backlight OFF	DCS	39h	53h	P1	00h	LED OFF
2	Display OFF	set_display_off	DCS	39h	28h	-	-	
3		- Wait Min. 20ms						
4		enter_sleep_mode	DCS	39h	10h	-	-	
5	Sleep Mode On	- Wait Min. 120ms						
6	note4	**DSI signal transfer stop**						
7		Manufacture Command Access Protect	Generic	29h	B0h	P1	04h	Unlock manufacturing command write
8			Generic	29h	B1h	P1	01h	Low power mode
9		Power Supply AVDD- OFF (GND=0V)						
10		- Wait 20ms						
11		Power Supply AVDD+ OFF (GND=0V)						
12	Deeptandby mode IN	- Wait 20ms						

NOTE4：STEP6 can be deleted if command mode is used.

(8-4)Deep standby OUT Sequence

Table 19

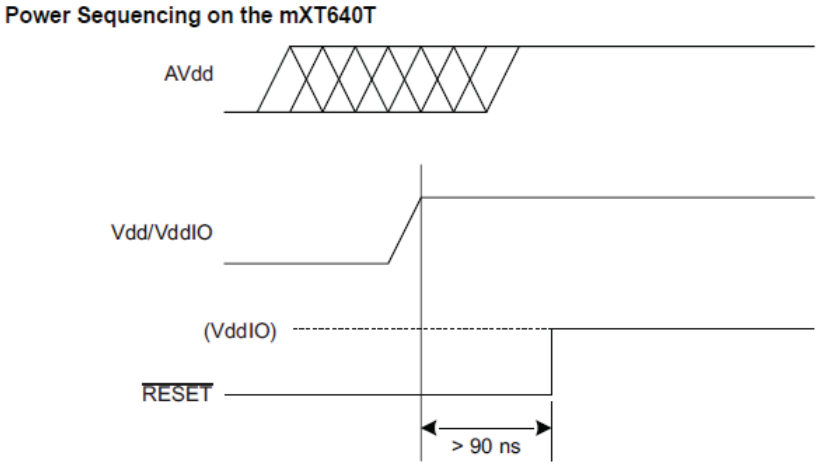
	State	Action/Command	DSI Data Type		Adress	Para.	Data	Note
1		RESX = L						
2		Power Supply AVDD+ ON (Typ5.9V)						
3		- Wait 20ms						Wait for VSP->VSN ordering (depends on Power Supply Circuit)
4		Power Supply AVDD- ON (Typ-5.9V)						
5		- Wait 20 ms						
6		RESX = L						
7		- Wait Min. 10ms						Wait to VSP/VSN=±90% and RESX=Low period (depends on Power Supply Circuit)
8		RESX = H						
9		- Wait MIN 10ms						
10	NVM Auto Load							
11	Sleep Mode On							
12		Manufacture Command Access Protect	Generic	29h	B0h	P1	04h	Unlock manufacturing command write (CE etc.)
13		NVM Load setting	Generic	29h	D6h	P1	01h	The command to remove NVM reload after sleep out
14		Set Mipi display mode	Generic	29h	B3h	P1	08h	Set Mipi display mode 0x08(command mode enable) 0x18(video RAM bypass mode enable)
15	(note4)	set column address	DCS	39h	2Ah	P1	00h	0x00/00h : Start Column Address = 0
						P2	00h	
						P3	05h	0x05/9Fh : End Column Address = 1439
						P4	9Fh	
16		If customer need, please add initial command in here						
17		Manufacture Command Access Protect	Generic	29h	B0h	P1	03h	Lock manufacturing command write
18	(note5)	**DSI signal transfer Start**						
19		Exit_sleep_mode	DCS	39h	11h	-	-	
20	Sleep Mode exit	- Wait 200ms						After Wait Min. 6 frame, automaticaly sleep mode off.
21		Write_Display_Brightness	DCS	39h	51h	P1	FFh	0xFFh : LED 100% Duty
22		Write_CTRL_Display	DCS	39h	53h	P1	0Ch	0x0Ch : LED ON(BL=1h), Dimming ON(DD=2h)
23	Display on	Set_display_on	DCS	39h	29h	-	-	
24	Deepstandby mode out	Send Picture image						Image write

NOTE5: STEP15 can be deleted if video mode is used.

NOTE6: The above Sequence applies on the premise of MIPI command mode.

If MIPI Video has been used, please set step18.

(8-5)Touch Panel Power ON Sequence



Note: Vdd/VddIO and AVdd can be powered up in any order

Fig .11

Touch Panel Power OFF Sequence
Power Off can be setted freely.

9. Optical Characteristics

Table 20

Vddio=1.8V, VSP=5.9V, VSN=-5.9V, ILED=20mA/pcs, Ta = 25℃

Optical Characteristics							
Parameter	symbol	condition	MIN	TYP	MAX	unit	Remark
Brightness	Br	θ=0°	300	400	-	cd/㎡	Note1,2
Contrast	Co	θ=0°	910	1300	-		Note1,3
Viewing Angle	θ11	Co > 10	80	-	-	deg	Note1
	θ12		80	-	-		
	θ21		80	-	-		
	θ22		80	-	-		
White chromaticity	x	θ=0°	0.27	0.30	0.33		Note.1,3
	y		0.29	0.32	0.35		
Uniformity	-	θ=0°	80	85	-	%	Note.5
NTSC ratio	-	θ=0°	-	90	-	%	Note.1,3
Response Time	(τr+td)	θ=0°	-	35	-	ms	Note1,6
Flicker ratio	-	θ=0°	-	-	10	%	Note.4

Note 1) Definition of range of visual angle

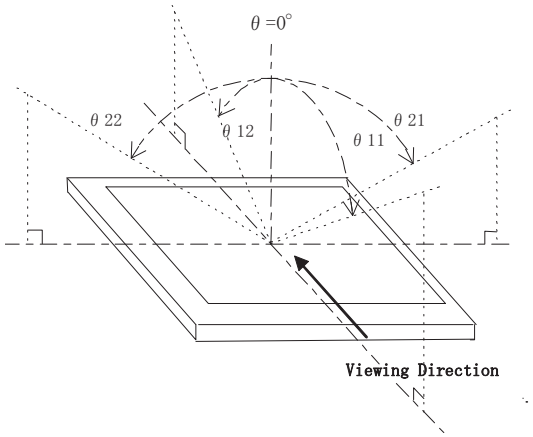


Fig .12 Definition of viewing angle

Note 2) Brightness is measured as shown in Fig.13, and is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

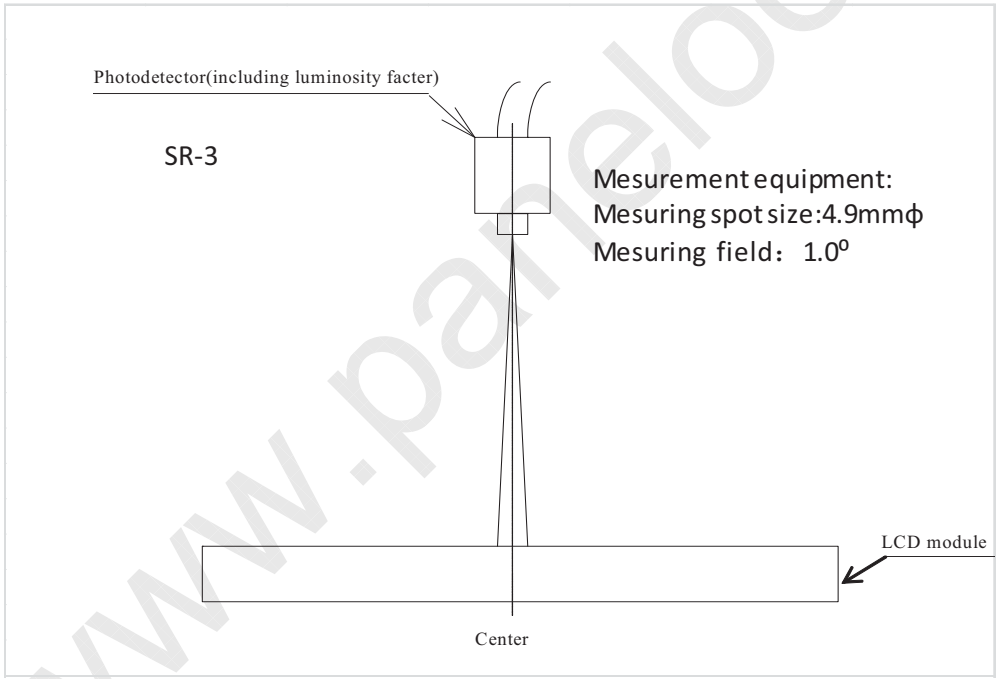


Fig. 13 Optical characteristics Test Method (Brightness)

Note 3) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixcels "White"}}{\text{Luminance(brightness) all pixcels "Black"}}$$

Note 4) Measuring systems: YOKOGAWA 3298_01 + 3298_11

- ·Temperature = 25℃(±3℃), Frame Frequency = 53Hz~62Hz, LED back-light: ON, Environment brightness < 300 lx
- ·Measured sample : New sample before a long term aging.
- ·Flicker ratio is very sensitive to measuring condition.
- ·Measuring pattern Please refer to figure below.

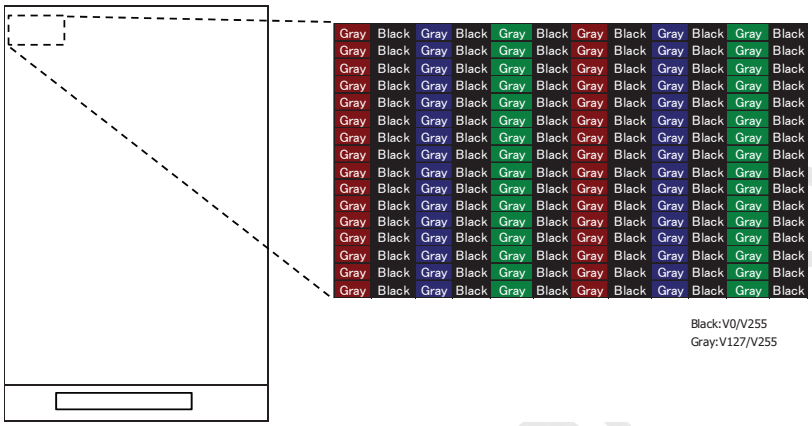


Fig. 14 Flicker Measuring pattern

Note 5) Uniformity is defined as follows:

$$\text{Uniformity} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

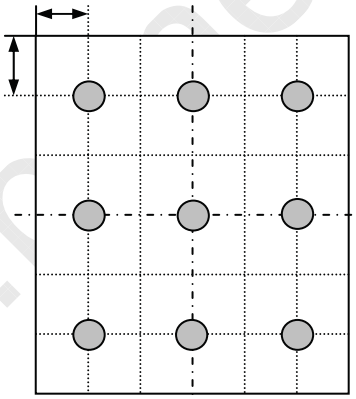


Fig. 15 Measuring Point

Note 6) Response time is defined as follows:

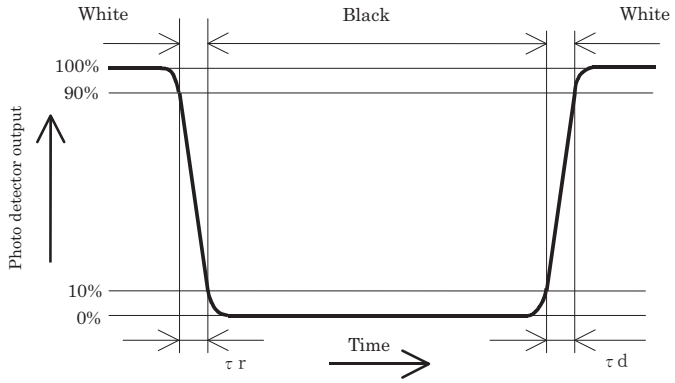


Fig.16 **Response time**

11. Reliability

Table.22

No.	Test	Condition	Judgment criteria
1	Temperature Cycling	-30℃ → 70℃ → -30℃ … 30min (3min) 30min (3min)30min 10cycle	Per table in below
2	High Temp. Storage	Ta=70℃ 240h	Per table in below
3	Low Temp. Storage	Ta=-30℃ 240h	Per table in below
4	Humidity Operation	Ta=40℃ 90%RH 240h	Per table in below (polarizer discoloration is excluded)
5	High Temp. Operation	Ta=60℃ 240h	Per table in below
6	Low Temp. Operation	Ta=-20℃ 240h	Per table in below
7	ESD	Discharge resistance: 0 Ω Discharge capacitor: 200 pF Discharge voltage: ±200 V Max Discharge 1 time to each input line ※ "GND" of display module is connected GND of test system ground.	Per table in below

⚠ ※Reliability test result is guaranteed at the conditions of a module attached with CG and OCA(~~ZY404~~-CBS-HC01).
(OCA recommended by Sharp: ~~ZY404~~-CBS-HC01 made in Hitachi Chemical.)
If CG laminating process is applied in customer factory, please confirm the reliability and CG laminating process is no problem before mass production began using the OCA and CG.
If problem happened at mass production，Sharp will not to follow.
Because Sharp cannot guarantee the customer 's CG laminating process.

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

12. Packaging specifications

(12-1) Details of packaging

1) Packaging style: Fig. 18, 19

(12-2) Reliability

1) Vibration test

Table.23

Item	Test			
Frequency	5 Hz to 50 Hz (3 minutes cycle)			
Direction	Up-Down, Left-Right, Front-Back (3 directions)			
Period	Up-Down	Left-Right	Front-Back	Total
	60min	15min	15min	90min

The frequency should start at 5 Hz and vary continuously.

Total amplitude 20mm 0.2mm 20mm 0.2mm

Frequency 5 Hz 50 Hz 5 Hz 50 Hz (For 9.8m/s^2)

2) Drop test

Drop height: 750mm

Number of drop: 10 times (Drop sequence: 1 corner, 3 edges, 6 faces)

(12-3) Packaging quantities

80 modules per master carton

(12-4) Packaging weight

About 8.5kg

(12-5) Packaging outline dimensions

575 mm×360 mm×225 mm (H)

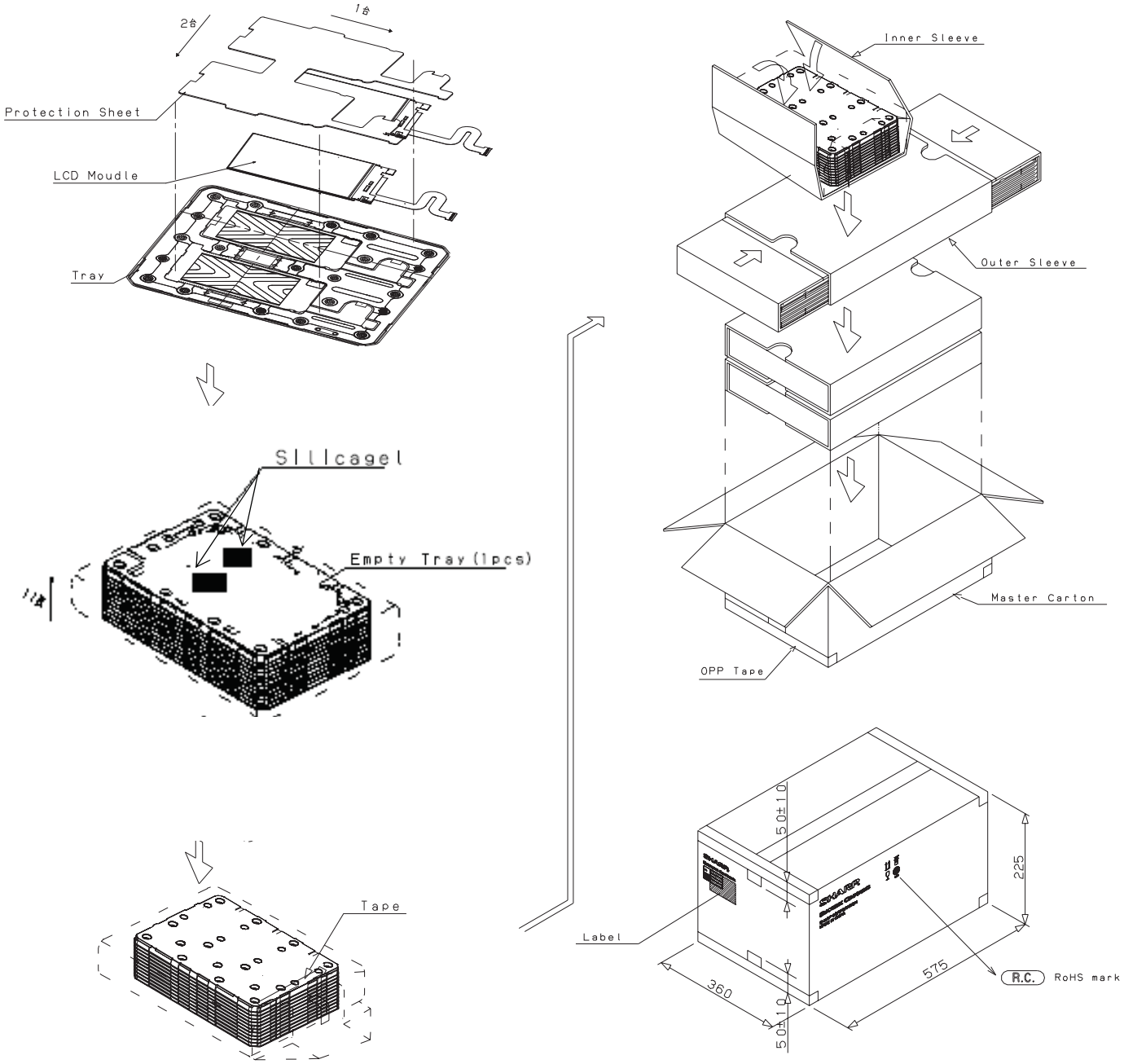


Fig.17 Packaging style (Tray for packaging)

Bar code label

Fig.18 Packaging style (Master carton for packaging)

13. Serial Number Label identification

Numbering is specified as follows.

4 X 000001 A Q

① ② ③ ④ ⑤

① product year (lower 1 digits)

4: 2014

5: 2015

② product month

1: January
2: February
3: March
:
9: September
X: October
Y: November
Z: December

③serial number

000001 ～ 999999

④ Version number

⑤ factory code

14. Outline dimensions

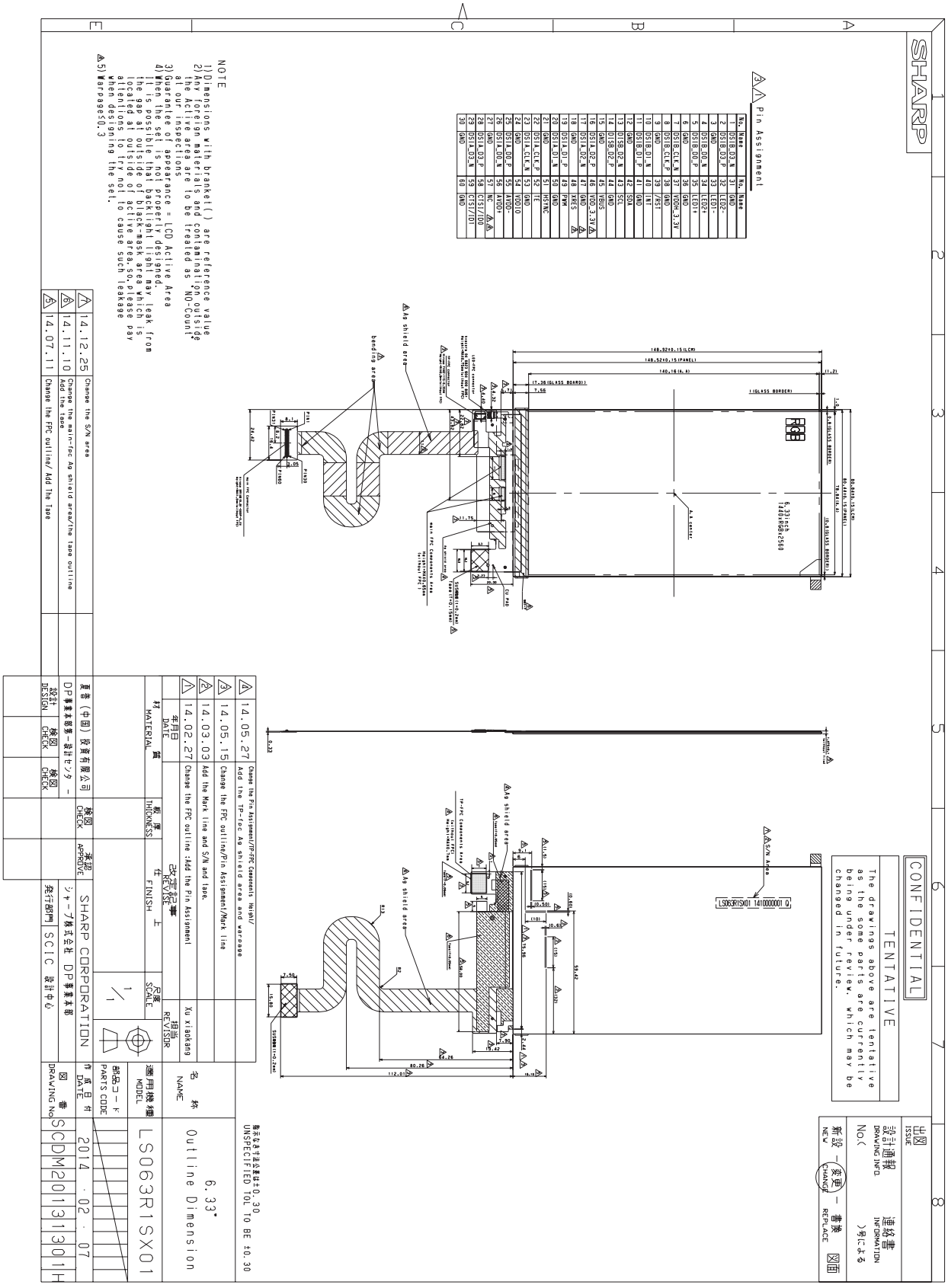


Fig. 19 MODULE Outline dimensions