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SPECIFICATION

DEVICE SPECIFICATION for
TFT LCD Module
(1080× RGB × 1920 dots)

Model No.

LS050T1SX06(G)

☐CUSTOMER'S APPROVAL

DATE _____

BY _____

PRESENTED
BY

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SHARP (CHINA) INVESTMENT CO.,LTD.

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LCY-W13702	*LS050T1SX06(G)*	1

NOTICE

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○ The device listed in these specification sheets was designed and manufactured for use in Telecommunication equipment (terminals)

○ In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

○ Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

○ SHARP assumes no responsibility for any damage resulting from the use of the device which does not comply with the instructions and the precautions specified in these specification sheets.

○ Contact and consult with a SHARP sales representative for any questions about this device.

[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ Floor

Floor is an important part to leak static electricity which is generated from human body or equipment. There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure(electrostatic earth:$1\times10^{8}\Omega$) should be made.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

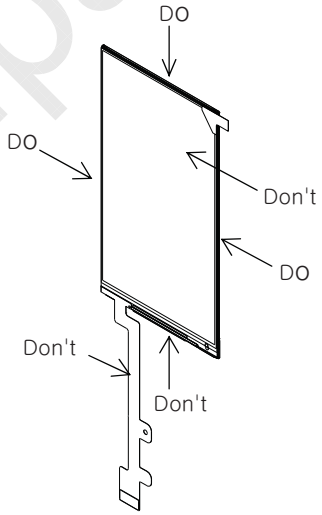
Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

[For operating LCD module]

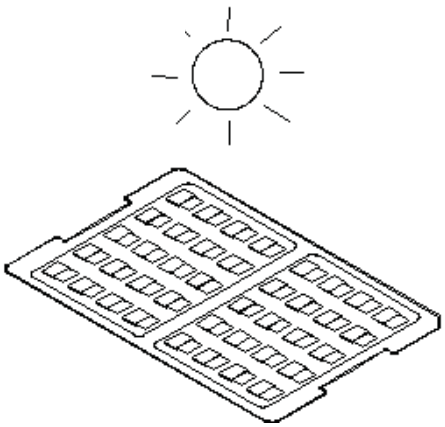
(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

[Precautions for Storage]

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.
(3) Keeping Method

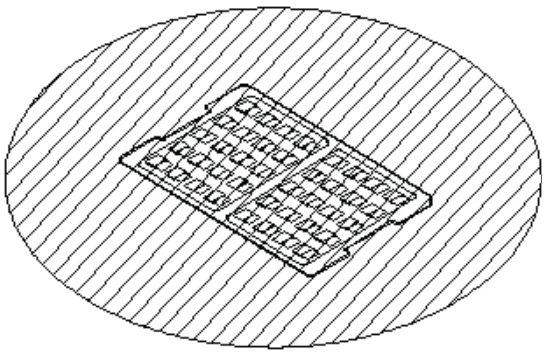
a. Don't keeping under the direct sunlight.

DON'T



b. Keeping in the tray under the dark place.

DO



(1) Do not operate or store the LCD module under outside of specified environmental conditions.
(2) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VDD-1V8/VSP/VSN-GND) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

(8) The connector used in this LCD module is the one Sharp have not ever used.
Therefore, please note that the quality of this connector concerned is out of Sharp's guarantee.

(9) Be sure to use a power supply with the safety protection circuit such as the fuse for excess voltage,excess current, electric discharge waveform and Latch-up occurring.

(10) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series), tray forming agent (azo compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardless of contact or noncontact to polarizer film.

Be sure to confirm the component of them.

(11) This module is designed for OCA TP bonding. If you are changing TP system, please contact us.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test:negative) material is employed.

FPC: Dispose of as similar way to circuit board from electric device.

1. Application

This data sheet is to introduce the specification of LS050T1SX06 active matrix 16,777,216color LCD module.
Main color LCD module is controlled by Driver IC(Renesas R63311).
If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

2. Construction and Outline

Construction: LCD panel, Driver (COG), FPC with electric components,
12 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame and metal frame to fix them mechanically.
Outline: See page 30
Connection: Board to board connector (HIROSE, BM20B(0.8)-34DP-0.4V(51))
There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.
So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge when LCD module is assembled into the cabinet.

3. Mechanical Specification

Table 1

Parameter		Specifications	Unit
Outline dimensions (typ)		64.3 (W) × 118.2 (H) × 1.4 (D) *2	mm
Main LCD Panel	Active area	61.884 (W) × 110.016(H)	mm
	Display format	1080(W) × RGB × 1920(H)	-
	Dot pitch	0.0191 (W) × 0.0573 (H)	mm
	Base color *1	Normally Black	-
	Illumination mode	Transmissive	
Mass		About:21.4	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.
*2 The above-mentioned table indicates module sizes without some projections and FPC.

4. Electrical Absolute Maximum Ratings

Table 2 Ta=25 ℃

Parameter	Symbol	Conditions	Rated value	Unit	Remarks
Driver IC (Positive Analog) Power Supply Voltage	VSP	Ta=+25℃	-0.3 ~ +6.5	V	【Note4-1,3】
Driver IC (Negative Analog) Power Supply Voltage	VSN	Ta=+25℃	+0.3 ~ -6.5	V	【Note4-1,3】
Driver IC (Digital) Power Supply Voltage	VDD-1V8	Ta=+25℃	-0.3 ~ +4.6	V	【Note4-1,2】

【Note4-1】If used beyond the absolute maximum ratings, the LSI may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during normal operation. The reliability of LSI is not guaranteed if used in the conditions beyond the limits and it may lead to malfunction.

【Note4-2】Make sure (High) VDD-1V8 ≥ GND (Low).

【Note4-3】Make sure (High) VSP ≥ AGND (Low), (Low) VSN≤AGND (High).

5.Environment Conditions

Table 3

Item	Top		Tstg		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-20 °C	+60°C	-30 °C	+70°C	【Note5-1】
Humidity	【Note5-1】		【Note5-1】		No condensation

【Note5-1】Humidity:95%RHMax.(at Ta≤40°C). Maximum wet-bulb temperature is less than 39°C (at Ta>40°C). Condensation of dew must be avoided.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

Be sure not to exceed the rated voltage, otherwise a malfunction may occur.

6. Electrical Specifications

(6-1) Power Supply Voltage Range

Table 4

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Driver IC(Positive Analog) Power Supply Voltage	VSP	4.75	5.00	5.25	V	【Note6-1】
Driver IC(Negative Analog) Power Supply Voltage	VSN	-4.75	-5.00	-5.25	V	【Note6-1】
Driver IC(Digital) Power Supply Voltage	VDD-1V8	1.71	1.80	3.30	V	【Note6-1】

(6-2) DC characteristics

Table 5

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Input voltage (Low)	V_{IL}	0	-	0.3VDD-1V8	V	【Note6-2】
Analog voltage ripple noise	AVDDn	-	-	100	mV	
Input voltage (High)	V_{IH}	0.7VDD-1V8	-	VDD-1V8	V	【Note6-2】
Input current (Low)	I_{IL}	-10	-	-	μA	
Input current (High)	I_{IH}	-	-	10	μA	
Output voltage (Low)	V_{OL}	0	-	0.2VDD-1V8	V	I_{OL}=+0.1mA
Output voltage (High)	V_{OH}	0.8VDD-1V8	-	-	V	I_{OH}=-0.1mA
Current consumption	I_{VSP}	-	14.3	21.5	mA	【Note6-3】
	I_{VSN}	-	9.6	13.9	mA	【Note6-3】
	$I_{VDD-1V8}$	-	16.8	25.4	mA	【Note6-3】
	I_{VSP}	-	0.004	0.02	mA	【Note6-4】
	I_{VSN}	-	0.004	0.02	mA	【Note6-4】
	$I_{VDD-1V8}$	-	0.004	0.02	mA	【Note6-4】

【Note6-1】Include Ripple Noise

【Note6-2】Applied overshoot

【Note6-3】Measurement Conditions : Full screen white pattern, AVDD(+/-)=5.00V,IOVDD=1.80V,60Hz Refresh

【Note6-4】Measurement Conditions : Deep standby mode

(6-3) MIPI DSI characteristics

<DC characteristics>

Table 6

Item		Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	70	3
	Differential input low threshold	VIDTL	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-70	-	-	3
	Single-ended input low voltage	VILHS	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-40	-	-	
	Single-ended input high voltage	VIHHS	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	460	
	Common-mode voltage HS receive mode	VCMRX(DC)	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	70	-	330	1
	Differential input impedance	ZID	Ω	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	100	-	2
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-50	-	550	
	Logic 1 input voltage	VIH	mV	IOVCC=1.65V~ 3.30V v	880	-	1350	
	I/O leakage current	ILEAK	μA	Vin = -50mV - 1350mV	-10	-	10	
LP-TX	Thevenin output low level	VOL	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-50	-	50	
	Thevenin output high level	VOH	V	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	1.1	1.2	1.3	
	Output impedance of LP transmitter	ZOLP	Ω	IOVCC=DPHYVCC= 1.80V	110	-	-	2
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	200	
	Logic 1 contention threshold	VIHCD	mV	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	450	-	-	

Notes: 1. VCMRX (DC) = (VP+VDN)/2
2. Excluding COG resistance (contact resistance and ITO wiring resistance). The values are tentative.
3. Minimum 110mV/-110mV HS differential swing is required for display data transfer.

<AC Characteristics>

Table 7

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
DSICLK Frequency	fDSICLK	MHz	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	100	-	500	4
DSICLK Cycle time	tCLKP	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	1	-	10	
DSI Data Transfer Rate	tDSIR	Mbps	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V DSI 2 lanes, 3 lanes,4lane	200	-	1000	4
Data to Clock Setup Time	tSETUP	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	6
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	5,6
Clock to Data Hold Time	tHOLD	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	6
		ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	0.15	-	-	5,6

Notes: 4. When fDSICLK<125MHz, change auto load NV setting so that it is compliant with THS-PREPARE+THS-ZERO spec.

5. Minimum tSETUP/tHOLD Time is 0.15UI. This value may change according to DSI transfer rate.

6. tSETUP/tHOLD Time are measured without HS-TX Jitter.

Table 8 **MIPI DSI LP-RX/TX Clock and Data-Clock Specifications**

Item	Symbol	Unit	Test condition	Min	Typ	Max	Notes
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	40 ns + 4*UI	-	85ns + 6*UI	
$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	145ns + 10*UI	-	-	
Time to drive flipped differential state after last payload data bit of a HS transmission burst	**$T_{HS-TRAIL}$**	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	max (n*8*UI, 60 ns + n*4*UI)	-	-	1,2
Time to drive LP-11after HS burst	$T_{HS-EXIT}$	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	100	-	-	
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	$4*T_{LPTX}$			
Time-out before new TX side starts driving	$T_{TA-SURE}$		IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	$1*T_{LPTX}$	-	$2*T_{LPTX}$	
Time to drive LP-00 by new TX	T_{TA-GET}		IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	$5*T_{LPTX}$			
Length of any Low-Power state period	T_{LPX}	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	50	-	-	
Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	Ratio T_{LPX}		IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	2/3	-	3/2	
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	**$T_{CLK-POST}$**	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	60 ns + 52UI	-	-	3
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	300	-	-	
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	8	-	-	
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	38	-	95	
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	60	-	-	
Time from start of THS-TRAIL period to start of LP-11 state	T_{EOT}		IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	-	105 ns + n*12*UI	2
Length of Low-Power TX period in case of using DSI clock	T_{LPTX1}	UI	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	32	-	4
Length of Low-Power TX period in case of using internal OSC clock	T_{LPTX2}	ns	IOVCC=1.65V~ 3.30V DPHYVCC=1.65V~ 3.30V	-	1/fosc	-	

Notes:
1. If a > b then max(a, b) = a, otherwise max(a, b) = b
2. Where n = 1 for Forward-direction HS mode.
3. The R63311 can work with this specification although the end part of internal process is remained when Clock Lane enter LP-11 and the R63311 can work without the remained process if tCLK-POST is more than 256 UI.
4. The R63311 uses DSI clock from the Host processor if Clock Lane is active, and internal oscillator clock if Clock Lane is disabled. Here, "fosc" is the frequency of oscillator clock, typical 28 MHz.

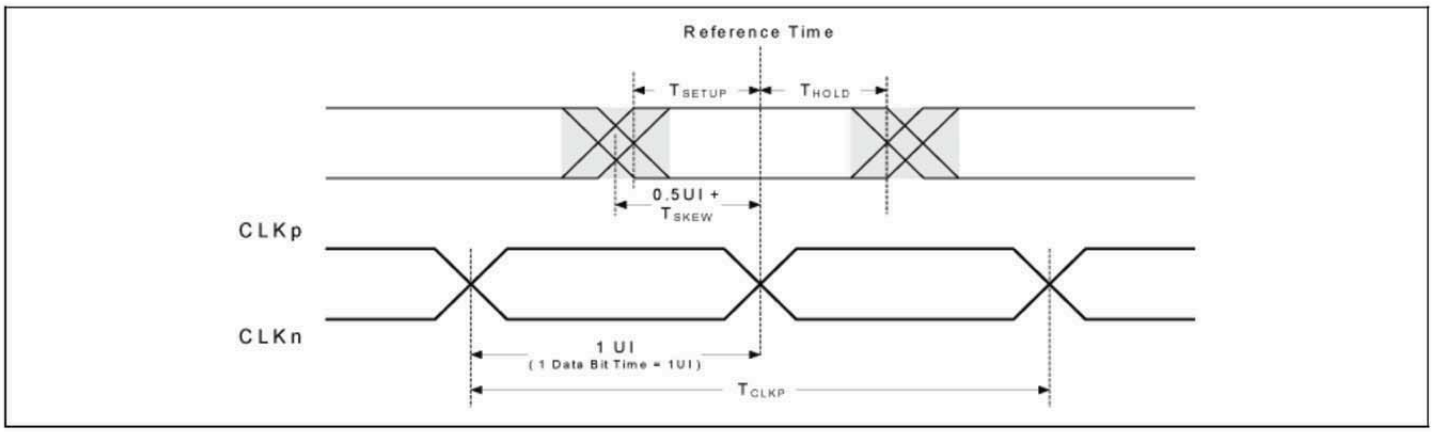


Fig.1 **Data to Clock Timing Definitions**

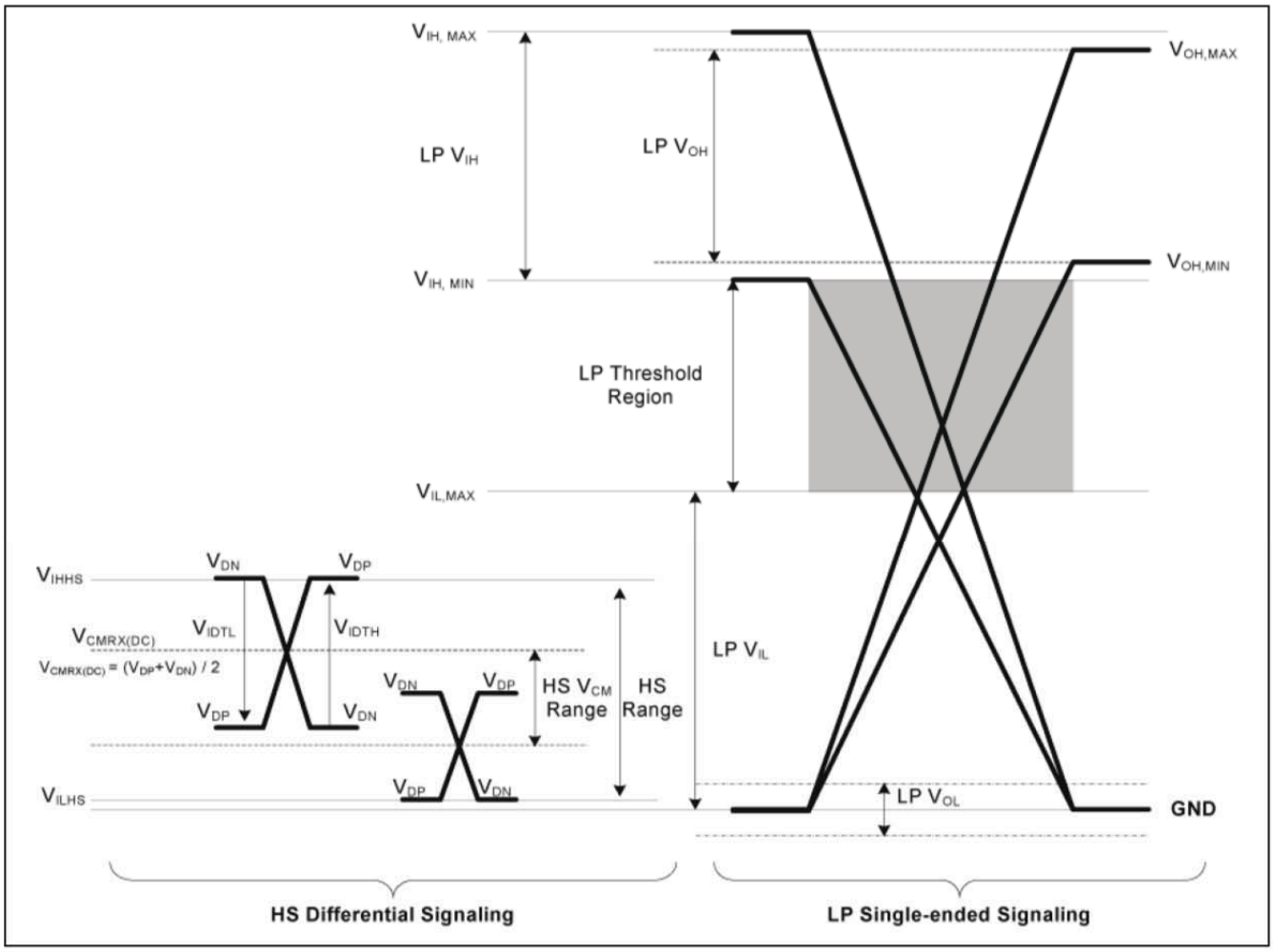


Fig.2 **DSI LP Mode**

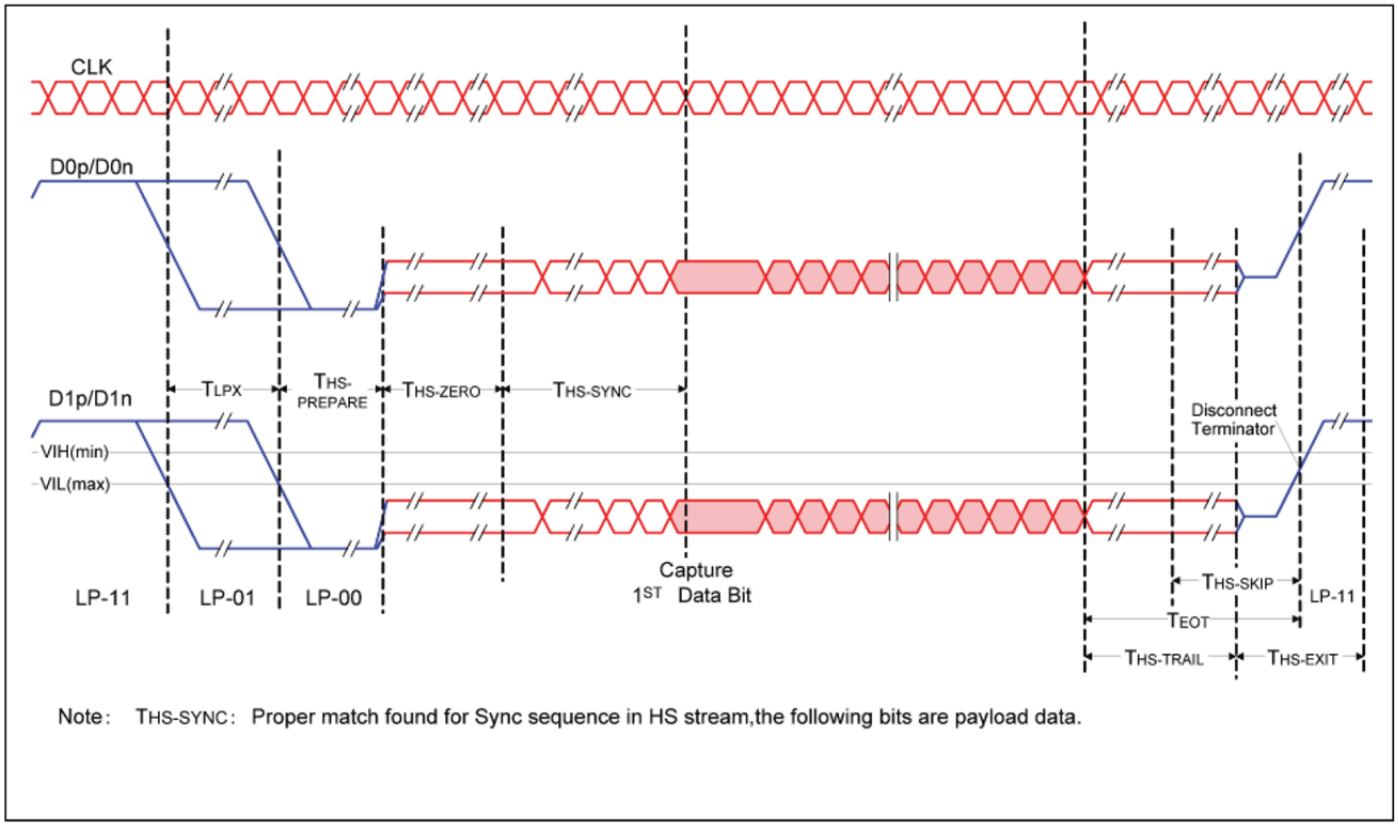


Fig.3 **HS Data Transmission in Bursts**

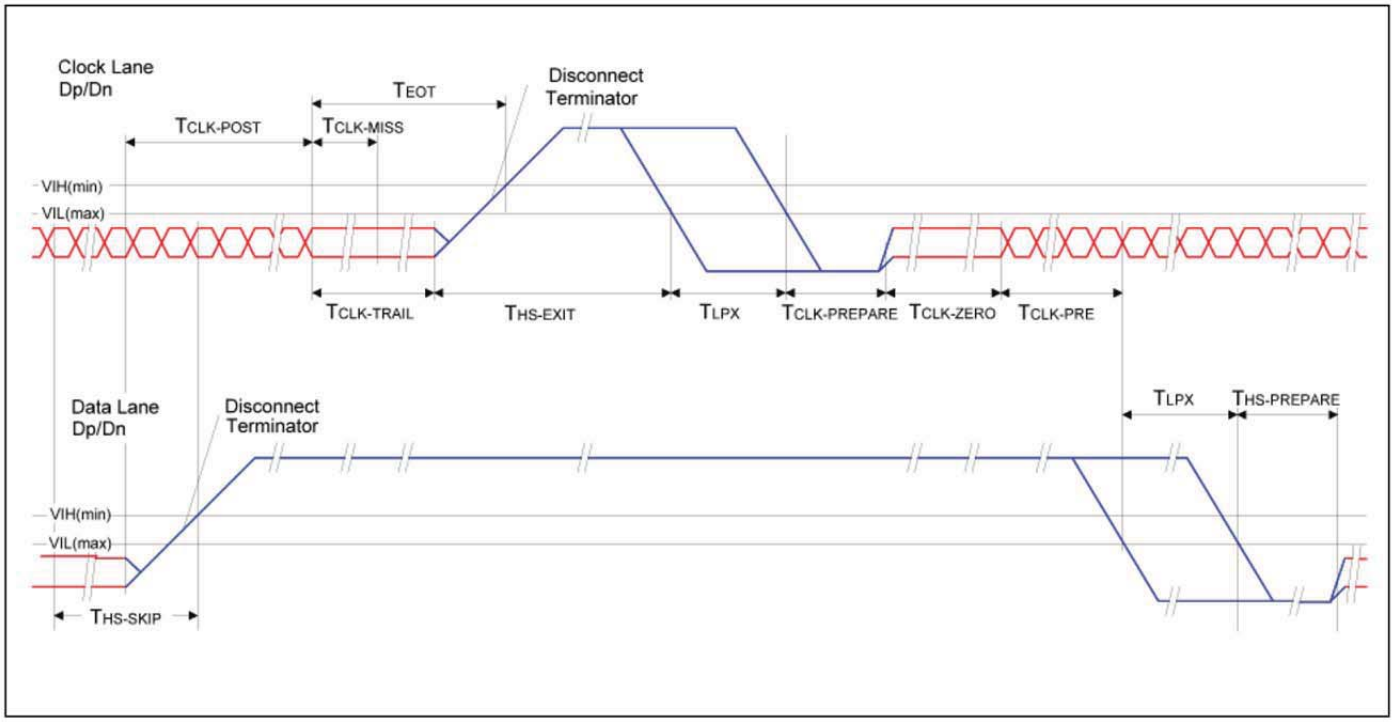


Fig.4 **Switching the Clock Lane between Clock Transmission and LP Mode**

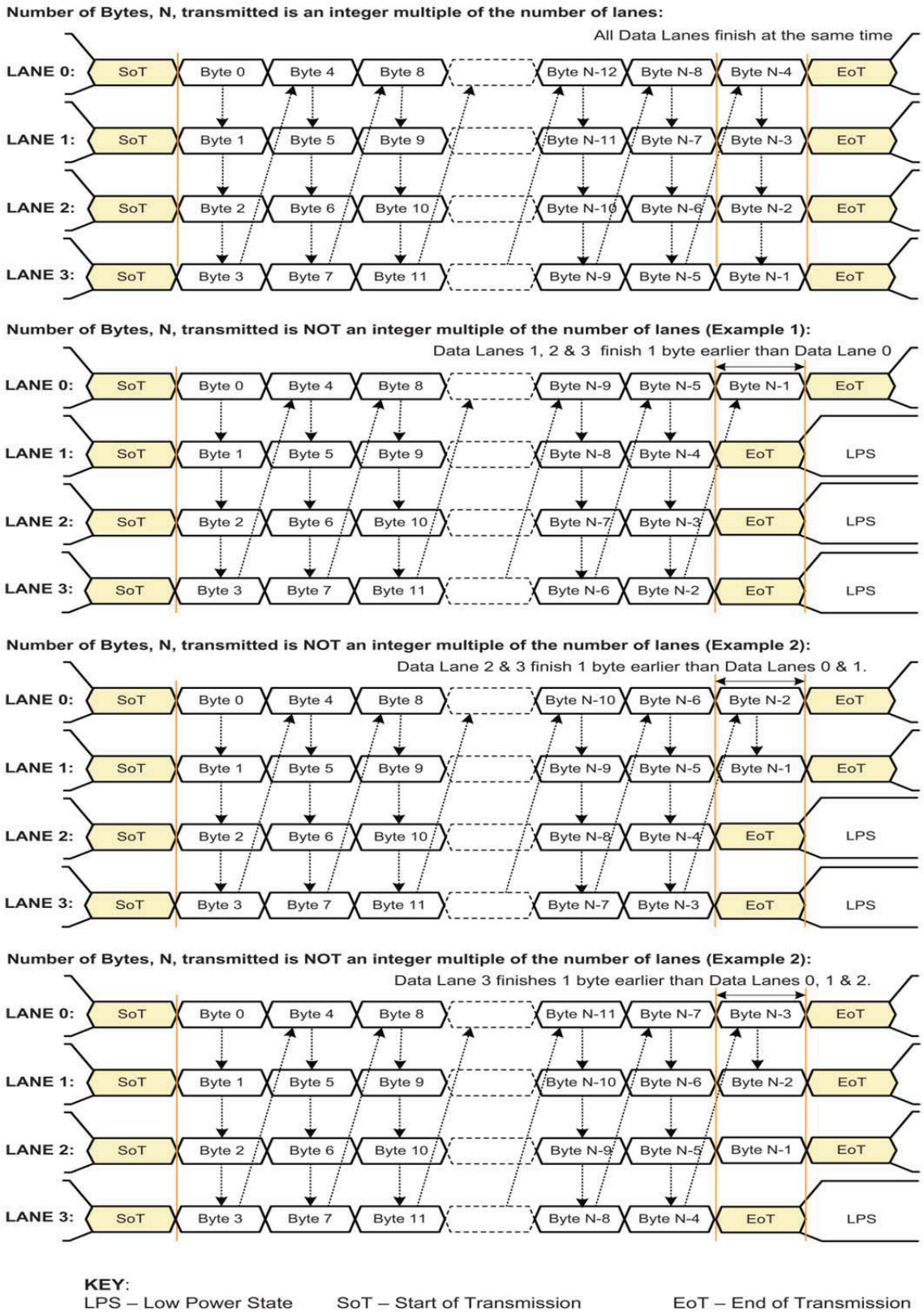


Fig.5 **Four Lanes HS Transmission Example**

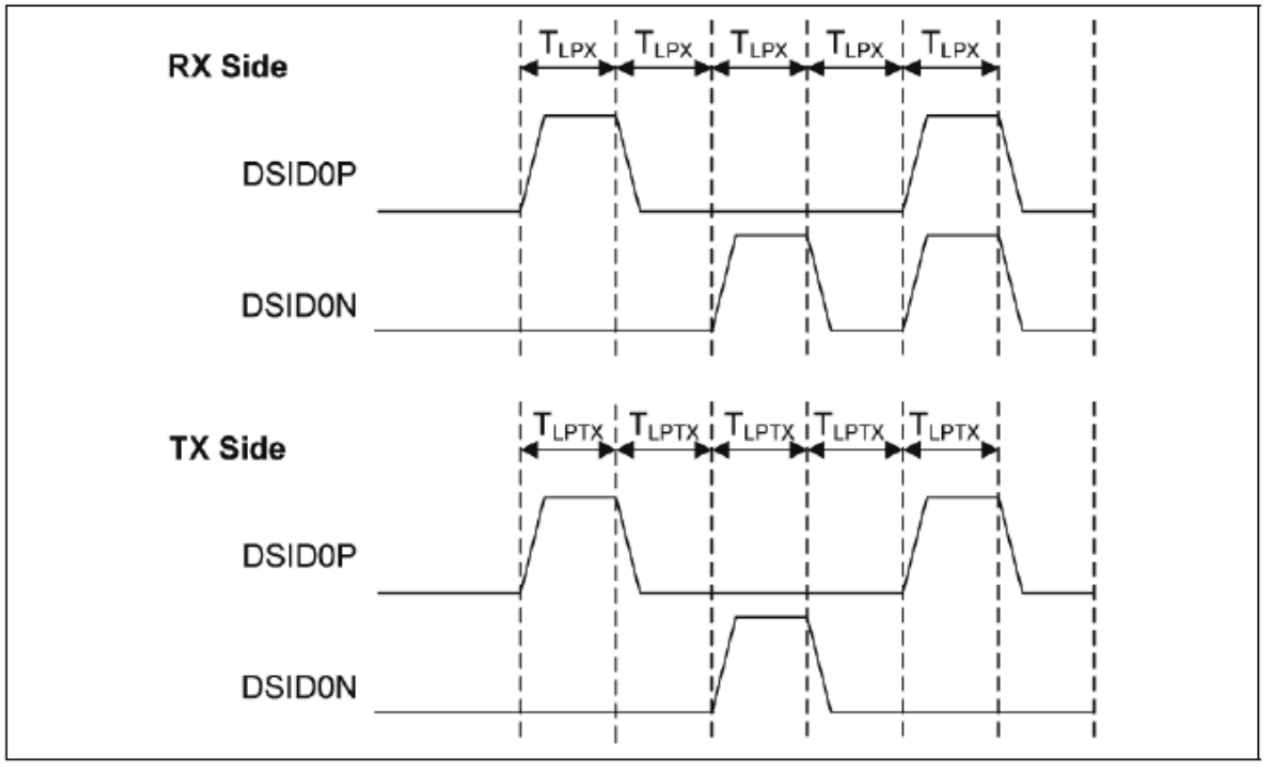


Fig.6 DSI LP Mode(Rx/Tx)

(6-4) LED backlight

At main panel the back light uses 12pcs edge light type white LED.

Table 9

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward current	Ta=25 °C	I_{LED}	-	20	-	mA	LEDA-LEDK
Number of LED components	12 pcs LED (6 pcs serial X 2 parallel)						

*Please consider Allowable Forward Current on used temperature

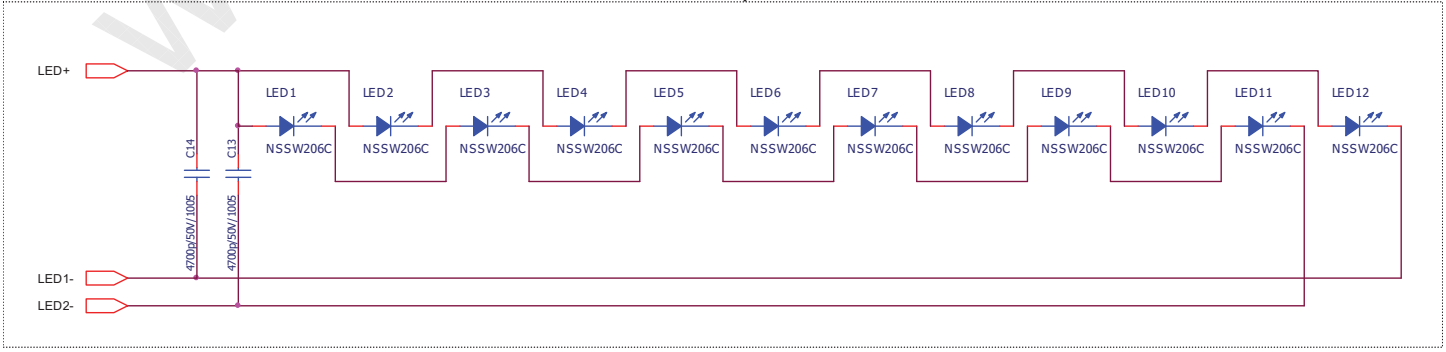


Fig.7 Schematics drawing of backlight

(6-5) Interface signals

Table 10

Pin No.	Symbol	I/O	Description	Remarks
1	GND	-	Ground	
2	NC	-	Not connect	
3	LCD-PWM	O	Backlight LED driver PWM	
4	GND	-	Ground	
5	LCD-TE	O	Tearing signal output from driver IC	
6	LANE2-P	I	MIPI data2 positive signal	
7	LCD-RESET-N	I	Device reset signal	"L" Active
8	LANE2-N	I	MIPI data2 negative signal	
9	LCD-ID-0	-	ID0(GND)	ID0="0"
10	GND	-	Ground	
11	LCD-ID-1	-	ID1(NC)	ID1="NC"
12	LANE1-P	I	MIPI data1 positive signal	
13	GND	-	Ground	
14	LANE1-N	I	MIPI data1 negative signal	
15	VSN	I	Power supply for analog(-5.0V)	
16	GND	-	Ground	
17	VSN	I	Power supply for analog(-5.0V)	
18	CLK-P	-	MIPI clock positive signal	
19	VSP	I	Power supply for analog(+5.0V)	
20	CLK-N	I	MIPI clock negative signal	
21	VSP	I	Power supply for analog(+5.0V)	
22	GND	-	Ground	
23	VDD-1V8	I	Power supply for I/O(1.8V)	
24	LANE0-P	I/O	MIPI data0 positive signal	
25	GND	-	Ground	
26	LANE0-N	I/O	MIPI data0 negative signal	
27	LED-ANODE		LED back light power positive	
28	GND	-	Ground	
29	NC	-	Not connect	
30	LANE3-P	I	MIPI data3 positive signal	
31	LED-CATHODE1	-	LED back light power group1 negative	
32	LANE3-N	I	MIPI data3 negative signal	
33	LED-CATHODE2	-	LED back light power group2 negative	
34	GND	-	Ground	

Notes:The direction is named with respect to the display module, I = from host to LCM, O = from LCM to host.

Table 11 **Connector description**

Assembled on	Item	Description
Phone PWB	Connector type	Board to Board
	Pin amount	34
	Manufacturer	Hirose
	Part number	BM20B(0.8)-34DP-0.4V(51)

(6-6) General Timing Diagram

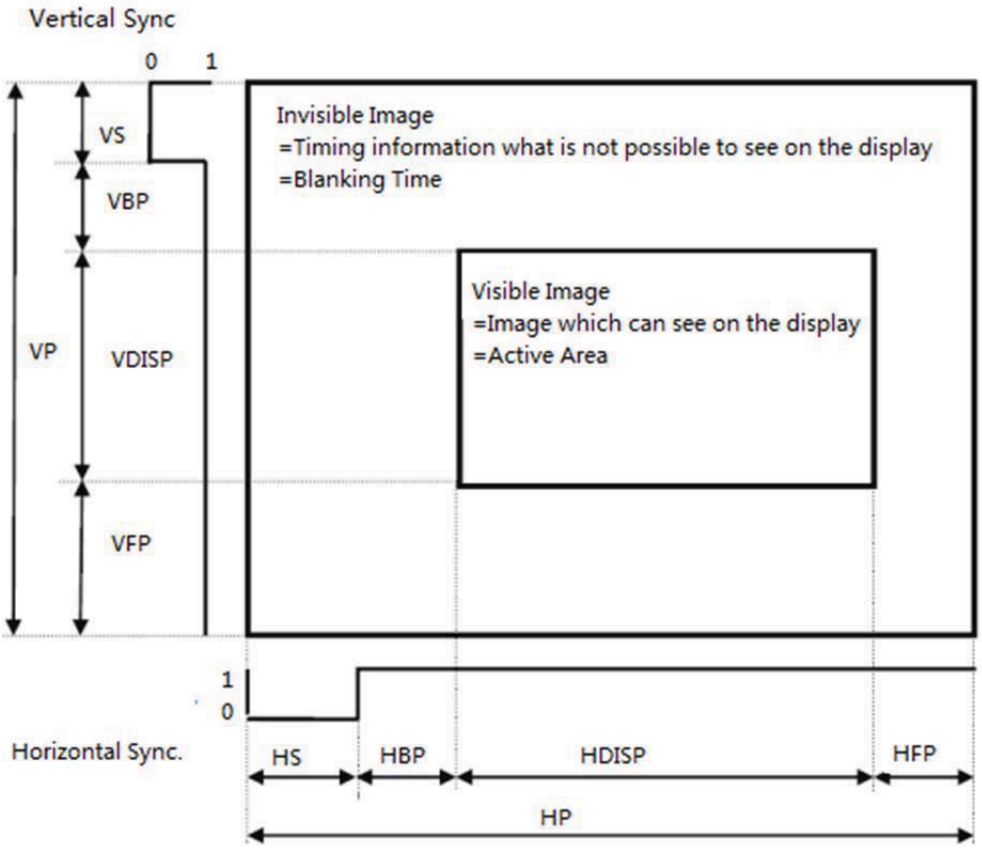


Fig.8

(6-7) Vertical Timing

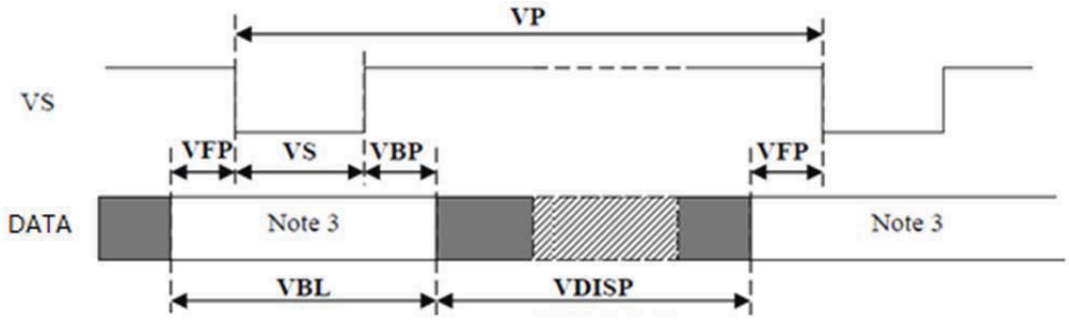


Fig.9

Table 12

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Vertical cycle	VP		-	1930	-	Line
Vertical low pulse width	VS		-	2	-	Line
Vertical front porch	VFP		-	4	-	Line
Vertical back porch	VBP		-	4	-	Line
Vertical data start point		VS+VBP	-	6	-	Line
Vertical blanking period	VBL	VFP+VS+VBP	-	10	-	Line
Vertical active area		VDISP	-	1920	-	Line
Vertical Refresh Rate	VRR		57	60	63	Hz

Ta = -20 °C ~ +60°C, VDD-1V8= 1.8 V, VSP=5.0V, VSN=-5.0V, GND = 0 V

(6-8) Horizontal Timing

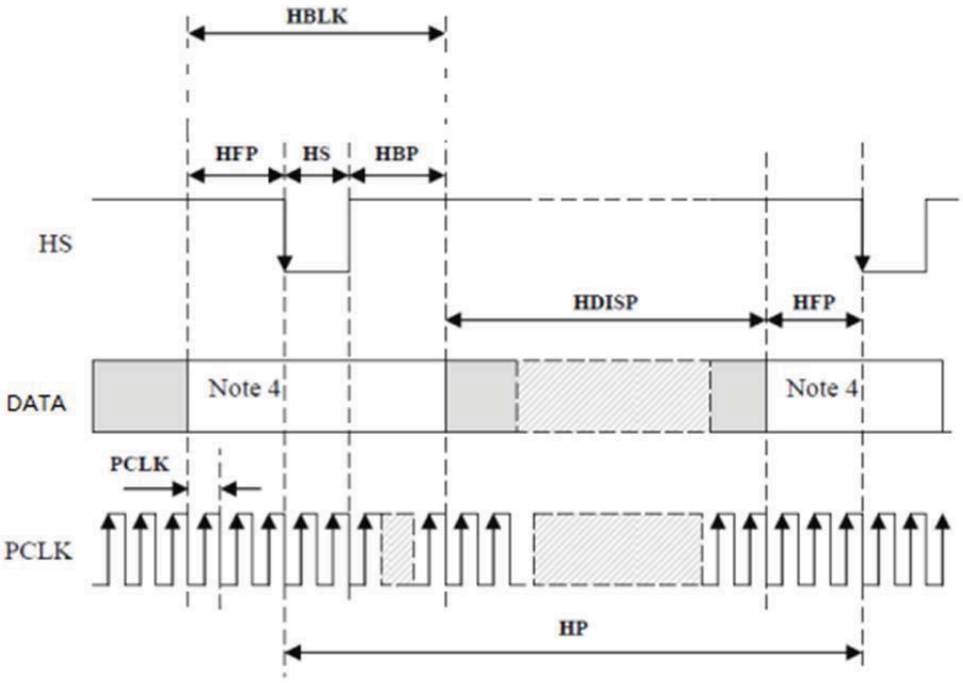


Fig.10

Table 13

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
HS cycle	HP			1240		PCLK
HS low Pulse width	HS			10		PCLK
Horizontal back porch	HBP			50		PCLK
Horizontal front porch	HFP			100		PCLK
Horizontal data start point		HS+HBP		60		PCLK
Horizontal blanking period	HBLK	HFP+HS+HBP		160		PCLK
Horizontal active area	HDISP			1080		PCLK
1 Horizontal timing			8.224	8.635	9.090	us
Pixel clock frequency	PCLK		7.33	6.96	6.63	ns
			136.42	143.6	150.78	MHz
MIPI Speed(4 lane)	-	-	950	1000	1050	Mbps/lane

Ta = -20°C ~+60°C, VDD-1V8= 1.8 V, VSP=5.0V, VSN=-5.0V, GND = 0 V

(6-9) Reset Timing Characteristics

Table 14

Item	Symbol	Unit	Test condition	Min.	Max.
Reset low-level width1	tRW1	us	Power supply on	1000	–
Reset low-level width2	tRW2	us	Operation	1000	–
Reset time (Sleep IN)	tRT1	ms	–	–	3
Reset time (Sleep OUT)	tRT2	ms	–	–	3
Noise reject width	tRESNR	us	–	–	1

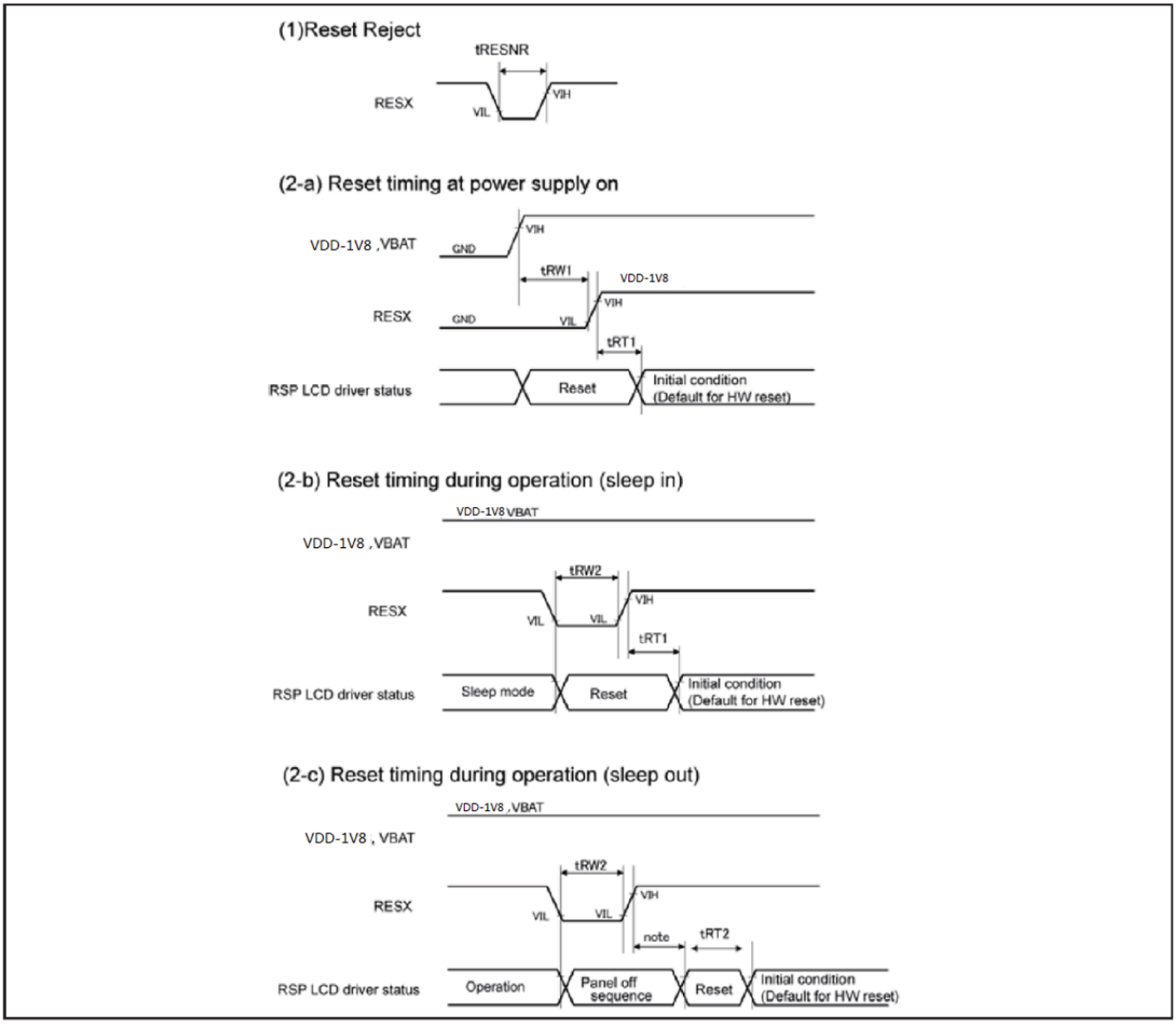


Fig.11 **Reset Timing Characteristics**

(6-10) Schematic of LCD module system

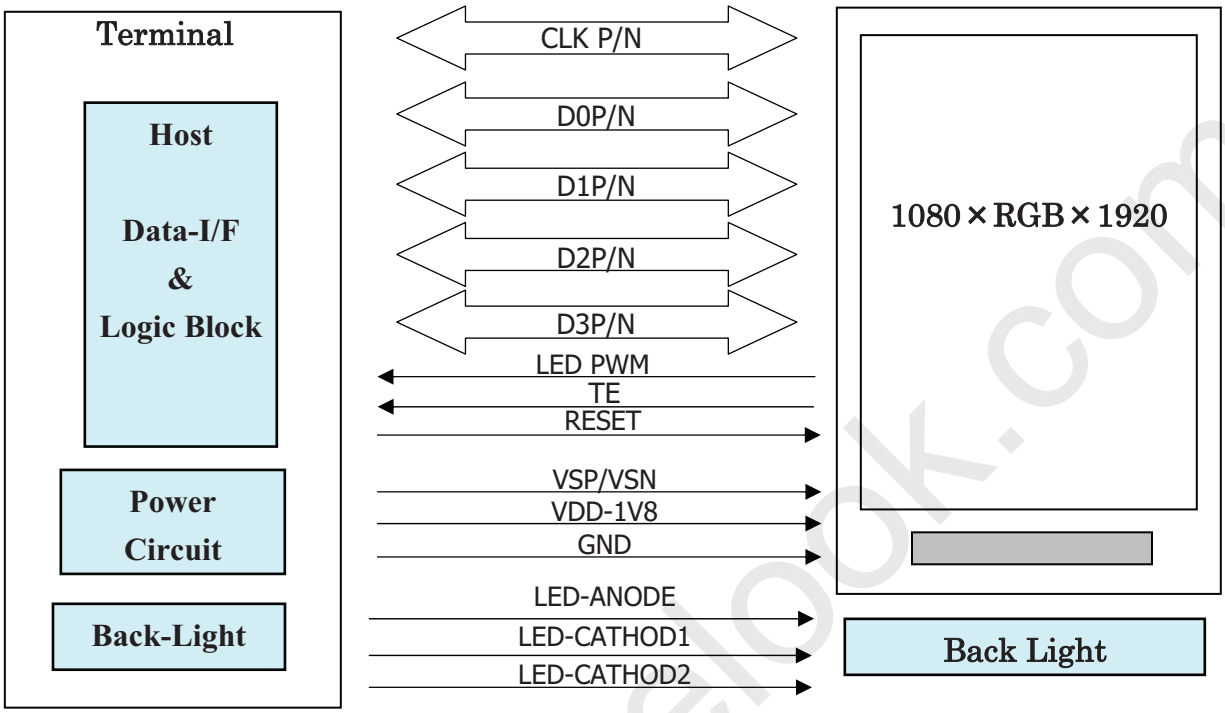


Fig.12 Schematic of LCD module system

7. Initial Sequence

Condition
I/F: MIPI DSI 4Lane,Video Mode 1GMbps
Dots Size : 1080 x RGB x 1920
Power Supply:VDD-1V8=1.8 V, VSP=5V, VSP=-5V,
Color Mode:24bit
Frame frequency :TYP 60Hz

Table 15**Power ON Sequence**

Power ON Sequence

ITEM	Command	Parameter	REMARK
Reset (Reset="L")			
VDD-1V8 ON			VDD-1V8: Typ 1.8V
WAIT 150ms(min 1ms)			
VSP ON			VSP: Typ 5.0V
WAIT 150ms(min 0ms)			
VSN ON			VSN: Typ -5.0V
WAIT 50ms(min 1ms)			
Reset release ("L"→"H")			
WAIT 10ms(min 3ms)			
Manufacturer command access Protect	0XB0	0X04	
Nop	0x00	-	LP mode :don't need
Nop	0x00	-	HS mode: need
NVM load control	0XD6	0x01	
IF customer need, please add initial command in here.			
Sleep out	0x11		
DSI Vedio mode transfer start			
WAIT MIN 6V (Frame)			
Display ON	0x29	-	
Backlight on			
Write_display_brightness	0x51	0x00	LED light:100%.
		0xFF	
Write_content_adaptive_brightness_control	0x55	0x02	CABC OFF=00h CABC ON=02h
Write_control_display (BackLight On)	0x53	0x2C	LED(PWM) On
Display pattern			Any pattern

Table 16 **Power OFF Sequence**

POWER OFF Sequence

ITEM	Command	Parameter	REMARK
Backlight OFF	0x53	00h	
Display OFF	0x28	-	-
Wait Min 1V(Frame)			
Sleep in	0x10	-	-
Wait Min 4V(Frame)			
DSI Vedio mode transfer stop			
Reset (Reset="L")			
Wait 10ms(min 0ms)			
VSN OFF(GND)			
WAIT 10ms(min 0ms)			
VSP OFF(GND)			
Wait 2ms(min 0ms)			
VDD-1V8 OFF(GND)			

Table 17 Deep standby In Sequence

Deep standby In Sequence (Normal->Deep standby In)

ITEM	Command	Parameter	REMARK
Backlight OFF	0x53	00h	
Display OFF	0x28	-	-
Wait Min 1V(Frame)			
Sleep IN	0x10	-	-
Wait Min 4V(Frame)			
DSI Vedio mode transfer stop			
Manufacturer Command Access Protect	0XB0	02h	No Lock
Low Power Mode Function	0XB1	01h	
VSN OFF(GND)			
WAIT 10ms(min 0ms)			
VSP OFF(GND)			
Wait 2ms(min 0ms)			
Reset (Reset="L")			

Table 18 Deep standby Out Sequence

Deep standby Out Sequence (Deep standby In -> Normal)

ITEM	Command	Parameter	REMARK
Reset (Reset="L")			
Wait min 1ms			
VSP ON			VSP: Typ 5.0V
WAIT 150ms(min 0ms)			
VSN ON			VSN: Typ -5.0V
WAIT 50ms(min 1ms)			
Reset release ("L"→"H")			
WAIT 10ms(min 3ms)			
Manufacturer Command Access Protect	0XB0	0X04	
Nop	0x00	-	LP mode :don't need HS mode: need
Nop	0x00	-	
NVM load control	0XD6	0x01	
IF customer need, please add initial command in here.			
Sleep out	0x11	Sleep out	
DSI Vedio mode transfer start			
WAIT MIN 6V (Frame)			
Display ON	0x29	-	
Backlight On			
Write_display_brightness	0x51	0x00	LED light:100%.
		0xFF	
Write_content_adaptive_brightness_control	0x55	0x02	CABC OFF=00h CABC ON=02h
Write_control_display (BackLight On)	0x53	0x2C	LED(PWM) On
Display pattern			Any pattern

8. Optical Characteristics

Table 19 VDD-1V8=1.8 V, VSP=5V, VSP=-5V, ILED=20mA, Ta = 25℃

Optical Characteristics

Parameter	symbol	condition	MIN	TYP	MAX	unit	Remark
Brightness	Br	θ=0°	360	480	-	cd/㎡	Note1,2
Contrast	Co	θ=0°	700	1000	-		Note1,3
Viewing Angle	θ11	CR > 10	85	-	-	deg	Note1
	θ12		85	-	-		
	θ21		85	-	-		
	θ22		85	-	-		
Response Time	(τr+td)	θ=0°	-	-	35	ms	Note1,4
White chromaticity	x	θ=0°	0.28	0.31	0.34		Note.1,3
	y		0.29	0.32	0.35		
Red	x	θ=0°	0.595	0.63	0.665		Note.1,3
	y		0.295	0.33	0.365		
Green	x	θ=0°	0.275	0.31	0.345		Note.1,3
	y		0.575	0.61	0.645		
Blue	x	θ=0°	0.115	0.15	0.185		Note.1,3
	y		0.015	0.05	0.085		
Uniformity	-	θ=0°	70	80	-	%	Note.5
NTSC ratio	-	θ=0°	-	70.8	-	%	Note.1
Flicker	F	θ=0°	-	-	10	%	Note.6
Crosstalk	CT	θ=0°	-	-	4.5	%	Note.7

Note 1) Definition of range of visual angle

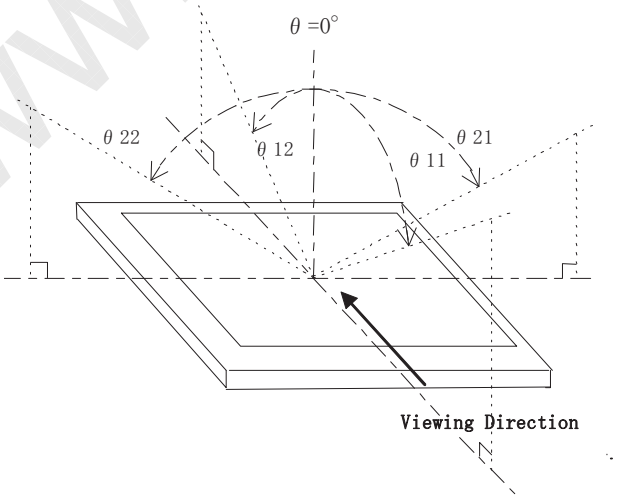


Fig.13 **Definition of viewing angle**

Note 2) Brightness is measured as shown in Fig.14, and is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

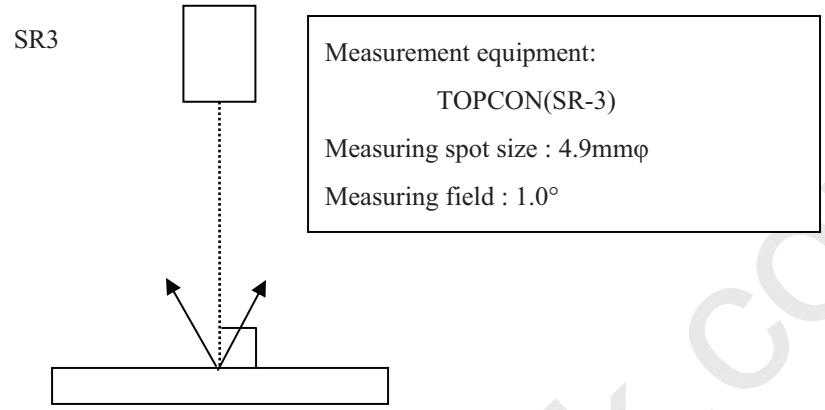


Fig.14 **Optical characteristics Test Method (Brightness)**

Note 3) Contrast ratio is defined as follows:

$$Co = \frac{Luminance(brightness)allpixcels"White"}{Luminance(brightness)allpixcels"Black"}$$

Note 4) Response time is defined as follows:

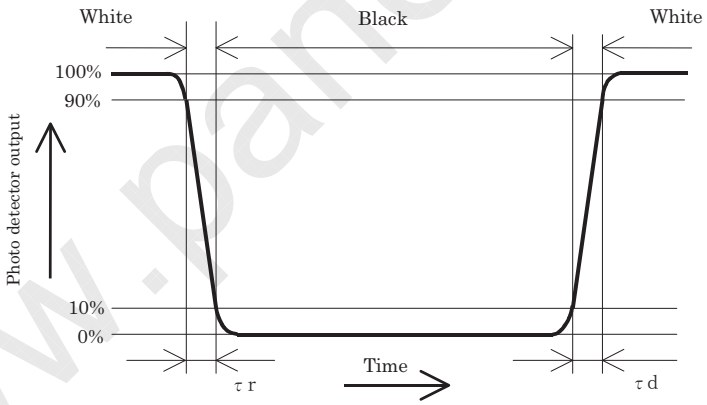


Fig.15 **Response time**

Note 5) Uniformity is defined as follows:

$$Uniformity = \frac{Minimum\ Luminance(brightness)\ in\ 9\ points}{Maximum\ Luminance(brightness)\ in\ 9\ points}$$

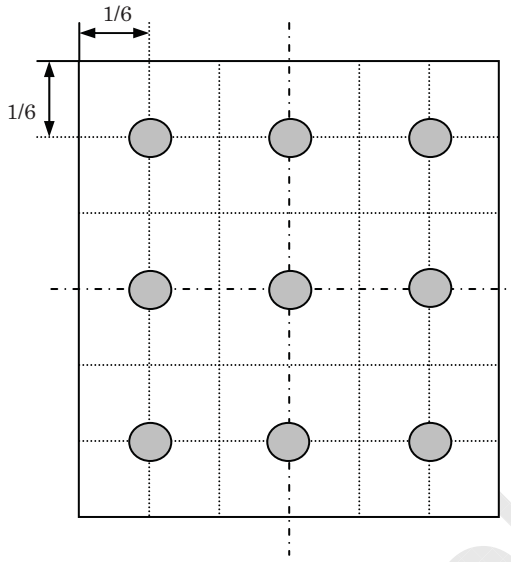


Fig.16 **Measuring Point**

Note 6) Flicker is defined as follows:

- ·Measuring systems: YOKOGAWA 3298_01 + 3298_11
- ·Temperature = 25℃(±3℃), Frame Frequency = 60Hz, LED back-light: ON, Environment brightness < 150 lx
- ·Measurement point is panel center.
- ·Conversion of Flicker ratio : Flicker[%] =ACrms/DC×100
- ·Measured sample : New sample before a long term aging.
- ·Flicker ratio is very sensitive to measuring condition.

Note 7) Crosstalk is defined as follows:

$CT=|Yw(X_i)-Y_G(X_i)|\times 100(\%)/Y_G(X_i)$ X=U,D,L,R i=gray 127

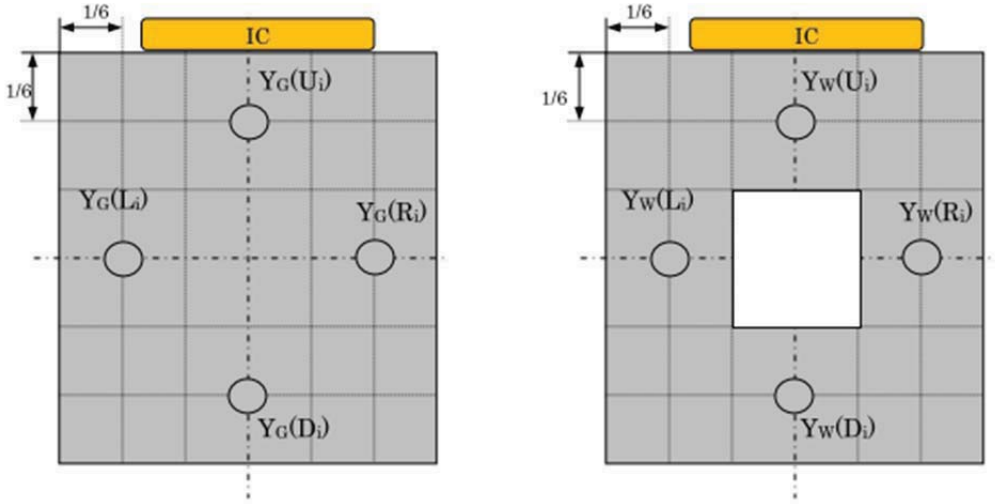


Fig.17 **Measuring Point**

9. Reliability

Table.20

No.	Test	Condition	Judgment criteria
1	Temperature Cycling	-20℃ → 70℃ … 30min(3min)30min 10cycle	Per table in below
2	High Temp. Storage	Ta= 70℃ 240h	Per table in below
3	Low Temp. Storage	Ta=-30℃ 240h	Per table in below
4	Humidity Operation	Ta=40℃ 90%RH 240h	Per table in below (polarizer discoloration is excluded)
5	High Temp. Operation	Ta= 60℃ 240h	Per table in below
6	Low Temp. Operation	Ta=-20℃ 240h	Per table in below
7	ESD	Discharge resistance: 0 Ω Discharge capacitor: 200 pF Discharge voltage: ±200 V Max Discharge 1 time to each input line ※ "GND" of display module is connected GND of test system ground.	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the LCD Panel
Alignment of LCD Panel	No Bubbles in the LCD Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

10. Packaging specifications

(10-1) Details of packaging

1) Packaging materials: Table.2.2
2) Packaging style : Fig.18,19

(10-2) Reliability

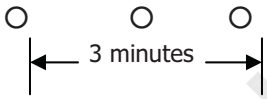
1) Vibration test

Table.21

Item	Test			
Frequency	5 Hz to 50 Hz (3 minutes cycle)			
Direction	Up-Down, Left-Right, Front-Back (3 directions)			
Period	Up-Down	Left-Right	Front-Back	Total
	60min	15min	15min	90min

The frequency should start at 5 Hz and vary continuously.

Total amplitude 20mm 0.2mm 20mm 0.2mm
Frequency 5 Hz 50 Hz 5 Hz 50 Hz (For 9.8m/s^2)



2) Drop test

Drop height: 750mm
Number of drop: 10 times (Drop sequence: 1 corner, 3 edges, 6 faces)

(10-3) Packaging quantities

120 modules per master carton

(10-4) Packaging weight

About: 8.5Kg

(10-5) Packaging outline dimensions

575 mm×360 mm×225 mm (H)
(Packaging materials)

Table.22

	Parts name	CRITERION(after test)
1	Master carton	Corrugate card board
2	Inside sleeve	Corrugate card board
3	Outside sleeve	Corrugate card board
4	Tray for packaging	Polystyrene with anti-static treatment +anti-static polystyrene
5	Protective bag	Polystyrene with anti-static treatment
6	OPP tape	Polypropylene
7	Bar code label	anti-static polystyrene

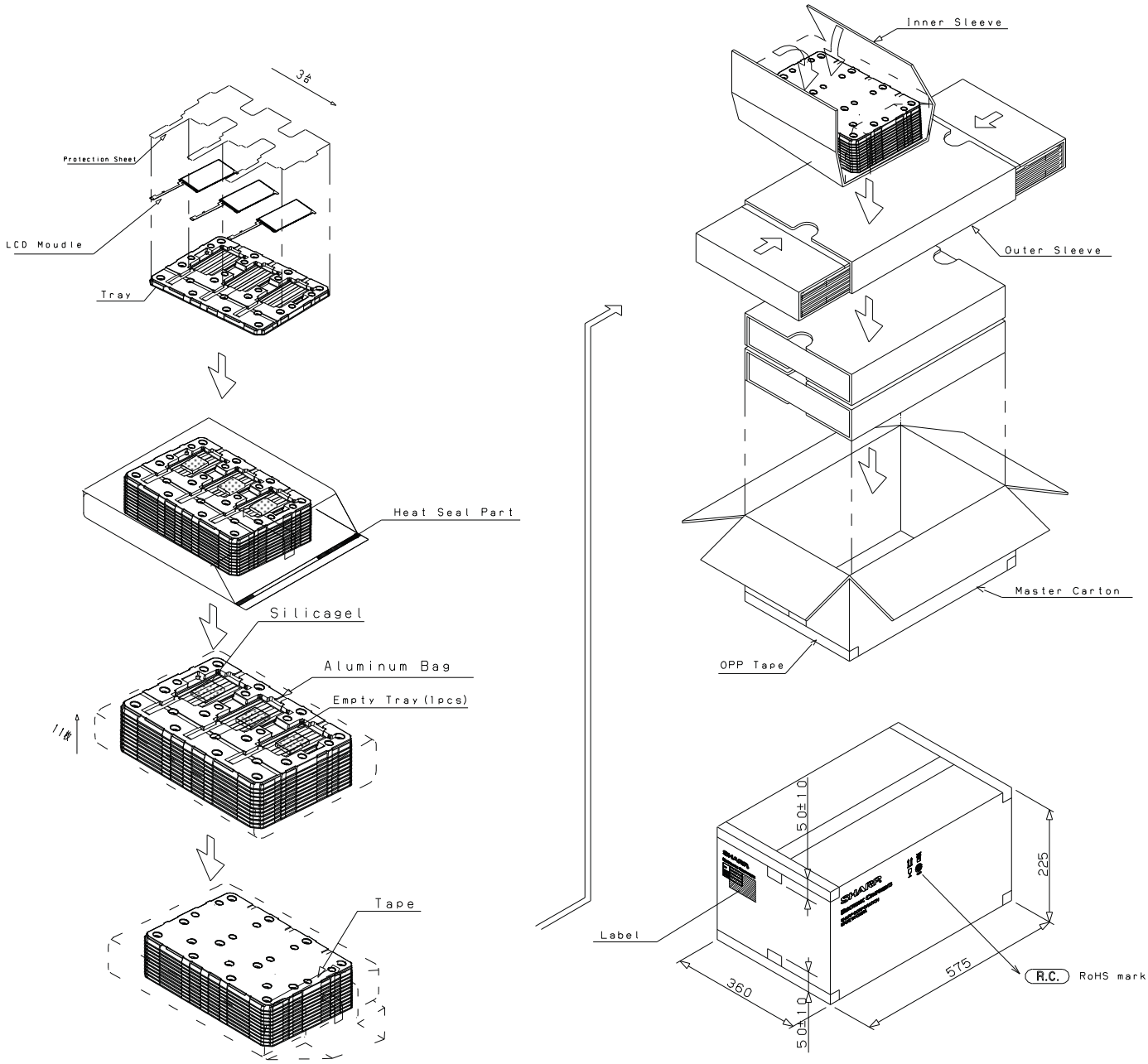


Fig.18 **Packaging style (Tray for packaging)**

Bar code label

Fig.19 **Packaging style (Master carton for packaging)**

11. Serial Number Label identification

Numbering is specified as follows.

3 X 0000001 A Q
①② ③ ④⑤

① product year (lower 1 digits)
3: 2013
4: 2014

② product month
1: January
2: February
3: March
:
9: September
X: October
Y: November
Z: December

③ serial number
0000001 ～ 9999999

④ Version number

⑤ factory code

12. Outline dimensions

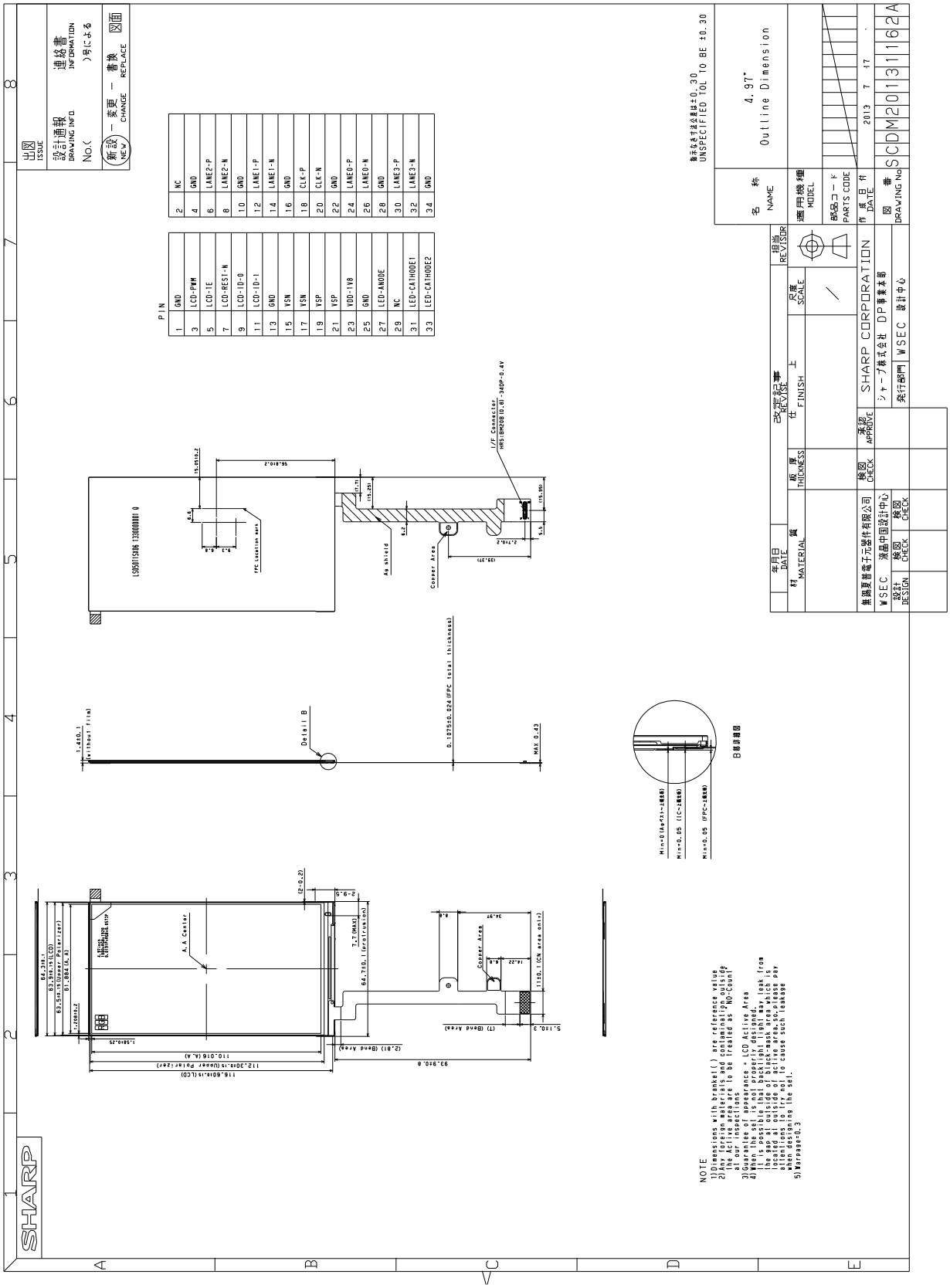


Fig. 20 **Outline dimensions**