Doc. Number:

☐ Tentative Specification
■ Preliminary Specification
☐ Approval Specification

MODEL NO.: P068HFB
SUFFIX: DK1

Customer:

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
簡豪慶	林耀楠	廖俊安

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REVISION HISTORY

Version	Date	Page	Description
1.0	2015.01.12	All	Spec Ver.1.0 was first issued.
1.1	2015.06.12	All	1-2. General Spec. 2. Absolute Maximum Ratings 5.1 TDM Drawing 5.3 Panel Outline Dimension 8. Package

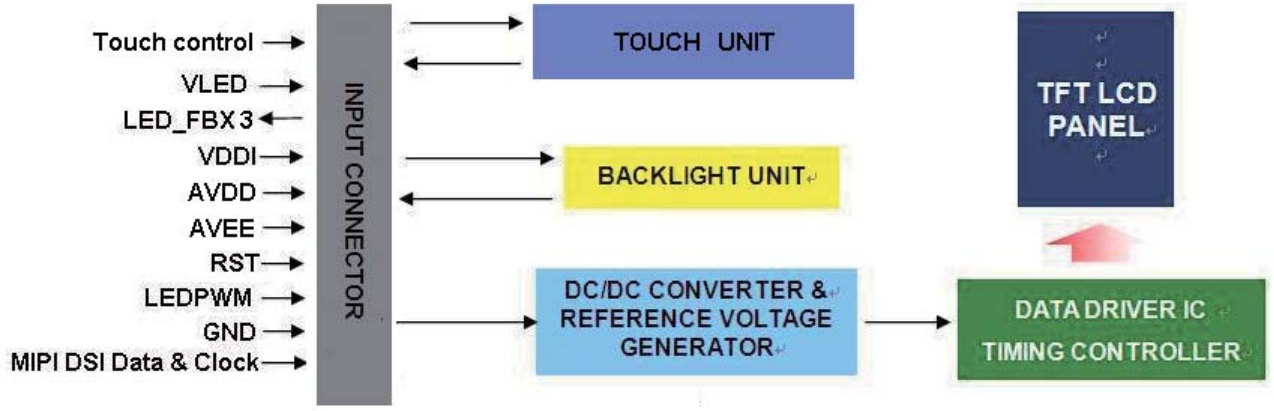
1. GENERAL DESCRIPTION

1.1 OVERVIEW

Features.

P068HFB-DK1 is 6.76” color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, MIPI driver ICs, control circuit and backlight. By applying 8 bit digital data, 1080×RGB (3) ×1920, 16.7M-color images are displayed on the 6.76” diagonal screen.

Block Diagram:



1.2 GENERAL SPECIFICATIONS

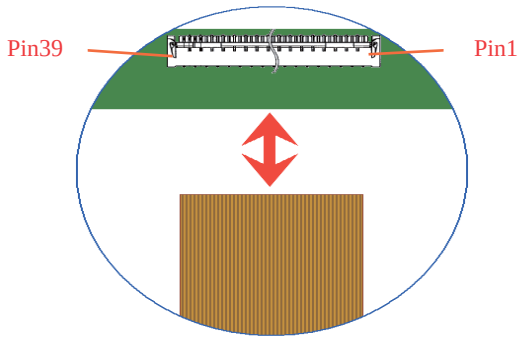
Item	Specification	Unit	Note
Screen Size	6.76” diagonal	inch	
Active Area	84.24 x 149.76	mm	
Panel Size	88.24 x 158.78	mm	TFT Glass size
Outline Dimension	92.35*182.35*2.7 (typ.)	mm	(w/o FPCa)
Display Resolution	1080 x R.G.B. x 1920	pixel	
Pixel Pitch	0.078 (H) x 0.078 (V)	mm	
Display Method	a-si		
Display Mode	IPS		
Display Color	16.7M (8bit color depth)		
Color Gamut	70%	%	typ
Luminance	350	nit	Typ, center P
Contrast Ratio	1000		Typ, center P
Viewing Angle	85/85/85/85	°	CR>10(U/D/L/R)
Pol Surface Treatment	HC		-
Weight	88.6+/-3	g	max
D-IC	NT35532	-	
Inversion Method	Column	-	Dot/Column
LED Q’ty	6S3P	ea	String*Parallel
Power Consumption	White Patten: 1.25W +0.4W	w	Backlight + Logic

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	92.27	92.35	92.43	mm	(1)
	Vertical (V)	182.5	182.35	182.51	mm	
	Thickness (T)	-	2.7(w/o FPCA) -	2.95(w/o FPCA) 4.87(w/i FPCA,CG to Al-foil)	mm	
Active Area	Horizontal	83.94	84.24	84.54	mm	
	Vertical	149.46	149.76	150.06	mm	
Weight		85.6	88.6	91.6	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: **I-PEX 20613-039E**

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

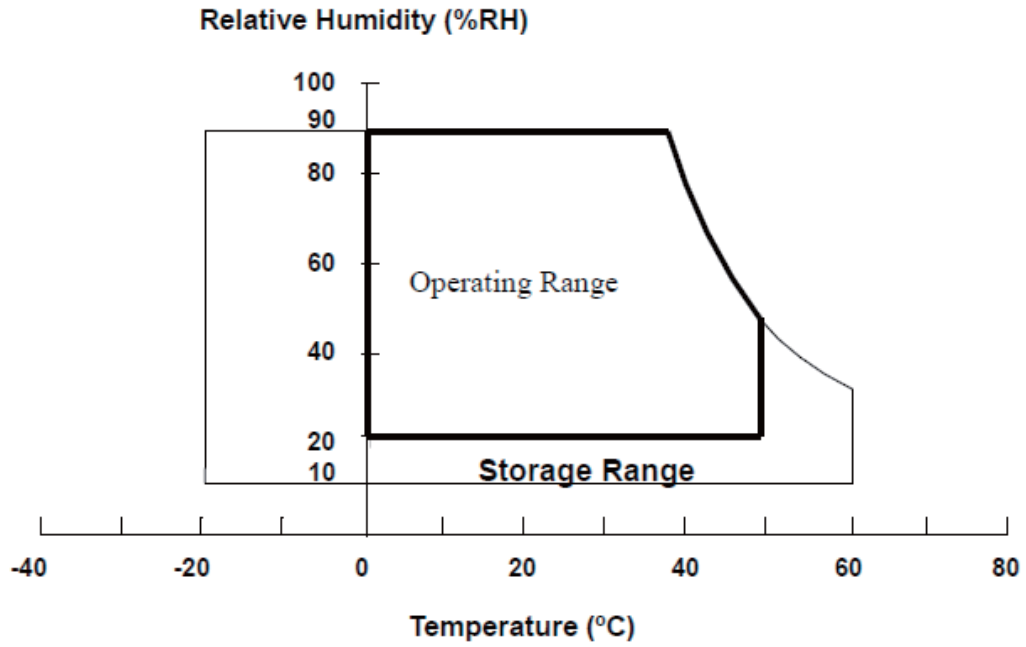
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be -10 ºC min. and 60 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

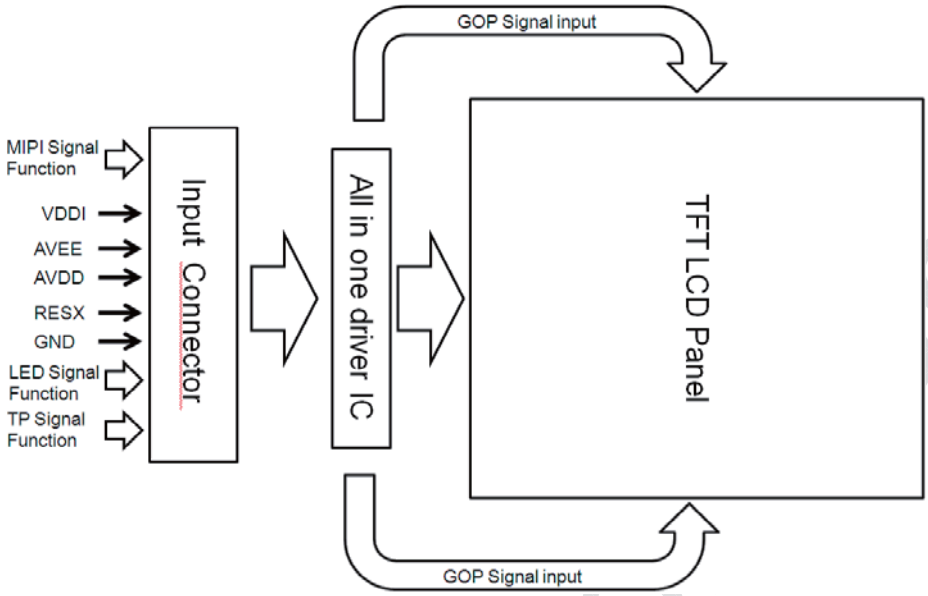
3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	**-0.3**	**+4.0**	V	(1)
Logic Input Voltage	-0.3	**-0.3**	**+4.0**	V	(1)
Converter Input Voltage	LED_VCCS	**-0.3**	**19.2**	V	(1)
Converter Control Signal Voltage	LED_PWM	**-0.3**	**5**	V	(1)
Converter Control Signal Voltage	LED_EN	**-0.3**	**5**	V	(1)

Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



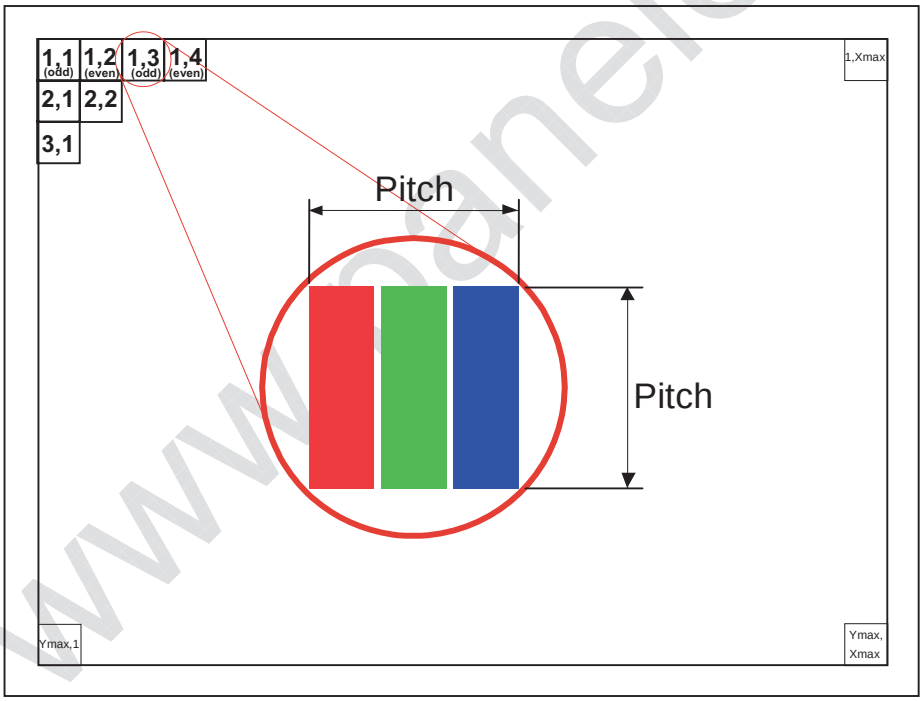
4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	TP-SCL	I2C CLOCK,TYP. 1.8V	
2	ESD_GND	ESD_GND	
3	TP-GND	Ground	
4	TP-RST	Reset Pin	
5	TP-AVDD	Analog Power supply, TYP. 3.3V	3.3V
6	TP-INT	Interrupt Pin	
7	TP-VDDIO	Power 1.8V (NC)	NC
8	TP-SDA	I2C data, TYP. 1.8V	
9	NC	NC Pin	
10	VLED	Anode for light bar	15.6V~19.2V
11	VLED	Anode for light bar	15.6V~19.2V
12	LED1	Catbode for light bar	
13	LED2	Catbode for light bar	
14	LED3	Catbode for light bar	
15	AVDD	6.0VDC Input	6V
16	AVDD	6.0VDC Input	6V
17	AVEE	-6.0VDC Input	-6V
18	AVEE	-6.0VDC Input	-6V
19	VDDI	1.8VDC Input	1.8V
20	VDDI	1.8VDC Input	1.8V
21	ID	Ground	
22	RESX	Device reset signal	1.8V

23	LEDPWM	PWM Control signal for LED driver	
24	GND	Ground	
25	D3_P	MIPI Differential data3 input(Positive)	
26	D3_N	MIPI Differential data3 input(Negative)	
27	GND	Ground	
28	D2_N	MIPI Differential data2 input(Negative)	
29	D2_P	MIPI Differential data2 input(Positive)	
30	GND	Ground	
31	CLK_P	MIPI Differential clock input(Positive)	
32	CLK_N	MIPI Differential clock input(Negative)	
33	GND	Ground	
34	D1_N	MIPI Differential data1 input(Negative)	
35	D1_P	MIPI Differential data1 input(Positive)	
36	GND	Ground	
37	D0_P	MIPI Differential data0 input(Positive)	
38	D0_N	MIPI Differential data0 input(Negative)	
39	GND	Ground	

Note (1) The first pixel is odd as shown in the following figure.



4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VDDI	1.7	1.8	1.9	V	(1)-
Positive Step-up Voltage		AVDD	5.8	-	6	V	(1)-
Negative Step-up Voltage		AVEE	-5.8	-	-6		
Ripple Voltage		V_{RP}		50		mV	(1)-
Inrush Current		I_{RUSH}			1.0	A	(1),(2)
Power Supply Current	Mosaic	Icc	-	220	240	mA	
	White	Icc	-	210	230	mA	

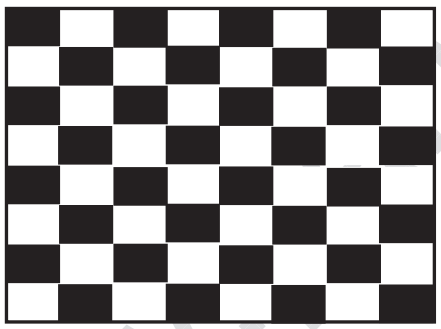
Note (1)) The specified current and power consumption are under the conditions at VSP = 6V, VSN = -6V,VDDI = 1.8V, T = 25°C, and fv = 60 Hz, at white pattern

Note (2) I_{RUSH}: the maximum current when AVDD & AVEE is rising

I_{IS}: the maximum current of the first 100ms after power-on

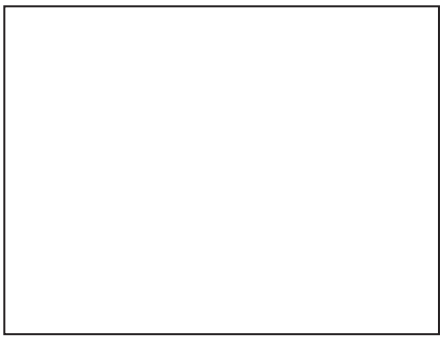
Measurement Conditions: Shown as the following figure. Test pattern: white.

a. Mosaic Pattern



Active Area

b. White Pattern



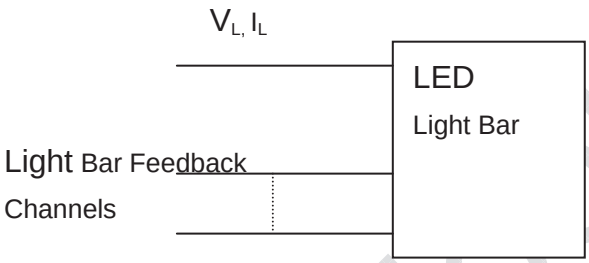
Active Area

4.3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	15.6	17.4	19.2	V	(1)(2) (Duty100%)
LED Light Bar Power Supply Current	I_L		60		mA	
Power Consumption	P_L			1.25	W	(3)
LED Life Time	L_{BL}	12000			Hrs	(4)

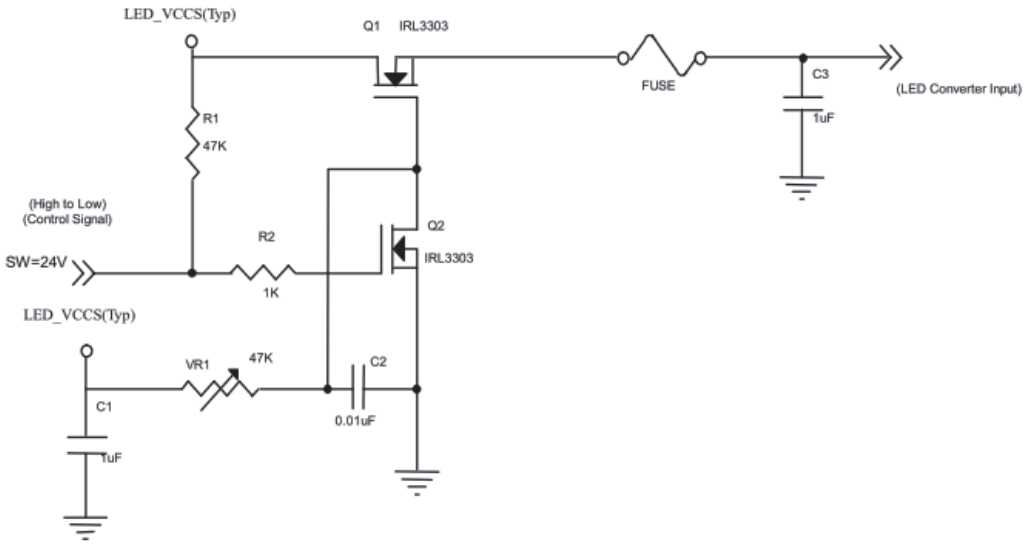
Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



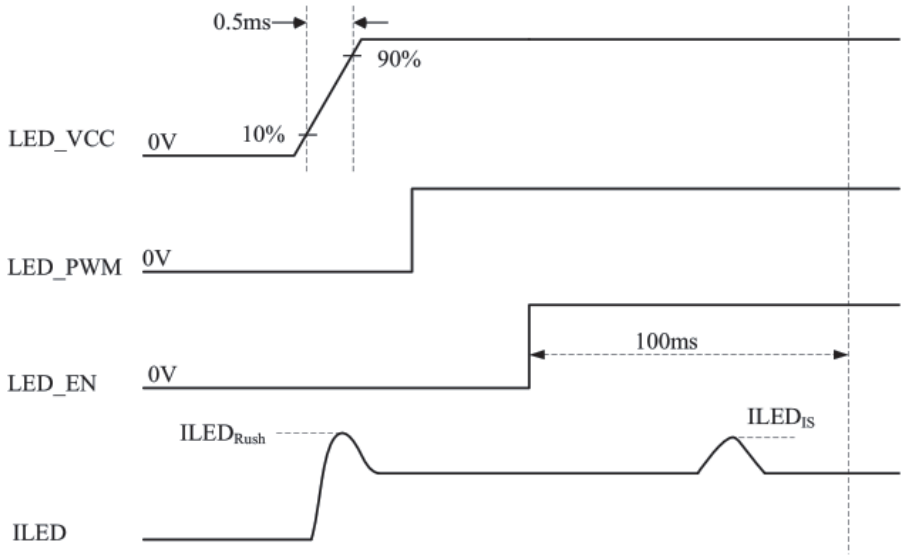
Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

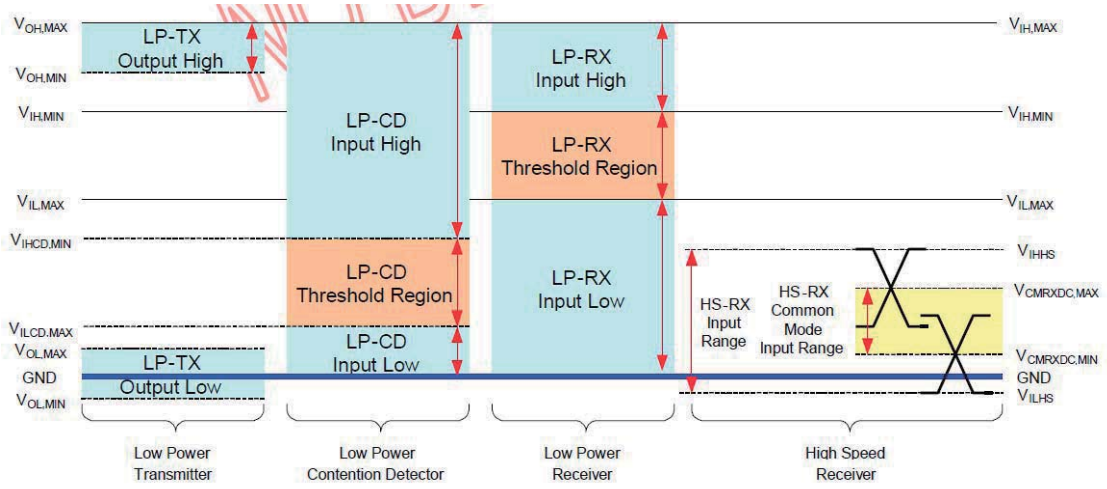
Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and IL = 20 mA(Per EA) until the brightness becomes ≦ 50% of its original value.



VLED rising time is 0.5ms



4.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS



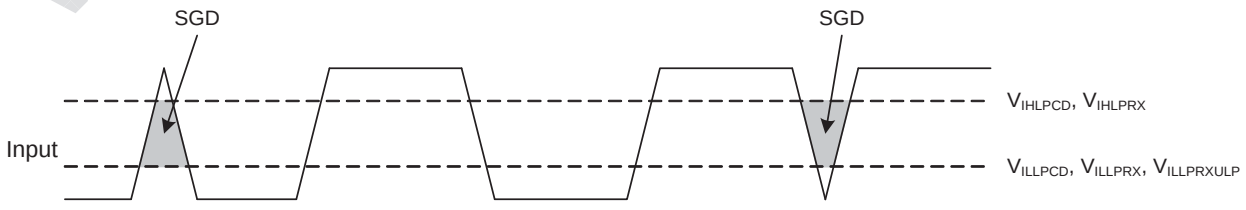
MIPI DC Diagram

4.4.1 DC Electrical Characteristic

4.4.1.1DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.7~1.9V, AVDD=5.8 to 6.0V, AVEE=-5.8~-6.0V,GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).
Note 2) DSI high speed is off.
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

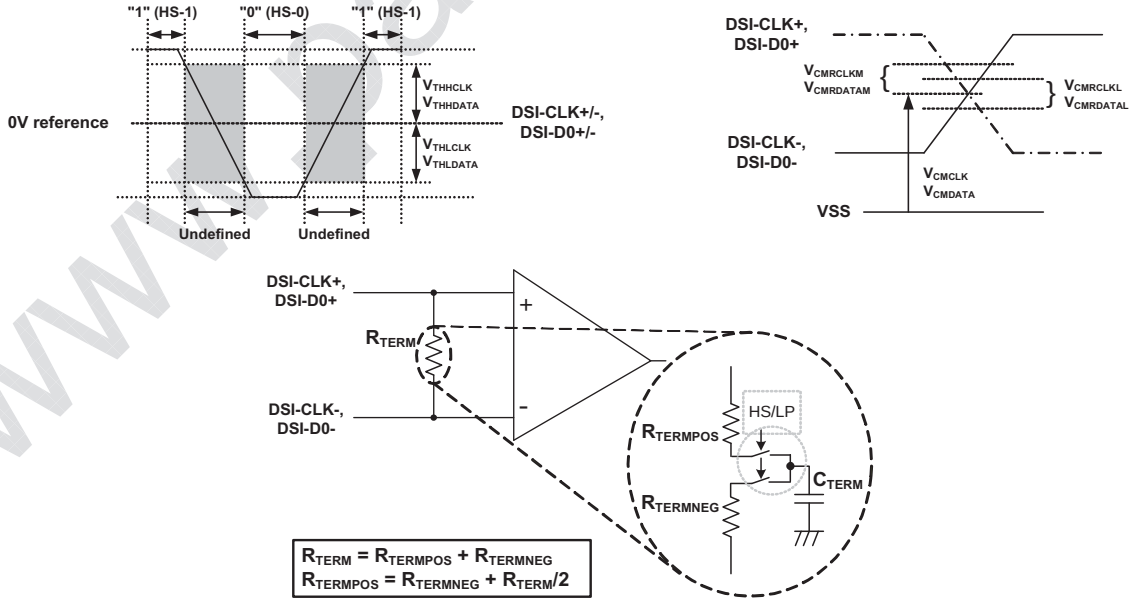


Spike/Glitch rejection-DSI

4.4.1.2DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) VDDI=1.7~1.9V, AVDD=5.8 to 6.0V, AVEE=-5.8~-6.0V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage)
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$.
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.



Differential voltage range, termination resistor and Common mode voltage

4.4.2 AC Electrical Characteristics

4.4.2.1 MIPI DSI Timing Characteristics

4.4.2.1.1 High Speed Mode

(*VDDI=1.7~1.9V, AVDD=5.8~6.0V,AVEE=-5.8~-6.0V, GND=0V,*Ta = -30 to 70°C)

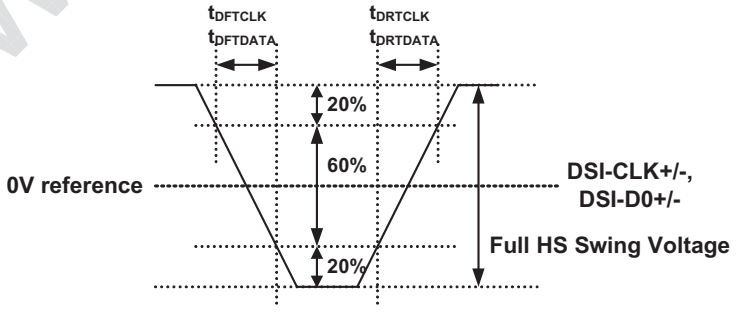
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs (UI = UI_{INSTA} = UI_{INSTB})	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.

DSI clock channel timing

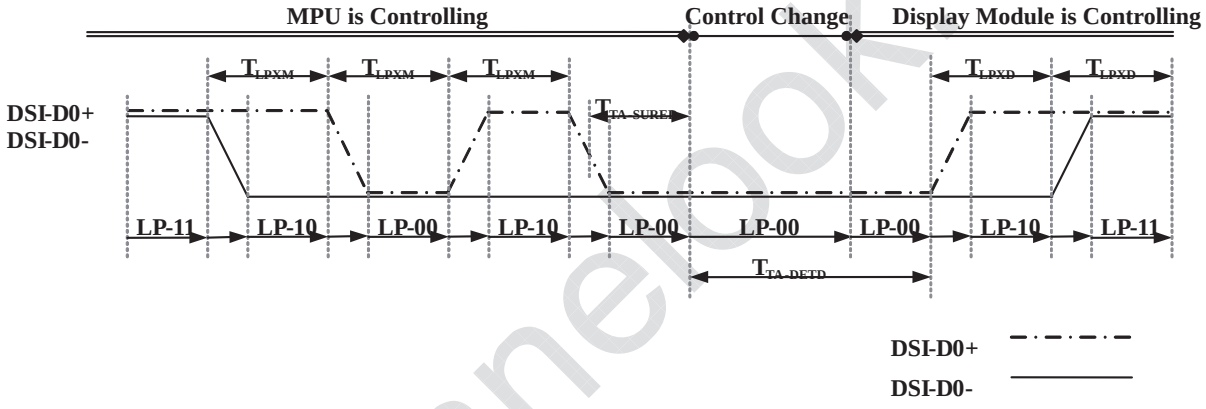


Rising and fall time on clock and data channel

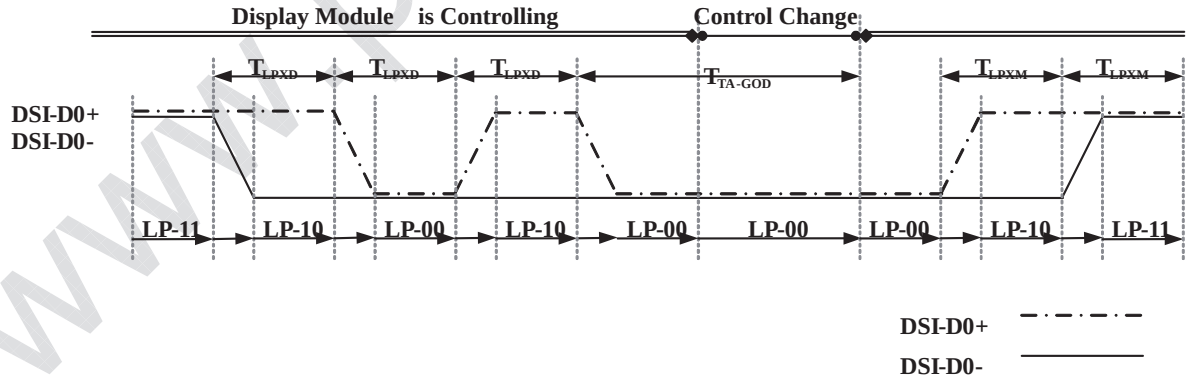
4.4.2.1.2 Low Power Mode

(*VDDI=1.7~1.9V, AVDD=5.8~6.0V,AVEE=-5.8~-6.0V, GND=0V,*Ta = -30 to 70°C)

ignal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	2xT_{LPXD}	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	5xT_{LPXD}	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	4xT_{LPXD}	-	-	ns	Output



Bus Turnaround (BAT) from MPU to display module Timing



Bus Turnaround (BAT) from display module to MPU Timing

4.4.2.1.3 DSI Bursts

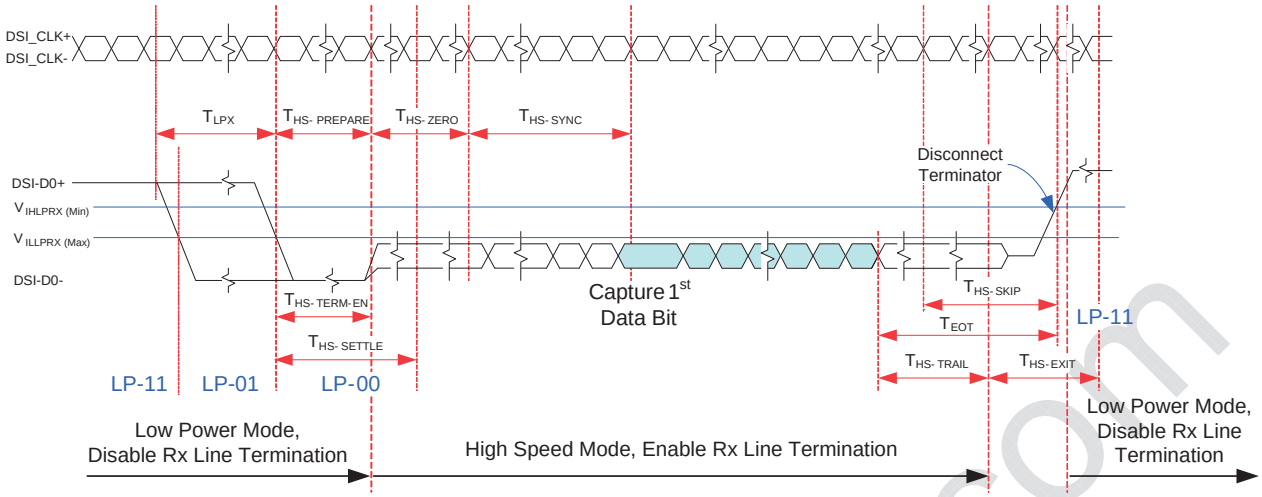
4.4.2.1.3 DSI Bursts

(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,*Ta = -30 to 70°C)

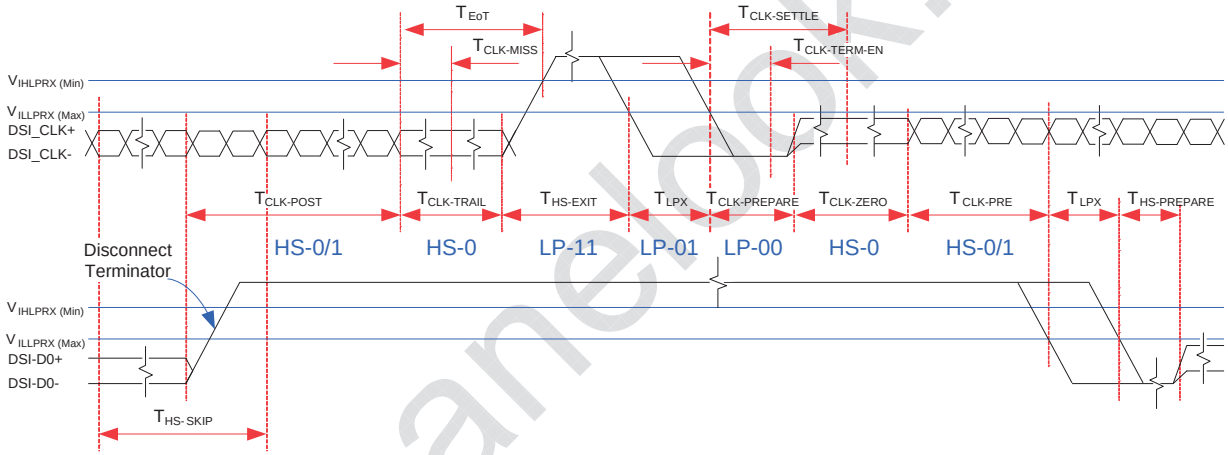
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as $T_{HS-EXIT}$ from each other in continuous clock mode. In discontinuous mode, the break is longer which account $T_{CLK-POS}$, $T_{CLK-TRAIL}$ and $T_{HS-EXIT}$, before activity in clock and data lanes again.

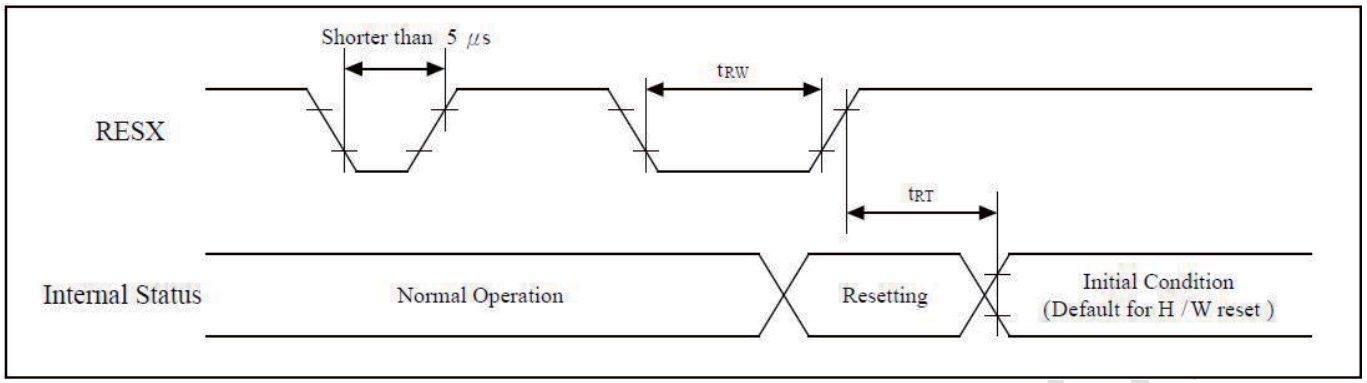


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

4.4.2.2 Reset Input Timing



Reset input timing

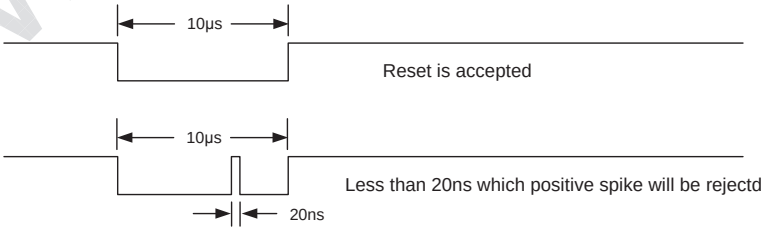
(*VDDI=1.7~1.9V, AVDD=5.8~6.0V,AVEE=-5.8~-6.0V GND=0V,*Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRW	Reset pulse duration	10	-	-	μs	Note
	tRT	Reset cancel	-	-	10	ms	Note
			-	-	120	ms	Note

Note) The reset cancel also includes required time for loading ID bytes, VCOM setting and other seeeings from EEPROM (or similar device) to registers.
This loading is done every time when there is HW reset cancel time (Trt) within 10ms after a rising edge of RESX.
Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

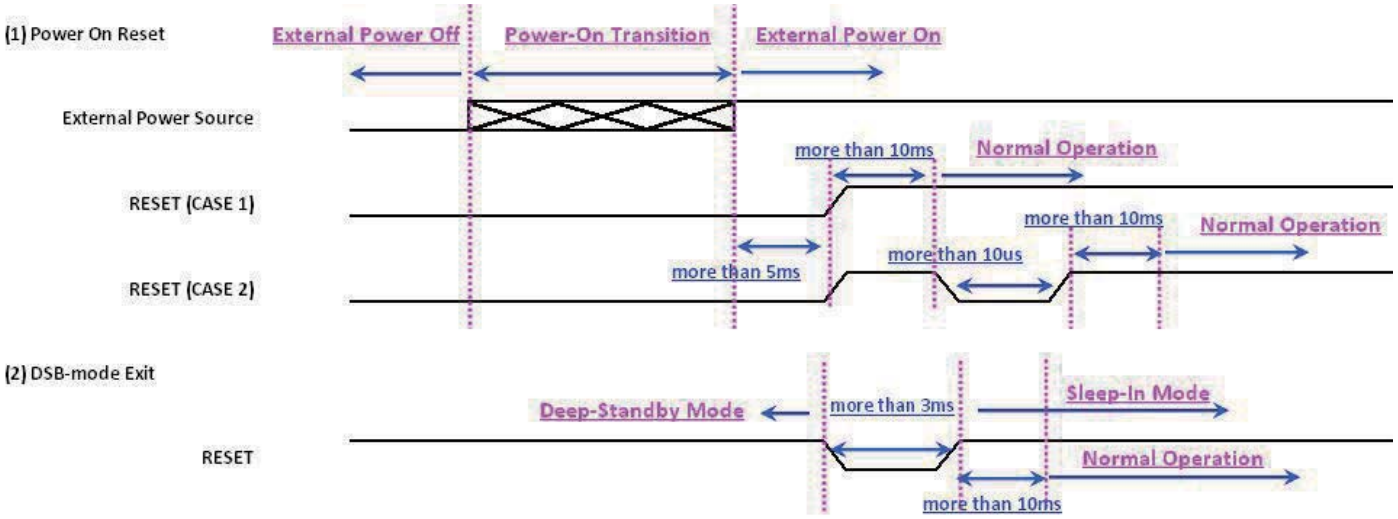
RESX	*Pulse Action*
Shorter than 5μs	*Reset Rejected*
Longer than 10μs	*Reset*
Between 5μs and 10μs	*Reset Start*

Note) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for H/W reset.
Note) Spike Rejection also applies during a valid reset pulse as shown below:
.



Note) When Reset applied during Sleep-In Mode
When Reset applied during Sleep-Out Mode
It is necessary to wait 10msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

4.4.2.3 Deep Standby Mode Timing



(*VDDI=1.7~1.9V, AVDD=5.8~6.0V,AVEE=-5.8~-6.0V, GND=0V*,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	$t_{discharge}$	Sleep in into DSTB delay time	-	-	100	ms	
	t_{rstlow}	Reset low pulse	3	-	-	ms	
	$t_{initial}$	Reset high to initial setting delay time	10	-	120	ms	

Note 1) $t_{\_discharge}$ suggested delay time over 100ms.

Note 2) $t_{\_initial}$ suggested delay time over 120ms..

4.5 MIPI interface (Mobile Industry Processing Interface)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode.

Note: The product only supports Video Mode operation.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

4.5.1 MIPI Lane Configuration

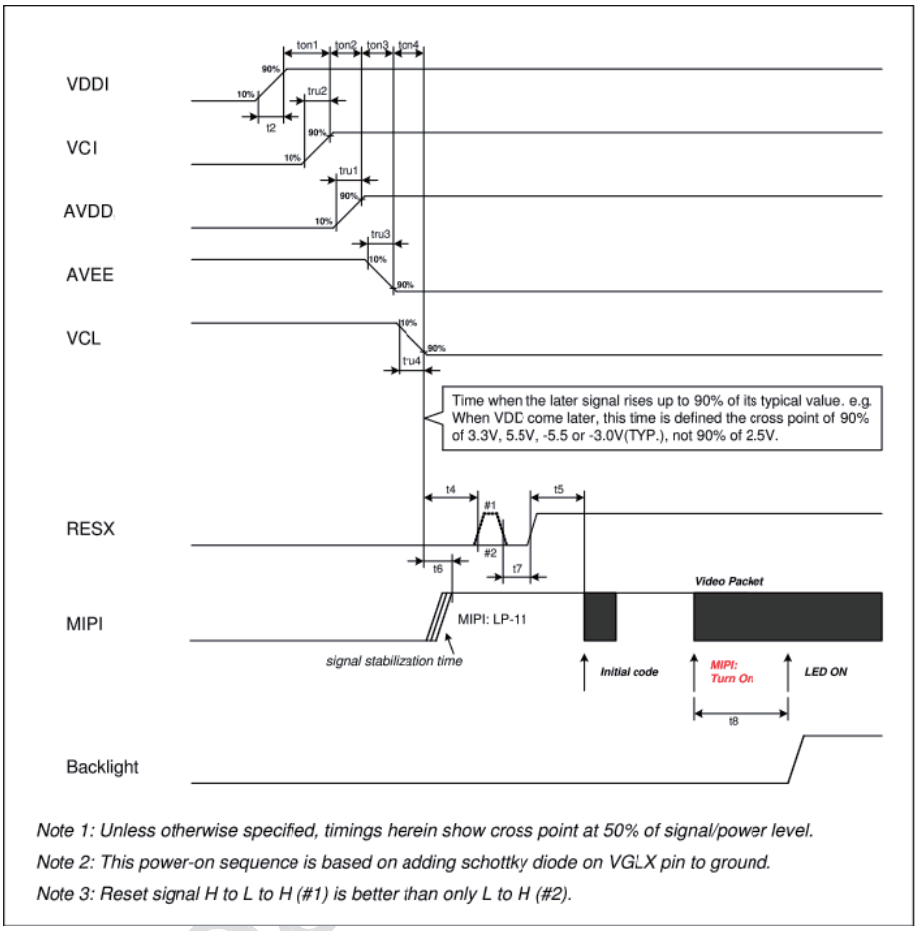
	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

The connection between host device and display module is as reference.

4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

a. Power On



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

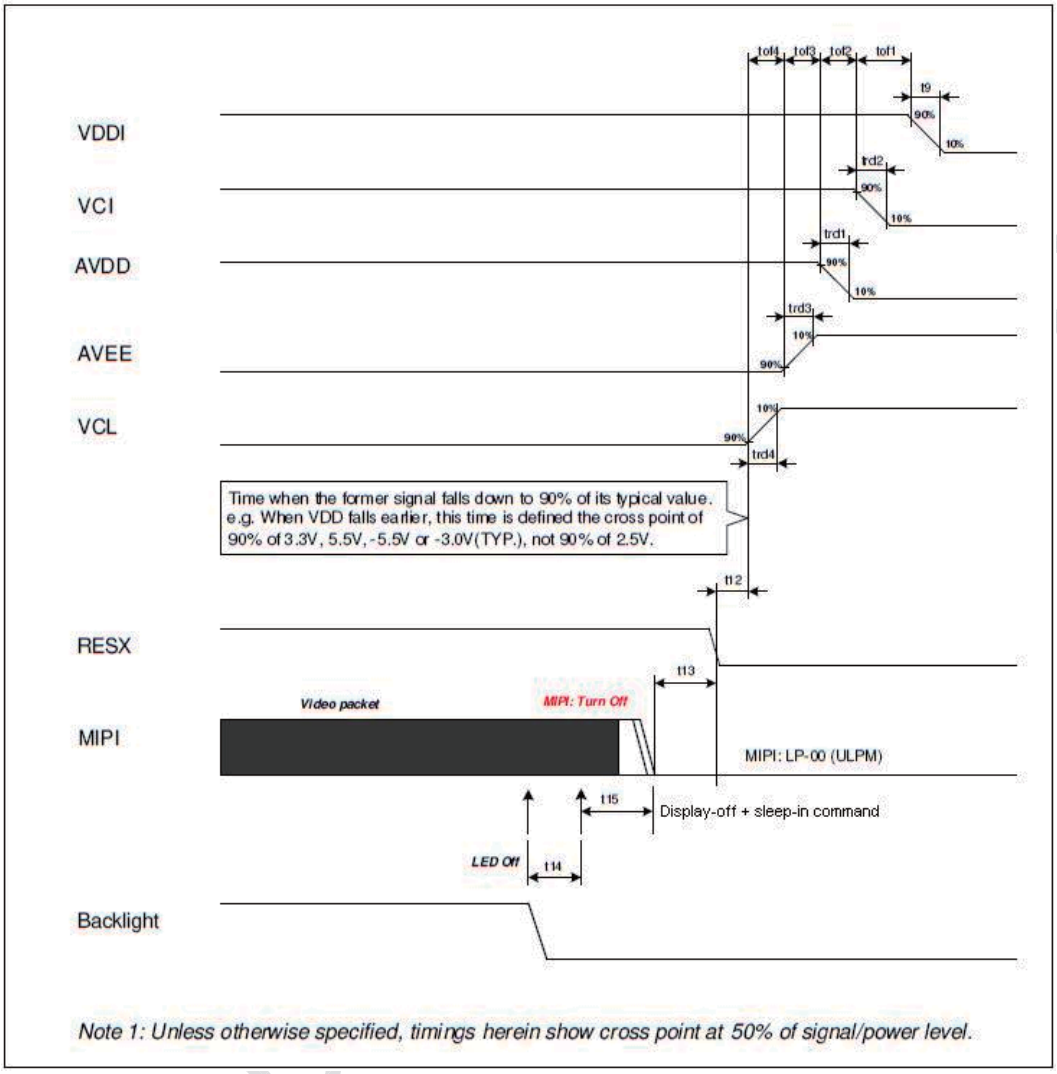
Note 2: This power-on sequence is based on adding schottky diode on VGLX pin to ground.

Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

Note 4 : If use 3 Power mode function (VDDI,AVDD,AVEE), Please to ignore the VCI

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		Min.
ton1		No limit		ton1	
ton2		0 (Note)		ton2	
ton3		No limit		ton3	
ton4		No limit		ton4	
t2			150	t2	
tru1			150	tru1	
tru2			150	tru2	
tru3			150	tru3	
tru4			150	tru4	
t4	40			t4	40
t5	120			t5	120
t6	>0		t4	t6	>0
t7	10			t7	10
t8	8			t8	8

a. Power On



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		Min.
t9	150	-	-	t9	150
tof1	-	No limit	-	tof1	-
tof2	-	0 (Note)	-	tof2	-
tof3	-	No limit	-	tof3	-
tof4	-	No limit	-	tof4	-
trd1	150	-	-	trd1	150
trd2	150	-	-	trd2	150
trd3	150	-	-	trd3	150
trd4	150	-	-	trd4	150
t12	>0	-	-	t12	>0
t13	>0	-	-	t13	>0
t14	>0	-	-	t14	>0
t15	>60	-	-	t15	>60

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

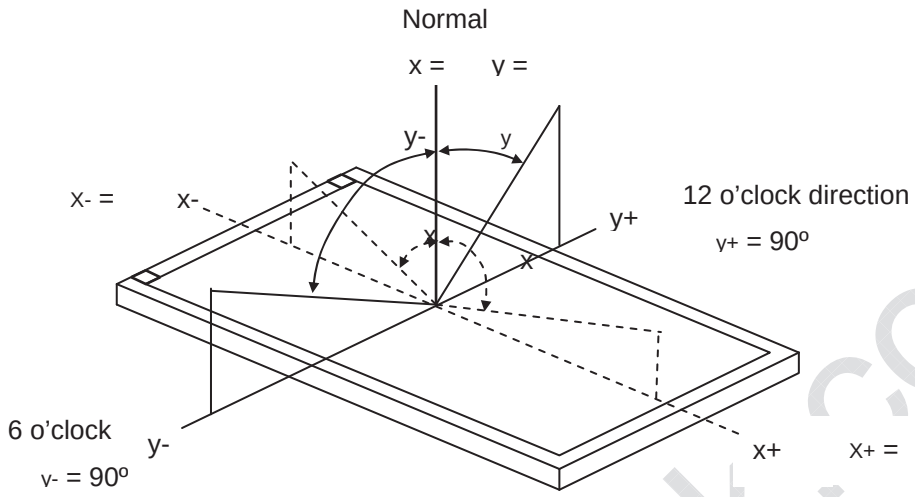
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	76	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	800	1000		-	(2), (5) ,(7)
Response Time		$T_{R+}T_F$			25	30	ms	(3) ,(7)
Center Point Luminance of White		L_{AVE}		300	350		cd/m^2	(4), (6) ,(7)
Color Chromaticity	Red	Rx		-0.03	0.63	+0.03	-	(1) ,(7)
		Ry			0.35		-	
	Green	Gx			0.31		-	
		Gy			0.62		-	
	Blue	Bx			0.15		-	
		By			0.06		-	
	White	Wx			0.305		-	
		Wy			0.325		-	
Viewing Angle	Horizontal	θ_x+	CR≥10	85			Deg.	(1),(5) , (7)
		θ_x-		85				
	Vertical	θ_Y+		85				
		θ_Y-		85				
White Variation of 13 Points		δW_{13p}	θ_x=0°, θ_Y =0°	70			%	(5),(6) , (7)

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

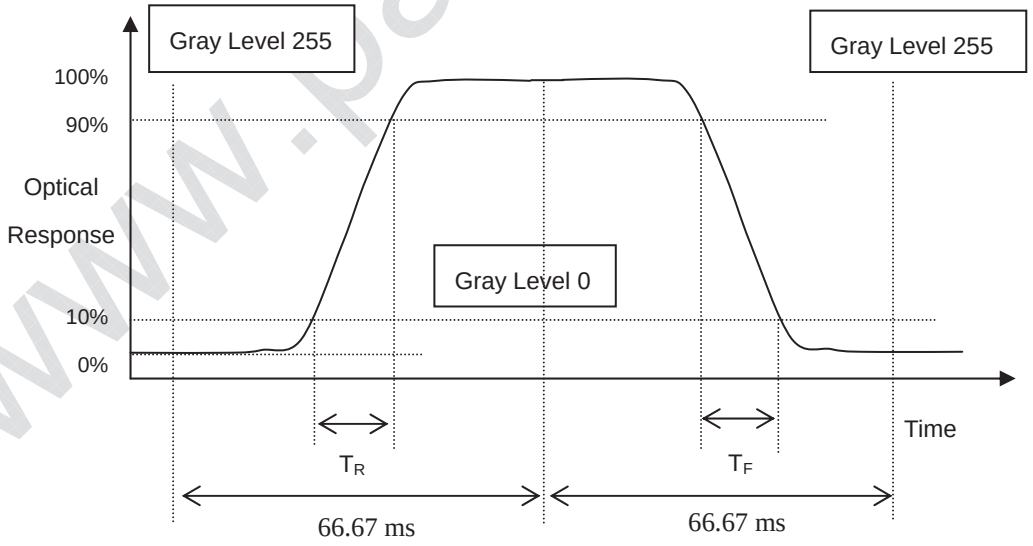
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



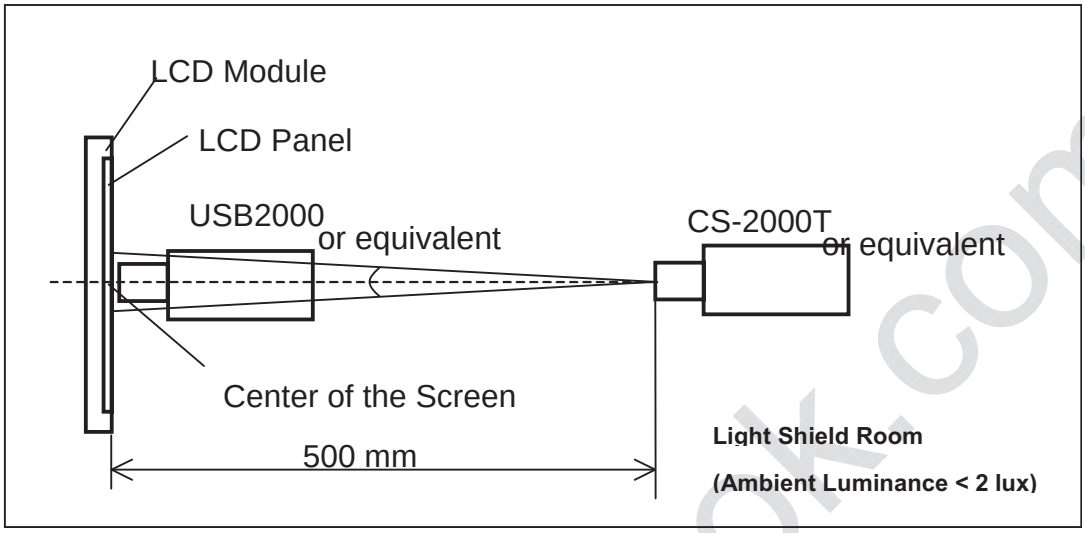
Note (4) Definition of Center Point Luminance of White (Lcp):

Measure the luminance of gray level 255 at point 1

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

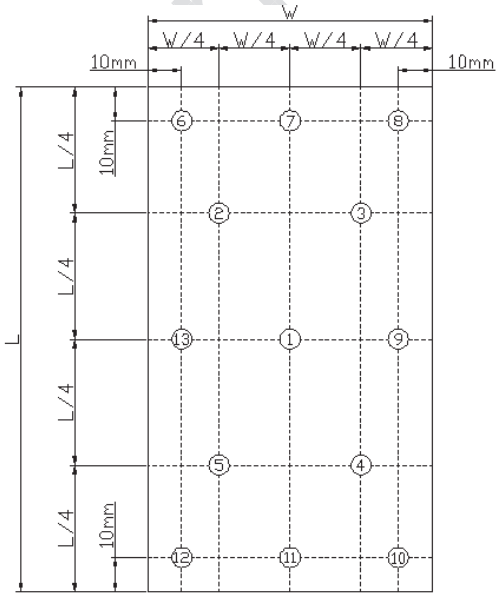
The LCD module should be stabilized at given temperature for 40 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW_{13p} = {Minimum [L (1) ~ L (13)] / Maximum [L (1) ~ L (13)]}*100%



Ⓧ : Test Point

X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

6. RELIABILITY TEST ITEM

Item	Test Conditions		Remark
High Temperature Storage	Ta = 60℃	240hrs	Note 1，Note 4
Low Temperature Storage	Ta = -20℃	240hrs	Note 1，Note 4
High Temperature Operation	Ts = 50℃	240hrs	Note 2，Note 4
Low Temperature Operation	Ta = -10℃	240hrs	Note 1，Note 4
Operate at High Temperature and Humidity	+40 ℃ , 90%RH	240hrs	Note 4
Storage at High Temperature and Humidity	+50℃, 90%RH	240hrs	Note 4
Thermal Shock	-20℃ /30 min ~ +/60 min for a total 100 cycles, Start with cold temperature and end with high temperature.		Note 4
Vibration Test	(non-operation) / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z		
Mechanical Shock	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z		
Electro Static Discharge	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±4KV Condition 2 : Air Discharge, ±8KV		Note 5

Note 1: Ta is the ambient temperature of samples.

Note 2: Ts is the temperature of panel’ s surface.

Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don’t guarantee all of the cosmetic specification.

Note 4: Before cosmetic and function test, the product must have enough recovery time,

Note 5: Standard is Class C.

7. PACKING

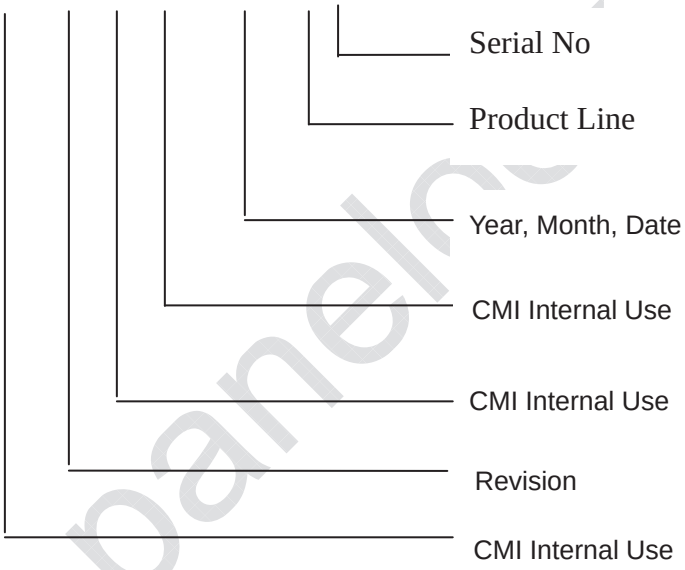
7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: **P068HFB-DK1**

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



(d) Production Location: MADE IN XXXX. XXXX stands for production location.

(e) UL logo: "XXXX" especially stands for panel manufactured by INX China satisfying UL requirement.

"LEOO" "COCKN" & "CANO" is the INX's UL factory code for Ningbo factory

CT Label

CPXP (A Code) : DUBE

7.2 CARTON

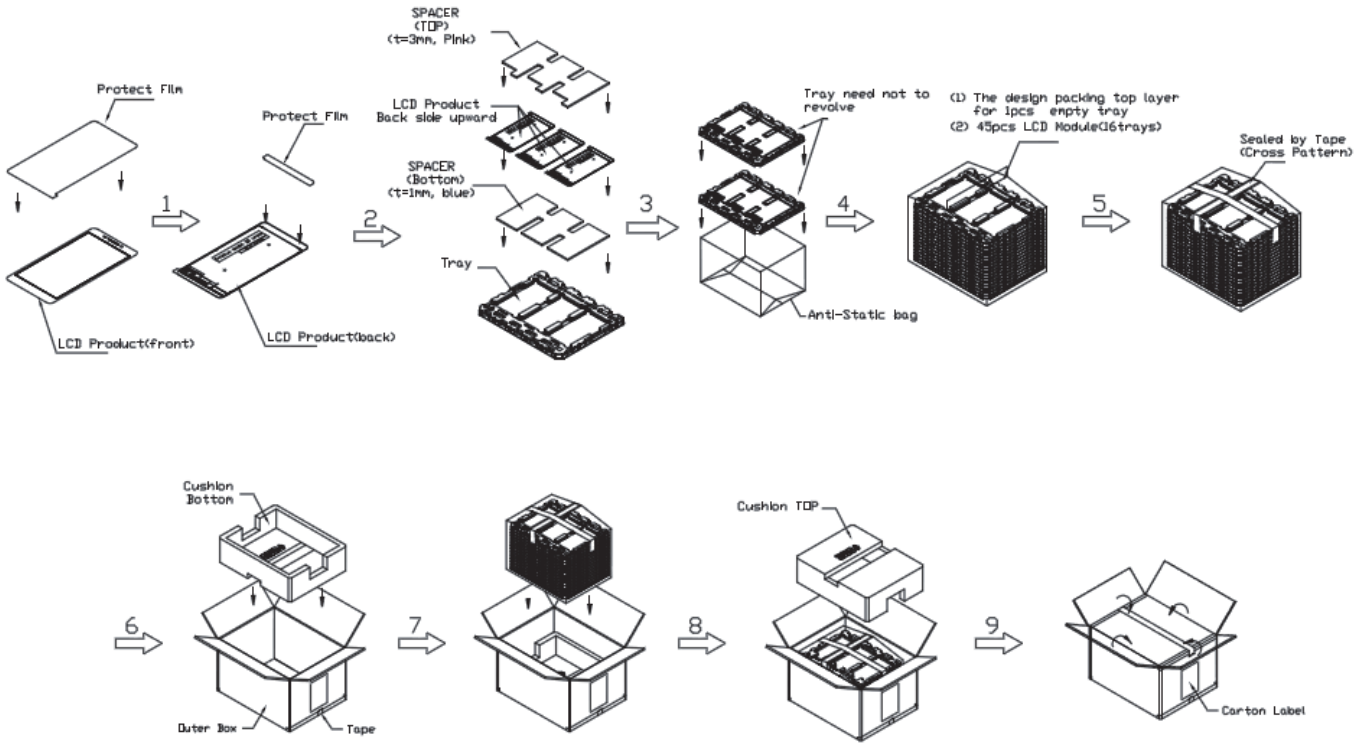
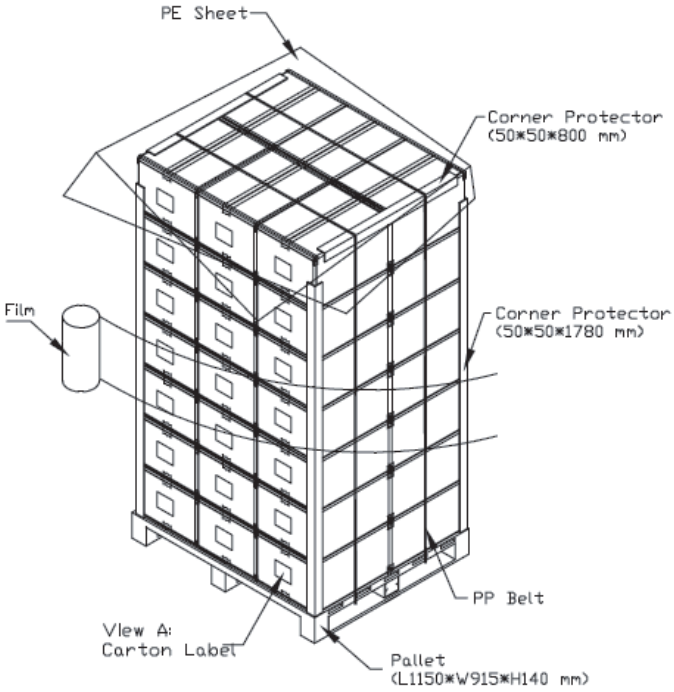


Figure. 7-1 Packing method

7.3 PALLET

Sea / Land Transportation
(40ft /40ft HQ Container)



Air Transportation

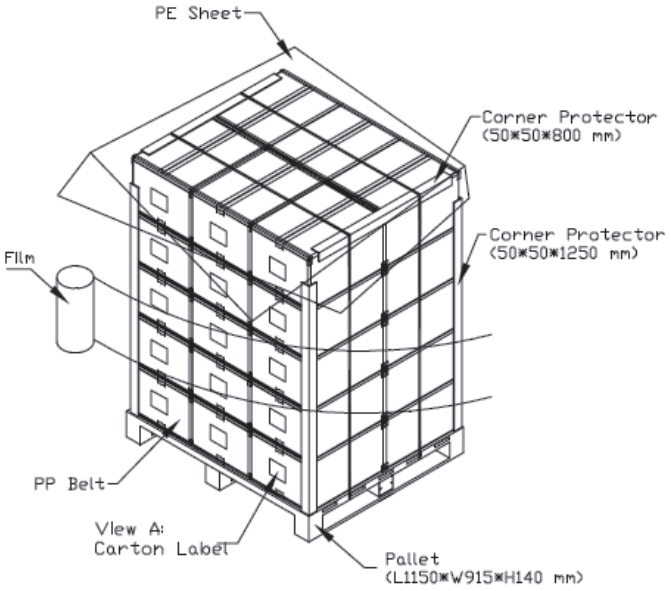


Figure. 7-2 Packing method

7.4 UN-PACKING

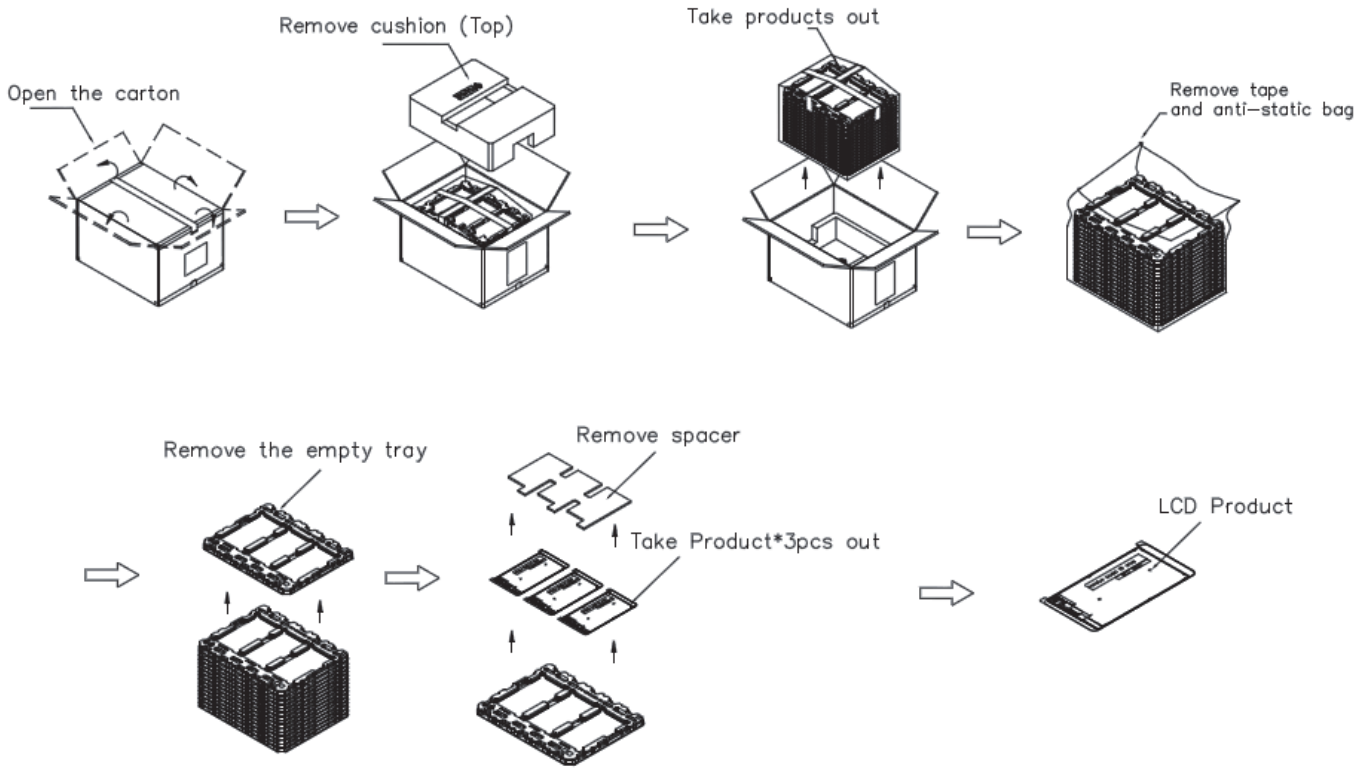


Figure. 7-3 Un-Packing method

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

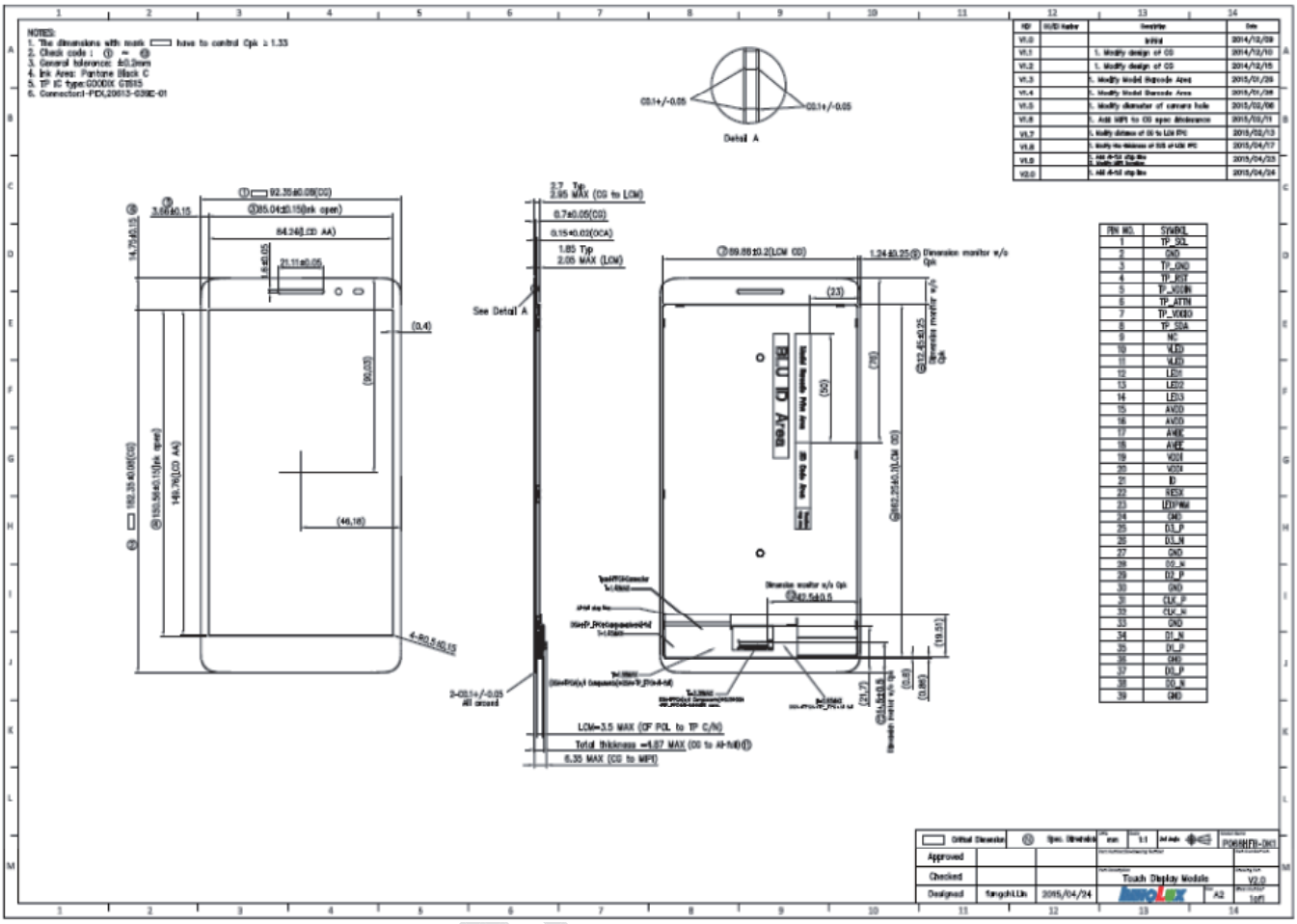
8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit

Appendix 1. OUTLINE DRAWING



Initial code

Command Set	Function	Register	Value	Remark
CMD1	Switch to CMD2_Page0 (Power,Gamma)	FFh	0x01	
CMD2 Page 0	Don't reload MTP	FBh	0x01	
	Power (Regulator/Pump) Setting	00h	0x01	
		01h	0x44	
		02h	0x59	
		04h	0x0C	
		05h	0x2A	
		06h	0x55	
		07h	0x41	
		0Dh	0x98	
		0Eh	0x98	
		0Fh	0x60	
		10h	0x03	
		11h	0x50	
		12h	0x5A	
		15h	0x60	
		16h	0x17	
		17h	0x17	
		2Bh	0x00	
		68h	0x13	
	Gamma R+	75h	0x00	
		76h	0x35	
		77h	0x00	
		78h	0x5A	
		79h	0x00	
		7Ah	0x89	
		7Bh	0x00	
		7Ch	0xA7	
		7Dh	0x00	
		7Eh	0xBE	

		7Fh	0x00	
		80h	0xD1	
		81h	0x00	
		82h	0xE1	
		83h	0x00	
		Register	Value	Remark
		84h	0xF1	
		85h	0x00	
		86h	0xFF	
		87h	0x01	
		88h	0x2C	
		89h	0x01	
		8Ah	0x50	
		8Bh	0x01	
		8Ch	0x88	
		8Dh	0x01	
		8Eh	0xB5	
		8Fh	0x01	
		90h	0xFC	
		91h	0x02	
		92h	0x34	
		93h	0x02	
		94h	0x36	
		95h	0x02	
		96h	0x6B	
		97h	0x02	
		98h	0xA6	
		99h	0x02	
		9Ah	0xCA	
		9Bh	0x02	
		9Ch	0xFC	
		9Dh	0x03	
		9Eh	0x1D	

		9Fh	0x03	
		A0h	0x47	
		A2h	0x03	
		A3h	0x55	
		A4h	0x03	
		A5h	0x63	
		A6h	0x03	
		A7h	0x73	
		A9h	0x03	
		AAh	0x84	
CMD2 Page0	Gamma R+	ABh	0x03	
		ACh	0x95	
		ADh	0x03	
		AEh	0xA6	
		AFh	0x03	
		B0h	0xB9	
		B1h	0x03	
		B2h	0xD2	
	Gamma R -	B3h	0x00	
		B4h	0x0D	
		B5h	0x00	
		B6h	0x5A	
		B7h	0x00	
		B8h	0x89	
		B9h	0x00	
		BAh	0xA7	
		BBh	0x00	
		BCh	0xBE	
		BDh	0x00	
		BEh	0xD1	
		BFh	0x00	
		C0h	0xE1	
		C1h	0x00	

		C2h	0xF1	
		C3h	0x00	
		C4h	0xFF	
		C5h	0x01	
		C6h	0x2C	
		C7h	0x01	
		C8h	0x50	
		C9h	0x01	
		CAh	0x88	
		CBh	0x01	
		CCh	0xB5	
		CDh	0x01	
		CEh	0xFC	
		CFh	0x02	
CMD2 Page0	Gamma R -	D0h	0x34	
		D1h	0x02	
		D2h	0x36	
		D3h	0x02	
		D4h	0x6B	
		D5h	0x02	
		D6h	0xA6	
		D7h	0x02	
		D8h	0xCA	
		D9h	0x02	
		DAh	0xFC	
		DBh	0x03	
		DCh	0x1D	
		DDh	0x03	
		DEh	0x47	
		DFh	0x03	
		E0h	0x55	
		E1h	0x03	
		E2h	0x63	

		E3h	0x03	
		E4h	0x73	
		E5h	0x03	
		E6h	0x84	
		E7h	0x03	
		E8h	0x95	
		E9h	0x03	
		EAh	0xA6	
		EBh	0x03	
		ECh	0xB9	
		EDh	0x03	
		EEh	0xD2	
	Gamma G +	EFh	0x00	
		F0h	0x35	
		F1h	0x00	
		F2h	0x5A	
		F3h	0x00	
		F4h	0x89	
CMD2 Page 0	Gamma G +	F5h	0x00	
		F6h	0xA7	
		F7h	0x00	
		F8h	0xBE	
		F9h	0x00	
		FAh	0xD1	
		FFh	0x02	
		FBh	0x01	
		00h	0x00	
		01h	0xE1	
CMD2 Page 1	Switch to CMD2_Page1(Gamma)	02h	0x00	
	Don't reload MTP	03h	0xF1	
	Gamma G +	04h	0x00	
		05h	0xFF	
		06h	0x01	

		07h	0x2C	
		08h	0x01	
		09h	0x50	
		0Ah	0x01	
		0Bh	0x88	
		0Ch	0x01	
		0Dh	0xB5	
		0Eh	0x01	
		0Fh	0xFC	
		10h	0x02	
		11h	0x34	
		12h	0x02	
		13h	0x36	
		14h	0x02	
		15h	0x6B	
		16h	0x02	
		17h	0xA6	
		18h	0x02	
		19h	0xCA	
		1Ah	0x02	
		1Bh	0xFC	
		1Ch	0x03	
CMD2 Page 1	Gamma G +	1Dh	0x1D	
		1Eh	0x03	
		1Fh	0x47	
		20h	0x03	
		21h	0x55	
		22h	0x03	
		23h	0x63	
		24h	0x03	
		25h	0x73	
		26h	0x03	
		27h	0x84	

		28h	0x03	
		29h	0x95	
		2Ah	0x03	
		2Bh	0xA6	
		2Dh	0x03	
		2Fh	0xB9	
		30h	0x03	
		31h	0xD2	
	Gamma G -	32h	0x00	
		33h	0x0D	
		34h	0x00	
		35h	0x5A	
		36h	0x00	
		37h	0x89	
		38h	0x00	
		39h	0xA7	
		3Ah	0x00	
		3Bh	0xBE	
		3Dh	0x00	
		3Fh	0xD1	
		40h	0x00	
		41h	0xE1	
		42h	0x00	
		43h	0xF1	
		44h	0x00	
		45h	0xFF	
CMD2 Page 1	Gamma G -	46h	0x01	
		47h	0x2C	
		48h	0x01	
		49h	0x50	
		4Ah	0x01	
		4Bh	0x88	
		4Ch	0x01	

		4Dh	0xB5	
		4Eh	0x01	
		4Fh	0xFC	
		50h	0x02	
		51h	0x34	
		52h	0x02	
		53h	0x36	
		54h	0x02	
		55h	0x6B	
		56h	0x02	
		58h	0xA6	
		59h	0x02	
		5Ah	0xCA	
		5Bh	0x02	
		5Ch	0xFC	
		5Dh	0x03	
		5Eh	0x1D	
		5Fh	0x03	
		60h	0x47	
		61h	0x03	
		62h	0x55	
		63h	0x03	
		64h	0x63	
		65h	0x03	
		66h	0x73	
		67h	0x03	
		68h	0x84	
		69h	0x03	
		6Ah	0x95	
		6Bh	0x03	
CMD2 Page 1	Gamma G -	6Ch	0xA6	
		6Dh	0x03	
		6Eh	0xB9	

		6Fh	0x03	
		70h	0xD2	
	Gamma B +	71h	0x00	
		72h	0x35	
		73h	0x00	
		74h	0x5A	
		75h	0x00	
		76h	0x89	
		77h	0x00	
		78h	0xA7	
		79h	0x00	
		7Ah	0xBE	
		7Bh	0x00	
		7Ch	0xD1	
		7Dh	0x00	
		7Eh	0xE1	
		7Fh	0x00	
		80h	0xF1	
		81h	0x00	
		82h	0xFF	
		83h	0x01	
		84h	0x2C	
		85h	0x01	
		86h	0x50	
		87h	0x01	
		88h	0x88	
		89h	0x01	
		8Ah	0xB5	
		8Bh	0x01	
		8Ch	0xFC	
		8Dh	0x02	
		8Eh	0x2A	
		8Fh	0x02	

		90h	0x2C	
CMD2 Page 1	Gamma B +	91h	0x02	
		92h	0x6B	
		93h	0x02	
		94h	0xA6	
		95h	0x02	
		96h	0xCA	
		97h	0x02	
		98h	0xFC	
		99h	0x03	
		9Ah	0x1D	
		9Bh	0x03	
		9Ch	0x47	
		9Dh	0x03	
		9Eh	0x55	
		9Fh	0x03	
		A0h	0x63	
		A2h	0x03	
		A3h	0x73	
		A4h	0x03	
		A5h	0x84	
		A6h	0x03	
		A7h	0x95	
		A9h	0x03	
		AAh	0xA6	
		ABh	0x03	

		ACh	0xB9	
		ADh	0x03	
		AEh	0xD2	
	Gamma B -	AFh	0x00	
		B0h	0x0D	
		B1h	0x00	
		B2h	0x5A	
		B3h	0x00	
		B4h	0x89	
		B5h	0x00	
		B6h	0xA7	
		B7h	0x00	
CMD2 Page 1	Gamma B -	B8h	0xBE	
		B9h	0x00	
		BAh	0xD1	
		BBh	0x00	
		BCh	0xE1	
		BDh	0x00	
		BEh	0xF1	
		BFh	0x00	
		C0h	0xFF	
		C1h	0x01	
		C2h	0x2C	
		C3h	0x01	
		C4h	0x50	
		C5h	0x01	

		C6h	0x88	
		C7h	0x01	
		C8h	0xB5	
		C9h	0x01	
		CAh	0xFC	
		CBh	0x02	
		CCh	0x34	
		CDh	0x02	
		CEh	0x36	
		CFh	0x02	
		D0h	0x6B	
		D1h	0x02	
		D2h	0xA6	
		D3h	0x02	
		D4h	0xCA	
		D5h	0x02	
		D6h	0xFC	
		D7h	0x03	
		D8h	0x1D	
		D9h	0x03	
		DAh	0x47	
		DBh	0x03	
		DCh	0x55	
CMD2 Page 1	Gamma B -	DDh	0x03	
		DEh	0x63	
		DFh	0x03	

		E0h	0x73	
		E1h	0x03	
		E2h	0x84	
		E3h	0x03	
		E4h	0x95	
		E5h	0x03	
		E6h	0xA6	
		E7h	0x03	
		E8h	0xB9	
		E9h	0x03	
		EAh	0xD2	
CMD2 Page 4	Switch to CMD2_Page4 (GOA Timing)	FFh	0x05	
	Don't reload MTP	FBh	0x01	
	CGOUT Pin Register Table	00h	0x40	
		01h	0x40	
		02h	0x40	
		03h	0x40	
		04h	0x40	
		05h	0x07	
		06h	0x17	
		07h	0x19	
		08h	0x1B	
		09h	0x1D	
		0Ah	0x1F	
		0Bh	0x21	
		0Ch	0x26	

		0Dh	0x28	
		0Eh	0x09	
		0Fh	0x38	
		10h	0x38	
		11h	0x0F	
		12h	0x40	
		13h	0x40	
		14h	0x40	
CMD2 Page 4	CGOUT Pin Register Table	15h	0x40	
		16h	0x40	
		17h	0x40	
		18h	0x40	
		19h	0x06	
		1Ah	0x16	
		1Bh	0x18	
		1Ch	0x1A	
		1Dh	0x1C	
		1Eh	0x1E	
		1Fh	0x20	
		20h	0x26	
		21h	0x28	
		22h	0x08	
		23h	0x38	
		24h	0x38	
		25h	0x0E	
		26h	0x40	

		27h	0x40	
		28h	0x40	
		29h	0x40	
		2Ah	0x40	
		2Bh	0x40	
		2Dh	0x40	
		2Fh	0x08	
		30h	0x20	
		31h	0x1E	
		32h	0x1C	
		33h	0x1A	
		34h	0x18	
		35h	0x16	
		36h	0x26	
		37h	0x28	
		38h	0x06	
		39h	0x38	
		3Ah	0x38	
		3Bh	0x0E	
CMD2 Page 4	CGOUT Pin Register Table	3Dh	0x40	
		3Fh	0x40	
		40h	0x40	
		41h	0x40	
		42h	0x40	
		43h	0x40	
		44h	0x40	

		45h	0x09	
		46h	0x21	
		47h	0x1F	
		48h	0x1D	
		49h	0x1B	
		4Ah	0x19	
		4Bh	0x17	
		4Ch	0x26	
		4Dh	0x28	
		4Eh	0x07	
		4Fh	0x38	
		50h	0x38	
		51h	0x0F	
		52h	0x40	
		53h	0x40	
	GIP Timing Register Setting	54h	0x06	
		55h	**0x18**	
		59h	0x1B	
		5Bh	0x02	
		5Ch	0x02	
		5Dh	0x01	
		5Eh	**0x23**	
		62h	0x19	
		63h	0x02	
		64h	0x02	
		66h	0x48	

		67h	0x11	
		68h	0x02	
		69h	0x12	
		6Ah	0x04	
CMD2 Page 4	GIP Timing Register Setting	6Bh	**0x2A**	
		6Ch	0x08	
		6Dh	0x18	
		6Fh	0x3C	
		70h	0x03	
		72h	0x22	
		73h	0x22	
		7Dh	0x01	
		7Eh	0x00	
		7Fh	0x00	
		80h	0x00	
		81h	0x00	
		85h	0xFC	
		86h	0xFC	
	GIP Power On/Off Sequence	B7h	0x00	
		BDh	0xA6	
		BEh	0x08	
		BFh	0x12	
		C8h	0x00	
		C9h	0x00	
		CAh	0x00	
		CBh	0x00	

		CCh	0x09	
		CFh	0x88	
		D0h	0x00	
		D1h	0x00	
		D2h	0x00	
		D3h	0x00	
		D4h	0x40	
		D5h	0x11	
	RTN	90h	0x78	
	BP,FP Setting	91h	0x0A	
		92h	0x1E	
	VSOUT, HSOUT	D7h	0x31	
		D8h	0x7E	
		FFh	0xEE	
		30h	0x60	
CMD1	Switch to CMD1	FFh	0x00	
	SLPOUT	11h		
		DELAY	120ms	
	DISPON	29h		
	VBP Setting	D3h	0x1E	
	VFP Setting	D4h	0x0A	
	HBP Setting	D5h	0x1E	
	HFP Setting	D6h	0x0A	