Lab 2

Interface and Channel Design for Transaction Level Modeling

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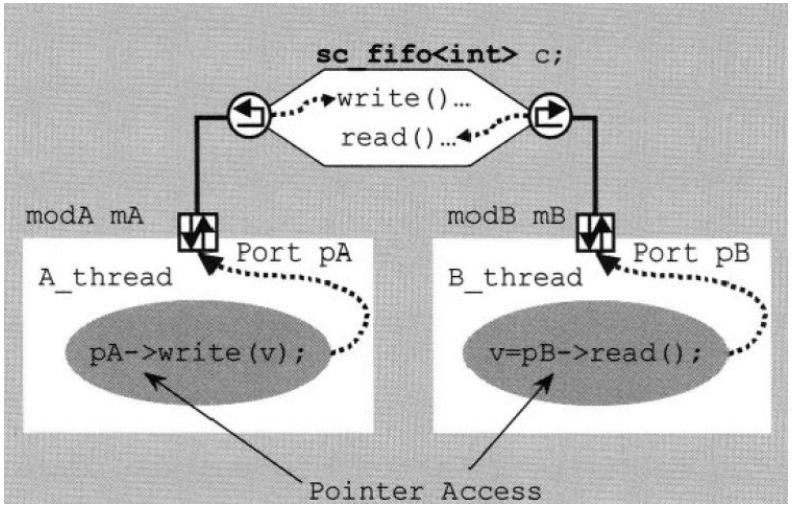
Outline

- Review: Ports, Channels, and Interfaces
- Transaction Level Modeling
- Lab 2 Practice: Simple FIFO / Perf

Review:
Ports, Channels, and Interfaces

Definition

- Interface : Abstract class
- Channel : Implementation class
- Port : Interface pointer



Pre-defined SystemC Interface

- sc_fifo_in_if
- sc_fifo_out_if
- sc_signal_in_if
  - sc_in ≈ *(sc_port<sc_signal_in_if>)
- sc_signal_out_if
  - sc_out ≈ *(sc_port<sc_signal_out_if>)
- sc_signal_inout_if
  - sc_inout ≈ *(sc_port<sc_signal_inout_if>)
- ….

Why do we customize interface?

- There are so many predefined interfaces for functional/architecture modeling, why?
  - Reduce design complexity, increase simulation speed, etc.
- Abstraction of communication, encapsulate low-level details
  - Physical: define higher level data types
  - Temporal: hide protocol details
  - Special purpose: debug supporting functions, etc.
- Help to refine models smoothly

Guidelines for Interface Design*

- Minimize the number of interfaces
- Layer specialized interfaces on more general interfaces and use the more general interfaces as much as possible to increase opportunities for channel reuse.
- Use class inheritance to group common interface methods and to reduce code duplication.
- Create a unified interface class from separate interfaces classes using C++ multiple inheritance.

*T. Grotker, S. Liao, G. Martin, S. Swan, System Level Design with SystemC, Kluwer Academic Publisher, 2002

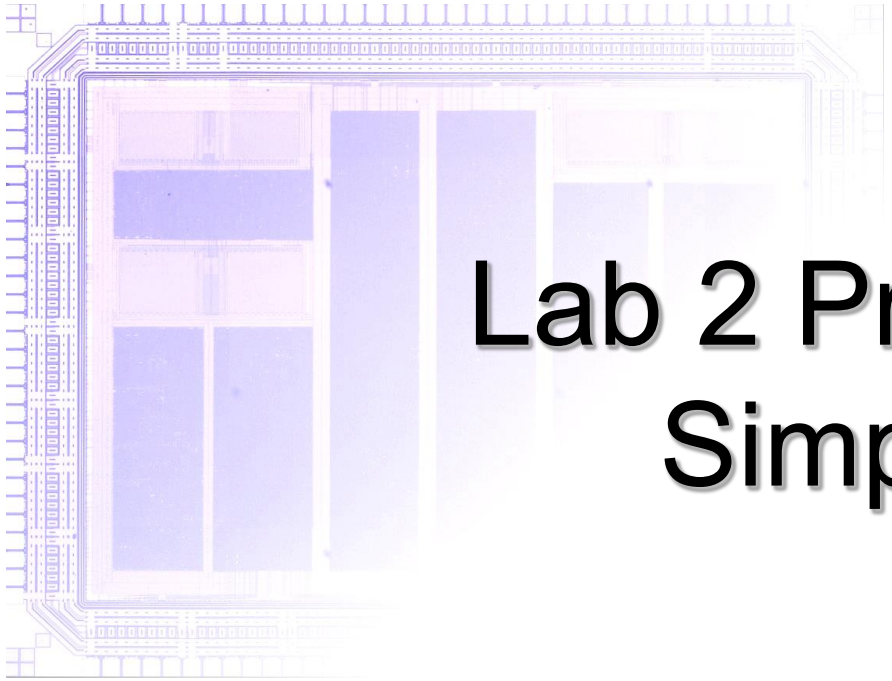
Transaction Level Modeling

Transaction Level Modeling

- Majorly used for functional modeling, platform modeling, and testbench constructing.
- Communication mechanisms such as buses or FIFOs are modeled as channel.
- Modules use interface to access channels
- Allow refining on implementation of interface

TLM for System Level Design

- Emphasis more on functionality of data transfer: what data are transferred, to and from what locations.
- Emphasis less on their actual implementation, that is, on the actual protocol used for data transfer.

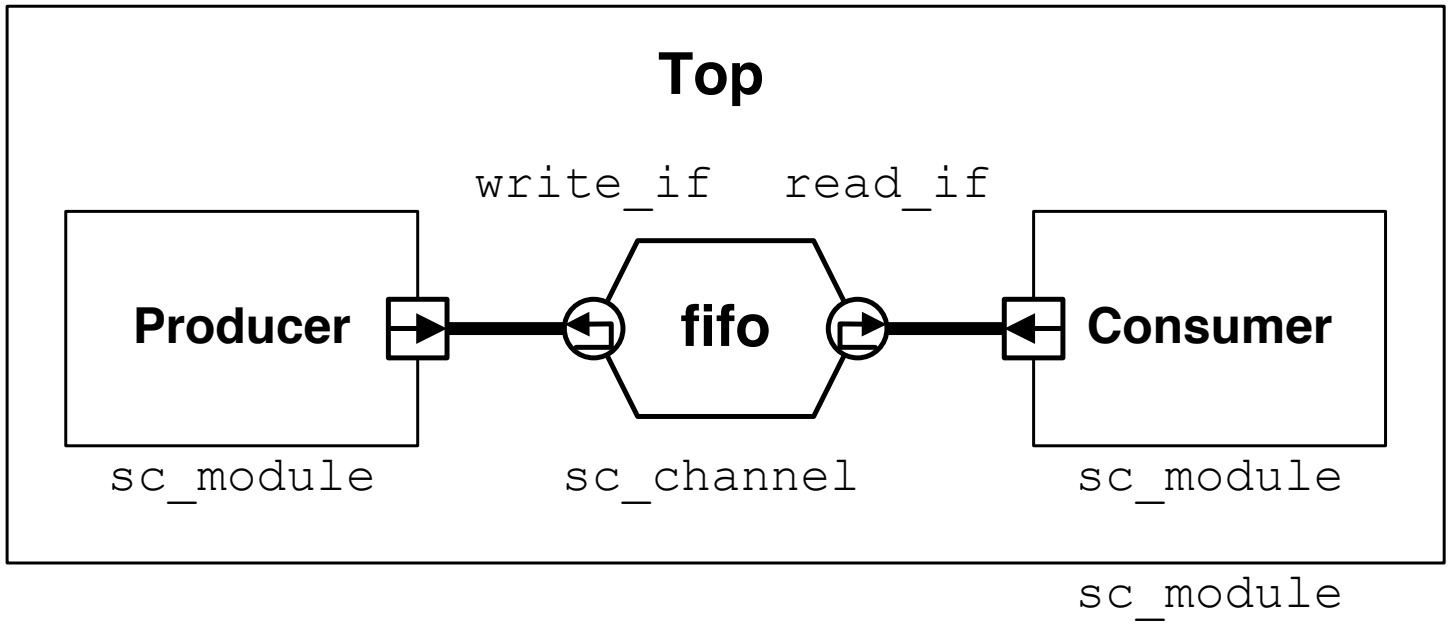


Lab 2 Practice: Simple FIFO / Perf

Run a simple example

- Try code/simple_perf/
  - Open simple_perf.sln in Visual Studio 2013
- This is a simple FIFO example
  - Customized read/write interface
    - Inherited from sc_interface
  - Hierarchical channel
    - Inherited from sc_channel
    - In SystemC, sc_channel and sc_module are identical! Hierarchical channel == Module

Simple FIFO / Simple Perf



Requirement

- Add bool isEmpty() to read_if
- Add bool isFull() to write_if
- Use these functions in producer and consumer to show the blocking access explicitly.