Parallel Sparse Matrix Solver for Circuits on FPGA

M.Tech Project Stage 1 Report

Submitted in partial fulfillment of the requirements

for the degree of

Master of Technology

by

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Under the guidance of

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Acknowledgement

I express my gratitude to my guide Prof. Sachin Patkarfor providing me the opportunity to work on this topic.

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Declaration

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I declare that I have properly and accurately acknowledged all sources used in the production of this report. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be a cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

Yogesh Mahajan

Date: October 9, 2018 (14D070022)

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test

Such Empty...
Adding some emojis 😐☹😁😂😄😇😉😈😋😍😱 and even cats: 😸!

Chapter 1

Introduction

Hello [1]

1.1 Section

Table 1.1: Design Requirements

Parameter	Value
$V_{out_{DC}}$	1.2 V
$Gain\ (A_v)$	5
Z_{in}	50 Ω
V_{Idc}	$> 0.3\ V$

Hello

1.1.1 SubSection

Hello

Chapter 2

Motivation

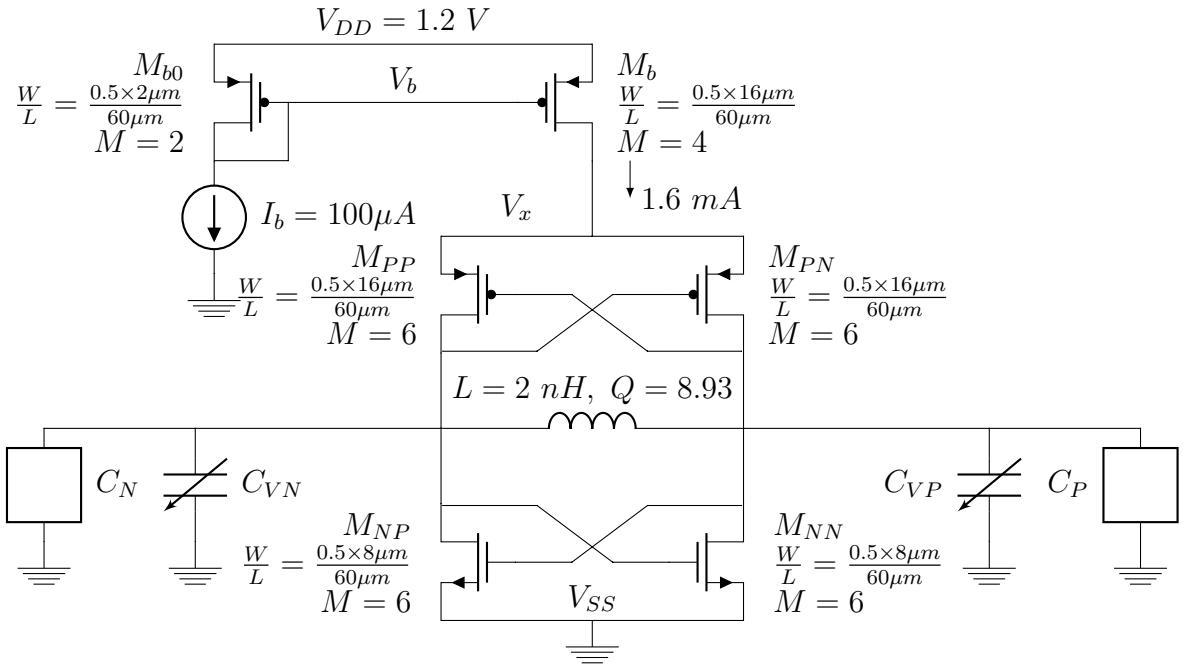

Figure 2.1: Cross coupled PMON-NMOS VCO with PMOS current source architecture

Hello

2.1 Section

Hello [1]

2.1.1 SubSection

Hello

...

...

Table 2.1: Dummy table

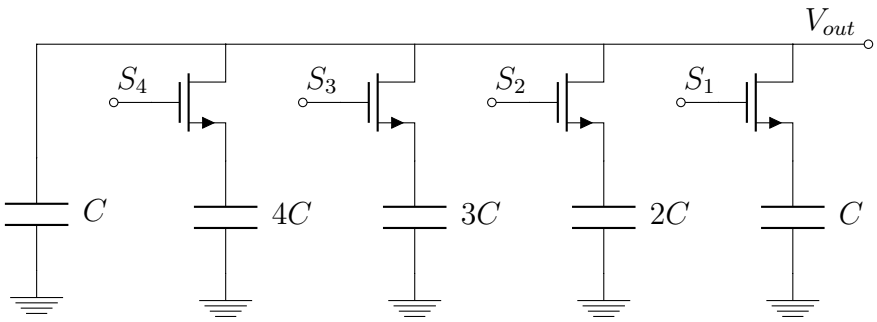

Figure 2.2: Capacitor Bank

Figure 2.3: Dummy figure

Table 2.2: Differential Noise Analysis

Noise Contributing Element	Total Noise Measured @ Von	
	V^2	$\% \, Total$
M0 (M1)	6.989×10^{-8}	49.81 %
R2 (R1)	2.676×10^{-10}	0.19 %
M1 (M2)	6.989×10^{-8}	49.81 %
R1 (R2)	2.676×10^{-10}	0.19 %
R0 (Rb)	1.283×10^{-39}	9.1×10^{-31} %
Total	$1.403 \times 10{-}7 \; V^2$	
Input Referred Noise	$1.168 \times 1032 \; V^2$	

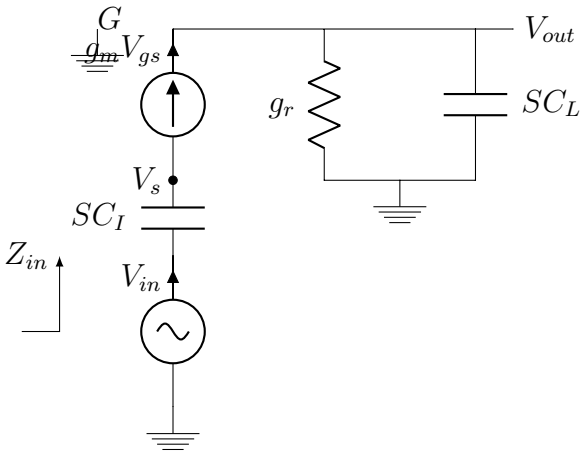

Figure 2.4: Small Signal model

Only one line here.	Same for column two.	Same for column three.
We have two lines here, each line centered.	This cell will have three lines and each line centered as well.	Here is a justified cell, please check this out!
This cell has one line.	So does this one.	And this one, too!

List of figures

List of tables

References

[1] S. Borkar and A. A. Chien, "The future of microprocessors," *Communications of the ACM*, vol. 54, no. 5, pp. 67–77, 2011.