VLSI Design

Design of 8X8 Wallace Tree Multiplier EE 671 : Homework #3

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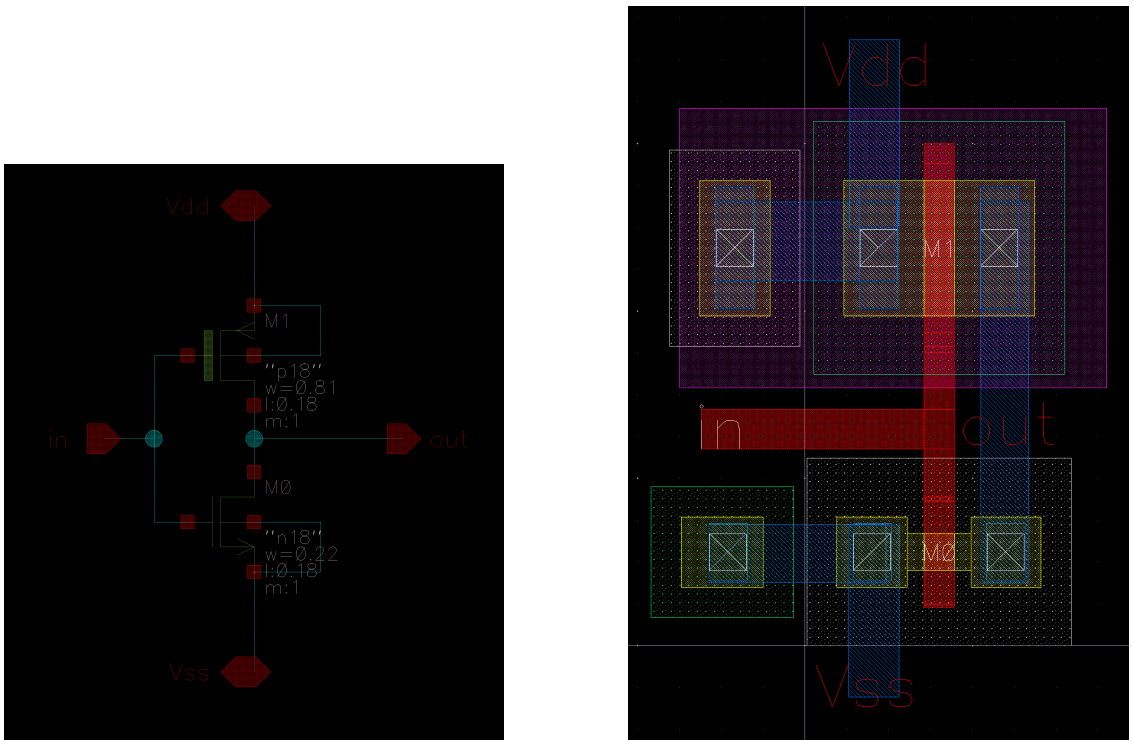
Basic Components

This section includes all the basic components required for multiplier. All the components are designed and simulated for SCL's 180 nm process.

Minimum Sized Inverter

Design and Layout



(a) Schematic

(b) Layout

Figure 1: Minimum Sized Inverter

Inverter Parameter γ $\left(\frac{W_p}{W_n}\right)$ is chosen to get nearly equal rise time and fall time under Typical-Typical process corner (SCL).

Table 1: Design

Parameter	Value
P-MOS Gate Width W_p	0.81 μm
P-MOS Gate Length L_p	0.18 μm
N-MOS Gate Width W_n	0.22 μm
N-MOS Gate Length L_n	0.81 μm

Simulation

Following figure shows I/O characteristics of above designed minimum Sized inverter tested at 125^oC under SS process corner and $V_{dd} = 1.7\ V$.

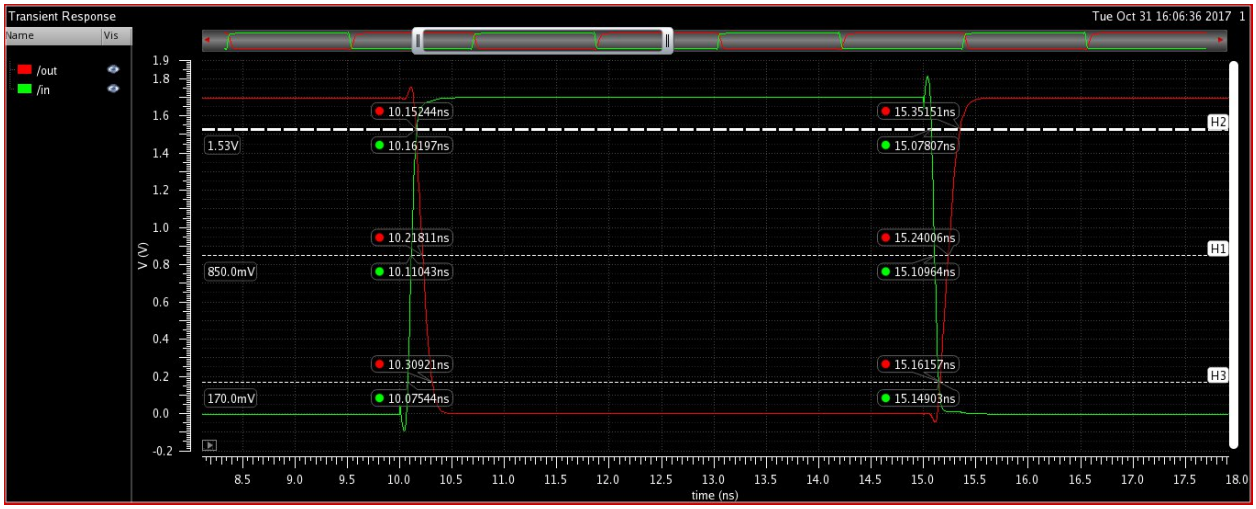


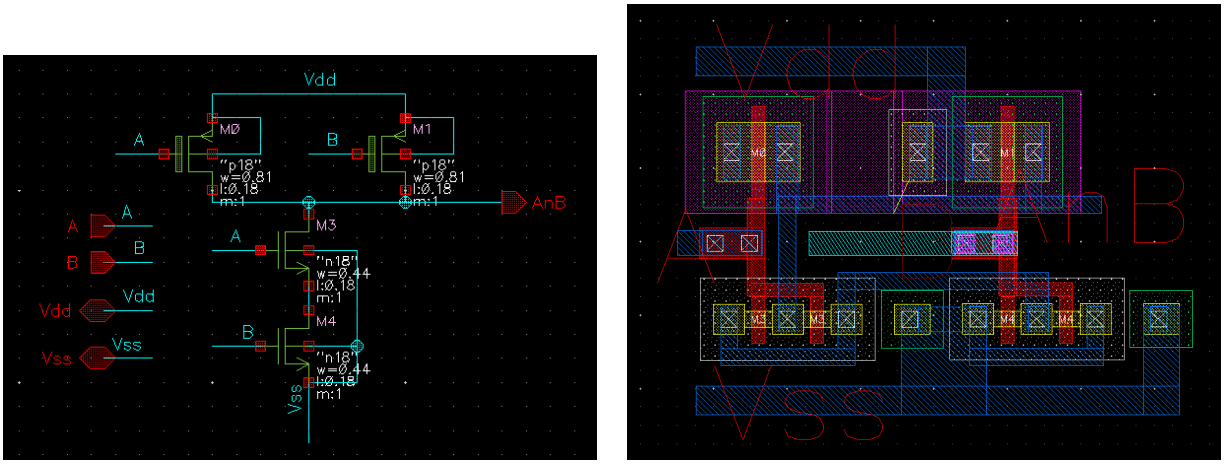
Figure 2: Inverter I/O [$125^oC,\ V_{dd} = 1.7\ V$] (Output Input)

Table 2: Specifications

Parameter	Value
Rise Time τ_{rise}	189.94 ps
Fall Time τ_{fall}	156.77 ps
Delay τ	130.42 ps

NAND-2 Gate

Design and Layout



(a) Schematic (b) Layout

Figure 3: NAND-2 Gate

Simulation

Following figure shows I/O characteristics of above designed NAND-2 gate tested at 125^oC under SS process corner and $V_{dd} = 1.7\ V$.

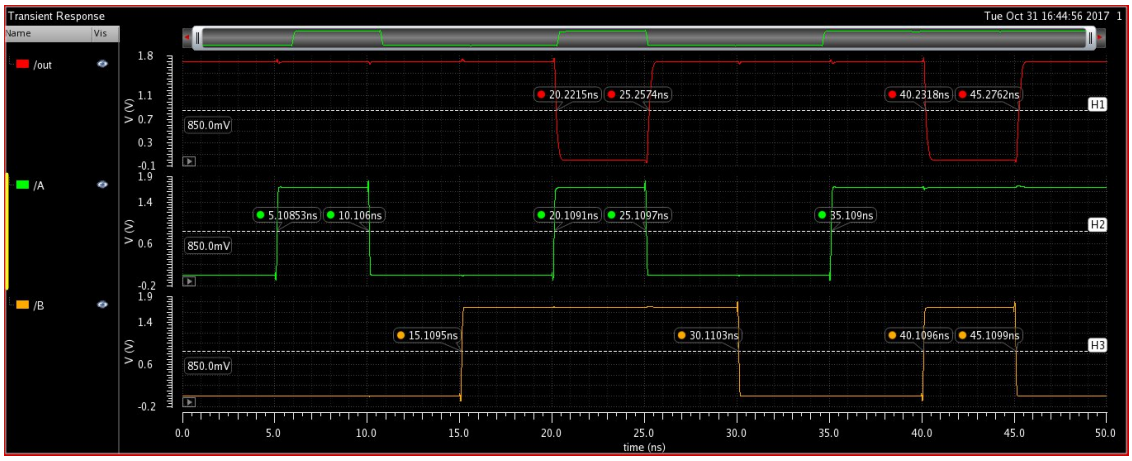
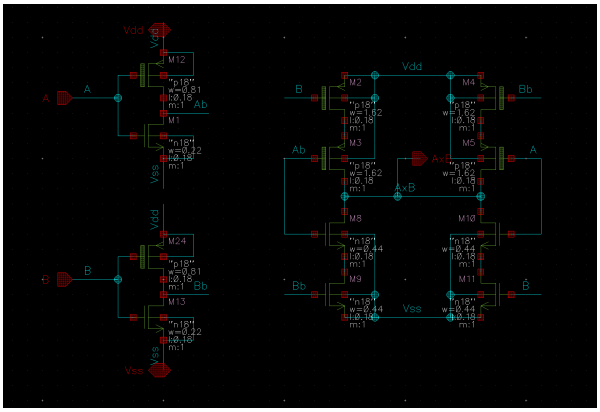


Figure 4: NAND-2 I/O [$125^oC,\ V_{dd} = 1.7\ V$]

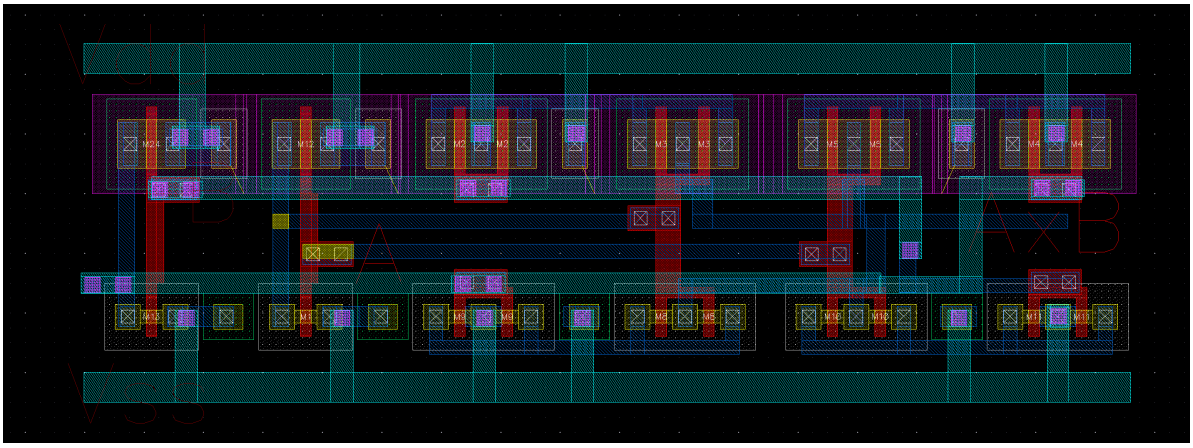
From above figure worst case delay for NAND-2 gate is 166.3 ps.

XOR-2 Gate

Design and Layout



(a) Schematic



(b) Layout

Figure 5: NAND-2 Gate

Simulation

Following figure shows I/O characteristics of above designed XOR-2 gate tested at 125^oC under SS process corner and $V_{dd} = 1.7\ V$.

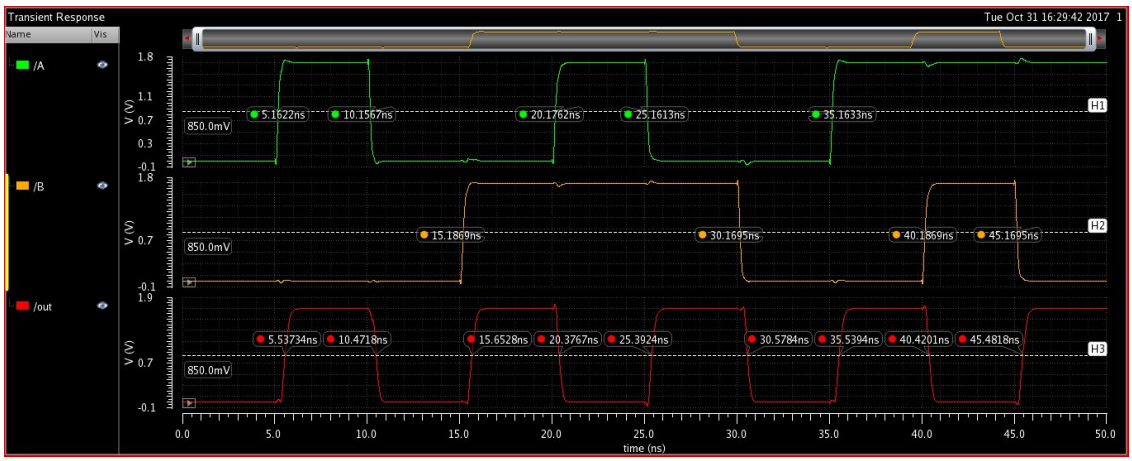
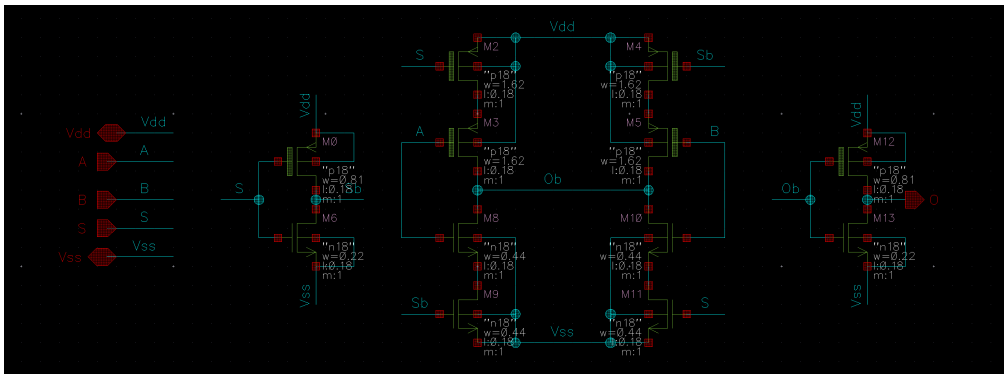


Figure 6: XOR-2 I/O [$125^a lignoC,\ V_{dd} = 1.7\ V$]

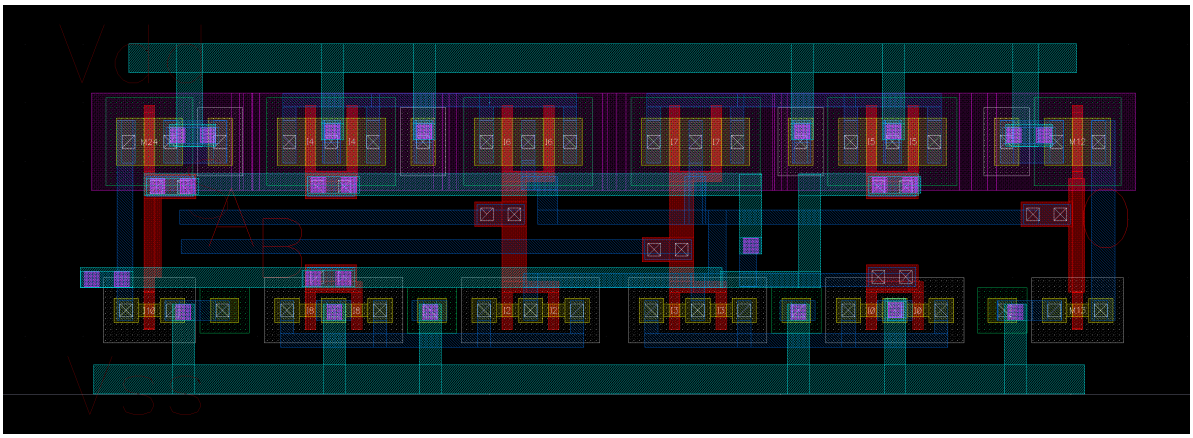
From above figure worst case delay for NAND-2 gate is 465.9 ps.

MUX-21

Design and Layout



(a) Schematic

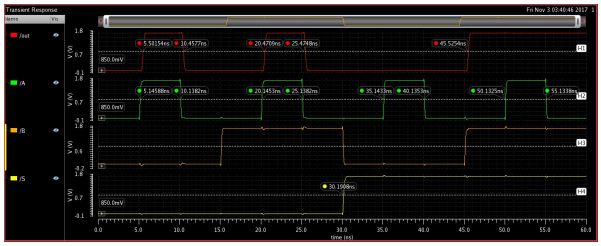


(b) Layout

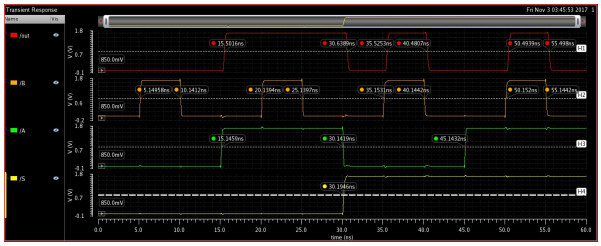
Figure 7: MUX-2:1

Simulation

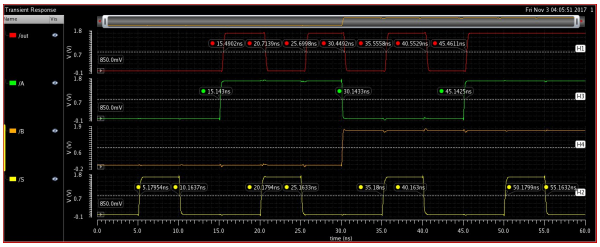
Following figure shows I/O characteristics of above designed 2:1 MUX tested at 125^oC under SS process corner and $V_{dd} = 1.7\ V$.



(a) Input A



(b) Input B



(c) Innput S

Figure 8: MUX-21 I/O $[125^oC,\ V_{dd} = 1.7\ V]$

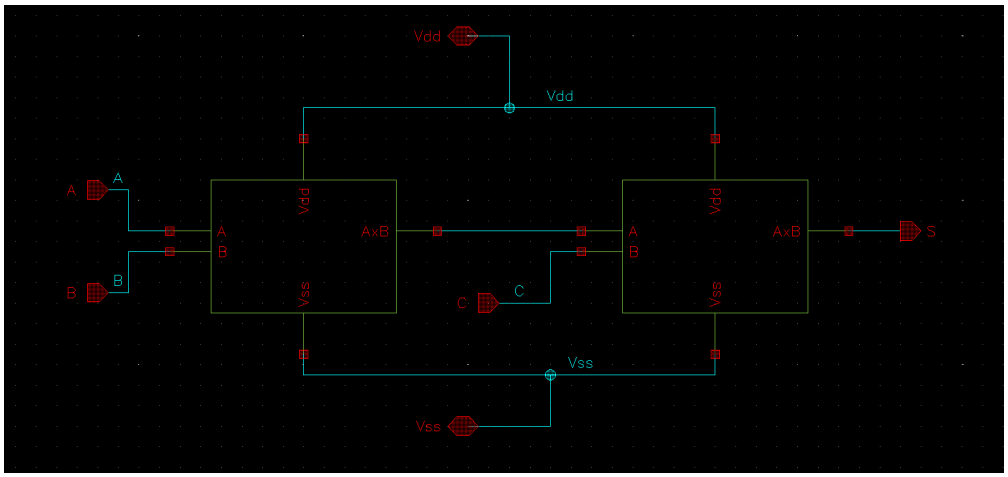
From above figure worst case delay for NAND-2 gate is 536.5 ps.

Half Adder

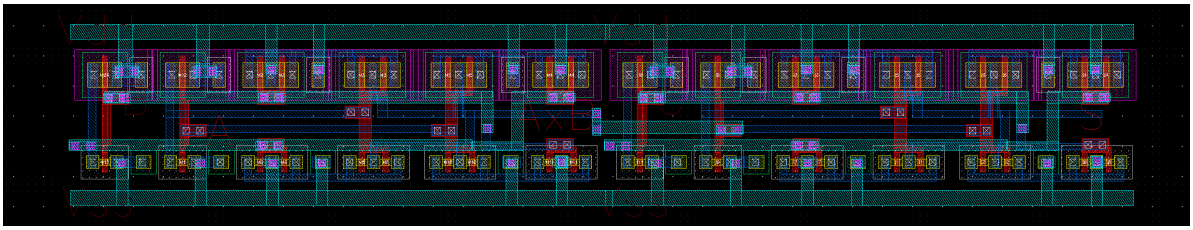
For half adder we can use XOR-2 gate and NAND-2 gate for sum and carry bar generation. Which we already have. Therefore worst case input to sum delay (XOR-2) is 0.47 ns and input to carry delay (NAND-2 + Inv) is 0.3 ns.

Full Adder

Sum



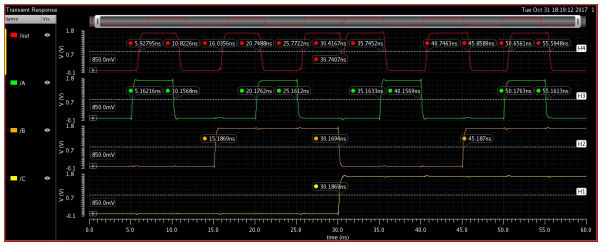
(a) Schematic



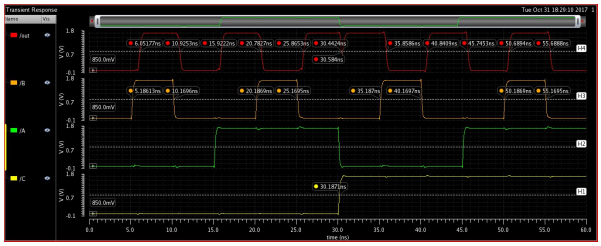
(b) Layout

Figure 9: Sum Circuit

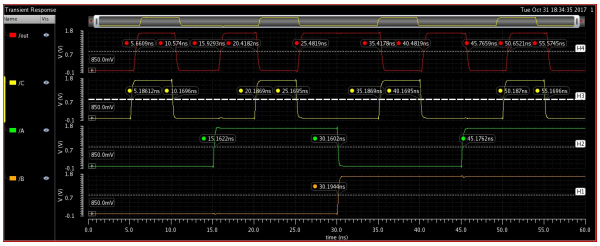
Following figure shows I/O characteristics of above designed sum tested at 125^oC under SS process corner and $V_{dd} = 1.7\ V$.



(a) Input A



(b) Input B

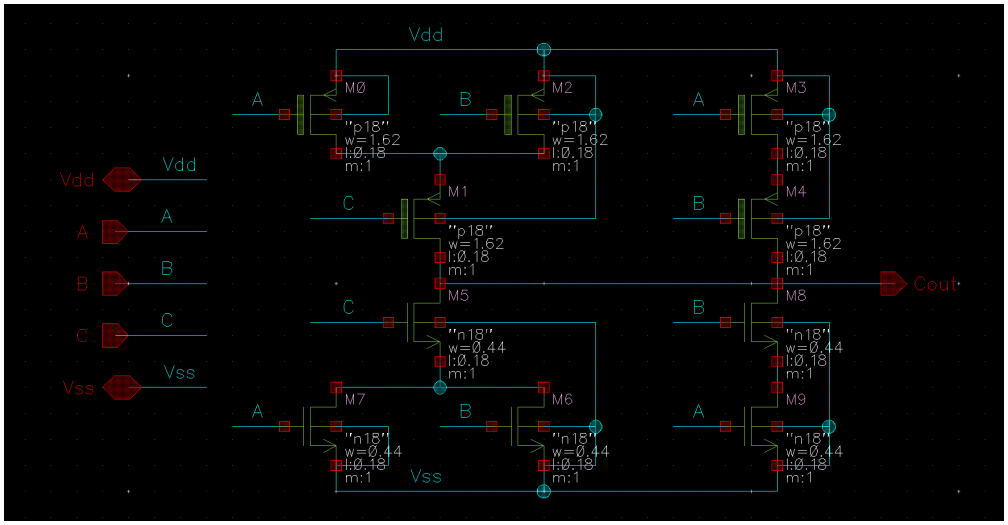


(c) Innput S

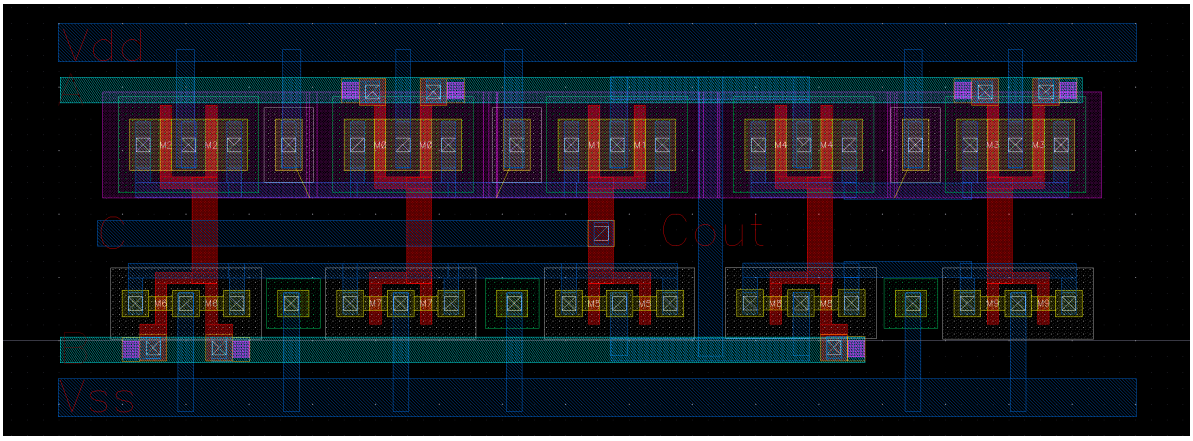
Figure 10: MUX-21 I/O [$125^oC,\ V_{dd} = 1.7\ V$]

From above figure worst case delay for full adder's sum is 829.64 ps.

Carry



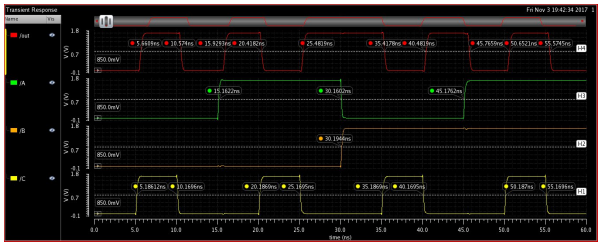
(a) Schematic



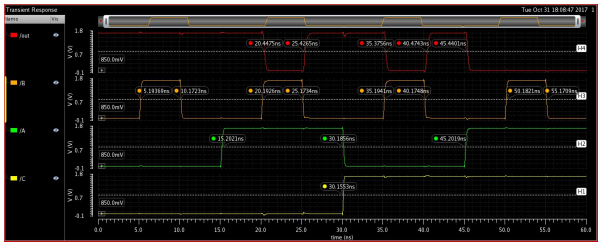
(b) Layout

Figure 11: Carry Bar

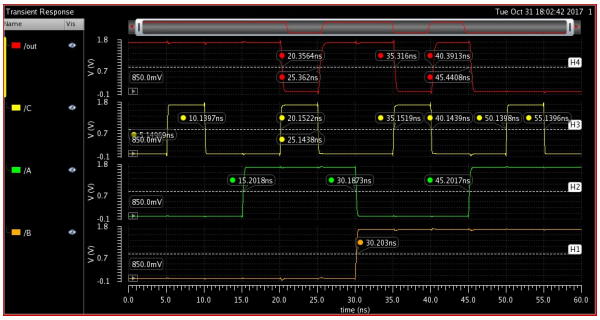
Following figure shows I/O characteristics of above designed carry circuit tested at 125^oC under SS process corner and $V_{dd} = 1.7\ V$.



(a) Input A



(b) Input B



(c) Innput S

Figure 12: Carry bar I/O [$125^oC,\ V_{dd} = 1.7\ V$]

From above figure worst case delay for full adders carry bar is 333.1 ps. // Therefore worst case input to sum delay for full adder is 0.87 ns and input to carry delay (Carry bar + Inv) is 0.4 ns.

Wallace Reduction Stage

Partial products are reduced using modified Wallace algorithm as shown in figure 13.

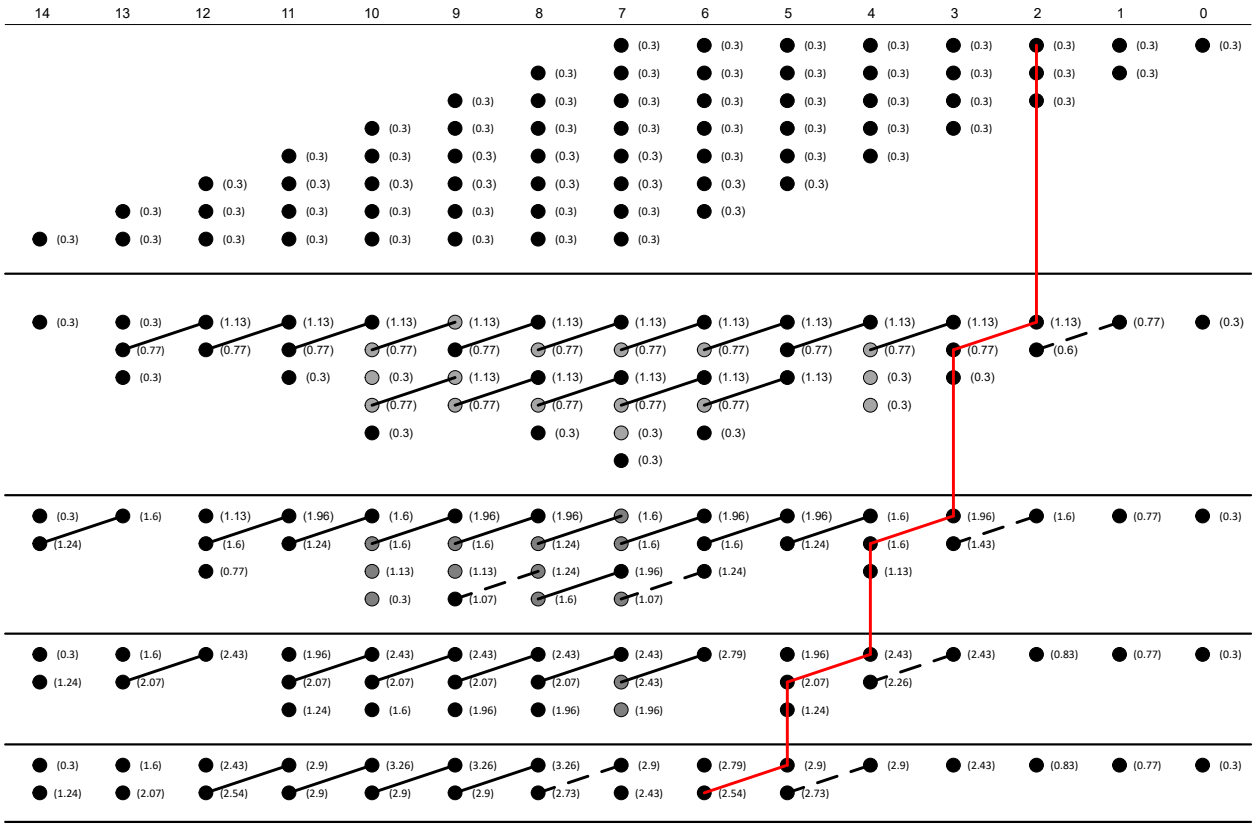


Figure 13: Dot diagram of Modified Wallace Reduction Stages

In above figure, values in bracket indicates worst case arrival time in nano seconds of corresponding bit. At each stage inputs are grouped to minimize overall delay.

Carry Select Adder with Square Root Stacking

Carry select adder with square root stacking is used for final addition. Adder has three stages with lengths 2, 3 and 5. Stage lengths are deciding considering delay of each adder and select Mux. Internally each stage is consist of ripple carry adder of appropriate length. First adder is half adder to minimize delay. RCA adders don't use complete full adder andd halh adder to minimize carry propagation delay.//

Exact calculation of delays of adder is shown in foloowing table.

Bit	MUX	9	8	7	6	5	MUX	4	3	2	MUX	1	0
Input A		0.3	1.6	2.43	2.9	3.26		3.26	3.26	2.9		2.79	2.9
Input B		1.24	2.07	2.54	2.9	2.9		2.9	2.73	2.43		2.54	2.73
Carry In	4.96	4.62	4.28	3.94	3.6	0	4.07	3.73	3.24	0	3.41	3.07	0
Inverter			1		1				1			1	0
Carry Bar		4.96	4.62	4.28	3.94	3.6		4.07	3.73	3.24		3.41	3.07
Sum		5.45	5.24	4.77	4.56	4.09		4.56	4.35	3.73		4.03	3.37
Final	5.63	5.99	5.99	5.99	5.99	5.99		5.1	5.1	5.1		4.57	4.57

Figure 14: Timing analysis of Carry Select Adder

Note: Refer excel sheet for more details.

Simulation Results

Critical path for reduction stage is shown in figure **??**. Complete carry select adder is in critical path as carry propagation is the slowest process. From calculations worst case delay for complete multiplier is about 6 ns. Exact values of delays are used to simulate multipler using VHDL. Testbench tests multiplier for all possible inputs with intial input for each case being **UNDEFINED ('U')**. Worst case delay for multiplier is 6.05 ns for inputs *"0b01001001"* and *"0b11100001"*.

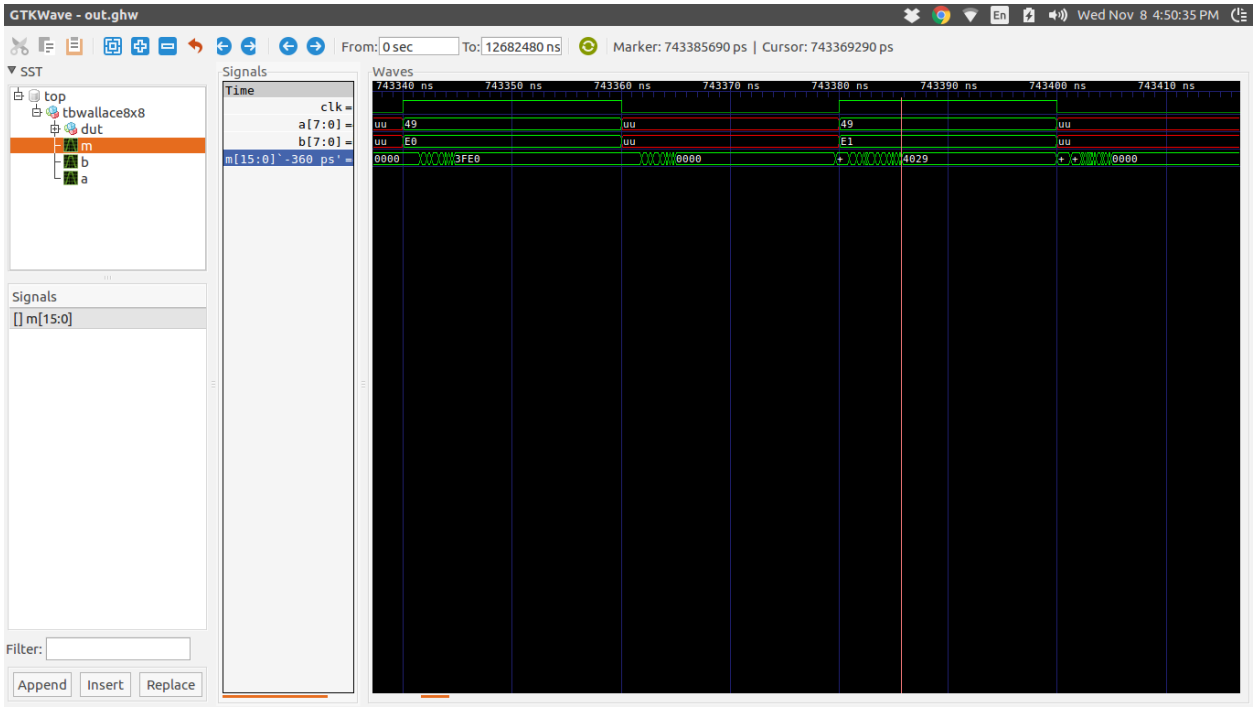


Figure 15: MAximum delay Case