VHDL Tutorial

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Our Assumptions

- Basic (OO)Programming in C/C++/Python
- Basics of Digital Electronics
- GHDL Installation
  - 10.107.2.210/BrC-2018/Installation%20Files/EE4%20_%20EE5/VHDL/
- VHDL Files downloaded
  - 10.107.2.210/BrC-2018/Tutorials/VHDL/

Where might this be useful?

- Courses
  - EE616: Electronic Systems Design
  - EE668 and 671: Systems and VLSI Design
  - EE705: VLSI Design Lab
  - EE709: Testing and Verification of VLSI Circuits
  - EE739: Processor Design
  - EE748: Advanced Topics in Computer Architecture
- Research work involving Design of Systems or FPGAs/CPLD Systems
- As a TA or RA in the WEL Lab or for Undergraduate Courses

Objectives: Not a formal lesson

- What's an HDL?
- What are some HDLs?
- How to get started with VHDL?
  - Designs and Testbenches
- How simulate VHDL?
- Example Codes: Base for the Future

HDL:
Hardware Description Language

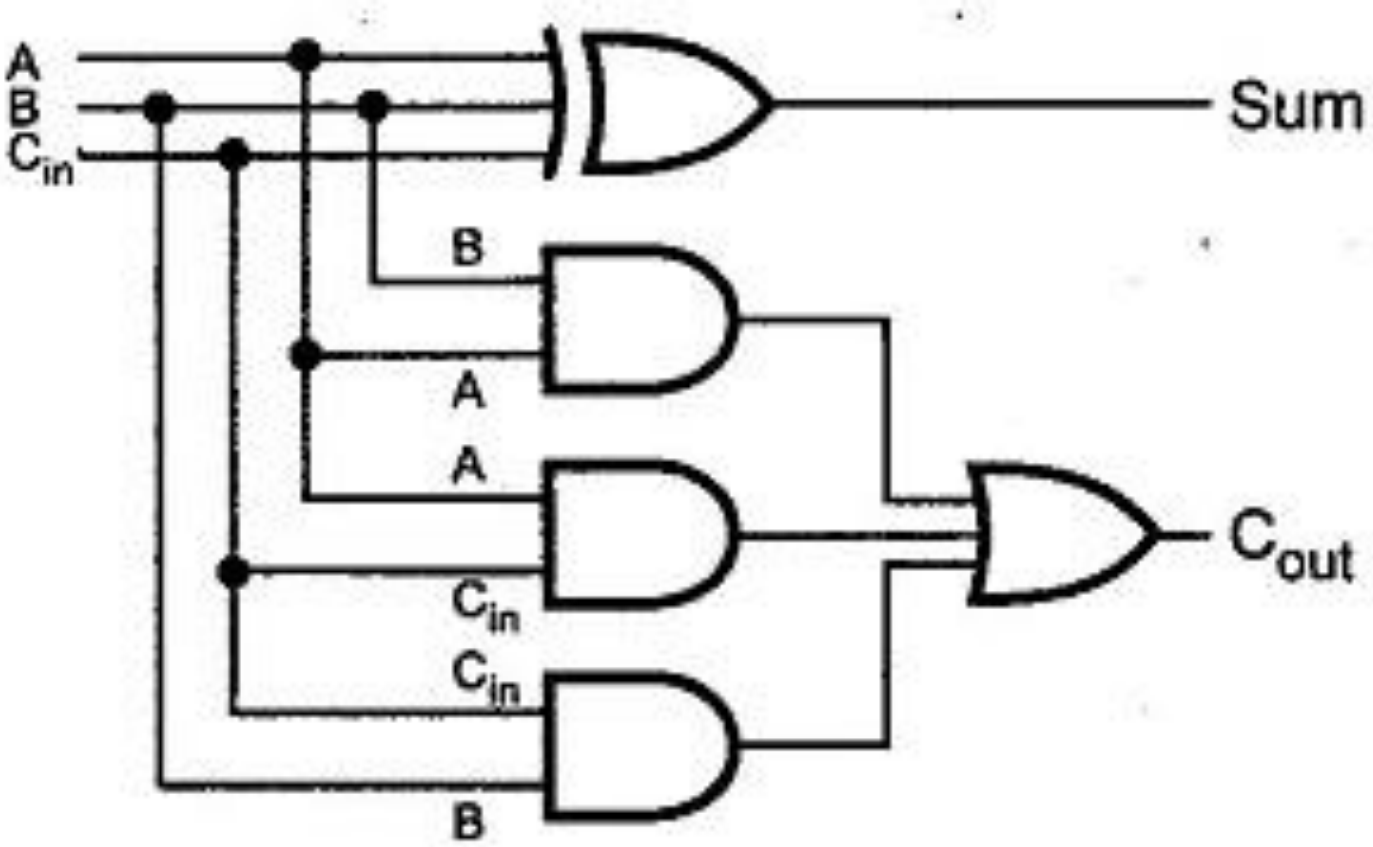
And not High-Density Lipo-Protein

Some HDLs:

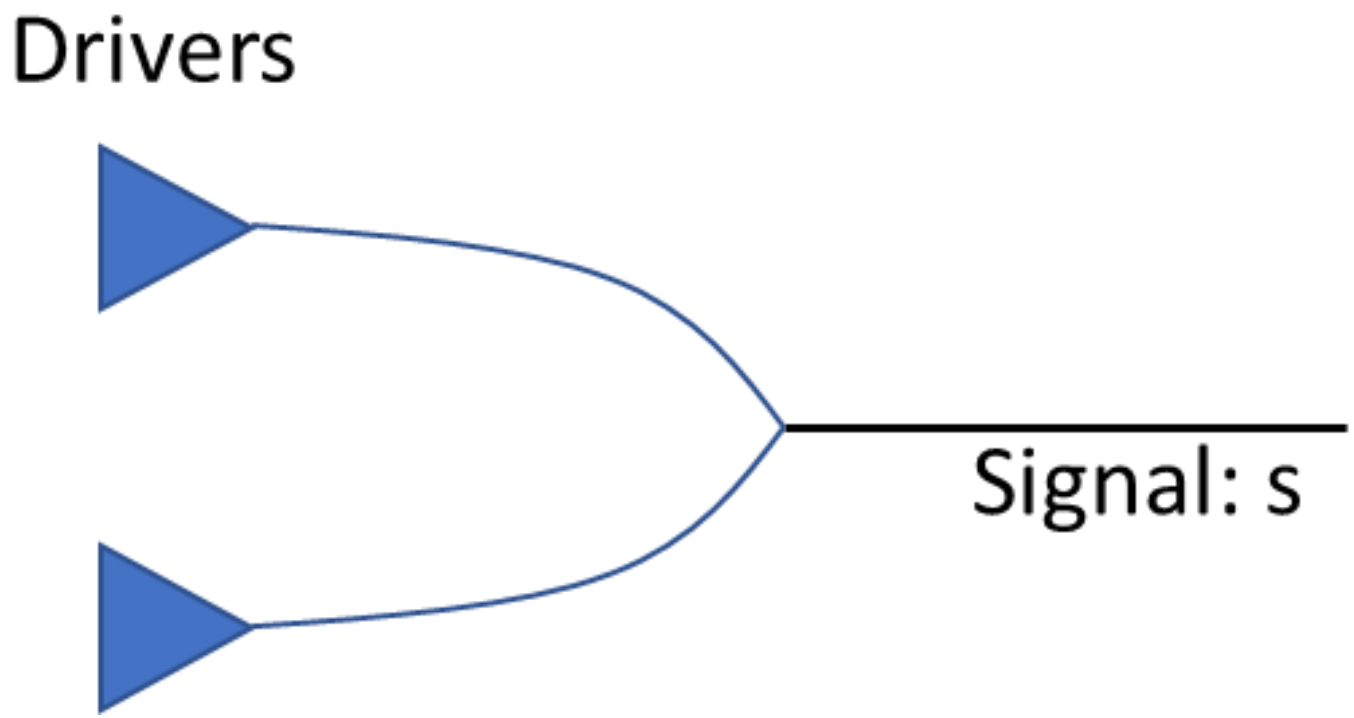
- VHDL: VHSIC HDL
  - Very High Speed Integrated Circuit
  - Strongly Typed and verbose like C/C++
  - Syntax: Somewhat closer to Python
- Verilog
  - Loose in terms of strictness like Python
  - Syntax similar to C/C++

Moving to Examples

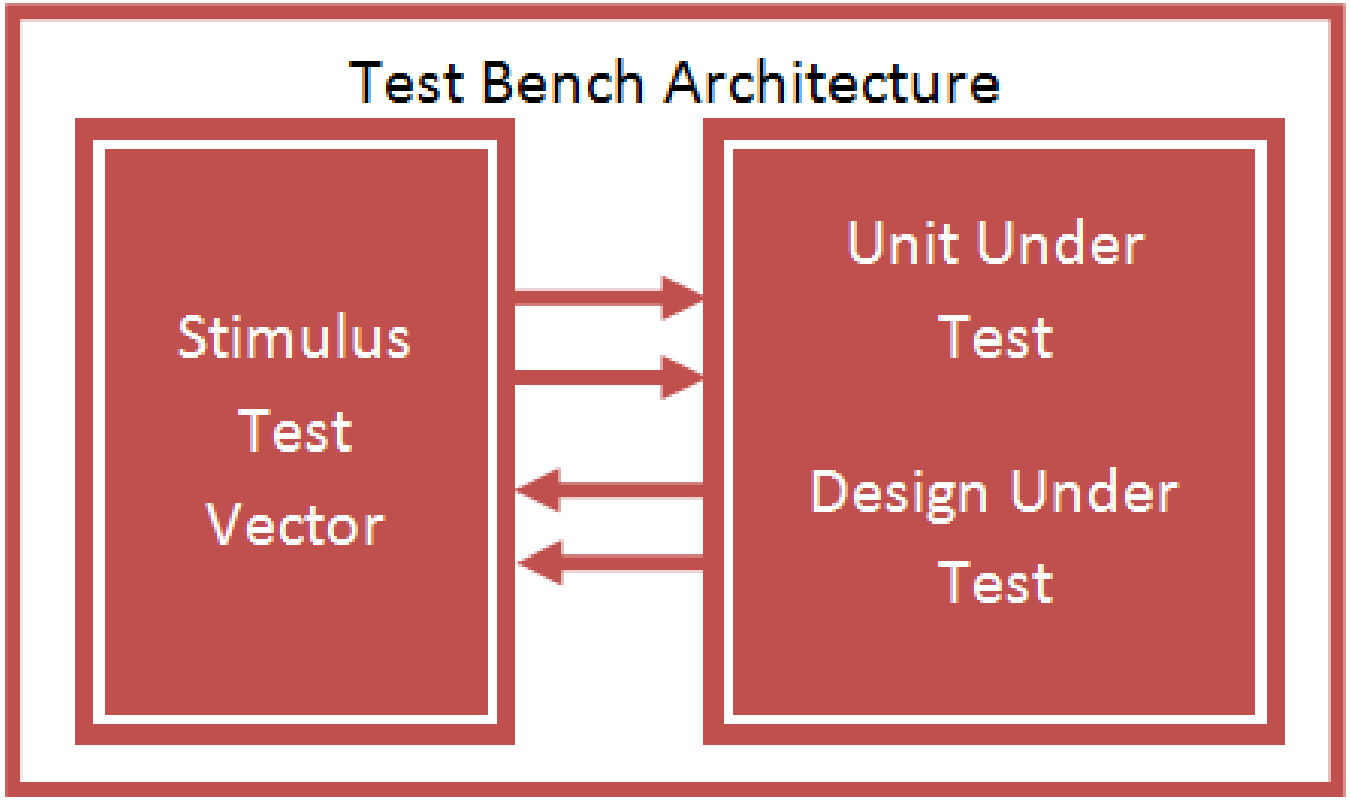
Full Adder



Concurrent Assignments



Testbench


Test Bench Architecture
Stimulus
Test
Vector
Unit Under
Test
Design Under
Test

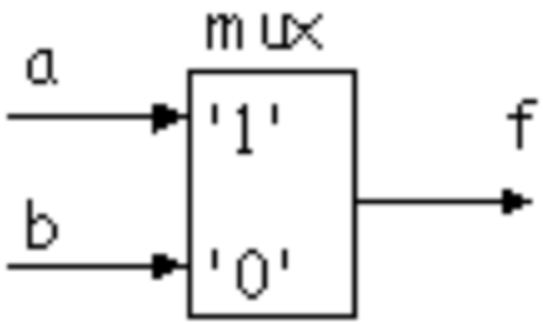
The std_logic type

- `'U'`: uninitialized. This signal hasn't been set yet.
- `'X'`: unknown. Impossible to determine this value/result.
- `'0'`: logic 0
- `'1'`: logic 1
- `'Z'`: High Impedance
- `'W'`: Weak signal, can't tell if it should be 0 or 1.
- `'L'`: Weak signal that should probably go to 0
- `'H'`: Weak signal that should probably go to 1
- `'-'`: Don't care.

Pitfall: Latch Generation

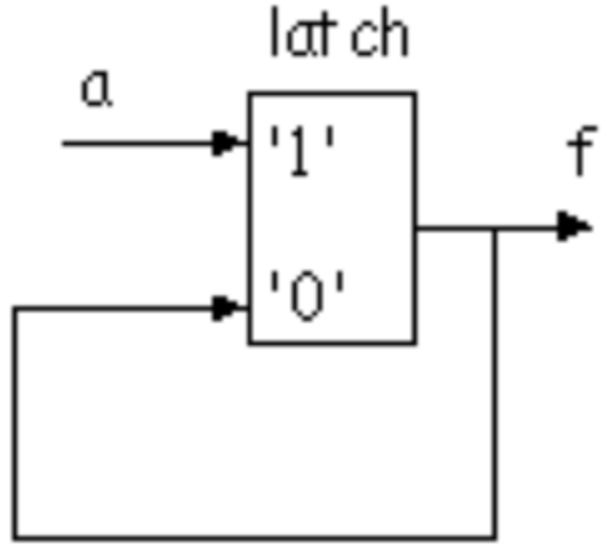
Complete if statement

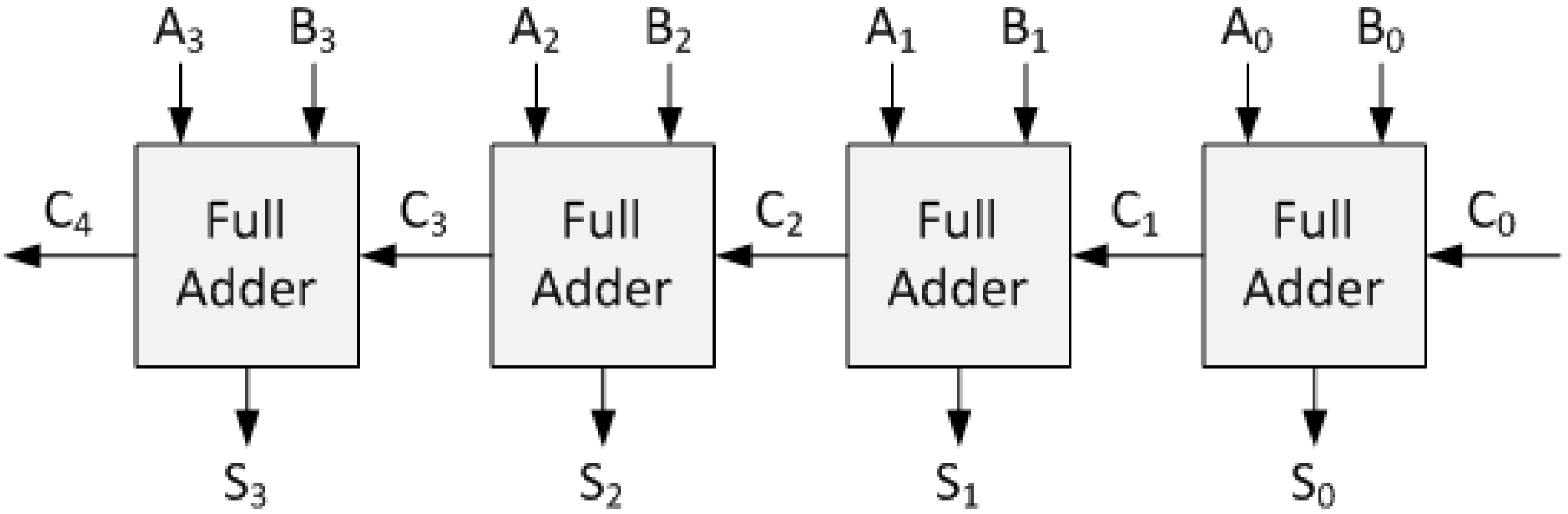
```
if_else: process (sel, a, b)
begin
  if sel = '1' then
    f <= a;
  else
    f <= b;
  end if;
end process;
```



Incomplete if statement

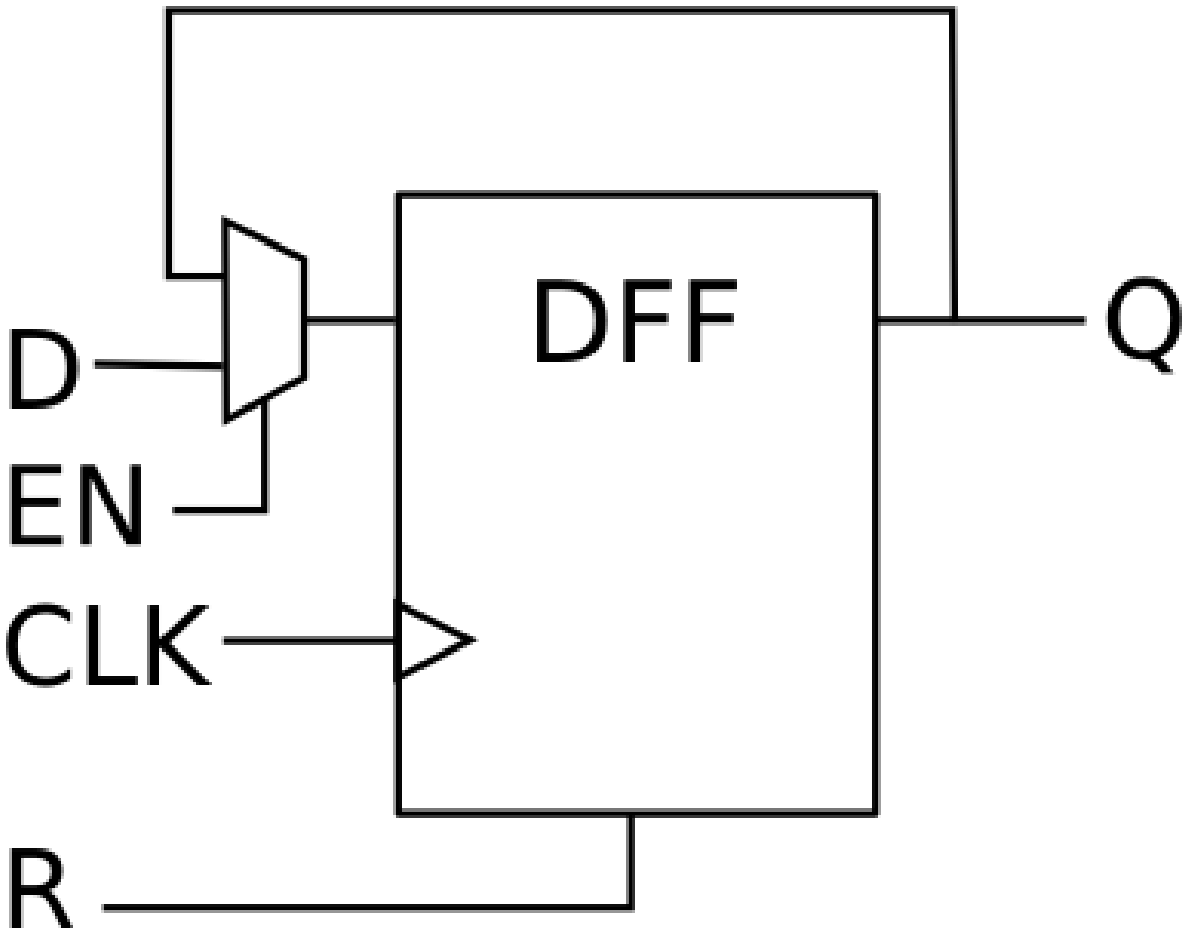
```
latching_if: process (sel, a)
begin
  if sel = '1' then
    f <= a;
  end if;
end process;
```



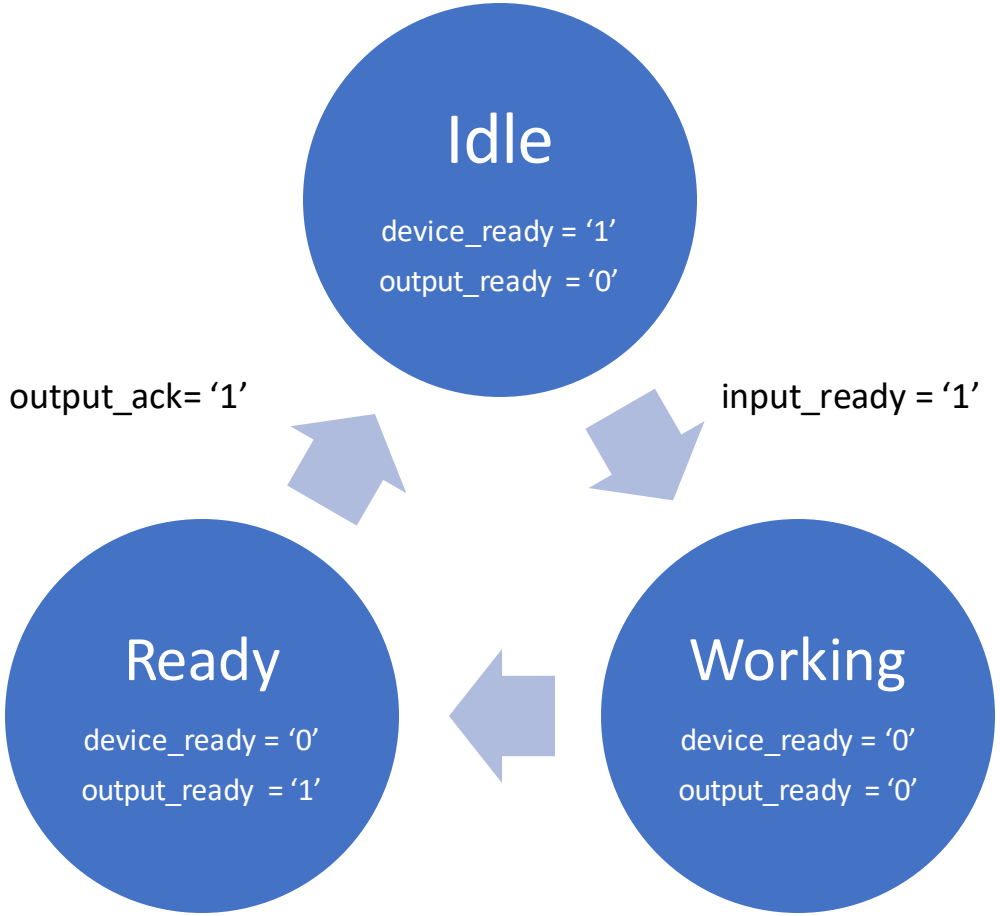


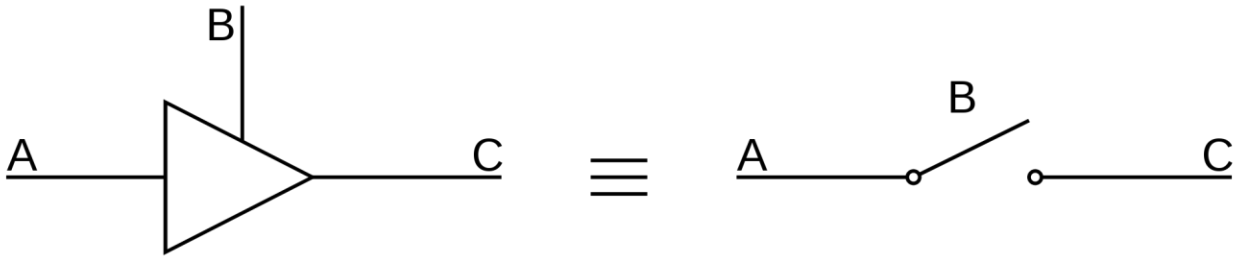
Ripple-Carry Adder

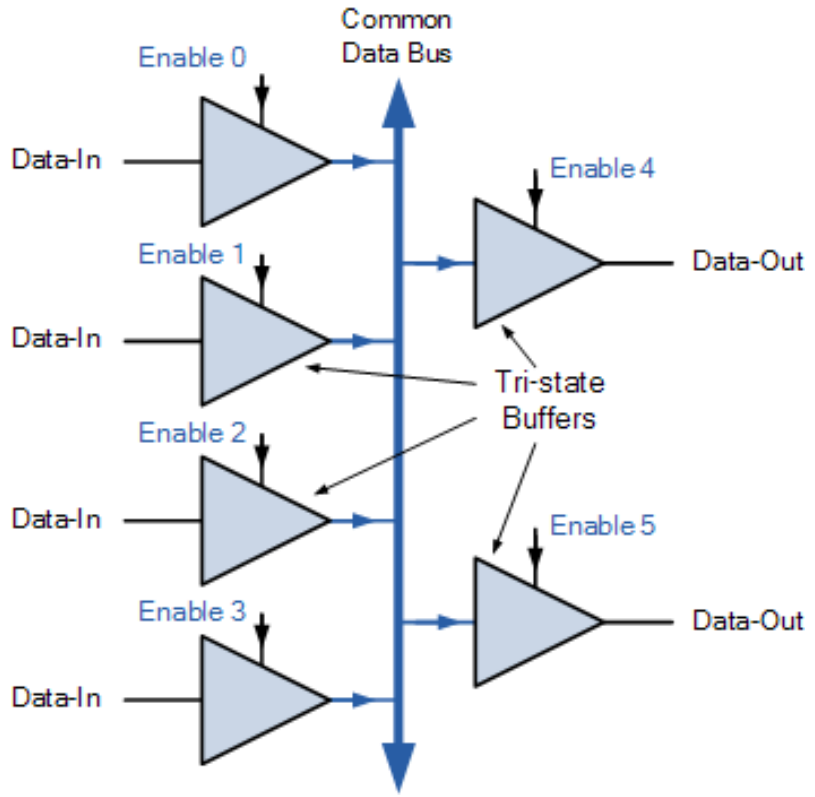
Register



Ready - Ready Handshake







Tri-State Buffer

Useful Resources

- GHDL Documentation Provided
- Tutorials
  - https://www.tutorialspoint.com/vlsi_design/vlsi_design_vhdl_introduction.htm
  - http://www.micc.unifi.it/seidenari/wp-content/uploads/2010/01/vhdl.pdf
  - https://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html
- Books
  - Digital Design: Principles and Practices, 4th Edition: Wakerly
  - The Designer's Guide to VHDL: Peter Ashenden
- References
  - https://www.ics.uci.edu/~jmoorkan/vhdlref/
  - http://web.engr.oregonstate.edu/~traylor/ece474/vhdl_lectures/essential_vhdl_pdfs/
- Debugging
  - Stack Overflow, etc.