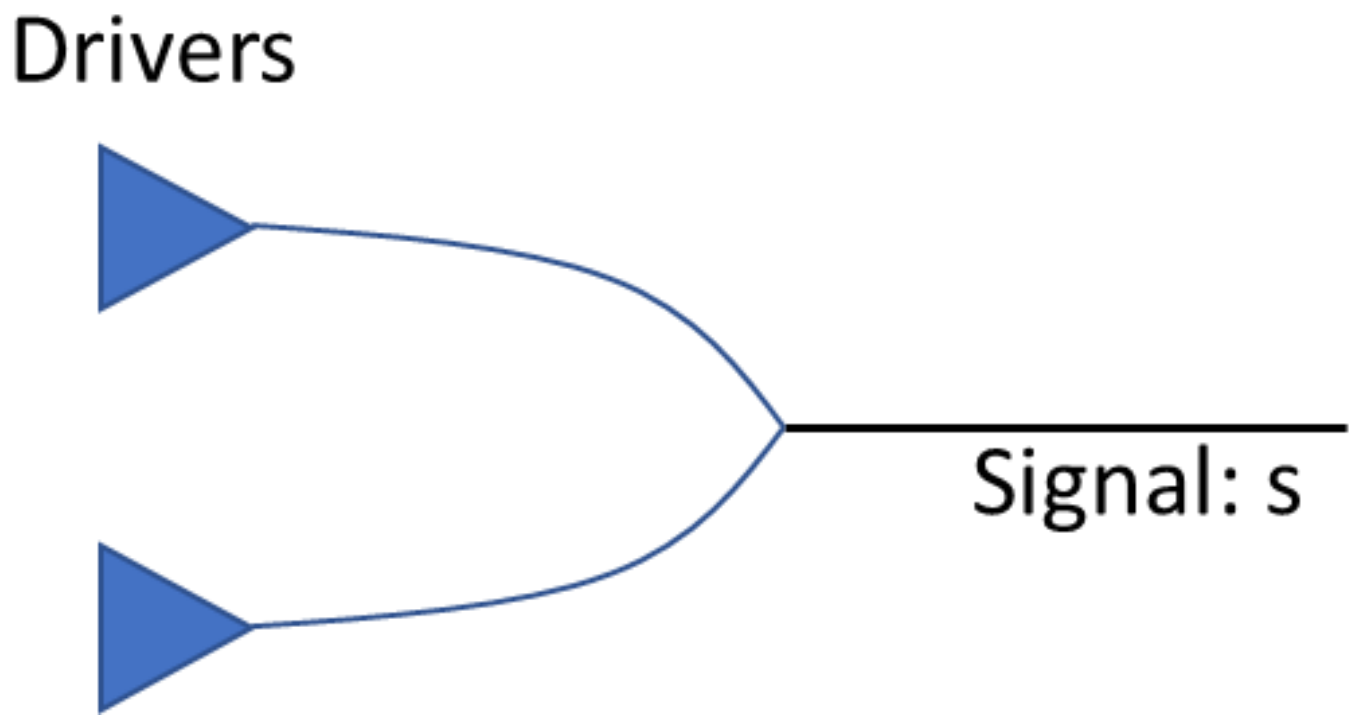
Concurrent Assignments



VHDL Tutorial: Session 2

22-07-2018

OV Shashank

Yogesh Mahajan

What we did last time

Recap!

- Simple Full Adder
- Single File Truth Table based Testbench
- Running GHDL and GTKWave

- Syntax using Multiplexer Example
- Syntax using 8-Bit Adder
  - Usage of Component

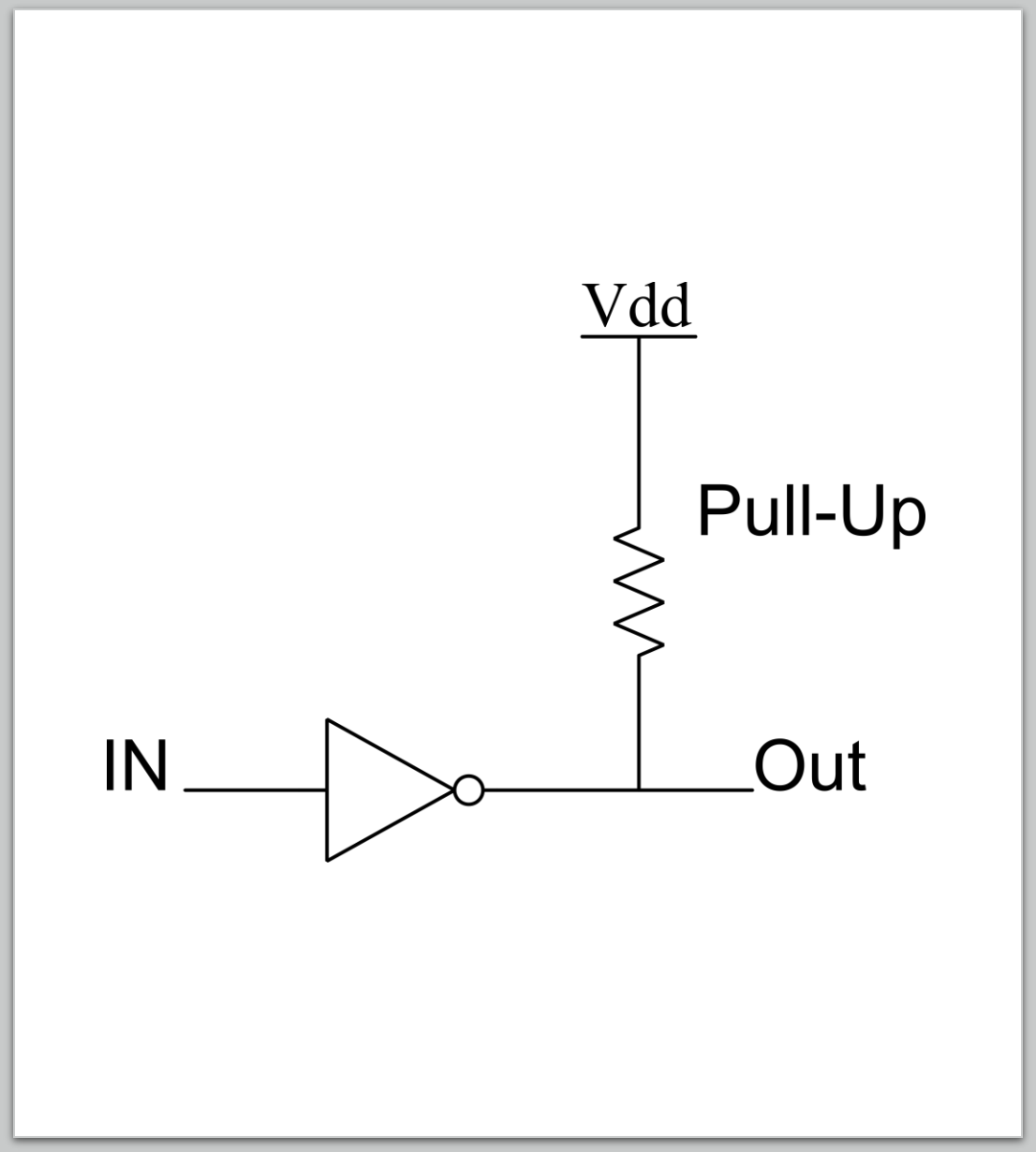
What we skipped

Work Library

- Not the name of a VHDL Library
- WORK denotes the current working library
- Analysed entities are placed in “WORK”

The std_logic Type

- Useful in Testbenches
  - Disconnected => Undefined
  - Before Initialization => Uninitialized
- Modelling pull-up resistors
  - Weak Drives
- Tristates (will come to this soon)
  - High Impedance

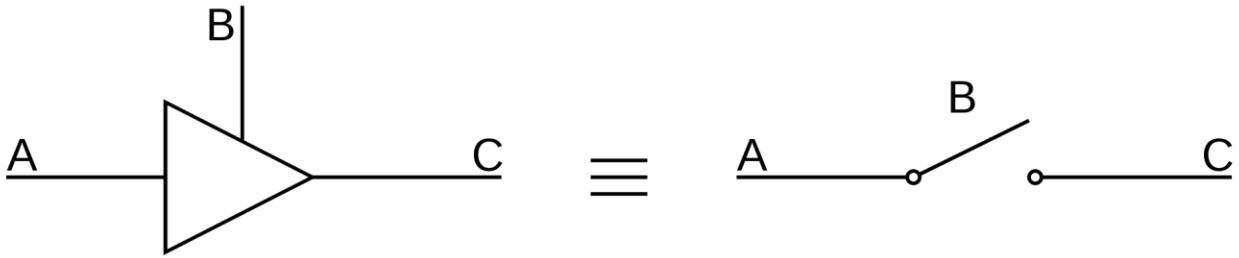


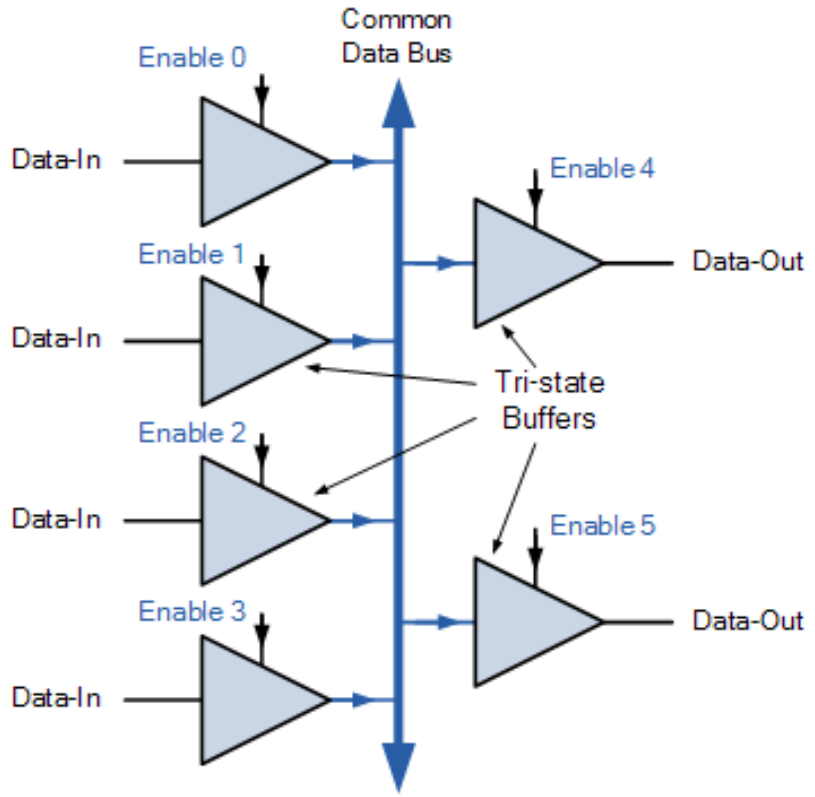
The std_logic type

- `'U'`: uninitialized. This signal hasn't been set yet.
- `'X'`: unknown. Impossible to determine this value/result.
- `'0'`: logic 0
- `'1'`: logic 1
- `'Z'`: High Impedance
- `'W'`: Weak signal, can't tell if it should be 0 or 1.
- `'L'`: Weak signal that should probably go to 0
- `'H'`: Weak signal that should probably go to 1
- `'-'`: Don't care.

Moving on…

First a new approach to a Testbench!

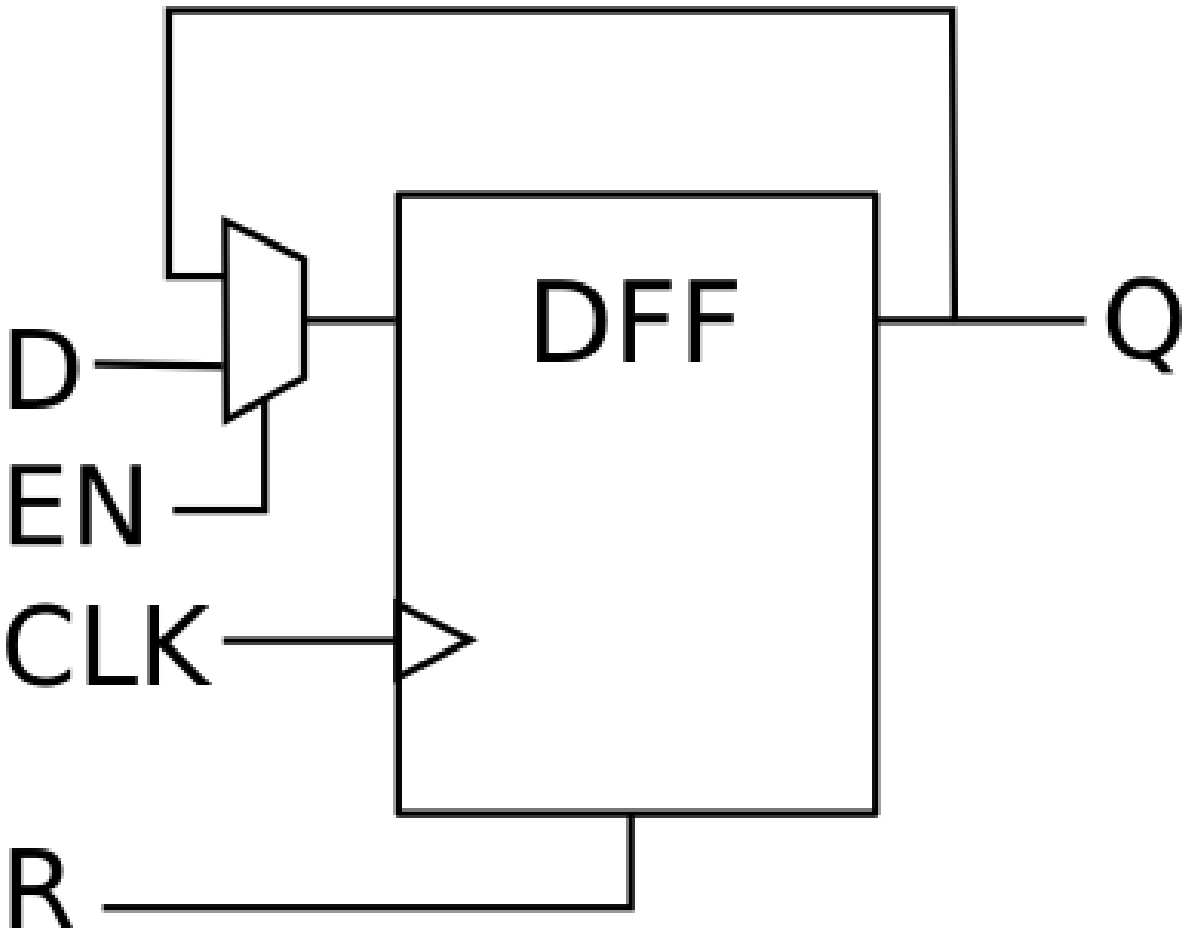




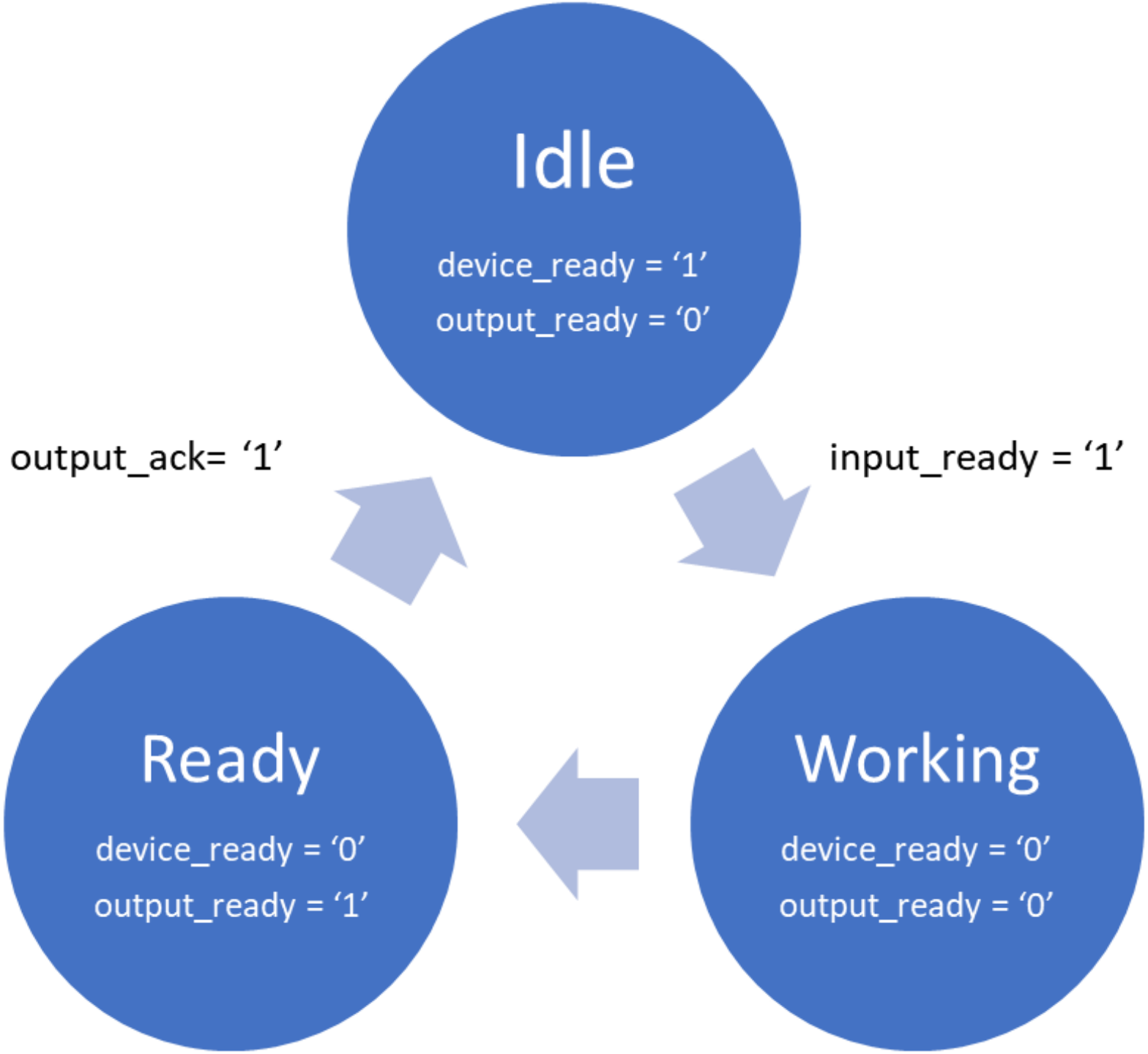
Tri-State Buffer

Combinational Circuits

Register



Ready - Ready Handshake



Useful Resources

- GHDL Documentation Provided
- Tutorials
  - https://www.tutorialspoint.com/vlsi_design/vlsi_design_vhdl_introduction.htm
  - http://www.micc.unifi.it/seidenari/wp-content/uploads/2010/01/vhdl.pdf
  - https://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html
- Books
  - Digital Design: Principles and Practices, 4th Edition: Wakerly
  - The Designer's Guide to VHDL: Peter Ashenden
- References
  - https://www.ics.uci.edu/~jmoorkan/vhdlref/
  - http://web.engr.oregonstate.edu/~traylor/ece474/vhdl_lectures/essential_vhdl_pdfs/
- Debugging
  - Stack Overflow, etc.