YATIN AVDHUT MANERKAR

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(beginning August 2021)

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RESEARCH ABSTRACT (please see research statement for details)

Many high-impact bugs have been found in computing systems in recent years, including security vulnerabilities, network routing errors, and concurrency bugs. My research addresses the challenge of creating correct computing systems by developing automated formal methodologies and tools for the design and verification of computing systems. Verification using such formal methods can provide strong correctness guarantees based on mathematical proofs.

My work spans the hardware/software stack, from high-level programming languages down to low-level Verilog circuits. I have developed methodologies and tools to verify that hardware and software uphold memory consistency (i.e., concurrency-related ordering) requirements on their respective sides of the hardware/software interface. My research has had real-world impact through discovering bugs in C++ compilers, a low-level processor implementation (Verilog), and the widely-used RISC-V ISA. My work has also enriched the formal methods community by developing new formal analysis techniques.

EDUCATION

PhD, Computer Science, September 2014 – December 2020 (to be conferred January 2021)
Princeton University, Princeton NJ, USA

- **Dissertation Title:** Progressive Automated Formal Verification of Memory Consistency in Parallel Processors (Adviser: Prof. Margaret Martonosi)

Master of Science, Computer Science and Engineering (Cumulative GPA: 8.5/9.0)
University of Michigan, Ann Arbor MI, USA (Sept. 2011 – May 2013)

- **Research Project:** Worked on Computational Sprinting with Prof. Thomas Wenisch

Bachelor of Applied Sciences, Honours Computer Engineering (Co-op) (Cumulative Avg: 94.65/100)
University of Waterloo, Waterloo ON, Canada (Sept. 2006 - June 2011)

- Graduated with two years work experience as part of the university's co-op education system

AWARDS AND NOMINATIONS

- 2020 – Finalist for Schmidt Science Fellows (interdisciplinary research fellowship) Class of 2020
- 2019 – Awarded School of Engineering and Applied Science Award for Excellence
- 2019 – Selected for Heidelberg Laureate Forum (1 of 200 young researchers chosen worldwide)
- 2019 – PipeProof paper selected as a 2018 IEEE Micro Top Picks Honorable Mention
- 2018 – PipeProof paper nominated for Best Paper at MICRO-51 conference
- 2018 – Awarded Wallace Memorial Honorific Fellowship by Princeton University Graduate School
- 2018 – RTLCheck paper selected as a 2017 IEEE Micro Top Picks Honorable Mention
- 2018 – TriCheck paper selected as a 2017 IEEE Micro Top Pick
- 2016 – Awarded 3rd place (tied) for demo (team project) at the C-FAR Annual Review
- 2015 – CCICheck paper nominated for Best Paper at MICRO-48 conference
- 2014 – Awarded Qualstar, a Qualcomm recognition of exceptional workplace contributions
- 2013 – Awarded membership in Honor Society of Phi Kappa Phi (top 10% of U-M grad students)
- 2010, 2011 – Awarded 2 Upper Year Scholarships by University of Waterloo Engineering
- 2010 – Awarded President's International Experience Award by University of Waterloo
- 2010 – Awarded President's Research Award by University of Waterloo

- 2006-2011 – Term Dean's Honours List in all 8 academic terms at University of Waterloo
- 2006 – Awarded President's Scholarship of Distinction and Nortel Networks Undergraduate Scholarship by the University of Waterloo

PEER-REVIEWED PUBLICATIONS

- **Yatin A. Manerkar**, Daniel Lustig, Margaret Martonosi, and Aarti Gupta. PipeProof: Automated Memory Consistency Proofs for Microarchitectural Specifications. The 51st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), October 2018. https://www.cs.princeton.edu/~manerkar/papers/manerkar_MICRO18.pdf
  - ► *Nominated for Best Paper at MICRO-51, **and** selected by peer review as an Honorable Mention for 2018 IEEE Micro "Top Picks" (12 most influential computer architecture papers).*
  - ► *First ever automated approach for all-program microarchitectural MCM verification.*
  - ► *74/351 full papers accepted (acceptance rate = 21.1%)*
- Hongce Zhang, Caroline Trippel, **Yatin A. Manerkar**, Aarti Gupta, Margaret Martonosi, and Sharad Malik. ILA-MCM: Integrating Memory Consistency Models with Instruction-Level Abstractions for Heterogeneous System-on-Chip Verification. The 18th Conference on Formal Methods in Computer-Aided Design (FMCAD), October 2018. https://mrmgroup.cs.princeton.edu/papers/fmcad2018.pdf
  - ► *Linked operational models for compute with axiomatic MCMs, enabling holistic SoC verification.*
  - ► *26/73 full papers accepted (acceptance rate = 35.6%)*
- Caroline Trippel, **Yatin A. Manerkar**, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. Full-Stack Memory Model Verification with TriCheck. IEEE Micro, 38 (3) (Top Picks), May 2018. https://www.cs.princeton.edu/~manerkar/papers/ctrippel_IEEETopPicks18.pdf
  - ► *Invited version of ASPLOS 2017 paper in IEEE Micro's "Top Picks" (most influential computer architecture papers, as determined by a peer-review process) issue for the year 2017.*
- **Yatin A. Manerkar**, Daniel Lustig, Margaret Martonosi, and Michael Pellauer. RTLCheck: Verifying the Memory Consistency of RTL Designs. The 50th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), October 2017. https://www.cs.princeton.edu/~manerkar/papers/MICRO-50_Manerkar.pdf
  - ► *Selected as an Honorable Mention for IEEE Micro "Top Picks" for 2017.*
  - ► *First ever automated approach for MCM verification of hardware RTL (Verilog).*
  - ► *61/327 full papers accepted (acceptance rate = 18.7%)*
- Caroline Trippel, **Yatin A. Manerkar**, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. TriCheck: Memory Model Verification at the Trisection of Software, Hardware, and ISA. The 22nd International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2017. https://www.cs.princeton.edu/~manerkar/papers/ctrippel_ASPLOS17.pdf
  - ► *Selected as an IEEE Micro "Top Pick" (1 of 12 most influential comp. arch. papers) for 2017.*
  - ► *Uncovered severe deficiencies in the MCM specification of the draft RISC-V ISA.*
  - ► *56/321 full papers accepted (acceptance rate = 17.4%)*
- **Yatin A. Manerkar**, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. CCICheck: Using μhb Graphs to Verify the Coherence-Consistency Interface. The 48th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), December 2015. https://www.cs.princeton.edu/~manerkar/papers/MICRO2015_Yatin_Manerkar.pdf
  - ► *Nominated for Best Paper at MICRO-48.*
  - ► *Enabled automatic detection of MCM bugs arising from pipeline-coherence protocol interactions.*
  - ► *61/283 full papers accepted (acceptance rate = 21.6%)*

UNPUBLISHED MANUSCRIPTS AND SHORT PAPERS

- **Yatin A. Manerkar**, Daniel Lustig, and Margaret Martonosi. RealityCheck: Bringing Modularity, Hierarchy, and Abstraction to Automated Microarchitectural Memory Consistency Verification. https://arxiv.org/pdf/2003.04892.pdf
  ► *First ever automated approach for modular and scalable microarchitectural MCM verification.*
- **Yatin A. Manerkar**, Caroline Trippel, Daniel Lustig, Michael Pellauer, and Margaret Martonosi. Counterexamples and Proof Loophole for the C/C++ to POWER and ARMv7 Trailing-Sync Compiler Mappings. CoRR abs/1611.01507, November 2016. https://arxiv.org/pdf/1611.01507.pdf
  ► *Uncovered an error in a formal proof underpinning much programming language MCM research for the prior four years.*

TALKS

- **Progressive Automated Formal Verification of Hardware and Software Systems.**
  Invited talk, University of Illinois Urbana-Champaign, Urbana IL, April 2020.
  Invited talk, Pennsylvania State University, State College PA, March 2020.
  Invited talk, Carnegie Mellon University, Pittsburgh PA, March 2020.
  Invited talk, University of Michigan, Ann Arbor MI, March 2020.
  Invited talk, Georgia Institute of Technology, Atlanta GA, February 2020.
  Invited talk, Rising Stars in Computer Architecture (RISC-A) Workshop, Atlanta GA, October 2019.
- **Automated Formal Memory Consistency Verification of Hardware.**
  Invited talk, DeepSpec Workshop at PLDI 2019, Phoenix AZ, June 2019.
- **Automated Formal Verification of Event Orderings in Parallel Hardware and Software.**
  Invited talk, University of Toronto, Toronto ON, Canada, March 2019.
- **PipeProof: Automated Memory Consistency Proofs for Microarchitectural Specifications.**
  MICRO-51 Conference Talk, Fukuoka, Japan, October 2018.
- **Automated Full-Stack Memory Model Verification with the Check Suite.**
  Invited talk, Imperial College London, UK, July 2018.
  Invited talk, University of Cambridge, UK, July 2018.
  Invited talk, ARM Cambridge, UK, July 2018.
- **RTLCheck: Automatically Verifying the Memory Consistency of Processor RTL.**
  Parallel Logical Reasoning (PLR) Workshop at FLoC 2018, Oxford, UK, July 2018.
- **RTLCheck: Verifying the Memory Consistency of RTL Designs.**
  MICRO-50 Conference Talk, Boston MA, October 2017.
- **C11 Compiler Mappings: Exploration, Verification, and Counterexamples.**
  Dagstuhl Seminar 16471: Concurrency with Weak Memory Models, Germany, November 2016.
- **CCICheck: Using μhb Graphs to Verify the Coherence-Consistency Interface.**
  MICRO-48 Conference Talk, Waikiki HI, December 2015.

TEACHING AND MENTORING EXPERIENCE

Mentor, Undergraduate Independent Work, September 2019 – January 2020

- Mentored Princeton undergraduate student Julian Knodt along with Prof. Margaret Martonosi
- Advised Julian on how to use my RealityCheck tool to modularly specify and conduct MCM verification for microarchitectural designs

Tutorial Instructor

► ISCA 2019 Conference, Phoenix AZ, June 2019
► ISCA 2017 Conference, Toronto, Canada, June 2017

- Helped create and organise two tutorials about our research group's tools for MCM verification
- Guided attendees through do-it-yourself activities that used our tools to verify hardware designs

Mentor, REACH (International Research Exchange) Program, June 2018 – August 2018

- Mentored Ying Jing (undergraduate student from HKUST) along with Prof. Margaret Martonosi

- Advised Ying on parallel programming and investigating event ordering issues in IoT devices

Instructor, UPMARC Summer School 2018, Uppsala University, Sweden, June 2018
- Taught students how to model and verify hardware designs using tools developed by our group
- Worked through a hands-on demonstration of modelling and verifying a hardware design

Teaching Assistant, Princeton University, Princeton NJ, February 2017 – June 2017
- **Course:** Great Moments in Computing (COS 583), Prof. Margaret Martonosi
- Course based on detailed discussions and projects related to 30 seminal computer science papers across a wide range of topics
- Evaluated student participation in classroom
- Graded student preparatory assignments (one before each lecture) for correctness and insight

Teaching Assistant, Princeton University, Princeton NJ, September 2016 – January 2017
- **Course:** Computer Organization and Design (COS 375), Prof. Margaret Martonosi
- Created specifications, solutions, and auto-grading scripts for two course projects: an ISA-level simulator and a cycle-accurate five-stage pipeline simulator (approx. 2000 lines of code)
- Answered student questions during office hours and on the course Piazza forum
- Graded student projects for correctness and style

Teaching Assistant, University of Michigan, Ann Arbor MI, September 2011 – April 2013
- **Course:** Programming and Introductory Data Structures (EECS 280)
- **Instructors:** Brian Noble, Jeff Ringenberg, Georg Essl, and Andrew DeOrio
- TA for the course for 4 semesters
- Presented supplementary course material in discussion (tutorial) sessions
- Updated and maintained discussion notes that were presented by all TAs in discussion sections
- Answered student questions during office hours and on the course Piazza forum
- Created and graded midterm and final exam questions, and graded student projects for style

CONTINUING EDUCATION

- **Ethics of AI Graduate Student Learning Cohort**, Princeton University, Princeton NJ, September – December 2019
  - Participated in an interdisciplinary seminar exploring the intersection of artificial intelligence and ethics through presentations, case studies, readings, and discussion
- **Summer School on Formal Techniques**, SRI International, Atherton CA (May 2019)
  - Instruction from world-renowned researchers on the principles and practices of formal techniques, including hands-on exercises.
- **Workshop: Grading as a Teaching Tool**, McGraw Center, Princeton NJ (November 2018)
  - Instruction on how to grade effectively and in a manner that advances students' learning
- **DeepSpec Summer School 2017**, University of Pennsylvania, Philadelphia PA (July 2017)
  - Received instruction on various projects that use the Coq proof assistant to create systems that can be formally proven to be "correct by construction".

TECHNICAL SERVICE

- **Program Committee Member**, YArch (Young Architect Workshop) 2021
- **External Review Committee**, ASPLOS (Architectural Support for Programming Languages and Operating Systems) 2021 Conference
- **Sub-Reviewer**, POPL (Principles of Programming Languages) 2021 Conference
- **Reviewer**, IEEE CAL (Computer Architecture Letters), July 2020
- **Sub-Reviewer**, CPP (Certified Programs and Proofs) 2020 Conference
- **Workshop Organizer**, Heidelberg Laureate Forum, September 2019
  - Organised a "Concurrency: Theory and Practice" workshop, including defining its structure, soliciting attendee contributions, and moderating the workshop
  - Mentors: Robert Tarjan and Leslie Lamport
- **Expo Round Judge, HackPrinceton Fall 2018**, November 2018

    - Judged student projects at HackPrinceton, a 36-hour hackathon comprised of over 600 students from around the world
- **Member, RISC-V Memory Model Working Group**, March 2017 – Present
    - Contributed to the development of the RISC-V ISA's new MCM (ratified September 2018), which fixed the issues identified in my ASPLOS 2017 paper and included other improvements
- **Reviewer, IEEE Micro**, March 2017

WORK EXPERIENCE

Assistant Professor, Computer Science and Eng. Department, University of Michigan, Ann Arbor MI (Beginning August 2021)

Volunteer, Dept. of Electrical Eng. and Computer Sciences, University of California, Berkeley CA December 2020 – present (working remotely)

- Working with Prof. Sanjit Seshia
- Contributing to research in formal methods for computer architecture verification and synthesis

Co-op Engineer, AMD Research, Bellevue, WA, June 2015 – October 2015

- Explored the scalability and efficiency of AMD's remote-scope-promotion technology

Engineer, Qualcomm Research, San Diego, CA, July 2013 – July 2014

- Wrote firmware and kernel-level code for embedded platform used in LTE research

Interim Engineering Intern, Qualcomm Innovation Center, San Diego, CA, May 2012 – August 2012

- Worked on the Linux kernel team
- Migrated an API for inter-processor communication on Snapdragon chips to use the Linux device model for event handling and `virtio` for data transfer while maintaining legacy API support

Software Development Engineer Intern, Amazon.com, Seattle WA, September 2010 – December 2010

- Worked on the Amazon Web Services Billing Team
- Designed and developed two persistent storage implementations (BerkeleyDB and MySQL) of an in-memory object structure, and integrated these implementations with a larger system
- Modified existing code and ran tests to ensure that the functional behavior of the persistent implementations was the same as that of the in-memory implementations
- Ran performance tests on both implementations to determine which was the optimal solution

Browser Developer Co-op, Research in Motion (BlackBerry), Waterloo ON, Canada
January 2009 – May 2009 and September 2009 – December 2009

- Found and fixed bugs (sometimes complicated ones) in the BlackBerry Browser's JavaScript, DOM, and layout implementation
- Worked on optimizing parts of the browser to improve performance
- Modified parts of the browser to comply with the HTML 5 specification

SKILLS SUMMARY

- Knowledge of C/C++, Java (SE/ME/EE), Coq, HTML, JavaScript, CSS, C#, ASP.NET, and some Verilog, OCaml, R, gem5 (simulator), databases (SQL Server, ADO.NET, BerkeleyDB, MySQL), and AJAX
- Over three years work experience in software development, including desktop & web applications, large codebases, and high-visibility products (Linux Kernel, Amazon Web Services)
- Experience programming a variety of software, including operating systems, firmware, parsers, browser layout and JavaScript engines, and user interfaces
- Knowledge of routers, switches, routing protocols, VLANs, OSI and TCP/IP models, and Cisco IOS. Held CCNA (Cisco Certified Network Associate) certification from 2005-2008