Digital Molecular Computer

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Abstract

Boolean satisfiability problem (SAT) is an NP-complete problem which is hard to solve in polynomial time with conventional computers. We propose **D**igital **M**olecular **C**omputer (DMC), an in-memory computing processor, which solves variable-limited SAT problems in polynomial time with current microelectronic technology and novel architecture. Inspired by molecular computing, DMC combines massive parallelism and efficiency organization of molecular computer, and fast speed and programmability of digital computer. DMC activates multiple memory-computing units parallelly by a decoder-like device, Transformer. Different SAT problems can be solved in a general DMC-architecture processor with different programs due to DMC's programmability. DMC provides an accurate solution and deterministic steps algorithm for SAT problems while past SAT solvers are hard to achieve. We implemented a prototype solving 10-variable SAT problems on an FPGA board.